Lab 3 – Adder

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1. Lab task:-

   Designing a 4-bit Ripple Carry Adder(RCA).

   First, we created a Half Adder. Then used it to create a Full adder. Then added full adder to IP catalogue so we can use it as an IP block. After that we created the 4-bit Ripple Carry Adder using FA blocks. Then ran simulation on it to make sure it functions correctly.

   Truth tables

A	B	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Sum = $A \oplus B$

$\text{Carry} = A.B$

$$\text{Sum} = A`.B`.C_{in} + A`.B.C_{in}` + A.B`.C_{in}` + A.B.C_{in}$$

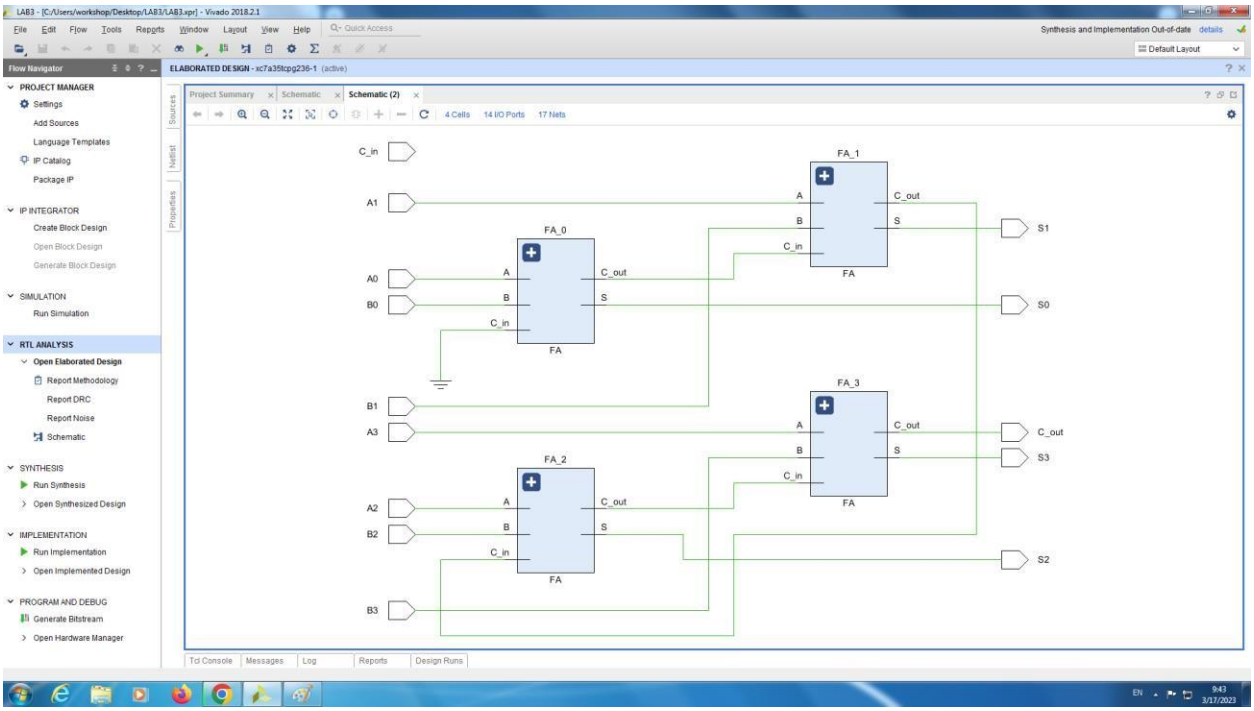
$$= A`(B`.C_{in} + B.C_{in}`) + A(B`.C_{in}` + B.C_{in})$$

$$= A \oplus B \oplus C_{in}$$

$$C_{out} = A`.B.C_{In} + A.B.C_{in}` + A.B`.C_{in} + A.B.C_{in}$$

$$= A.B + C_{In}(A \oplus B)$$

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1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Schematic
Schematic (2)
4 Cells
14 I/O Ports
17 Nets
C_in
A1
A0
B0
B1
A3
A2
B2
B3
FA_0
FA_1
FA_2
FA_3
A
B
C_in
C_out
S
FA
S1
S0
S2
S3
C_out
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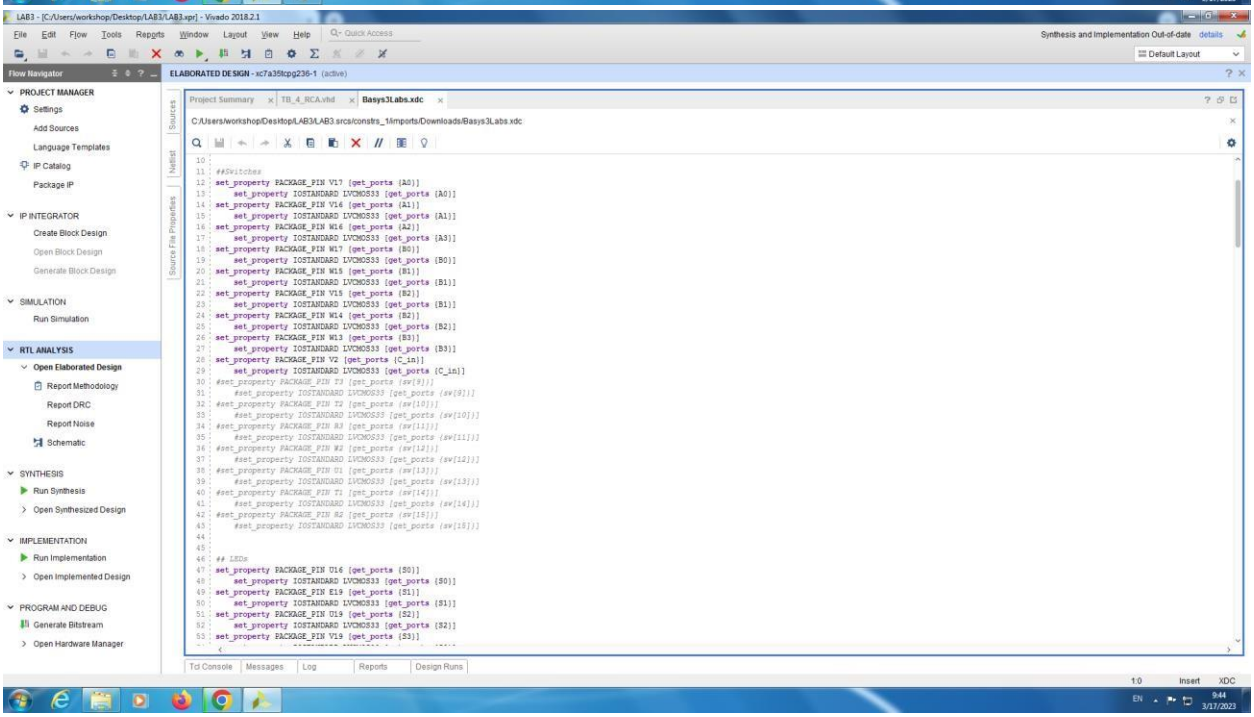
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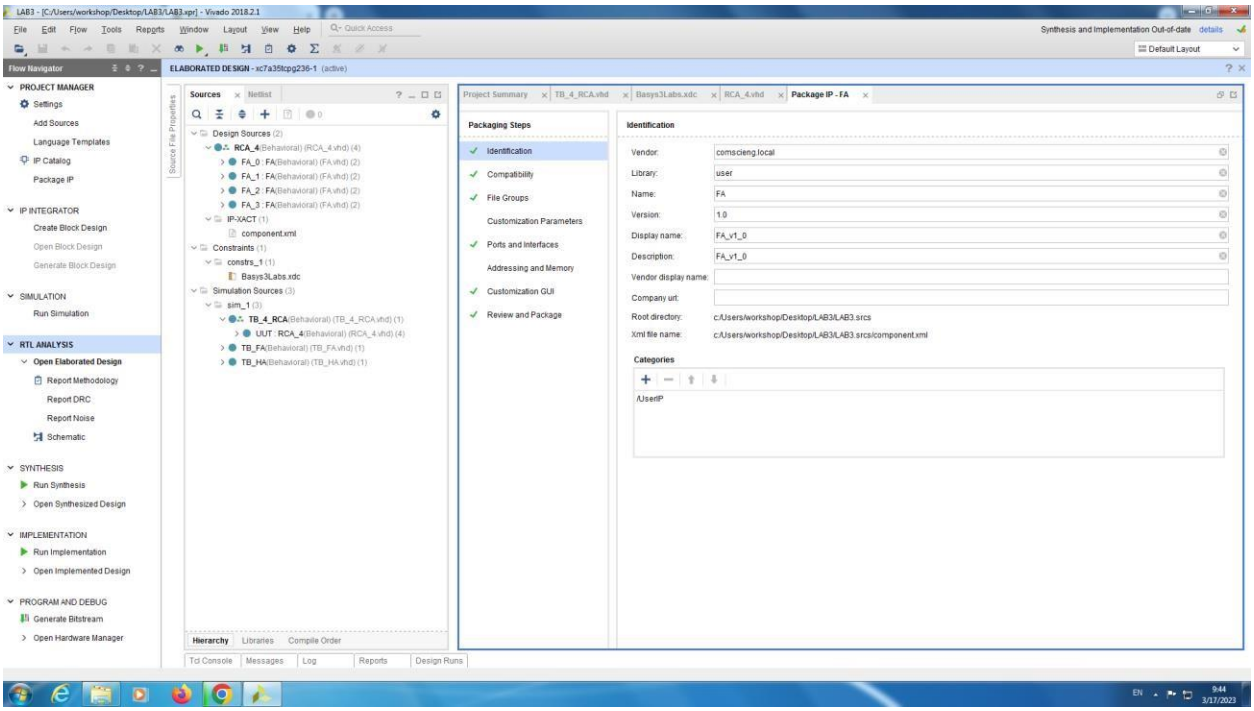
TB_4_RCA.vhd
Basys3Labs.xdc
C:/Users/workshop/Desktop/LAB3/LAB3.srcs/constrs_1/imports/Downloads/Basys3Labs.xdc
##Switches
set_property PACKAGE_PIN V17 [get_ports {A0}]
set_property IOSTANDARD LVCMOS33 [get_ports {A0}]
set_property PACKAGE_PIN V16 [get_ports {A1}]
set_property IOSTANDARD LVCMOS33 [get_ports {A1}]
set_property PACKAGE_PIN W16 [get_ports {A2}]
set_property IOSTANDARD LVCMOS33 [get_ports {A3}]
set_property PACKAGE_PIN W17 [get_ports {B0}]
set_property IOSTANDARD LVCMOS33 [get_ports {B0}]
set_property PACKAGE_PIN W15 [get_ports {B1}]
set_property IOSTANDARD LVCMOS33 [get_ports {B1}]
set_property PACKAGE_PIN V15 [get_ports {B2}]
set_property IOSTANDARD LVCMOS33 [get_ports {B1}]
set_property PACKAGE_PIN W14 [get_ports {B2}]
set_property IOSTANDARD LVCMOS33 [get_ports {B2}]
set_property PACKAGE_PIN W13 [get_ports {B3}]
set_property IOSTANDARD LVCMOS33 [get_ports {B3}]
set_property PACKAGE_PIN V2 [get_ports {C_in}]
set_property IOSTANDARD LVCMOS33 [get_ports {C_in}]
#set_property PACKAGE_PIN T3 [get_ports {sw[9]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[9]}]
#set_property PACKAGE_PIN T2 [get_ports {sw[10]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[10]}]
#set_property PACKAGE_PIN R3 [get_ports {sw[11]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[11]}]
#set_property PACKAGE_PIN W2 [get_ports {sw[12]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[12]}]
#set_property PACKAGE_PIN U1 [get_ports {sw[13]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[13]}]
#set_property PACKAGE_PIN T1 [get_ports {sw[14]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[14]}]
#set_property PACKAGE_PIN R2 [get_ports {sw[15]}]
#set_property IOSTANDARD LVCMOS33 [get_ports {sw[15]}]
LEDs
set_property PACKAGE_PIN U16 [get_ports {S0}]
set_property IOSTANDARD LVCMOS33 [get_ports {S0}]
set_property PACKAGE_PIN E19 [get_ports {S1}]
set_property IOSTANDARD LVCMOS33 [get_ports {S1}]
set_property PACKAGE_PIN U19 [get_ports {S2}]
set_property IOSTANDARD LVCMOS33 [get_ports {S2}]
set_property PACKAGE_PIN V19 [get_ports {S3}]
Tcl Console
Messages
Log
Reports
Design Runs
1:0
Insert
XDC
9:44
3/17/2023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Source File Properties
Sources
Netlist
Design Sources (2)
RCA_4 (Behavioral) (RCA_4.vhd) (4)
FA_0 : FA (Behavioral) (FA.vhd) (2)
FA_1 : FA (Behavioral) (FA.vhd) (2)
FA_2 : FA (Behavioral) (FA.vhd) (2)
FA_3 : FA (Behavioral) (FA.vhd) (2)
IP-XACT (1)
component.xml
Constraints (1)
constrs_1 (1)
Basys3Labs.xdc
Simulation Sources (3)
sim_1 (3)
TB_4_RCA (Behavioral) (TB_4_RCA.vhd) (1)
UUT : RCA_4 (Behavioral) (RCA_4.vhd) (4)
TB_FA (Behavioral) (TB_FA.vhd) (1)
TB_HA (Behavioral) (TB_HA.vhd) (1)
Hierarchy Libraries Compile Order
Project Summary
TB_4_RCA.vhd
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RCA_4.vhd
Package IP - FA
Packaging Steps
Identification
Compatibility
File Groups
Customization Parameters
Ports and Interfaces
Addressing and Memory
Customization GUI
Review and Package
Identification
Vendor: comscieng.local
Library: user
Name: FA
Version: 1.0
Display name: FA_v1_0
Description: FA_v1_0
Vendor display name:
Company url:
Root directory: c:/Users/workshop/Desktop/LAB3/LAB3.srcs
Xml file name: c:/Users/workshop/Desktop/LAB3/LAB3.srcs/component.xml
Categories
/UserIP
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EN
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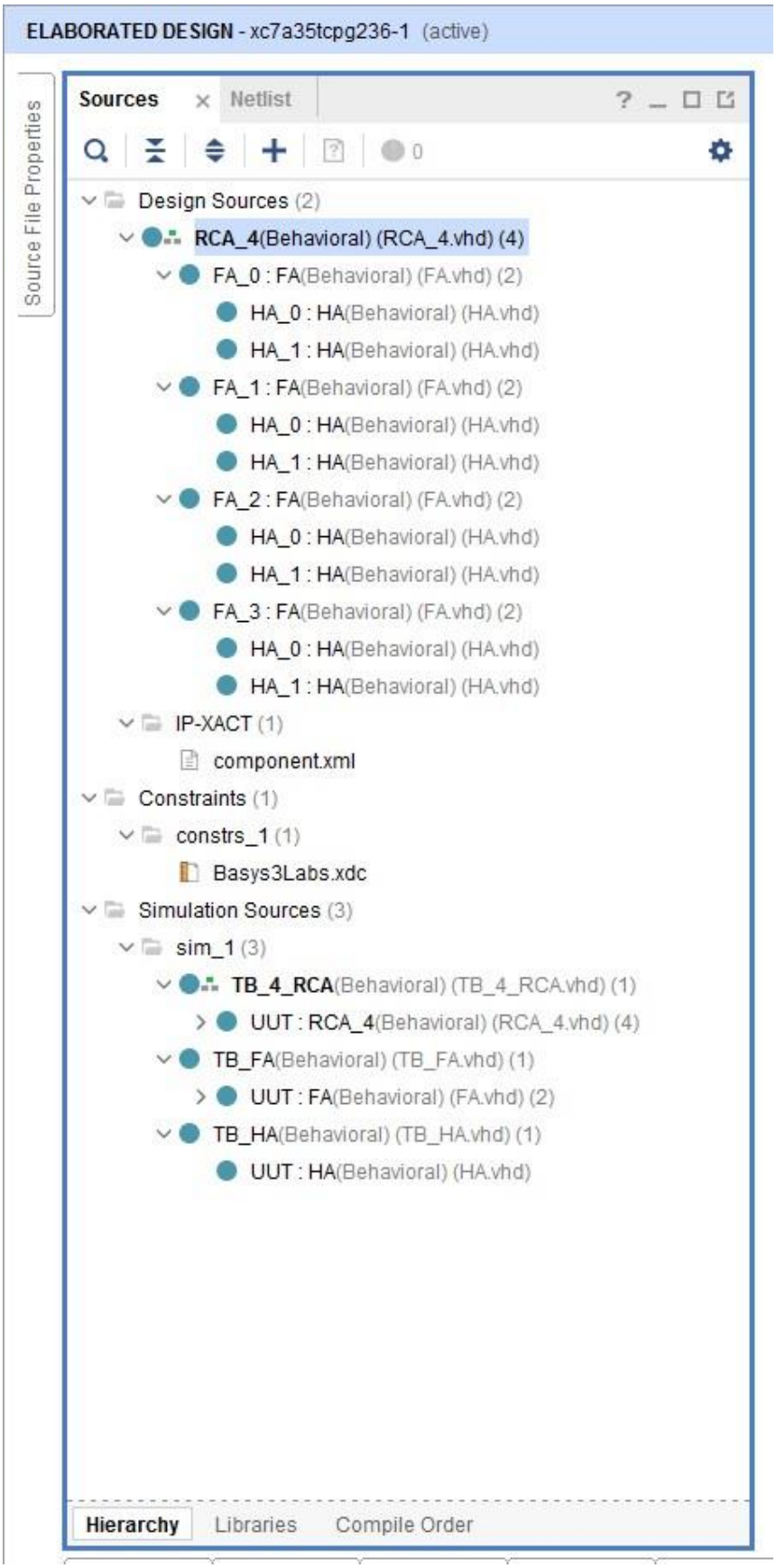
ELABORATED DESIGN - xc7a35tcpg236-1 (active)
Source File Properties
Sources
Netlist
0
Design Sources (2)
RCA_4(Behavioral) (RCA_4.vhd) (4)
FA_0 : FA(Behavioral) (FA.vhd) (2)
HA_0 : HA(Behavioral) (HA.vhd)
HA_1 : HA(Behavioral) (HA.vhd)
FA_1 : FA(Behavioral) (FA.vhd) (2)
HA_0 : HA(Behavioral) (HA.vhd)
HA_1 : HA(Behavioral) (HA.vhd)
FA_2 : FA(Behavioral) (FA.vhd) (2)
HA_0 : HA(Behavioral) (HA.vhd)
HA_1 : HA(Behavioral) (HA.vhd)
FA_3 : FA(Behavioral) (FA.vhd) (2)
HA_0 : HA(Behavioral) (HA.vhd)
HA_1 : HA(Behavioral) (HA.vhd)
IP-XACT (1)
component.xml
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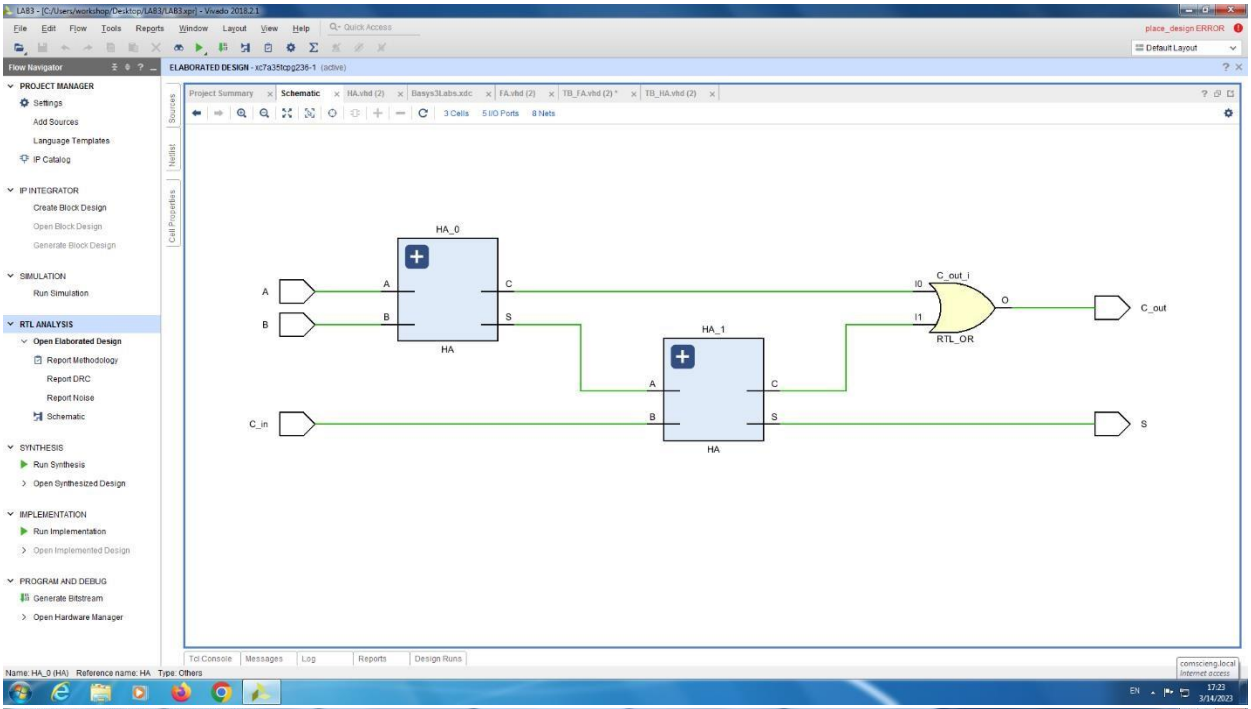
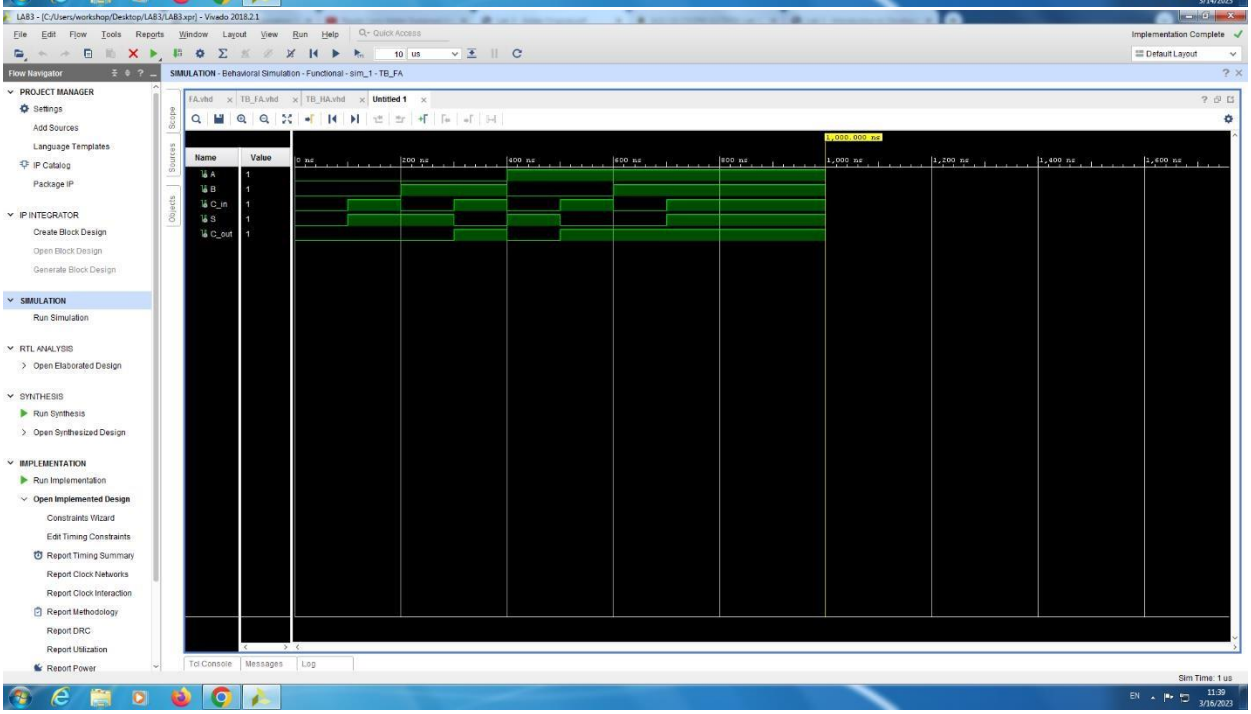
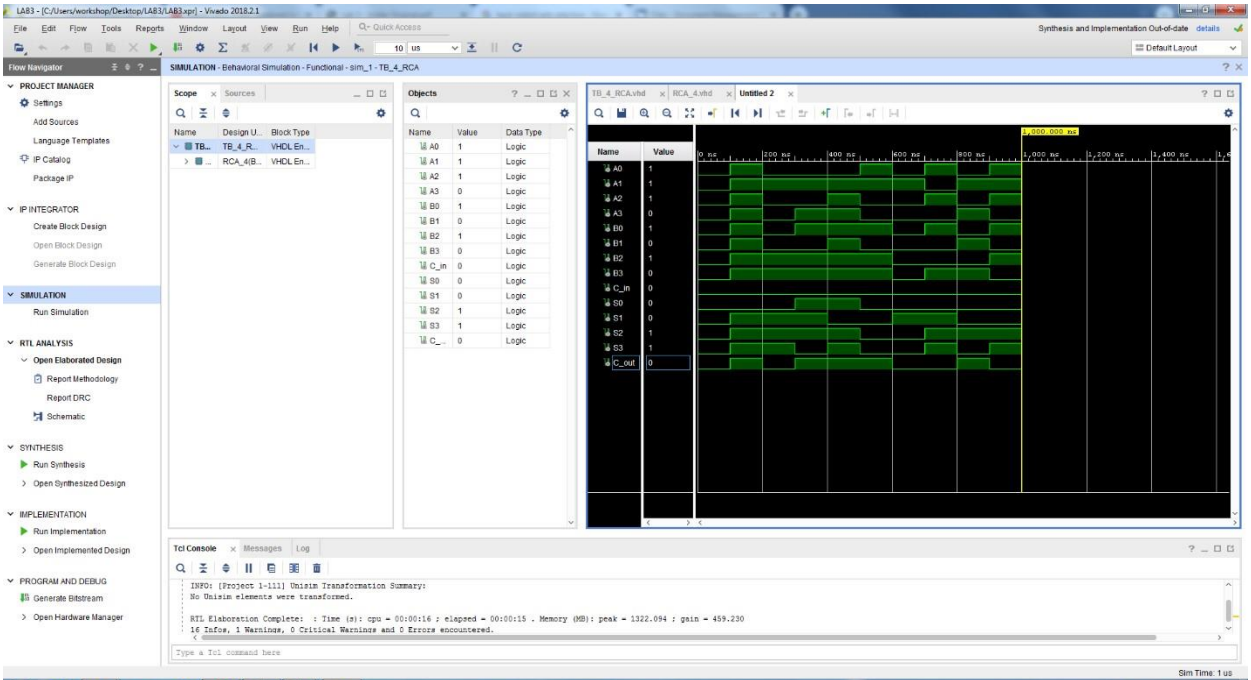
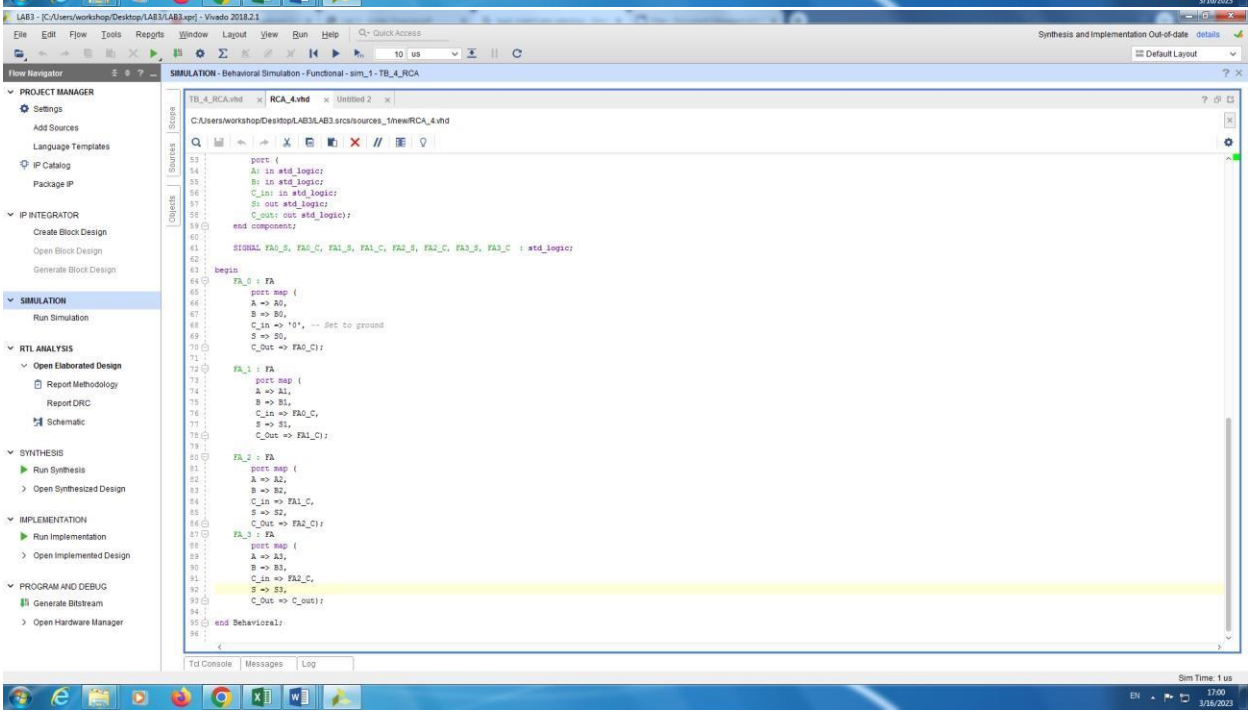
Simulation Sources (3)
sim_1 (3)
TB_4_RCA(Behavioral) (TB_4_RCA.vhd) (1)
UUT : RCA_4(Behavioral) (RCA_4.vhd) (4)
TB_FA(Behavioral) (TB_FA.vhd) (1)
UUT : FA(Behavioral) (FA.vhd) (2)
TB_HA(Behavioral) (TB_HA.vhd) (1)
UUT : HA(Behavioral) (HA.vhd)
Hierarchy
Libraries
Compile Order

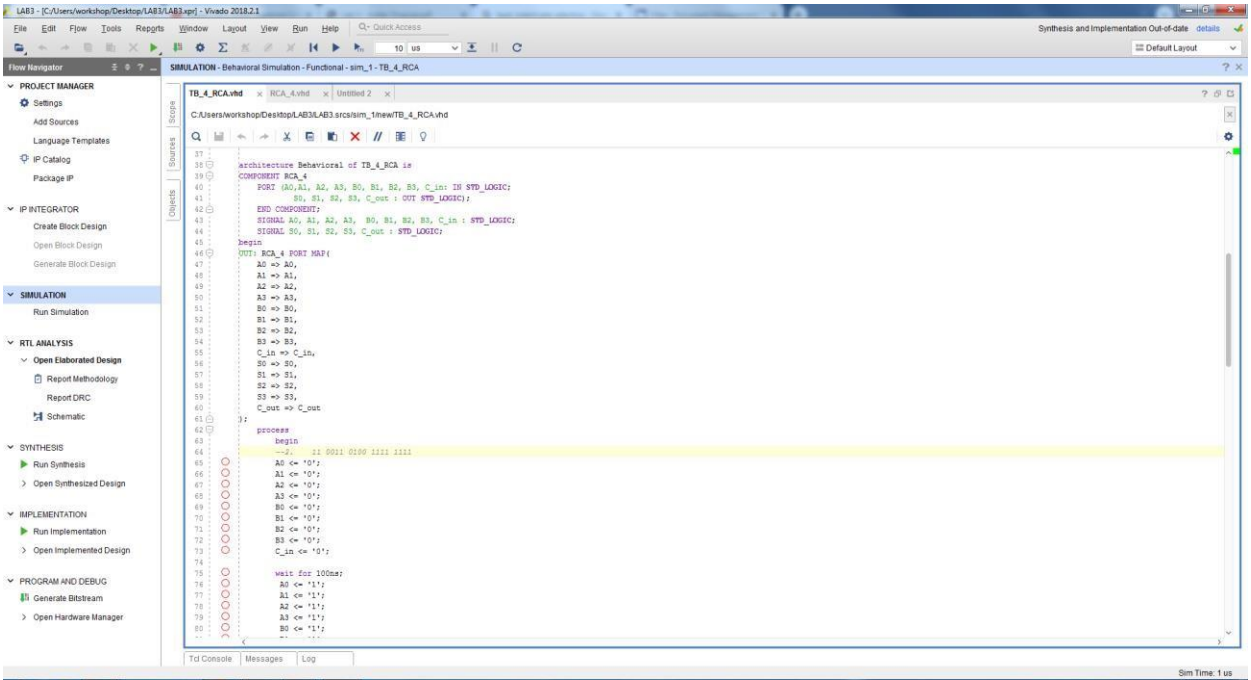

LAB3 - [C:/Users/workshop/Desktop/LAB3/LAB3.xpr] - Vivado 2018.2.1
ELABORATED DESIGN - xc7a35tcpg236-1 (active)
HA_0
HA
HA_1
HA
C_out_i
RTL_OR
A
B
C_in
C_out
S


LAB3 - [C:/Users/workshop/Desktop/LAB3/LAB3.xpr] - Vivado 2018.2.1
SIMULATION - Behavioral Simulation - Functional - sim_1 - TB_FA
Name
Value
A
B
C_in
S
C_out






```
        port (
        A: in std_logic;
        B: in std_logic;
        C_in: in std_logic;
        S: out std_logic;
        C_out: out std_logic);
    end component;

    SIGNAL FA0_S, FA0_C, FA1_S, FA1_C, FA2_S, FA2_C, FA3_S, FA3_C  : std_logic;

begin
    FA_0 : FA
        port map (
        A => A0,
        B => B0,
        C_in => '0', -- Set to ground
        S => S0,
        C_Out => FA0_C);

    FA_1 : FA
         port map (
         A => A1,
         B => B1,
         C_in => FA0_C,
         S => S1,
         C_Out => FA1_C);

    FA_2 : FA
        port map (
        A => A2,
        B => B2,
        C_in => FA1_C,
        S => S2,
        C_Out => FA2_C);
    FA_3 : FA
        port map (
        A => A3,
        B => B3,
        C_in => FA2_C,
        S => S3,
        C_Out => C_out);

end Behavioral;
```


LAB3 - [C:/Users/workshop/Desktop/LAB3/LAB3.xpr] - Vivado 2018.2.1
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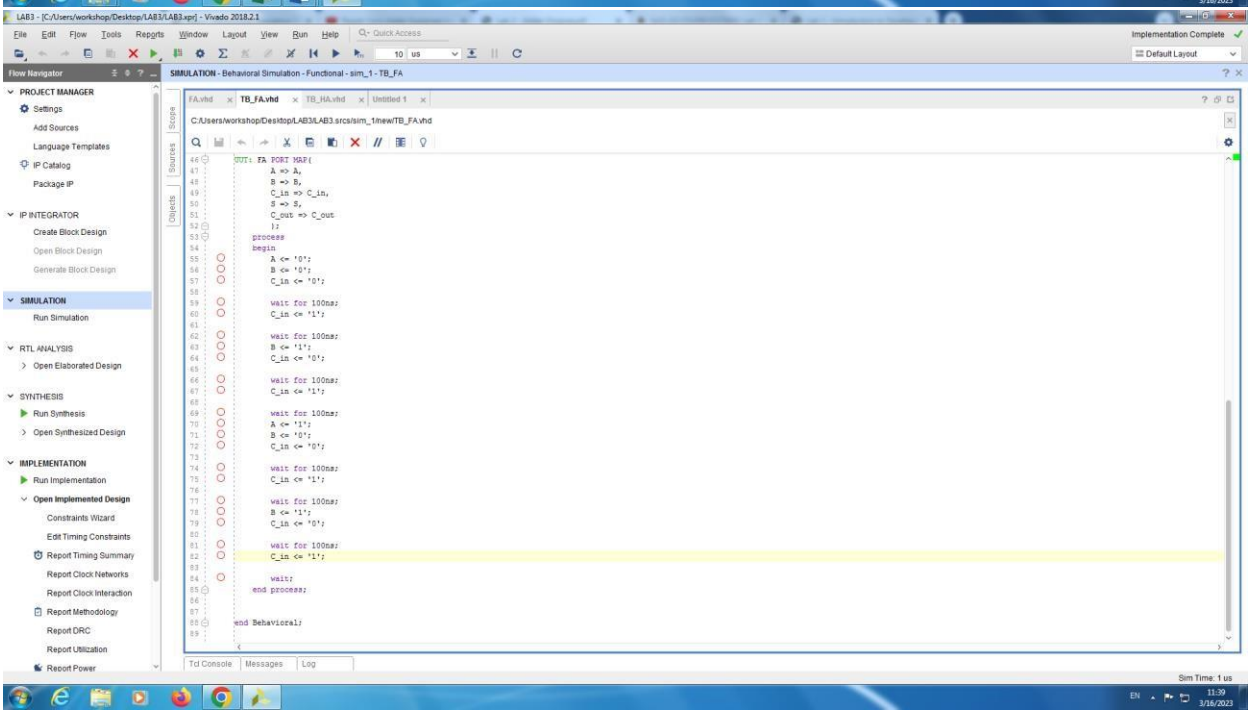
SIMULATION - Behavioral Simulation - Functional - sim_1 - TB_4_RCA
TB_4_RCA.vhd
RCA_4.vhd
Untitled 2
C:/Users/workshop/Desktop/LAB3/LAB3.srcs/sim_1/new/TB_4_RCA.vhd
architecture Behavioral of TB_4_RCA is
COMPONENT RCA_4
PORT (A0,A1, A2, A3, B0, B1, B2, B3, C_in: IN STD_LOGIC;
S0, S1, S2, S3, C_out : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A0, A1, A2, A3, B0, B1, B2, B3, C_in : STD_LOGIC;
SIGNAL S0, S1, S2, S3, C_out : STD_LOGIC;
begin
UUT: RCA_4 PORT MAP(
A0 => A0,
A1 => A1,
A2 => A2,
A3 => A3,
B0 => B0,
B1 => B1,
B2 => B2,
B3 => B3,
C_in => C_in,
S0 => S0,
S1 => S1,
S2 => S2,
S3 => S3,
C_out => C_out
);
process
begin
--2. 11 0011 0100 1111 1111
A0 <= '0';
A1 <= '0';
A2 <= '0';
A3 <= '0';
B0 <= '0';
B1 <= '0';
B2 <= '0';
B3 <= '0';
C_in <= '0';
wait for 100ns;
A0 <= '1';
A1 <= '1';
A2 <= '1';
A3 <= '1';
B0 <= '1';
Tcl Console
Messages
Log
Sim Time: 1 us
17:01
3/16/2023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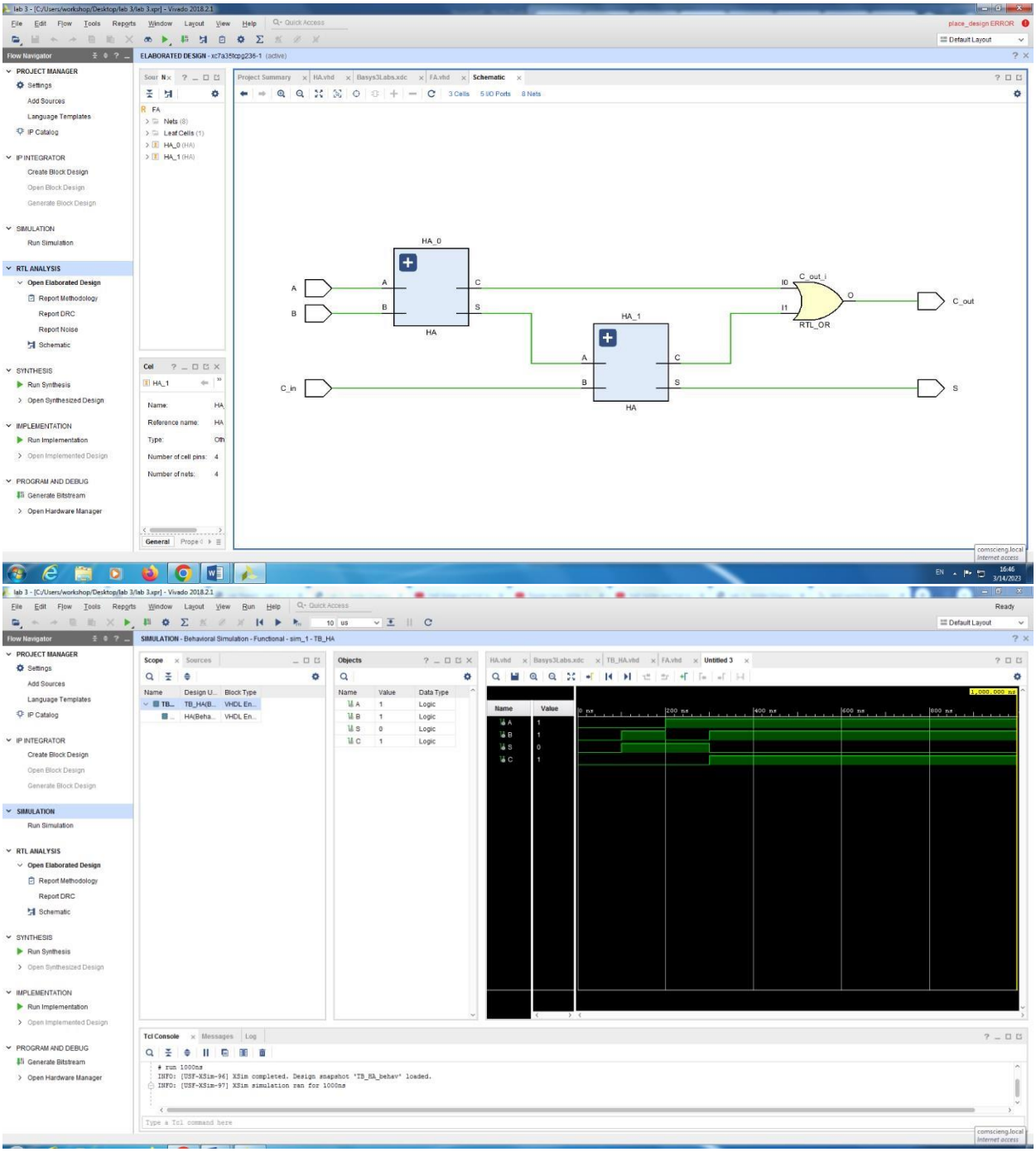
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
SIMULATION - Behavioral Simulation - Functional - sim_1 - TB_FA
FA.vhd
TB_FA.vhd
TB_HA.vhd
Untitled 1
C:/Users/workshop/Desktop/LAB3/LAB3.srcs/sim_1/new/TB_FA.vhd
UUT: FA PORT MAP(
A => A,
B => B,
C_in => C_in,
S => S,
C_out => C_out
);
process
begin
A <= '0';
B <= '0';
C_in <= '0';
wait for 100ns;
C_in <= '1';
wait for 100ns;
B <= '1';
C_in <= '0';
wait for 100ns;
C_in <= '1';
wait for 100ns;
A <= '1';
B <= '0';
C_in <= '0';
wait for 100ns;
C_in <= '1';
wait for 100ns;
B <= '1';
C_in <= '0';
wait for 100ns;
C_in <= '1';
wait;
end process;
end Behavioral;
Tcl Console
Messages
Log
Sim Time: 1 us
11:39
3/16/2023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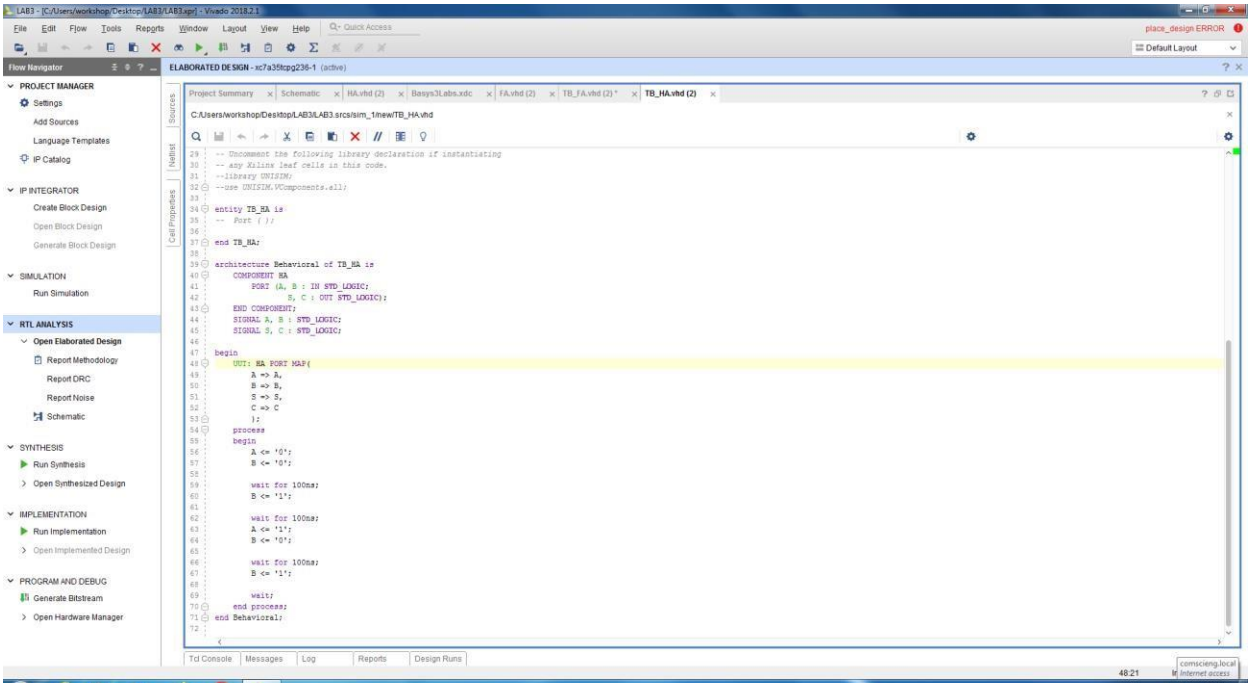
ELABORATED DESIGN - xc7a35tcpg236-1 (active)
Project Summary
HA.vhd
Basys3Labs.xdc
FA.vhd
Schematic
3 Cells
5 I/O Ports
8 Nets
FA
Nets (8)
Leaf Cells (1)
HA_0 (HA)
HA_1 (HA)
HA_1
Name: HA
Reference name: HA
Type: Oth
Number of cell pins: 4
Number of nets: 4
HA_0
A
B
C
S
HA
HA_1
C_in
C_out_i
I0
I1
O
RTL_OR
C_out
SIMULATION - Behavioral Simulation - Functional - sim_1 - TB_HA
Scope
Sources
Objects
Untitled 3
Name
Value
Data Type
Logic
1,000.000 ns
200 ns
400 ns
600 ns
800 ns
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'TB_HA_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
Type a Tcl command here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ELABORATED DESIGN - xc7a35tcpg236-1 (active)
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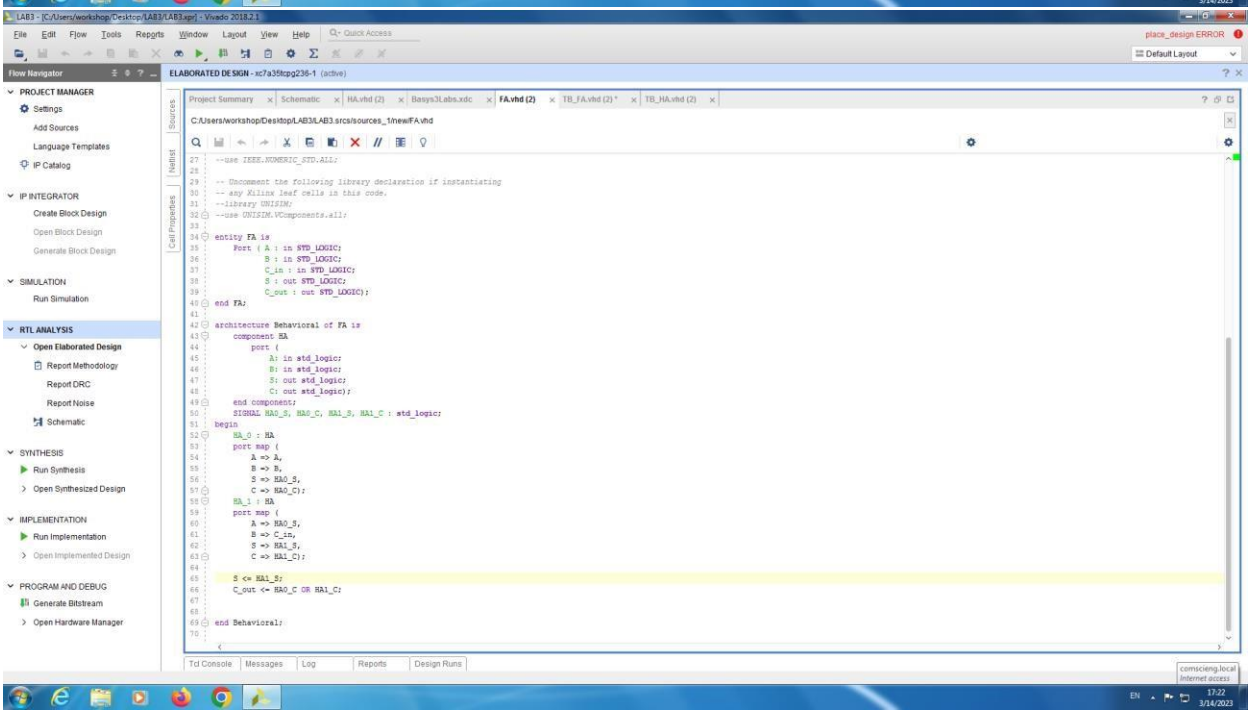
Schematic
HA.vhd (2)
Basys3Labs.xdc
FA.vhd (2)
TB_FA.vhd (2) *
TB_HA.vhd (2)
C:/Users/workshop/Desktop/LAB3/LAB3.srcs/sim_1/new/TB_HA.vhd
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity TB_HA is
-- Port ( );
end TB_HA;
architecture Behavioral of TB_HA is
COMPONENT HA
PORT (A, B : IN STD_LOGIC;
S, C : OUT STD_LOGIC);
END COMPONENT;
SIGNAL A, B : STD_LOGIC;
SIGNAL S, C : STD_LOGIC;
begin
UUT: HA PORT MAP(
A => A,
B => B,
S => S,
C => C
);
process
begin
A <= '0';
B <= '0';
wait for 100ns;
B <= '1';
wait for 100ns;
A <= '1';
B <= '0';
wait for 100ns;
B <= '1';
wait;
end process;
end Behavioral;
Tcl Console
Messages
Log
Reports
Design Runs
48:21
comsciengl.local
Internet access
EN
17:22
3/14/2023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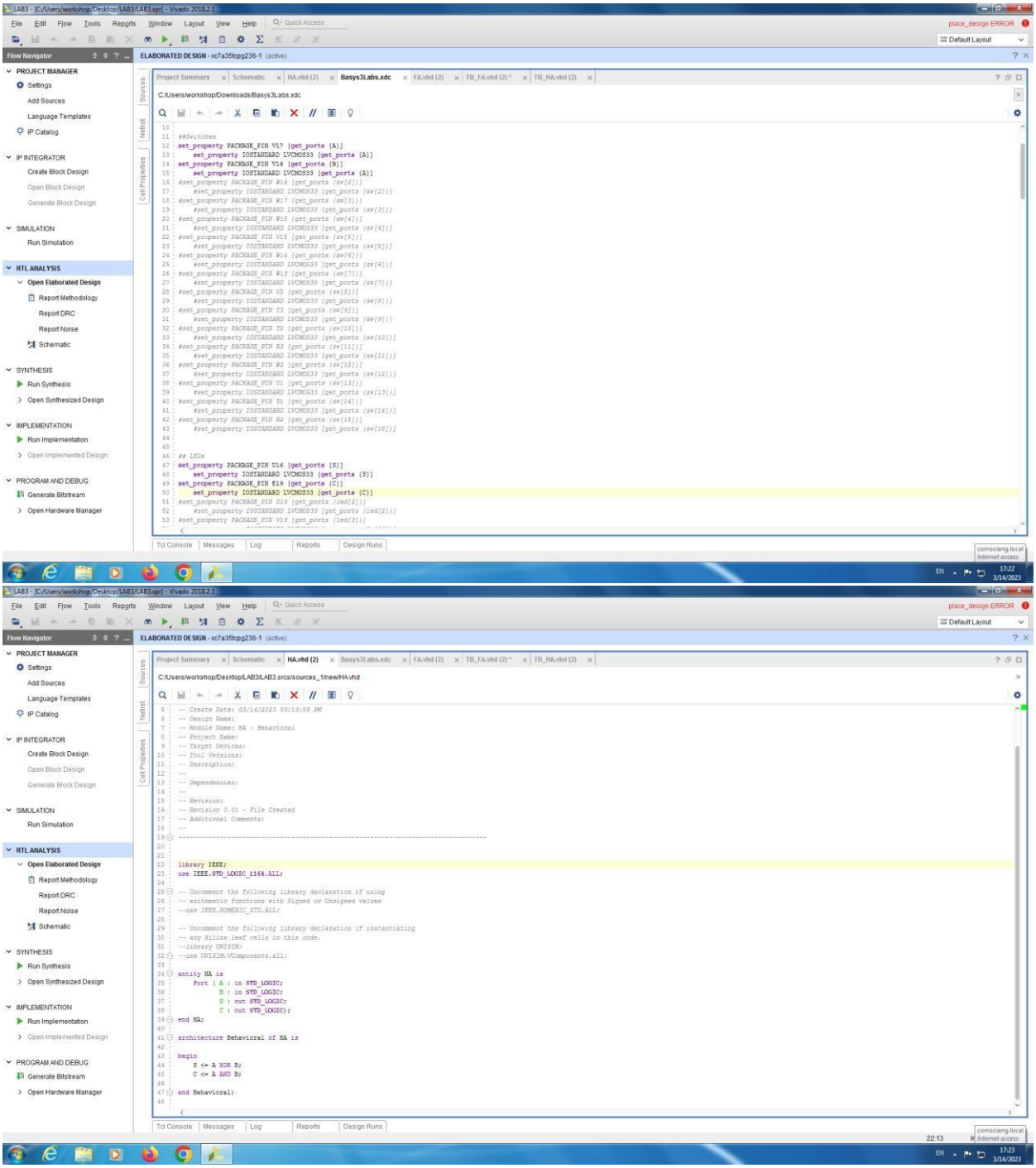
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
ELABORATED DESIGN - xc7a35tcpg236-1 (active)
Project Summary
Schematic
HA.vhd (2)
Basys3Labs.xdc
FA.vhd (2)
TB_FA.vhd (2) *
TB_HA.vhd (2)
C:/Users/workshop/Desktop/LAB3/LAB3.srcs/sources_1/new/FA.vhd
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity FA is
Port (A : in STD_LOGIC;
B : in STD_LOGIC;
C_in : in STD_LOGIC;
S : out STD_LOGIC;
C_out : out STD_LOGIC);
end FA;
architecture Behavioral of FA is
component HA
port (
A: in std_logic;
B: in std_logic;
S: out std_logic;
C: out std_logic);
end component;
SIGNAL HA0_S, HA0_C, HA1_S, HA1_C : std_logic;
begin
HA_0 : HA
port map (
A => A,
B => B,
S => HA0_S,
C => HA0_C);
HA_1 : HA
port map (
A => HA0_S,
B => C_in,
S => HA1_S,
C => HA1_C);
S <= HA1_S;
C_out <= HA0_C OR HA1_C;
end Behavioral;
Tcl Console
Messages
Log
Reports
Design Runs
comsciengl.local
Internet access
EN
17:22
3/14/2023



Some of the input combinations result in a carry bit. So we can't represent that by only 4 LEDs, because they represent only the 4bits of the result. So we need LD15 to represent the carry bit.

Conclusion

We learned that we can create 4 bit adder using FAs. And also we can create even larger adders using FAs.