

Each of the MCQ is out of 3 marks

The model Answer: b d d c e d

1. The output F of the circuit in Figure 1 is

- implemented as Product of Sum.
- $A + CD + (A + D')(C' + D)$.
- all of the above.
- $A' + C'D + (A + D')(C' + D)$.
- $A' + CD' + (A + D')(C' + D)$.

2. In Figure 1, F can be minimized using K-Map to

- $A'C'D + A'CD'$.
- $A + A'C'D' + A'CD$.
- $C'D' + CD + AC'D + ACD'$.
- $A + CD + C'D'$.
- $C'D' + CD + AC' + AC$.

3. What is/are the missing statement(s) in the following Verilog code that models the circuit in Figure 1?

```
module CircuitInFigure(A, B, C, D, F)
    input  A, B, C, D;
    output F;
    wire  j, k, l, m, n, Cp, Dp;
    not    (Cp, C);
    not    (Dp, D);
    and    (j, C, D);
    or     (k, A, Dp);
    or     (l, Cp, D);
    or     (m, A, j)
    :
    or     (F, m, n);
endmodule
```

- and (Cp, k, l);
- and (F, k, l);
- or (F, k, l);
- and (n, k, l);
- All of the above.

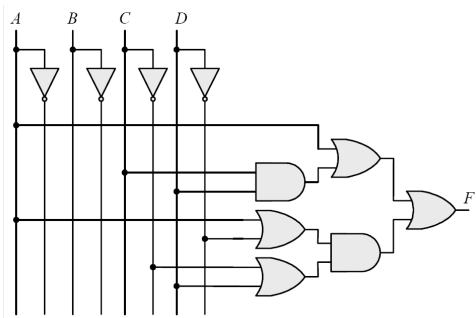


Figure 1

4. A circuit with one output, G , and 4 inputs, $w x y z$, generates 1 when the number of 1s in the input are **more than or equal** to the number of 0s. The output, $G =$

- $\prod(0, 1, 2, 4, 8)$.
- $\Sigma(3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15)$.
- all of the above.
- $\Sigma(7, 11, 13, 14, 15)$.

e) $\Sigma(0, 1, 2, 4, 8)$.

5. Now, assume that the inputs of the circuit in Question 4 will never take the values 0010 or 1000. Then, the best minimization leads to $G =$

- $wx + yz + xz + xy + wz + wy$.
- $w'x'yz' + wx'y'z'$.
- $w'y'z' + w'x'y'$.
- $x + z + wy + w'y'$.
- $w + y + xz$.

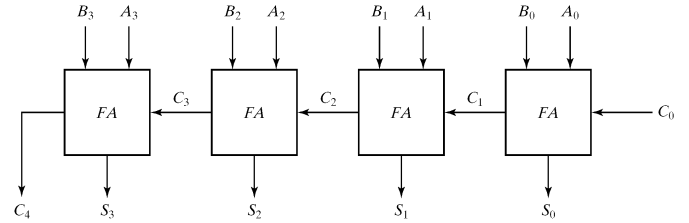


Figure 2. Each FA is a 1-bit Full Adder

6. In Figure 2, if $A = 1110$, $B = 0111$, and $c_0 = 0$ then

- $c_3 = 0$ and $s_2 = 0$.
- $c_3 = 0$ and $s_2 = 1$.
- $c_3 = 1$ and $s_2 = 0$.
- $c_3 = 1$ and $s_2 = 1$.
- c_3 and s_2 depend on the implementation of each FA.

7. In Figure 3

- F_1 is a synchronous circuit.
- $F_2 = A'B'C' + A'BC$.
- $F_3 = m_4 + m_5 + m_6$.
- the decoder output $m_6 = 0$.
- all of the above.

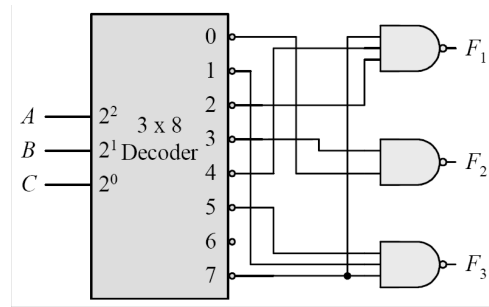


Figure 3

The following question is out of 10

8. Using an 8×1 MUX, implement the function:
 $F(w, x, y, z) = \Sigma(3, 5, 11, 14)$.