Helwan University
Faculty of Computers and Information

Department of Computer Science
Digital Design
Fall 2007

Homework 6

1- Using the appropriate F/F type, design a 4-bit register with parallel load, increment, and **synchronous** clear; write the function table of this register. Assume that the clear control is prior to load which is prior to increment, also assume that each F/F used has an asynchronous clear.

2- Using one IC binary counter, as the one that was designed in the previous problem, show how to obtain a counter counting from 5 to 13.

3- Design a 4-bit Shift Register that has a control to circulate the bits to the left by 1, 2 or 3 locations.

4- Design a Word-Time controller whose pulse width is 4 clock cycles using F/F's only. The Word-Time should start exactly after the end of triggering pulse which is synchronized with clock cycles.

5- Redesign the previous problem using one 4-bit counter dedicated to this Word-Time only; i.e., the counter should start and stop counting by the start and end of Word-Time.

6- Repeat the previous problem to make the counter free running without stopping to control other devices.
Hint: in this case you should detect the count number of the counter when applying the triggering signal then disable the Word-Time after the appropriate width without stopping the counter; this can be made by means of a parallel adder, register with parallel load, and external gates.

7- Using 4 IC binary counters, show how to obtain a 16-bit binary counter.