Helwan University
Faculty of Computers and Information

# Course Syllabus

Department of Computer Science
Digital Design

**Office Hours:** See webpage

**Prerequisites:** A little knowledge of Electronic Circuits is beneficial but not necessary.

**Objectives:** This course combines three approaches to teach students *Digital Design*, which is the fundamental prerequisite to understand computer design and architecture. First, and most importantly, theoretical aspects of the subject will be covered in lectures, along with exercises in sections. Students, by the end of the course, should be able to design, analyze, and implement combinational and synchronous digital circuits.

A second objective is to teach students the digital design using a Hardware Descriptive Language (HDL). Students by the end of the semester will be able to analyze logic circuits with Verilog (one of the available HDLs).

A third objective is to develop the practical sense of the students through lab. experiments. Students will be able to implement logic circuits using breadboards and ICs. If time permits, introduction to the Field Programable Gate Arrays (FPGA) technology will be given.

**Text:** Mano, M. M. and Ciletti, M. D. (2007), *Digital design*, Upper Saddle River, NJ: Prentice-Hall, 4th ed.
The book comes with a CD that includes a version of Verilog. You can also download Verilog from:
`http://www.syncad.com/syn_down.htm`

**Course Syllabus:** Fast introduction (few sections from Chapter 1) is offered and followed by detailed study of Chapters 2–7; very few sections will be skipped. At the end of each chapter Verilog code for some circuits will be explained. If time permits, Chapter 8 will be covered in full or in parts. Also, if time permits introduction to the FPGA technology will be given.

**Assignments:** Assignments will include both, problems and computer programs in Verilog to analyze some circuits. Some of the sections (around 3) will be dedicated to running experiments on breadboards in the Electronics lab.

**Course Project:** Every group, typically around 5 students, should be formed by the end of second week in the semester. Members of every group have to register their names with their TA and take a numerical group number that will be the ID of this group. By the mid-term, every group has to settle on a course project to implement. Simulation of the circuits should be carried out first by Verilog before hardware implementation. After making sure of the simulated performance, circuits should be hardware implemented on breadboards.
**Hint:** In labs., all of the groups running experiments should be the same groups as those of the course project. This is why all of the groups should be formed by the end of second week.

**Grading Policy:**

- 60% of the grade will be on the final exam.
- 10% on the midterm.
- 10% on homework, lab-work, and class participation. Solving assignments, in both formats the paper-and-pencil and computer exercises, is crucial for acquiring the skills to solve the exam. **No late assignments please.**
- 20% of the grade will be given on the course project and the oral exam. Every group, at the time of practical exam, will present and defend their project. The 20% will be given on the project simulation by Verilog, hardware implementation, and project defense (oral exam).

**General Info:**

- All handouts, grades, and assignments will be posted on the course webpage.
- Final exam will be in the form of Multiple Choice Questions (MCQ). Every question will have five answers, one of them is correct. Every four wrong answers cancel one correct answer. Exams will be open book. So, focus in your course on learning and understanding **NOT** on memorizing.