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Digital Design
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Homework 4 (cont.)

1. An error comparator is required to compare two 2-bit binary numbers **A** and **B** and give three separate outputs for the conditions **A**=**B**, **A**>**B**, and **A**<**B**. Design a combinational logic circuit that will perform this function and implement the design using NAND gates.

2. A circuit receives two 2-bit binary numbers **X**=xo x1 and **Y**=y0 y1. The 2-bit output **Z**=z1 z0 should equal 11 if **X=Y**, 10 if **X>Y**, and 01 if **X<Y**. Design a minimal sum of product realization. (This circuit is called a 2-bit magnitude comparator.)

3. If only two 2-bit magnitude comparators (as designed above) are available, how can you use them to build a 4-bit magnitude comparator? A 4-bit magnitude comparator is similar to a 2-bit magnitude comparator except that it receives two 4-bit numbers as its inputs.
   Hint: Use a minimal number of additional **NAND** gates.

4. Design a combinational logic circuit that produces the product of two numbers **A**= (a1 a2) and **B**= (b1 b2). The product is in the form **P**= (p1 p2 p3 p4) where a1, b1 and p1 are the most significant digits. Give the expressions of p1, p2, p3, and p4 and simplify using Karnaugh-maps. Compare this design to the design of the book that uses 4 AND Gates and 2 Half-Adders from the following points of view (**this part is very Important**):

   a. the difficulty of the design.
   b. the complexity of the circuit.
   c. the speed of the circuit.

5. Design a combinational logic circuit that produces the product of two binary numbers **A**=a1 a0 and **B**=b2 b1 b0, **A** ranges from 0-3 while **B** ranges from 0 to 5. How many output bits are required? Give a minimal SOP expression for each output bit. Redesign this circuit using AND Gates and half-adders; compare as above.

6. There are four adjacent parking slots in a parking area. Each slot is equipped with a special sensor whose output is **LOW** when a car is occupying the slot and **HIGH** otherwise. It is required to design and implement a decoding system that generates a **LOW** output if and only if there are two or more adjacent empty slots.

7. The table below gives a price list of some computer languages manuals.

MANUAL	PRICE
Turbo C	45 L.E
Turbo Pascal	30 L.E
Turbo Assembler	15 L.E
Turbo Prolog	10 L.E

   It is required to design a logic circuit that gives a HIGH output when you cannot buy a given set of manual if you have only 50 L.E. Implement the circuit using (a) **NOR** gates only and (b) **OR-NAND** combination.

8. It is desired to design and implement a combinational circuit that has four inputs **A,B,C,** and **D** and one output **F**. **F** should equal 1 if **A** = 1 independently of the values of the other inputs. If **A**=0, however, **F** should be 1 if **B**=1 independently of the values of the remaining two inputs. If both **A** and **B** are 0s, then **F** is 1 if **C** is 1. However, if both **A, B** and **C** are 0s, the **F** should equal **D**.

9. Implement a full-subtractor with two half-subtractors and an OR Gate.

10. Implement a full-adder using two 2-by-4 decoders (with enable inputs), an inverter, and two OR Gates.

11. Using only 2-by-1 MUXs implement a half-adder.