Helwan University
Faculty of Computers and Information

Department of Computer Science
Digital Design
Fall 2007

Homework 5 (a)

1. Give the circuit symbol ,the excitation table and the characteristic equation of each of the following flip-flops:

   R-S flip-flop.
   D flip-flop.
   J-K flip-flop.
   T flip-flop.

2. A set dominate flip-flop has a set and a reset input. It differs from a conventional R-S flip-flop in that an attempt to simultaneously set and reset results in setting the flip-flop.

   Obtain the characteristic table and characteristic equation for such a flip-flop.
   Obtain a logic diagram for an asynchronous set-dominate flip-flop.

3. Beginning with an R-S flip-flop show how to get

   D flip-flop.
   J-K flip-flop.
   T flip-flop.

4. Beginning with an D flip-flop show how to get

   J-K flip-flop.
   T flip-flop.

5. Beginning with an J-K flip-flop show how to get

   D flip-flop.
   T flip-flop.

6. Beginning with an T flip-flop show how to get

   D flip-flop.
   J-K flip-flop.

7. Implement a new flip-flop type, called X-Y flip-flop, that has the following truth table

X	Y	Q(t+1)
0	0	Reset
0	1	Q(t)
1	0	Q'(t)
1	1	Set

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Homework 5 (b)

1. Draw the state diagram only for a clocked sequential circuit that has one input X and one output Z. The output Z is required to be 1 if four consecutive 1's appear at the input X. For example, if: X: 1011110111110 then Z: 0000010000110

2. Draw only the state diagram for a clocked synchronous circuit that has one input X and one output Z for each of the following cases.
- **a.** Z=1 when two consecutive 1's appear at the input. the next input causes Z to be 0.for example, if: X: 01100111110 then Z: 00100010100
- **b.** To detect the sequence 101, overlap permissible. For example, if: X: 010101101 then Z: 000101001
- **c.** As part(b)but without overlapping. For example, if: X: 010101101 then Z: 000100001

3. A long sequence of pulses enters a one-input/one-output synchronous circuit. The input is X and the output is Z which equals 1 whenever the sequence 1111 occurs. Overlapping sequences are accepted. For example if: X: 01011111 then Z: 00000011
- **a.** Draw the state diagram.
- **b.** Select an assignment and show the excitation and output tables.
- **c.** Write down the excitation functions for S-R flip-flops and draw the corresponding logic diagram.

4. Repeat problem (3) for the sequence 01101 and implement the circuit using T flip-flops as memory elements.

5. Design a modulo-8 counter which counts in the way specified in Fig 1; use J-K flip-flops in your realization.

6. Design a sequential synchronous circuit which examines its input X sequence in non-overlapping strings of three pulses and produces 1 at the output, Z, if and only if the string consists of either two or three 1's.use R-S flip-flops in your realization. An example of input and output sequences is this: X: 010101110 then Z: 000001001

7. Design a synchronous sequential circuit that produces an output Z=1 whenever any of the input sequences 1100, 1010, or 1001 occurs. The circuit resets to its initial state after a logic 1 output has been generated. Use J-K flip-flops in your implementation.

8. A sequential circuit has two J-K flip-flops, one input x, and one output y. The logic diagram of the circuit is shown in Fig.1. Derive the state table and state diagram, hence the timing diagram, of the circuit. For the timing diagram assume that the input x has the following sequence: 10011.

Decimal	Gray Code
0	000
1	001
2	011
3	010
4	110
5	111
6	101
7	100

Table 1

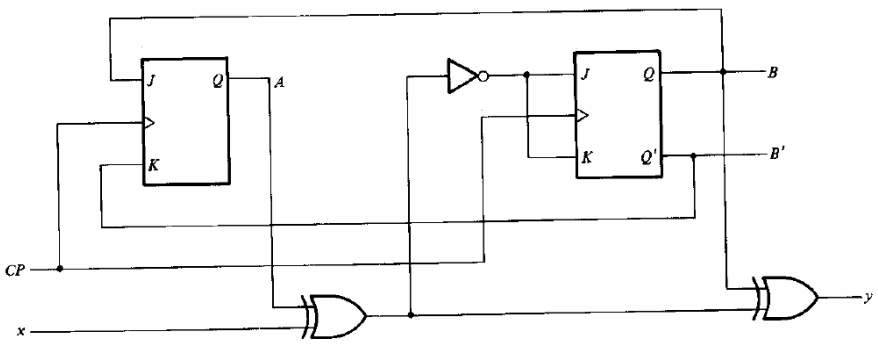

Figure 1