MPEG2 forward DCT 8x8 with Vivado HLS

Daniele Bagni: DSP Specialist for EMEA

July 2015

Outlines

- **Background:**
  - Part 1: DCT
  - Part 2: JPEG baseline
- **Forward Wang's DCT with Vivado HLS**

Background: DCT

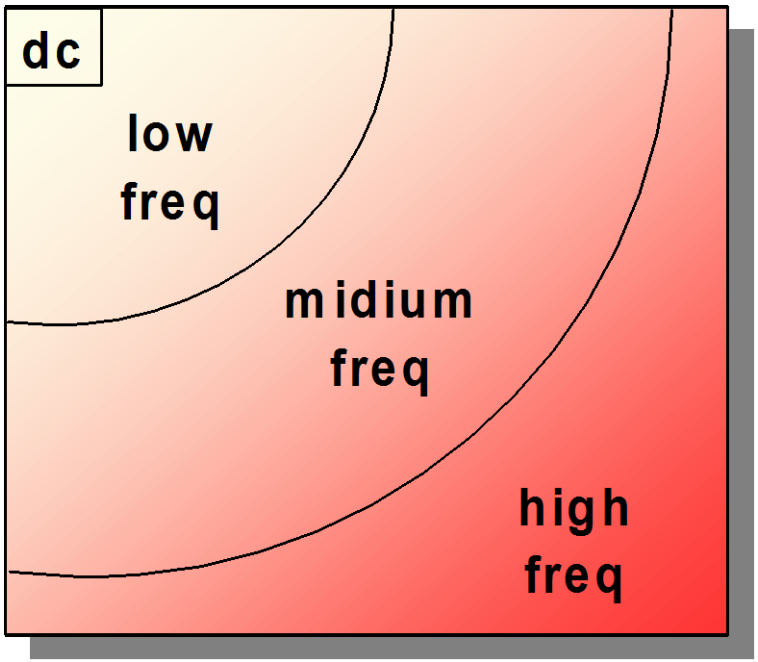
Daniele Bagni
EMEA DSP Specialist FAE

Part 1: DCT

- DCT overview
- 2-D DCT
- 1-D DCT
- Matrix formalism (1-2)
- DCT basis functions
- Blocking Artifacts (1-6)
- Wang's algorithm DCT (1-2)
- AAN's algorithm (1-2)

DCT overview 1/2

The DCT concentrates most of the pixels energy distribution into a few frequency coefficients



DCT overview 2/2

- **DCT is a valuable tool for pictures compression, when associated with Quantization and VLC**
- **The transform itself does not compress images and it is accurately reversible**
- **DCT is a separable transform: 2-D F-DCT and I-DCT can be done as consecutive 1-D transforms**

2-D DCT

- **The MPEG-2 standard defines an F-DCT that produces coefficients F(u,v) according to:**

$$F(u, v) = 1/4\, C(u)\, C(v) \left\{ \sum_{x=0}^{7} \sum_{y=0}^{7} f(x, y) \cos \frac{(2x + 1)\, u\pi}{16} \cos \frac{(2y + 1)\, v\pi}{16} \right\}$$

- **The inverse I-DCT is defined as:**

$$f(x, y) = 1/4 \left\{ \sum_{u=0}^{7} \sum_{v=0}^{7} C(u)\, C(v)\, F(u, v) \cos \frac{(2x + 1)\, u\pi}{16} \cos \frac{(2y + 1)\, v\pi}{16} \right\}$$

with:

$$C(u), C(v) = 1 \quad u \neq v \neq 0$$

$$C(u), C(v) = 1/\sqrt{2} \quad u=v=0$$

1-D DCT

- $F(u,v)= C_v/2 \Sigma_y \cos((2y+1)\pi v/16) [C_u/2 \Sigma_x f(x,y) \cos((2x+1)\pi u/16)]$

  vertical direction **[horizontal direction]**

- **1-D F-DCT:**

  $F(u)= C_u/2 \Sigma_x f(x) \cos((2x+1)\pi u/16)$

  - **ex: $F(1)= 1/2 [f(0)\cos\pi/16 + f(1)\cos3\pi/16 + f(2)\cos5\pi/16 + \ldots]$**

- **1-D I-DCT:**

  $f(x)= \Sigma_u C_u/2 F(u) \cos((2x+1)\pi u/16)$

Matrix formalism 1/2

- **In matrix notation:**
  - **$F = C \quad f$**
  - **$f = C^{-1} \; F$**
  - **with F and f respectively matrices of DCT coefficients and pixel values,**
  - **C and C^{-1} representing the F- and I- DCT matrix.**

- **F-DCT and the I-DCT are ortho-normal transforms:**
  - **$C^T C = I \implies C^T = C^{-1}$**

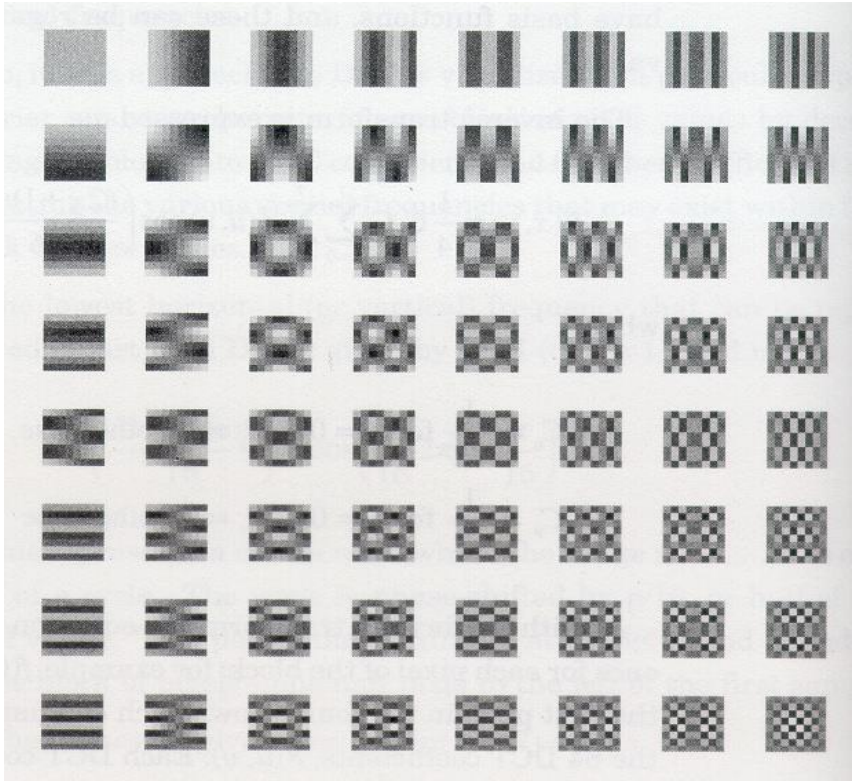
Matrix formalism 2/2

- **C is the transform matrix (8x8), derived as:**

$$C_8^{II} = \begin{bmatrix} \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} & \frac{c_0}{\sqrt{2}} \\ c_1 & c_3 & c_5 & c_7 & c_9 & c_{11} & c_{13} & c_{15} \\ c_2 & c_6 & c_{10} & c_{14} & c_{18} & c_{22} & c_{26} & c_{30} \\ c_3 & c_9 & c_{15} & c_{21} & c_{27} & c_{33} & c_{39} & c_{45} \\ c_4 & c_{12} & c_{20} & c_{28} & c_{36} & c_{44} & c_{52} & c_{60} \\ c_5 & c_{15} & c_{25} & c_{35} & c_{45} & c_{55} & c_{65} & c_{75} \\ c_6 & c_{18} & c_{30} & c_{42} & c_{54} & c_{66} & c_{78} & c_{90} \\ c_7 & c_{21} & c_{35} & c_{49} & c_{63} & c_{77} & c_{91} & c_{105} \end{bmatrix}^T$$

$$c_n = \cos\left(\frac{n\pi}{16}\right)$$

DCT basis functions



From Video Compression (Peter D. Symes, Mc Graw Hill):

"Each DCT coefficient has an associated basis function, that is, the pixels pattern that results when that particular DCT coefficient is set to its maximum value, and all the other coefficients are set to zero.

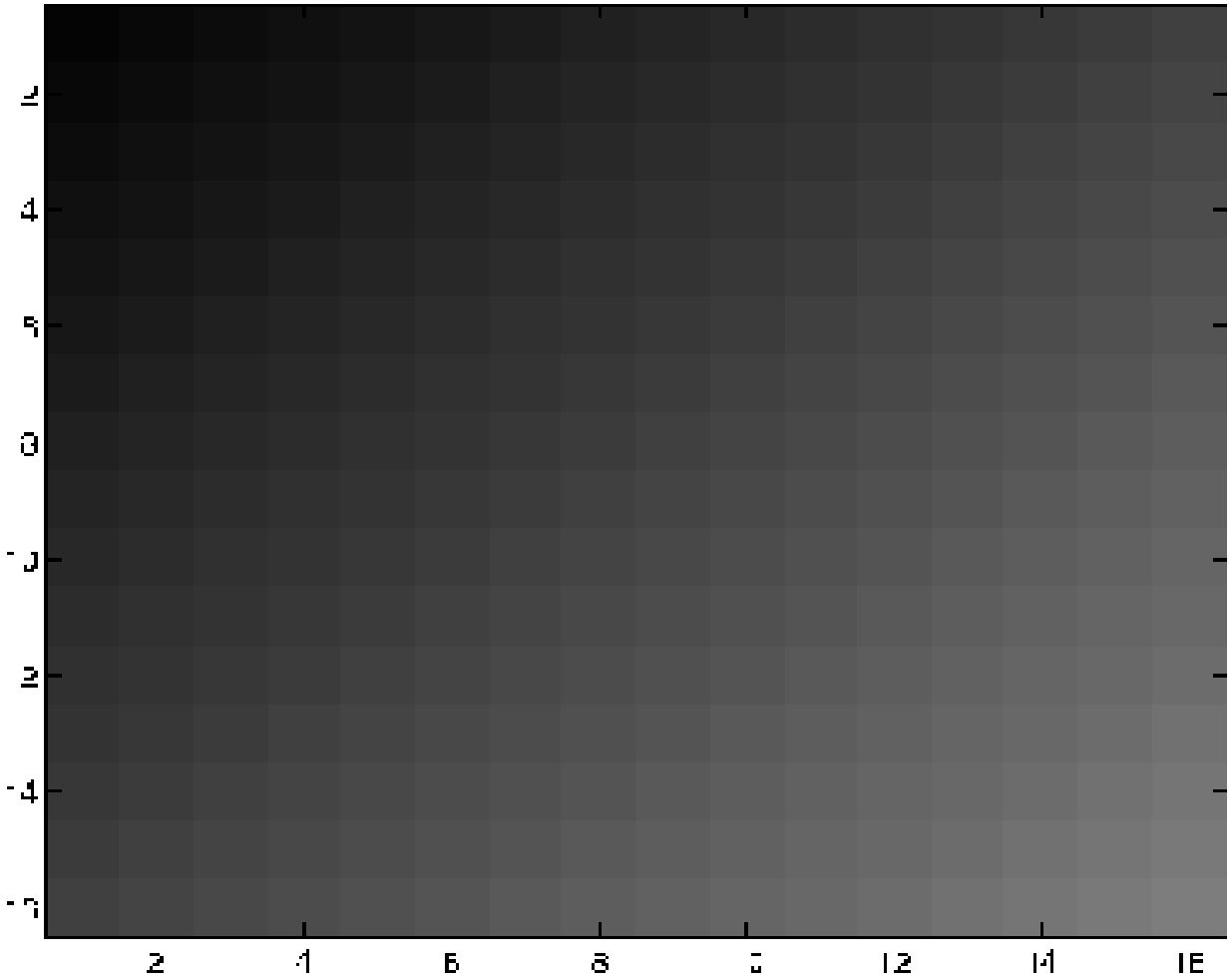
The basis functions represent 64 different arrays of pixel values. Given a set of DCT coefficients, the IDCT consists of multiplying each basis function by its corresponding coefficient."

Blocking Artifacts 1/6

- **When DCT is combined with quantization, the reconstructed images exhibit visually annoying artifacts, named Blocking and Ringing noise.**
- **These artifacts are basically due to quantization that suppresses the high frequency DCT coefficients with lower values.**

- **Blocking noise: a luminance discontinuity present at block boundaries (on 8x8 pixels and lines).**
- **Ringing or mosquito noise: the effect that quantization has over a sharp edge in a flat (luminance) region.**

Blocking Artifacts 2/6

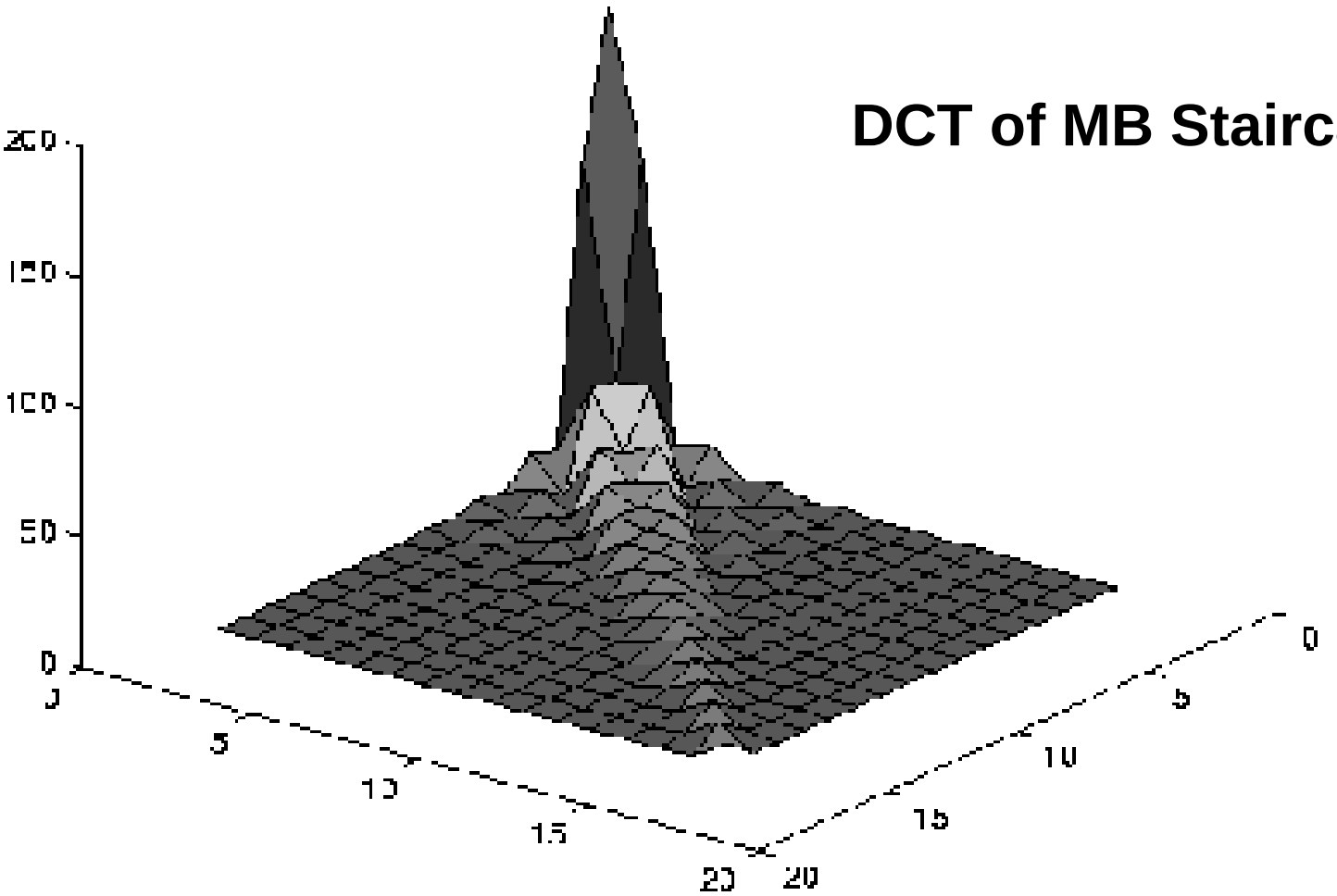


MB Luminance Staircase:

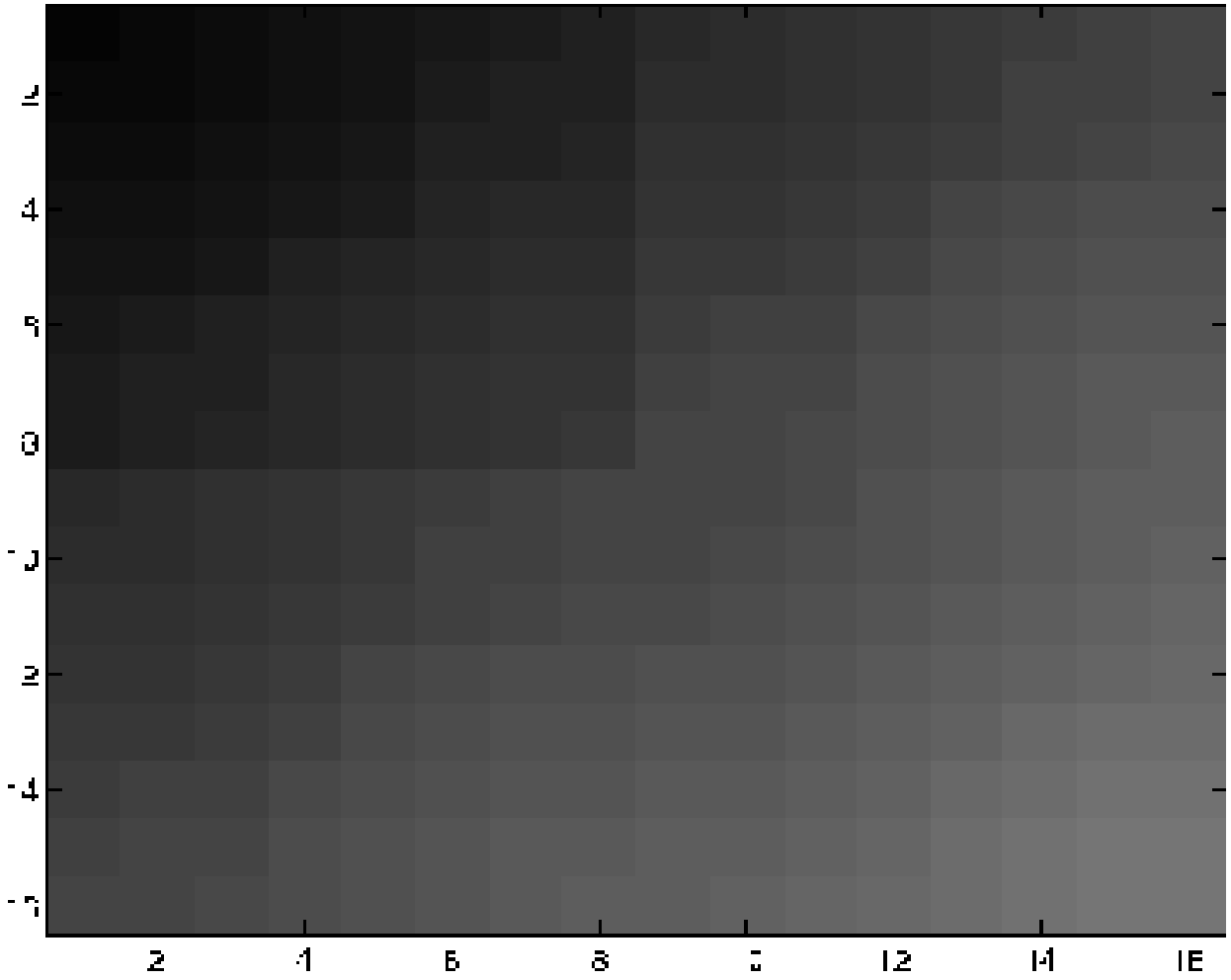
f(x,y) = x + y

with x, y = 1..8

Blocking Artifacts 3/6



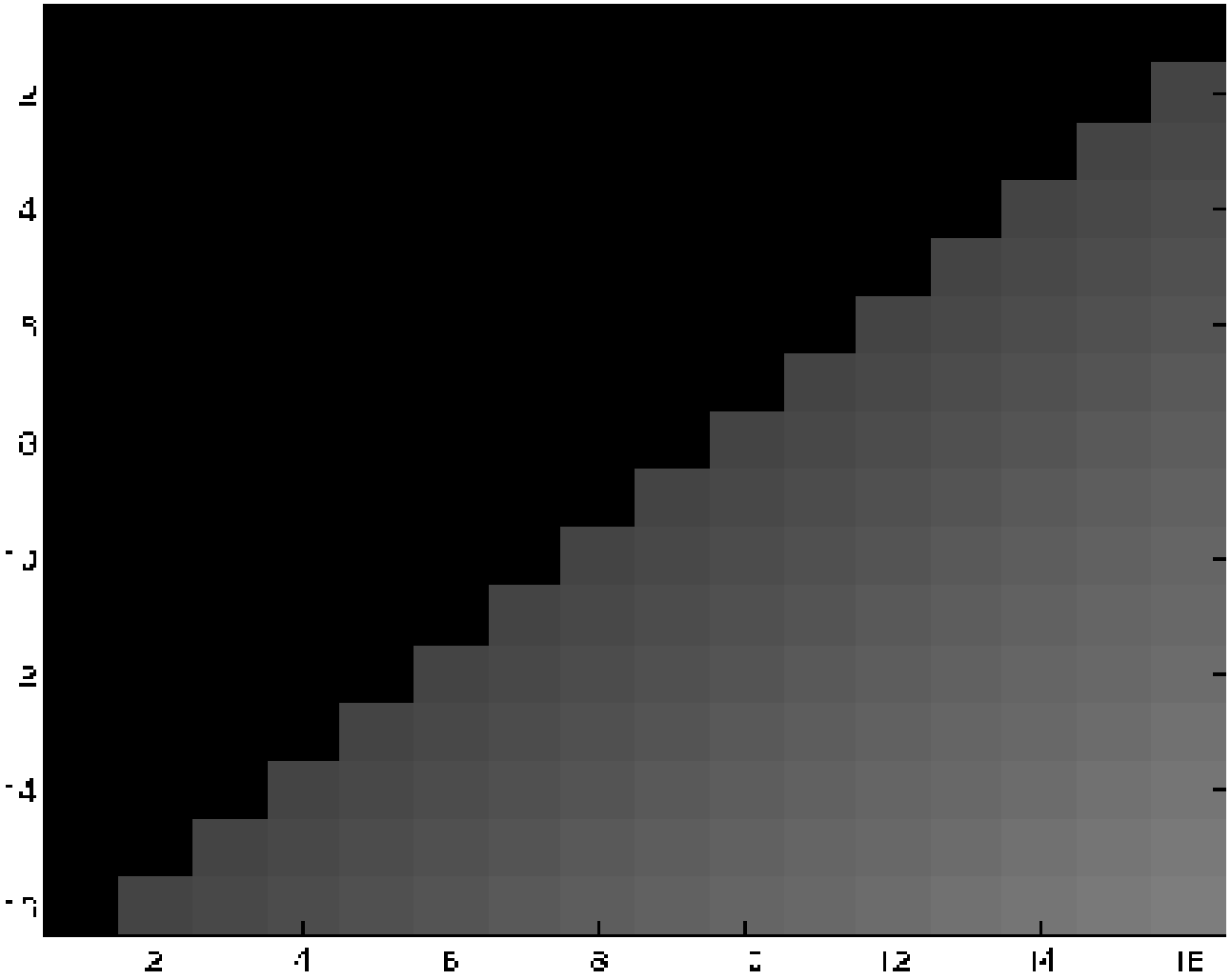
Blocking Artifacts 4/6



MB Staircase, quantized by Q=18

Blocking Noise: the reconstructed Macro-block has very visible discontinuities at the boundary of the four blocks.

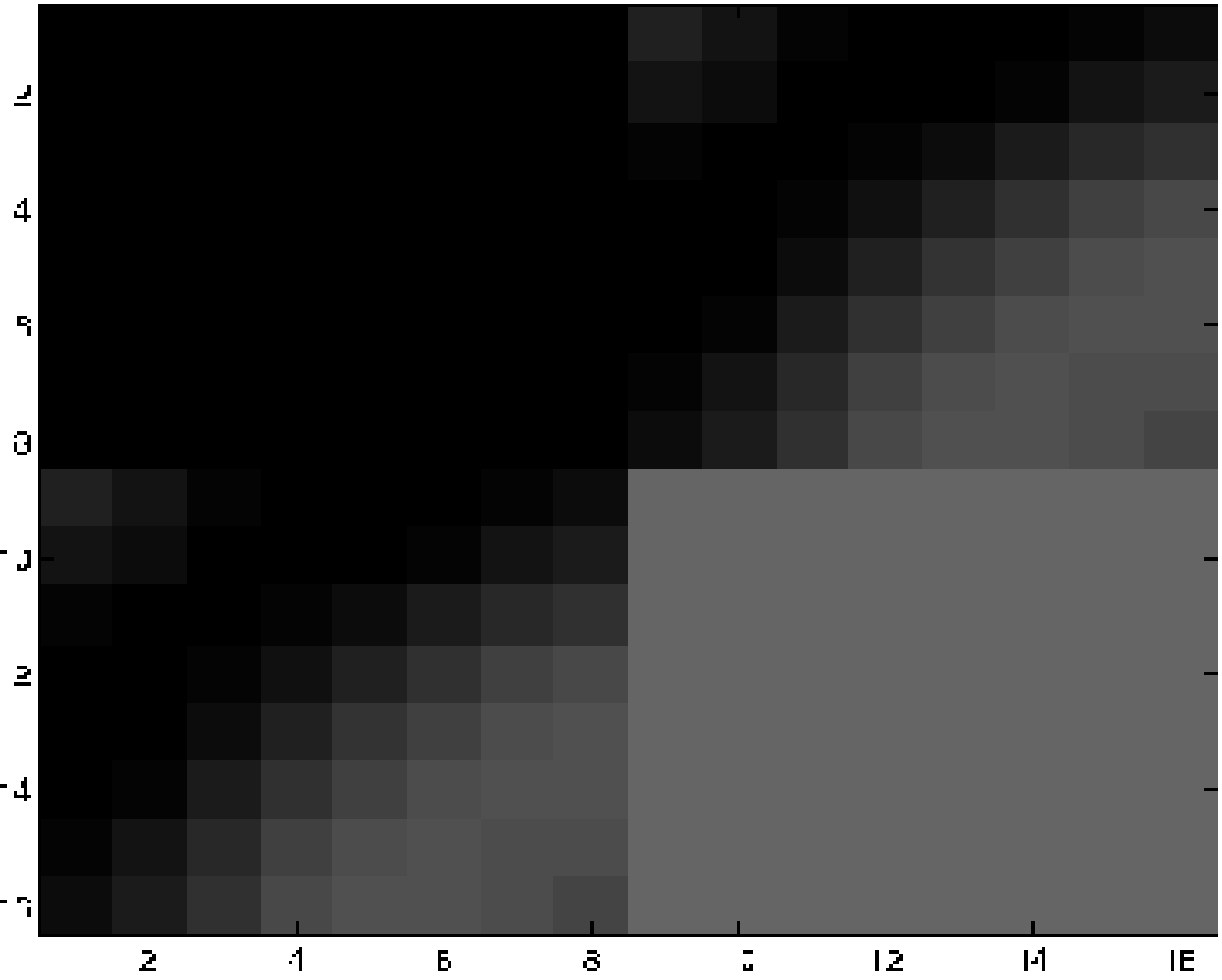
Blocking Artifacts 5/6



Linear ramp MB luminance:

f(x, y) = x + y
if x + y > 17
elsewhere
f(x, y) = 0

Blocking Artifacts 6/6



Linear ramp MB luminance quantized by Q=18

The blocks in top-left and bottom-right positions have only the DC coefficient.

Ringing noise in bottom-left and top-right blocks.

Grid noise in top-left and bottom-right blocks.

Wang's IDCT algorithm 1/2

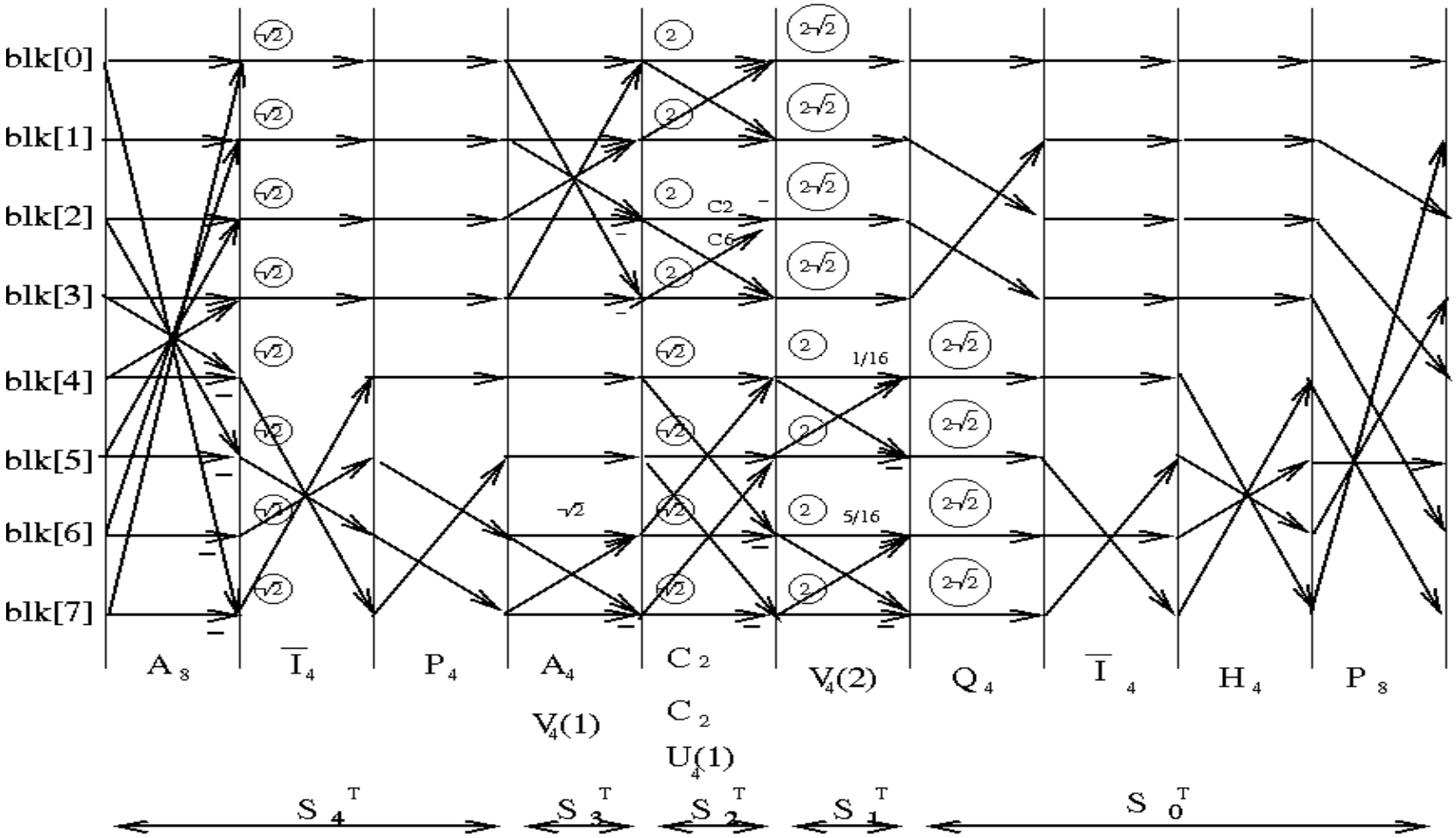
- **Wang's 8-points IDCT uses only 29 *add* and 11 *mult* instead of the 56 *add* and 64 *mult* required theorically.**
- **Wang's algorithm is a 5-stages approach, based on sparse matrices:**

$$IDCT = S_4^T \cdot S_3^T \cdot S_2^T \cdot S_1^T \cdot S_0^T$$

- **Butterfly multiplications (rotations) are reduced as in the following (*A=cosa, B=sena*):**

$$\begin{aligned} x_4 &= A*x_4 + B*x_5 \\ x_5 &= B*x_4 - A*x_5 \end{aligned} \longrightarrow \begin{aligned} x_8 &= B*(x_4 + x_5) \\ x_4 &= x_8 + (A-B)*x_4 \\ x_5 &= x_8 - (A+B)*x_5 \end{aligned}$$

Wang's IDCT algorithm 2/2



Forward DCT with Vivado HLS: design & performance

Daniele Bagni
EMEA DSP Specialist FAE

DCT example from HLS Tutorial

- **This DCT example comes from the Vivado HLS tutorial (UG871):**
  - Chapter6: “Design Analysis”
  - Lab 1

DCT ex. from HLS tutorial: code

my_dct.cpp

```
1
2  #include "dct.h"
3
4  // REMEMBER TO SCALE BY 8 THE OUTPUT RESULTS (>>3)
5
6  void new_dct_1d(dct_data_t src[N], dct_data_t dst[N], char off)
7  {
8  #pragma HLS PIPELINE
9     unsigned char k, n;
10    int tmp;
11    const dct_data_t dct_coeff_table[DCT_SIZE][DCT_SIZE] = {
12     #include "dct_coeff_table.h"
13    };
14
15 DCT_Outer_Loop:
16    for (k = 0; k < DCT_SIZE; k++) {
17 #pragma HLS PIPELINE
18 DCT_Inner_Loop:
19       for(n = 0, tmp = 0; n < DCT_SIZE; n++) {
20 #pragma HLS UNROLL factor=8
21 #pragma HLS PIPELINE
22          int coeff = (int)dct_coeff_table[k][n];
23          tmp += src[n] * coeff;
24       }
25       dst[k*DCT_SIZE+off] = DESCALE(tmp, CONST_BITS);
26    }
27 }
28
```

```
29 void my_dct(dct_data_t in_block[N], dct_data_t out_block[N])
30 {
31 #pragma HLS INLINE
32
33    dct_data_t row_outbuf[N];
34    unsigned char i, j;
35
36    // DCT rows
37 Row_DCT_Loop:
38    for(i = 0; i < DCT_SIZE; i++) {
39 #pragma HLS PIPELINE
40       new_dct_1d(in_block+DCT_SIZE*i, row_outbuf, i);
41    }
42
43
44    // DCT columns
45 Col_DCT_Loop:
46    for (i = 0; i < DCT_SIZE; i++) {
47 #pragma HLS PIPELINE
48       new_dct_1d(row_outbuf+DCT_SIZE*i, out_block, i);
49    }
50
51
52 }
53
54
55
56
57 void top_fdct(dct_data_t in_block[N], dct_data_t out_block[N])
58 {
59 #ifdef DB_ORIGINAL
60     my_dct(in_block, out_block);
61 #else
62     wang_fdct(in_block, out_block);
63 #endif
64 }
```

DCT ex. from HLS tutorial: Synthesis Estimation & CoSimulation reports

Synthesis(solution_tutorial)

Product family: kintex7

Target device: xc7k325tffg900-2

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	4.00	3.41	0.50

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
83	83	84	84	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	12
FIFO	-	-	-	-
Instance	-	48	2012	772
Memory	1	-	0	0
Multiplexer	-	-	-	86
Register	-	-	37	2
Total	1	48	2049	872
Available	890	840	407600	203800
Utilization (%)	~0	5	~0	~0

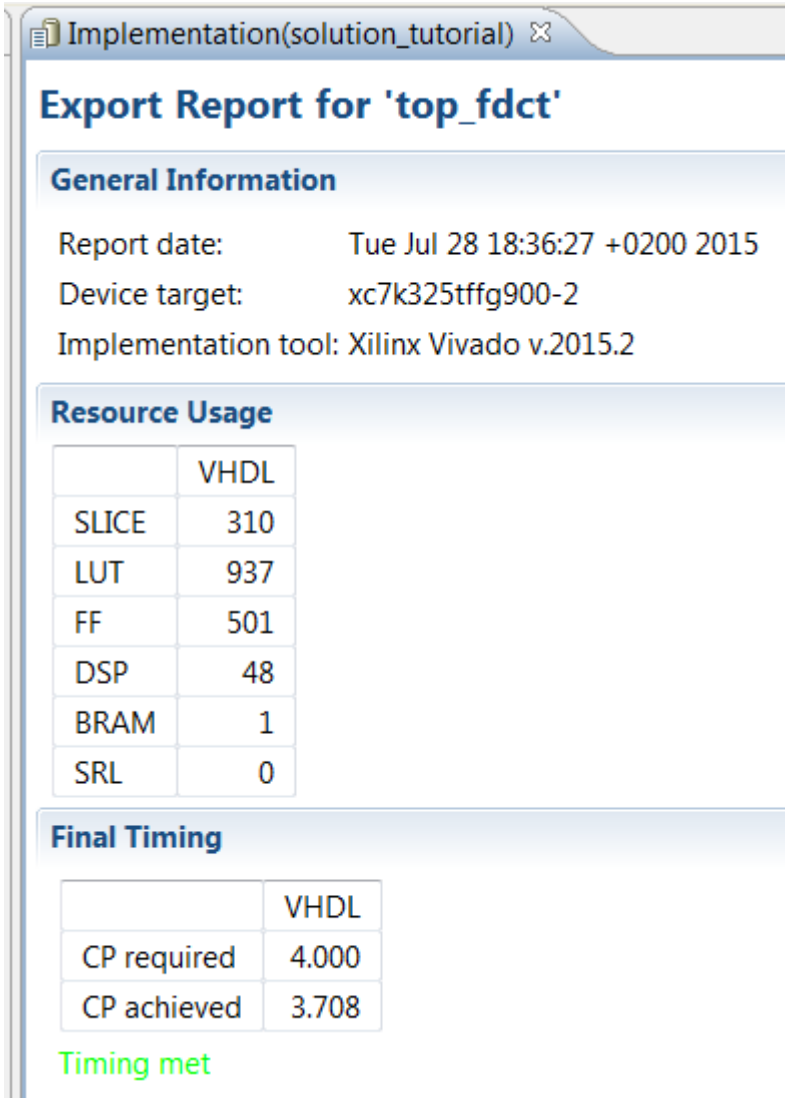
Simulation(solution_tutorial)

Cosimulation Report for 'top_fdct'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	83	83	83	84	84	84

DCT ex. from HLS tutorial: Implementation report



Implementation(solution_tutorial)

Export Report for 'top_fdct'

General Information

Report date: Tue Jul 28 18:36:27 +0200 2015
Device target: xc7k325tffg900-2
Implementation tool: Xilinx Vivado v.2015.2

Resource Usage

	VHDL
SLICE	310
LUT	937
FF	501
DSP	48
BRAM	1
SRL	0

Final Timing

	VHDL
CP required	4.000
CP achieved	3.708

Timing met

- **Kintex7 325T-2 FPGA**
- **Results after Place-And-Route:**
  - 937 LUT
  - 501 FF
  - 48 DSP48
  - 83 clock cycles latency
  - 269MHz clock frequency

Wang's DCT: rationale

- **The TM5 MPEG-2 encoder reference C model applies fixed point Wang's IDCT algorithm (see slides at pp. 18-19)**
- **By reversing such a flow (plus some changes) the C code of the forward DCT can be derived**

Wang's DCT: Synthesis Estimation & CoSimulation reports

Synthesis(solution_wang)

Product family: kintex7

Target device: xc7k325tffg900-2

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	4.00	3.41	0.50

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
91	91	92	92	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	12
FIFO	-	-	-	-
Instance	-	11	838	637
Memory	1	-	0	0
Multiplexer	-	-	-	87
Register	-	-	39	2
Total	1	11	877	738
Available	890	840	407600	203800
Utilization (%)	~0	1	~0	~0

Simulation(solution_wang)

Cosimulation Report for 'top_fdct'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	91	91	91	92	92	92

Wang's DCT: Implementation report

Export Report for 'top_fdct'

General Information

Report date: Tue Jul 28 18:44:21 +0200 2015
Device target: xc7k325tffg900-2
Implementation tool: Xilinx Vivado v.2015.2

Resource Usage

	VHDL
SLICE	254
LUT	710
FF	702
DSP	11
BRAM	1
SRL	0

Final Timing

	VHDL
CP required	4.000
CP achieved	3.573

Timing met

- **Kintex7 325T-2 FPGA**
- **Results after Place-And-Route:**
  - 710 LUT
  - 702 FF
  - 11 DSP48
  - 1 BRAM
  - 91 clock cycles latency
  - 279MHz clock frequency

Performance comparison

- **On the right, the Synthesis Estimations comparison**
- **Below, the effective results after Place-And-Route:**
  - Lab1 tutorial:
    - 937 LUT, 501 FF, 48 DSP48
    - 269MHz clock freq
  - Wang's DCR:
    - 710 LUT, 702 FF, 11 DSP48, 1 BRAM
    - 279MHz clock freq
- **Wang's DCT is more efficient from area point of view**

Vivado HLS Report Comparison

All Compared Solutions

solution_tutorial: xc7k325tffg900-2

solution_wang: xc7k325tffg900-2

Performance Estimates

Timing (ns)

Clock		solution_tutorial	solution_wang
ap_clk	Target	4.00	4.00
	Estimated	3.41	3.41

Latency (clock cycles)

		solution_tutorial	solution_wang
Latency	min	83	91
	max	83	91
Interval	min	84	92
	max	84	92

Utilization Estimates

	solution_tutorial	solution_wang
BRAM_18K	1	1
DSP48E	48	11
FF	2049	877
LUT	872	738