苏州诺存微电子有限公司 机密信息 NOR-MEM Confidential 2019
NM25Q64EVB

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3 V, 64 M-BIT<x 1/x 2/x

4>SERIAL MULTI I/O

3伏64兆位< x 1 /x 2 /x 4 >

串行多路输入/输出

FLASH MEMORY
闪存

Key Features
Key Features

- Protocol Support - Single I/O, Dual I/O and Quad
- I/O Protocol Support - Single I/O, Dual I/O and Quad I/O
- Quad Peripheral Interface(QPI) available
- Quad Peripheral Interface(QPI) available
- Support clock frequency up to 104MHz
- Support clock frequency up to 104MHz

Contents
内容

1. FEATURES
2. 特征

GENERAL
一般

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 支持串行外设接口-模式 0 和模式 3
- Single Power Supply Operation
- 单电源操作
  - 2.7 to 3.6 volt for read, erase, and program operations
  - 用于读取、擦除和编程操作 2.7 到 3.6 伏
- 64Mb: 67,108,864 x 1 bit structure or 33,554,432 x 2 bits (Dual I/O mode) structure or 16,777,216 x 4bits (Quad I/O output mode) structure
- 64Mb：67，108，864 x 1 位结构或 33，554，432 x 2 位(双 I/O 模式)结构或 16，777，216 x 4 位(四 I/O 输出模式)结构
- Protocol Support
- 协议支持
  - Single I/O, Dual I/O and Quad I/O
  - 单输入/输出、双输入/输出和四输入/输出
- Fast frequency support
- 快速频率支持
  - Support clock frequency up to
  - 支持时钟频率高达
    - Single I/O mode: 104MHz
    - 单一输入/输出模式:104MHz
    - Dual I/O mode: 104MHz
    - 双 I/O 模式:104MHz
    - Quad I/O mode: 104MHz
    - 四路 I/O 模式:104MHz
  - Configurable dummy cycle number for fast read operation
  - 快速读取操作的可配置虚拟周期数
- Quad Peripheral Interface (QPI) available
- 提供四外设接口(QPI)
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each, or Equal Blocks with 64K byte each
- 每个具有 4K 字节相等扇区，或者每个具有 32K 字节的相等块，或者每个具有 64K 字节的相等块
  - Any Sector/Block can be erased individually
  - 任何扇区/块都可以单独擦除
- Programming :
- 编程:
  - 256byte page buffer
  - 256 字节页面缓冲区
  - Quad Input / Output page program(4PP) to enhance program performance

- 增强程序性能的四输入/输出页面程序(4PP)

- Typical 100,000 erase/program cycles
- 典型的 100，000 次擦除/编程周期
- 20 years data retention
- 20 年数据保留

SOFTWARE FEATURES

软件功能

- Input Data Format
- 输入数据格式
  - 1-byte command code
    - 1 字节命令代码
- Advanced Security Features
- 高级安全功能
  - Block lock protection
  - 块锁定保护
  - The BP0-BP3 and TB status bits define the size of the area to be protected against program and erase commands
  - BP0-BP3 和 TB 状态位定义了受编程和擦除命令保护的区域大小
  - Individual Block/Sector array Protection
  - 单个数据块/扇区阵列保护
- Additional 2 x 8K bit security Registers with OTP Locks
- 带 OTP 锁的附加 2 x 8K 位安全寄存器
- Command Reset
- 命令复位
- Program/Erase Suspend and Resume operation
- 编程/擦除暂停和恢复操作
- Electronic Identification
- 电子识别
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - JEDEC 1 字节制造商 ID 和 2 字节器件 ID
  - RES command for 1-byte Device ID
  - 1 字节设备 ID 的 RES 命令
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
  - 1 字节制造商 ID 和 1 字节设备 ID 的 REMS 命令

- Support Serial Flash Discoverable Parameters (SFDP) mode
- 支持串行闪存可发现参数(SFDP)模式

HARDWARE FEATURES
硬件功能

- SCLK Input
- SCLK 输入
  - Serial clock input
  - 串行时钟输入
- SI/SIO0
- 硅/氧化硅
  - Serial Data Input or Serial Data Input/Output for 2 x I/O and 4 x I/O read mode
  - 2 x I/O 和 4 x I/O 读取模式的串行数据输入或串行数据输入/输出
- SO/SIO1
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O and 4 x I/O read mode
  - 2 x I/O 和 4 x I/O 读取模式的串行数据输出或串行数据输入/输出
- WP#/SIO2
- WP #/二氧化硅
  -Hardware write protection or serial data Input/Output for 4 x I/O read mode
  4 x I/O 读取模式的 Hardware 写保护或串行数据输入/输出
- RESET#/HOLD#/SIO3
- 复位#/保持#/SIO3
  - Hardware Reset pin or Hardware Hold pin or serial data Input/Output for 4 x I/O read mode
  - 4 x I/O 读取模式的硬件复位引脚或硬件保持引脚或串行数据输入/输出
- RESET# (16-pin package)
- RESET# (16 引脚封装)
  - Hardware Reset pin
    - 硬件复位引脚
- PACKAGE
- 包裹
  - 8-pin SOP
  - 8 引脚 SOP
  - 8-land WSON
  - 8-土地 WSON
  - 16-pin SOP
  - 16 引脚 SOP 封装
  - 24-Ball BGA (5x5 ball array)
  - 24 引脚 BGA (5x5 引脚阵列)
  - All devices are RoHS Compliant and Halogen Free
  - 所有器件都符合 RoHS 标准，不含卤素

3. GENERAL DESCRIPTION

4. 总体描述

NM25Q64EVB is 64M bits Serial NOR Flash memory, which is configured as 8,388,608 x 8 internally. NM25Q64EVB feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

NM25Q64EVB 是 64M 位串行 NOR 闪存，内部配置为 8，388，608 x 8。NM25Q64EVB 具有串行外设接口和软件协议，允许在单 I/O 模式下在简单的三线总线上运行。三个总线信号是时钟输入(SCLK)、串行数据输入(SI)和串行数据输出(SO)。CS#输入使能对器件的串行访问。

When it is in two I/O read mode, the SI pin and SO pin become SIO0 and SIO1 pin for address and dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and RESET# pin (of the 8-pin package) become SIO0pin, SIO1 pin, SIO2 pin and SIO3 pin for address and dummy bits input and data output.

在双 I/O 读取模式下，SI 引脚和 SO 引脚变为 SIO0 和 SIO1 引脚，用于地址和虚拟位输入和数据输出。在四 I/O 读取模式下，SI 引脚、SO 引脚、WP#引脚和 RESET#引脚(8 引脚封装)变为 SiO 0 引脚、SIO1 引脚、SIO2 引脚和 SIO3 引脚，用于地址和虚拟位输入和数据输出。

The NM25Q64EVB ® (Serial Multi I/O) provides sequential read operation on whole chip.

NM25Q64EVB(串行多路 I/O)提供整个芯片上的顺序读取操作。

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on sector (4K-byte), or block (32K-byte), or block (64K-byte), or whole chip basis.

发出编程/擦除命令后，将执行自动编程/擦除算法，该算法对指定的页面或扇区/块位置进行编程/擦除和验证。程序命令以字节为基础，或以页(256 字节)为基础，或以字为基础执行。擦除命令在扇区(4K 字节)、块(32K 字节)、块(64K 字节)或整个芯片基础上执行。

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

为了给用户提供方便的接口，还包括一个状态寄存器来指示芯片的状态。可以通过 WIP 位发出状态读取命令来检测编程或擦除操作的完成状态。

When the device is not in operation and CS# is high, it is put in standby mode.

当器件不工作且 CS#为高电平时，它会进入待机模式。

The NM25Q64EVB utilizes NOR-MEM's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

NM25Q64EVB 采用 NOR-MEM 的专有存储单元，即使在 100，000 次编程和擦除循环后也能可靠地存储存储内容。

Table 1. Read Performance Comparison
表 1。读取性能比较

SPI/QPI mode	Read Mode	Continuous Read mode bit cycle	Numbers of Dummy cycles (1)	Read Frequency (MHz)
SPI mode	Normal Read	0	0	80
	Fast Read	0	8	104
	Dual Output Read	0	8	104/80
	Quad Output Read	0	8	104/80
	Dual I/O Read	2	4	104/80
	Quad I/O Read	2	6	104/80
	Quad I/O Word Read	2	4	55
QPI mode	Fast Read	0	4	55
			6	80
			8	104/80
	Burst Read with Wrap	0	4	55
			6	80
			8	104/80
	Quad I/O Read	2	4	55
			6	80
			8	104/80
SPI/QPI 模式	读取模式	连续读取模式位周期	虚拟循环的数量(1)	读取频率(MHz)
	正常读取	0	0	80
	快速阅读	0	8	104
	双输出读取	0	8	104/80

SPI 模式	四路输出读取	0	8	104/80
	双 I/O 读取	2	四	104/80
	四路 I/O 读取	2	6	104/80
	四路 I/O 字读取	2	四	55
QPI 模式	快速阅读	0	四	55
			6	80
			8	104/80
	带换行的突发读取	0	四	55
			6	80
			8	104/80
	四路 I/O 读取	2	四	55
			6	80
			8	104/80

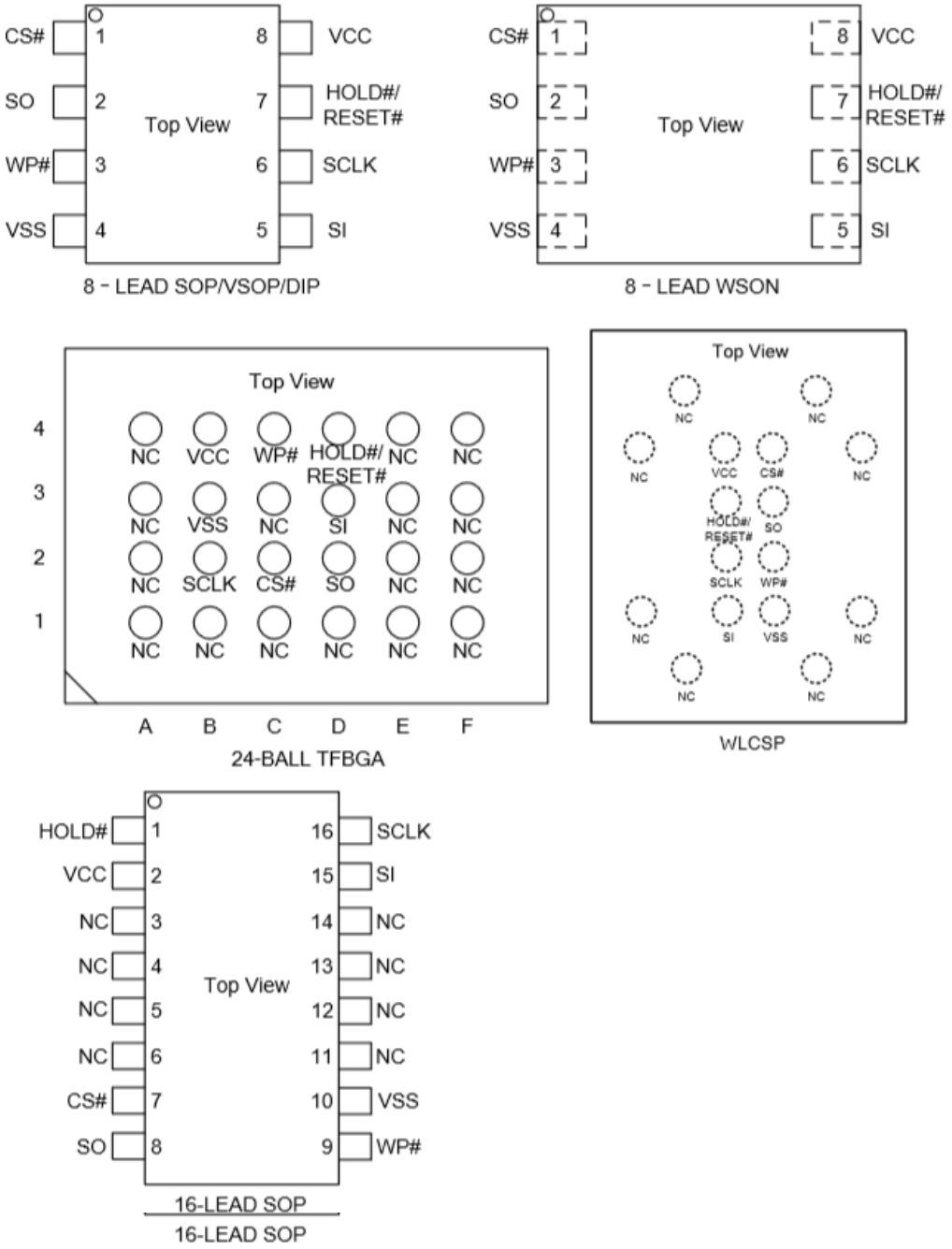
Note:
注意:

(1) Numbers of Dummy cycles include Continuous Read mode bit cycle number.
(2) 虚拟周期数包括连续读取模式位周期数。

(3) Maximum 104MHz for fast read on 3.0 - 3.6V power supply, and 80MHz for fast read on 2.7 - 3.0V power supply
(4) 在 3.0 – 3.6V 电源下快速读取的最高频率为 104MHz，在 2.7 – 3.0V 电源下快速读取的最高频率为 80MHz

5. PIN CONFIGURATIONS

6. 引脚配置



Note: Only for special order, Pin 3 is RESET# pin in 16-LEAD SOP package. Please connect NORMEM for detail

注:仅针对特殊订单，引脚 3 是 16 引脚 SOP 封装中的 RESET#引脚。详情请联系 NORMEM

Table 2. PIN DESCRIPTION

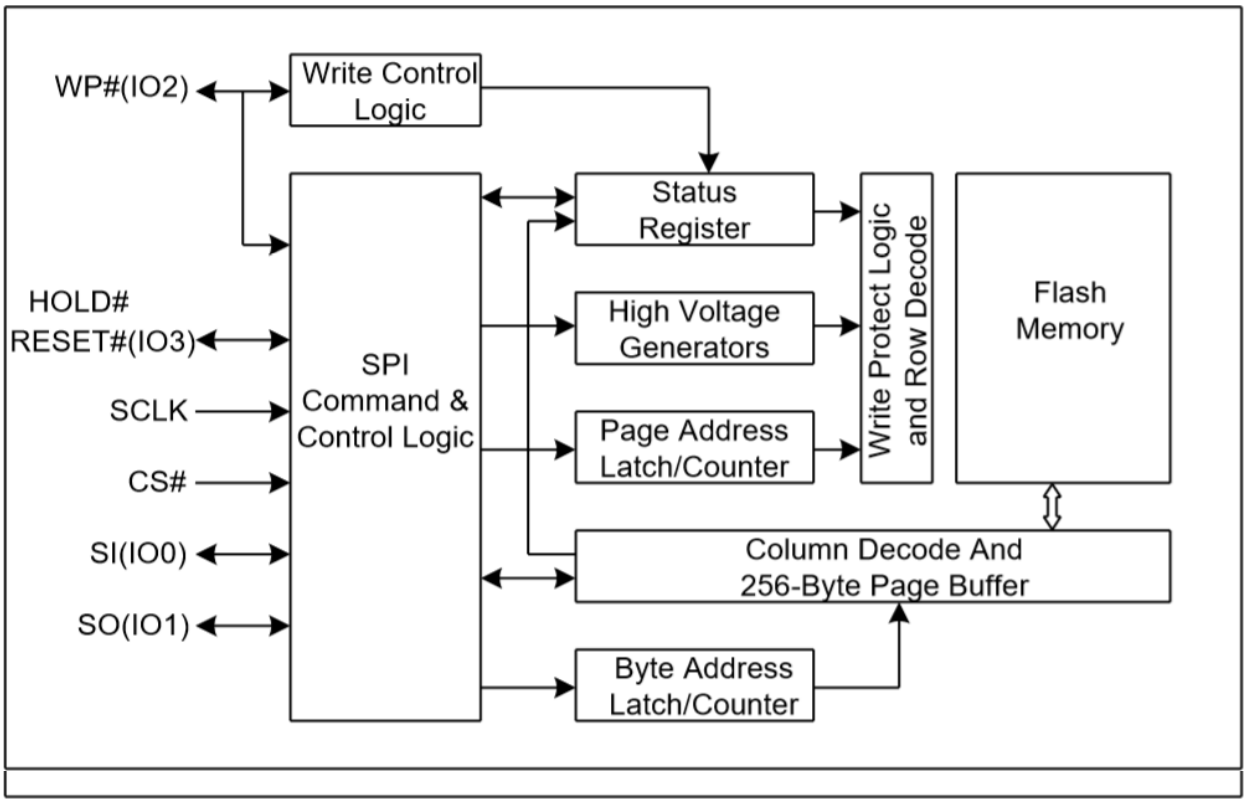
表二。PIN 描述

SYMBOL	DESCRIPTION
CS#	Chip Select
SCLK	Clock Input
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2 x I/O or 4 x I/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2 x I/O or 4 x I/O read mode)
WP#/SIO2	Write protection Active low or Serial Data Input & Output (for 4 x I/O read mode)
RESET#/HOLD#/SIO3	Hardware Reset pin Active low or Hardware Hold pin Active low or Serial Data Input & Output (for 4 x I/O read mode)
RESET#	Hardware Reset pin Active low only for special order in 16-LEAD SOP package
VSS	Ground
VCC	Power supply
标志	**描述**
CS#	芯片选择
SCLK	时钟输入
硅/氧化硅	串行数据输入(1 x I/O)/串行数据输入和输出(2 x I/O 或 4 x I/O 读取模式)
SO/SIO1	串行数据输出(用于 1 x I/O)/串行数据输入和输出(用于 2 x 个输入/输出或 4 个输入/输出读取模式)
WP #/二氧化硅	写保护低电平有效或串行数据输入和输出(用于 4 x I/O 读取模式)
复位#/保持#/SIO3	硬件复位引脚低电平有效或硬件保持引脚低电平有效或串行数据输入和输出(用于 4 x I/O 读取模式)
重置#	硬件复位引脚低电平有效，仅用于 16-中的特殊订单引线 SOP 封装
虚存系统	地面
VCC	电源

Notes: RESET# pin has internal pull up.

注意:RESET#引脚有内部上拉电阻。

7. BLOCK DIAGRAM
8. 框图



9. MEMORY ORGANIZATION

10. 存储器组织

Block	Sector	Address range		Advanced Block Protection unit
127	2047	7F F000H	7F FFFFH	4KB
	……	……	……	……
	2032	7F 0000H	7F 0FFFH	4KB
126	2031	7E F000H	7E FFFFH	64KB
	……	……	……	
	2016	7E 0000H	7E 0FFFH	
125	2015	7D F000H	7D FFFFH	64KB
	……	……	……	
	2000	7D 0000H	7D 0FFFH	
……	……	……	……	……
	……	……	……	
	……	……	……	
……	……	……	……	
	……	……	……	
	……	……	……	
2	47	02 F000H	02 FFFFH	64KB
	……	……	……	
	32	02 0000H	02 0FFFH	
1	31	01 F000H	01 FFFFH	64KB
	……	……	……	
	16	01 0000H	01 0FFFH	
0	15	00 F000H	00 FFFFH	4KB
	……	……	……	……
	0	00 0000H	00 0FFFH	4KB
街区	部门	地址范围		高级块保护单元
	2047	7F F000H	7F FFFFH	4KB

127	……	……	……	……
	2032	7F 0000H	7F 0FFFH	4KB
126	2031	7E F000H	7E FFFFH	64KB
	……	……	……	
	2016	7E 0000H	7E 0FFFH	
125	2015	7D F000H	7D FFFFH	64KB
	……	……	……	
	2000	7D 0000H	7D 0FFFH	
……	……	……	……	……
	……	……	……	
	……	……	……	
……	……	……	……	
	……	……	……	
	……	……	……	
2	47	02 F000H	02 FFFFH	64KB
	……	……	……	
	32	02 0000H	02 0FFFH	
—	31	01 F000H	01 FFFFH	64KB
	……	……	……	
	16	01 0000H	01 0FFFH	
0	15	00 F000H	00 FFFFH	4KB
	……	……	……	……
	0	00 0000H	00 0FFFH	4KB

11. DATA PROTECTION

12. 数据保护

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

在电源转换期间，可能会有一些错误的系统级信号，从而导致意外擦除或编程。该器件旨在保护自身免受这些意外写入周期的影响。

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

在加电期间，状态机将自动复位为待机模式。此外，器件的控制寄存器架构限制了存储器内容只能在特定命令序列成功完成后更改。

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

在下文中，有几个功能可以保护系统免受 VCC 上电和断电期间意外写入周期的影响，或者免受系统噪声的影响。

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- 有效命令长度检查:将检查命令长度是否在字节基础上，是否在字节边界上完成。
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- 写使能(WREN)命令:在其它命令改变数据之前，需要 WREN 命令来设置写使能锁存位(WEL)。
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and Soft-reset command.
- 深度掉电模式:通过进入深度掉电模式，闪存设备也受到保护，不能写入除了从深度掉电模式释放命令(RDP)和读取电子签名命令(RES)以及软复位命令之外的所有命令。
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.
- 高级安全功能:有一些保护和安全功能可以保护内容免受无意写入和恶意访问。

6.1 Block lock protection

6.2 块锁定保护

The Software Block Protected Mode (BPM) use (BP4, BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as Table 3 Protected Area Sizes, the protected areas are more flexible which may protect various area by setting value of BP0-BP4 bits.

软件块保护模式(BPM)使用(BP4、BP3、BP2、BP1、BP0)位来保护部分存储器为只读。受保护区域的定义如表 3“受保护区域大小”所示，受保护区域更加灵活，可以通过设置 BP0-BP4 位的值来保护不同的区域。

Table 3. Protected Area Sizes（WPS=0, CMP=0）
表 3。保护区大小(WPS=0，CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 to 127	7E0000h – 7FFFFFh	128KB	Upper 1/64
0	0	0	1	0	124 to 127	7C0000h – 7FFFFFh	256KB	Upper 1/32
0	0	0	1	1	120 to 127	780000h – 7FFFFFh	512KB	Upper 1/16
0	0	1	0	0	112 to 127	700000h – 7FFFFFh	1MB	Upper 1/8
0	0	1	0	1	96 to 127	600000h – 7FFFFFh	2MB	Upper 1/4
0	0	1	1	0	64 to 127	400000h – 7FFFFFh	4MB	Upper 1/2
0	1	0	0	1	0 to 1	000000h – 01FFFFh	128KB	Lower 1/64
0	1	0	1	0	0 to 3	000000h – 03FFFFh	256KB	Lower 1/32
0	1	0	1	1	0 to 7	000000h – 07FFFFh	512KB	Lower 1/16
0	1	1	0	0	0 to 15	000000h – 0FFFFFh	1M	Lower 1/8
0	1	1	0	1	0 to 31	000000h – 1FFFFFh	2MB	Lower 1/4
0	1	1	1	0	0 to 63	000000h – 3FFFFFh	4MB	Lower 1/2
X	X	1	1	1	0 to 127	000000h – 7FFFFFh	8MB	ALL
1	0	0	0	1	127	7FF000H - 7FFFFFH	4KB	Top Block
1	0	0	1	0	127	7FE000H - 7FFFFFH	8KB	Top Block
1	0	0	1	1	127	7FC000H - 7FFFFFH	16KB	Top Block
1	0	1	0	X	127	7F8000H - 7FFFFFH	32KB	Top Block
1	0	1	1	0	127	7F8000H - 7FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H - 000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H - 001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H - 003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H - 007FFFH	32KB	Bottom Block

1	1	1	1	0	0	000000H - 007FFFH	32KB	Bottom Block
状态寄存器内容					内存内容			
BP4	BP3	BP2	BP1	BP0	阻碍	地址	密度	部分
X	X	0	0	0	没有人	没有人	没有人	没有人
0	0	0	0	—	126 至 127	7e 0000h - 7 fffffh	128KB	上 1/64
0	0	0	—	0	124 至 127	7c 0000h - 7 fffffh	256KB	上部 1/32
0	0	0	—	—	120 到 127	780000h - 7 fffffh	512KB	上 1/16
0	0	—	0	0	112 至 127	700000 小时 - 7 分钟	1MB	上 1/8
0	0	—	0	—	96 至 127	600000 小时 - 7 fffffh	2MB	上 1/4
0	0	—	—	0	64 岁至 127 岁	400000 小时 - 7 分钟	4MB	上 1/2
0	—	0	0	—	0 到 1	000000h - 01 ffffh	128KB	下 1/64
0	—	0	—	0	0 到 3	000000h - 03 ffffh	256KB	下 1/32
0	—	0	—	—	0 到 7	000000h - 07 ffffh	512KB	低 1/16
0	—	—	0	0	0 到 15 岁	000000h - 0 fffffh	1M	下 1/8
0	—	—	0	—	0 到 31	000000h - 1 fffffh	2MB	下 1/4
0	—	—	—	0	0 到 63	000000h - 3 fffffh	4MB	低 1/2
X	X	—	—	—	0 到 127	000000h - 7 fffffh	8MB	全部
—	0	0	0	—	127	7FF000H - 7FFFFFH	4KB	顶部块
—	0	0	—	0	127	7FE000H - 7FFFFFH	8KB	顶部块
—	0	0	—	—	127	7FC000H - 7FFFFFH	16KB	顶部块
—	0	—	0	X	127	7F8000H - 7FFFFFH	32KB	顶部块
—	0	—	—	0	127	7F8000H - 7FFFFFH	32KB	顶部块
—	—	0	0	—	0	000000H - 000FFFH	4KB	桶底大块砖
—	—	0	—	0	0	000000H - 001FFFH	8KB	桶底大块砖
—	—	0	—	—	0	000000H - 003FFFH	16KB	桶底大块砖
—	—	—	0	X	0	000000H - 007FFFH	32KB	桶底大块砖
—	—	—	—	0	0	000000H - 007FFFH	32KB	桶底大块砖

Table 4. Protected Area Sizes（WPS=0, CMP=1）

表 4。保护区大小(WPS=0，CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 127	000000h – 7FFFFFh	8MB	ALL
0	0	0	0	1	0 to 125	000000h – 7DFFFFh	8,064KB	Lower 63/64
0	0	0	1	0	0 to 123	000000h – 7BFFFFh	7,936KB	Lower 31/32
0	0	0	1	1	0 to 119	000000h – 77FFFFh	7,680KB	Lower 15/16
0	0	1	0	0	0 to 111	000000h – 6FFFFFh	7MB	Lower 7/8
0	0	1	0	1	0 to 95	000000h – 5FFFFFh	5MB	Lower 3/4
0	0	1	1	0	0 to 63	000000h – 3FFFFFh	4MB	Lower 1/2
0	1	0	0	1	2 to 127	020000h – 7FFFFFh	8,064KB	Upper 63/64
0	1	0	1	0	4 to 127	040000h – 7FFFFFh	7,936KB	Upper 31/32
0	1	0	1	1	8 to 127	080000h – 7FFFFFh	7,680KB	Upper 15/16
0	1	1	0	0	16 to 127	100000h – 7FFFFFh	7MB	Upper 7/8
0	1	1	0	1	32 to 127	200000h – 7FFFFFh	5MB	Upper 3/4
0	1	1	1	0	64 to 127	400000h – 7FFFFFh	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 127	000000H – 7FEFFFH	8188KB	L-2047/2048
1	0	0	1	0	0 to 127	000000H – 7FDFFFH	8184KB	L-1023/1024
1	0	0	1	1	0 to 127	000000H – 7FBFFFH	8176KB	L-511/512
1	0	1	0	X	0 to 127	000000H – 7F7FFFH	8160KB	L-255/256
1	0	1	1	0	0 to 127	000000H – 7F7FFFH	8160KB	L-255/256
1	1	0	0	1	0 to 127	001000H – 7FFFFFH	8188KB	U-2047/2048
1	1	0	1	0	0 to 127	002000H – 7FFFFFH	8184KB	U-1023/1024
1	1	0	1	1	0 to 127	004000H – 7FFFFFH	8176KB	U-511/512
1	1	1	0	X	0 to 127	008000H – 7FFFFFH	8180KB	U-255/256
1	1	1	1	0	0 to 127	008000H – 7FFFFFH	8180KB	U-255/256
状态寄存器内容					内存内容			
BP4	BP3	BP2	BP1	BP0	阻碍	地址	密度	部分
X	X	0	0	0	0 到 127	000000h - 7 fffffh	8MB	全部
0	0	0	0	一	0 到 125	000000h - 7 dfffh	8064 千字节	下 63/64
0	0	0	一	0	0 到 123	000000 小时 - 7 英尺/小时	7,936KB	下 31/32
0	0	0	一	一	0 到 119	000000h - 77 ffffh	7680 千字节	下 15/16

0	0	—	0	0	0 到 111	000000h - 6 fffffh	7MB	下 7/8
0	0	—	0	—	0 到 95	000000h - 5 fffffh	5MB	下 3/4
0	0	—	—	0	0 到 63	000000h - 3 fffffh	4MB	低 1/2
0	—	0	0	—	2 至 127	020000h - 7 fffffh	8064 千字节	上部 63/64
0	—	0	—	0	4 至 127	040000h - 7 fffffh	7,936KB	鞋面 31/32
0	—	0	—	—	8 至 127	080000h - 7 fffffh	7680 千字节	上 15/16
0	—	—	0	0	16 至 127 岁	100000 小时 - 7 分钟	7MB	上 7/8
0	—	—	0	—	32 至 127	200000 小时 - 7 年	5MB	上 3/4
0	—	—	—	0	64 岁至 127 岁	400000 小时 - 7 分钟	4MB	上 1/2
X	X	—	—	—	没有人	没有人	没有人	没有人
—	0	0	0	—	0 到 127	000000 小时 - 7 年	8188KB	L-2047/2048
—	0	0	—	0	0 到 127	000000h - 7 fdfffh	8184KB	L-1023/1024
—	0	0	—	—	0 到 127	000000 小时 - 7 英尺/小时	8176KB	L-511/512
—	0	—	0	X	0 到 127	000000h - 7 F7 fffh	8160KB	L-255/256 号文件
—	0	—	—	0	0 到 127	000000h - 7 F7 fffh	8160KB	L-255/256 号文件
—	—	0	0	—	0 到 127	001000h - 7 fffffh	8188KB	U-2047/2048
—	—	0	—	0	0 到 127	002000h - 7 fffffh	8184KB	U-1023/1024
—	—	0	—	—	0 到 127	004000h - 7 fffffh	8176KB	U-511/512
—	—	—	0	X	0 到 127	008000h - 7 fffffh	8180KB	U-255/256
—	—	—	—	0	0 到 127	008000h - 7 fffffh	8180KB	U-255/256

Table 5. NM25Q64EVB Individual Block Protection (WPS=1)

表 5。NM25Q64EVB 独立块保护(WPS=1)

Block	Sector	Address range		Individual Block Lock Operation
127	2047	7F F000H	7F FFFFH	32 Sectors(Top/Bottom)&64 Blocks Block Lock: 36H+Address Block Unlock: 39H+Address Read Block Lock: 3DH+Address Global Block Lock: 7EH Global Block Unlock: 98H
	……	……	……	
	2032	7F 0000H	7F 0FFFH	
126	2031	7E F000H	7E FFFFH	
	……	……	……	
	2016	7E 0000H	7E 0FFFH	
125	2015	7D F000H	7D FFFFH	
	……	……	……	
	2000	7D 0000H	7D 0FFFH	
……	……	……	……	
	……	……	……	
	……	……	……	
……	……	……	……	
	……	……	……	
	……	……	……	
2	47	02 F000H	02 FFFFH	
	……	……	……	
	32	02 0000H	02 0FFFH	
1	31	01 F000H	01 FFFFH	
	……	……	……	
	16	01 0000H	01 0FFFH	
0	15	00 F000H	00 FFFFH	
	……	……	……	
	0	00 0000H	00 0FFFH	

街区	部门	地址范围		单个块锁定操作
127	2047	7F F000H	7F FFFFH	32 个扇区(顶部/底部)和 64 个块块锁:36H+地址 块解锁:39H+地址读取块锁定:3DH+地址全局块锁定:7EH 全局块解锁:98H
	……	……	……	
	2032	7F 0000H	7F 0FFFH	
126	2031	7E F000H	7E FFFFH	
	……	……	……	
	2016	7E 0000H	7E 0FFFH	
125	2015	7D F000H	7D FFFFH	
	……	……	……	
	2000	7D 0000H	7D 0FFFH	
……	……	……	……	
	……	……	……	
	……	……	……	
……	……	……	……	
	……	……	……	
	……	……	……	
2	47	02 F000H	02 FFFFH	
	……	……	……	
	32	02 0000H	02 0FFFH	
	31	01 F000H	01 FFFFH	
	……	……	……	

一	16	01 0000H	01 0FFFH	
0	15	00 F000H	00 FFFFH	
	.....	.....	.....	
	0	00 0000H	00 0FFFH	

6.3 Additional 2 x 8K-bit secured registers with OTP Locks
6.4 带 OTP 锁的额外 2 个 8K 位安全寄存器

The NM25Q64EVB provides 2 x 8K-bit Security Registers which can erased and programmed individually. These two registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

NM25Q64EVB 提供 2 个 8K 位安全寄存器，可以单独擦除和编程。系统制造商可以使用这两个寄存器来存储与主存储器阵列分开的安全和其他重要信息。

The Security Register Lock Bits (LB2-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction and Program Security Register instruction to that register will be ignored. Please refer to "Chapter 9 Register Description" for status register bit definition.

状态寄存器 2 中的安全寄存器锁定位(LB2-1)可用于 OTP 保护安全寄存器。一旦锁定位被设置为 1，相应的安全寄存器将被永久锁定，对该寄存器的擦除安全寄存器指令和编程安全寄存器指令将被忽略。关于状态寄存器位的定义，请参考“第 9 章寄存器描述”。

Table 6. Secured Register Definition
表 6。安全寄存器定义

Security Register	Address Range	Size	Lock bit
Security Register 1	24'h000000~24'h0003FF	8K bits	LB1
Security Register 2	24'h001000~24'h0013FF	8K bits	LB2
安全寄存器	地址范围	大小	锁定位
安全寄存器 1	24'h000000~24'h0003FF	8K 位	LB1
安全寄存器 2	24'h001000~24'h0013FF	8K 位	LB2

13. DEVICE OPERATION

14. 设备操作

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. 在发出命令之前，应检查状态寄存器，以确保设备为预期操作做好准备。

3. When incorrect command# sequence is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

4. 当不正确的命令#序列输入到该器件时，该器件变为待机模式，并保持待机模式直到下一个 CS#下降沿。在待机模式下，该器件的引脚应为高阻态。

5. When correct command# sequence is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

6. 当正确的命令#序列输入到该器件时，该器件变为激活模式，并保持激活模式直到下一个 CS#上升沿。

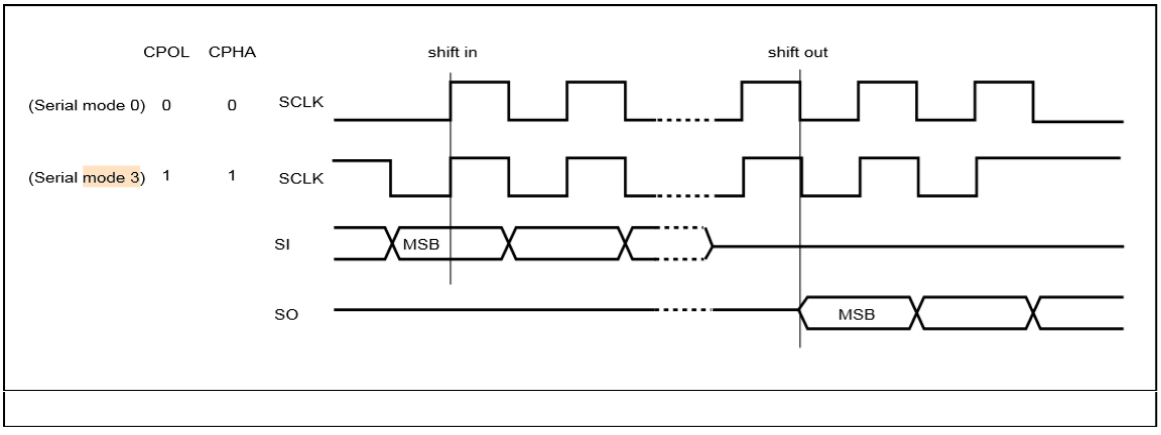
7. When device under STR mode, input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK.

8. 当器件处于 STR 模式时，输入数据在串行时钟(SCLK)的上升沿被锁存，数据在 SCLK 的下降沿移出。

9. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

10. 当写状态寄存器、编程或擦除操作正在进行时，对存储器阵列的访问被忽略，并且不影响写状态寄存器、编程、擦除的当前操作。

Figure 1. Serial Modes Supported
图一。支持串行模式



Note: CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

注意:CPOL 表示串行主机的时钟极性，空闲时 SCLK 为高电平，CPOL=1，不发送时 SCLK 为低电平，CPOL=0。CPHA 表示时钟相位。CPOL 位和 CPHA 位的组合决定支持哪种串行模式。

15. COMMAND SET

16. 指挥台

8.1 Command Set

8.1 指令集

Table 7. Array Access Command Set

表 7。阵列访问命令集

Command Description	Code	SPI	QPI	Address Byte1	Address Byte2	Address Byte3	Dummy Cycle(1)	Data Byte
Normal Read (READ)	03H	V		ADD1	ADD2	ADD3	0	1~
Fast Read (FAST_READ)	0BH	V	V	ADD1	ADD2	ADD3	8 or 4/6/8	1~
Dual Output Read (DREAD)	3BH	V		ADD1	ADD2	ADD3	8	1~
Quad Output Read (QREAD)	6BH	V		ADD1	ADD2	ADD3	8	1~
Dual I/O Read (2READ)	BBH	V		ADD1	ADD2	ADD3	4	1~
Quad I/O Read (4READ)	EBH	V	V	ADD1	ADD2	ADD3	6 or 4/6/8	1~
Quad I/O Word Read (4READ_WD)	E7H	V		ADD1	ADD2	ADD3	4	1~
Quad I/O Burst Read (4READ_BST)	0CH		V	ADD1	ADD2	ADD3	4/6/8	8/16/32/64
Page Program (PP)	02H	V	V	ADD1	ADD2	ADD3	0	1-256
Quad Page Program (QPP)	32H	V		ADD1	ADD2	ADD3	0	1-256
Sector Erase 4KB (SE)	20H	V	V	ADD1	ADD2	ADD3	0	0
Block Erase 32KB (BE32)	52H	V	V	ADD1	ADD2	ADD3	0	0
Block Erase 64KB (BE)	D8H	V	V	ADD1	ADD2	ADD3	0	0
Chip Erase (CE)	60H/C7H	V	V				0	0
命令描述	密码	精力	QPI	地址 字节 1	地址 字节 2	地址 字节 3	假的 周期(1)	数据 字节
正常读取(读取)	03H	V		ADD1	ADD2	ADD3	0	1~
快速读取(FAST_READ)	0BH	V	V	ADD1	ADD2	ADD3	8 或 4/6/8	1~
双输出读取(DREAD)	3BH	V		ADD1	ADD2	ADD3	8	1~
四路输出读取(QREAD)	6BH	V		ADD1	ADD2	ADD3	8	1~
双 I/O 读取(2 个读取)	BBH	V		ADD1	ADD2	ADD3	四	1~
四路 I/O 读取(4 路)	EBH	V	V	ADD1	ADD2	ADD3	6 或 4/6/8	1~
四路 I/O 字读取(4READ_WD)	E7H	V		ADD1	ADD2	ADD3	四	1~
四路 I/O 突发读取(4READ_BST)	0CH		V	ADD1	ADD2	ADD3	4/6/8	8/16/32/64
页面程序	02H	V	V	ADD1	ADD2	ADD3	0	1-256
四页程序(QPP)	32 小时	V		ADD1	ADD2	ADD3	0	1-256
扇区擦除 4KB (SE)	20H	V	V	ADD1	ADD2	ADD3	0	0

块擦除 32KB (BE32)	52H	V	V	ADD1	ADD2	ADD3	0	0
块擦除 64KB (BE)	D8H	V	V	ADD1	ADD2	ADD3	0	0
芯片擦除	60H/C7H	V	V				0	0

Note: (1) Detail dummy cycle numbers for read see table 1.

注:(1)详细的虚拟循环数，请参阅 table 1.

Table 8. Device Operation Command Set

表 8。设备操作命令集

Command Description	Code	SPI	QPI	Address Byte1	Address Byte2	Address Byte3	Dummy Cycle	Data Byte
Write Enable (WREN)	06H	V	V				0	0
Write Disable (WRDI)	04H	V	V				0	0
Write Enable for Volatile Status Register	50H	V	V				0	0
Enable QPI (EQIO)	38H	V					0	0
Reset QPI (RSTQIO)	FFH		V				0	0
Enable Reset (RSTEN)	66H	V	V				0	0
Reset Memory (RST)	99H	V	V				0	0
Program/Erase Suspend (Suspend)	75H	V	V				0	0
Program/Erase Resume (Resume)	7AH	V	V				0	0
Deep Power Down (DPW)	B9H	V	V				0	0
Release From Deep Power Down (RDP)	ABH	V	V				0	0
命令描述	密码	精力	QPI	地址字节 1	地址字节 2	地址字节 3	假的循环	数据字节
写使能(WREN)	06H	V	V				0	0
禁止写入(WRDI)	04H	V	V				0	0
易失性状态寄存器的写使能	50 小时	V	V				0	0
启用 QPI (EQIO)	38 小时	V					0	0
复位 QPI (RSTQIO)	familial benign hypercalcemia 家族性良性高钙学症		V				0	0
使能复位(RSTEN)	66H	V	V				0	0
重置存储器(RST)	99H	V	V				0	0
编程/擦除暂停(暂停)	75H	V	V				0	0
编程/擦除恢复(恢复)	7AH	V	V				0	0
深度断电(DPW)	B9H	V	V				0	0
从深度断电中释放(RDP)	人身伤害	V	V				0	0

Table 9. Register Access Command Set

表 9。寄存器访问命令集

Command Description	Code	SPI	QPI	Address Byte1	Address Byte2	Address Byte3	Dummy Cycle	Data Byte
Read Status Register 1 (RDSR1)	05H	V	V				0	1
Read Status Register 2 (RDSR2)	35H	V	V				0	1
Read Status Register 3 (RDSR3)	15H	V	V				0	1
Write Status Register 1 (WRSR1)	01H	V	V				0	1
Write Status Register 2 (WRSR2)	31H	V	V				0	1
Write Status Register 3 (WRSR3)	11H	V	V				0	1
Read Identification (RDID)	9FH	V	V				0	3
RDP and Read Device ID (RDI)	ABH	V	V	ADD1(1)	ADD2(1)	ADD3(1)	0	1
Read Electronic manufacturer & Device ID (REMS)	90H	V	V	ADD1(1)	ADD2(1)	ADD3(2)	0	2
Read Electronic manufacturer & Device ID by Dual I/O (REMS2)	92H	V		ADD1(1)	ADD2(1)	ADD3(2)	0	2
Read Electronic manufacturer & Device ID by Quad I/O (REMS4)	94H	V		ADD1(1)	ADD2(1)	ADD3(2)	0	2
Read Serial Flash Discoverable Parameter (RDSFDP)	5AH	V	V	ADD1	ADD2	ADD3	8 or 4/6/8	1~
Read Security Register (RDSECR)	48H	V		ADD1	ADD2	ADD3	8	0
Program Security Register (PGSECR)	42H	V		ADD1	ADD2	ADD3	0	1-256
Erase Security Register (ERSECR)	44H	V		ADD1	ADD2	ADD3	0	0
Individual Block Lock (SBLK)	36H	V	V	ADD1	ADD2	ADD3	0	0
Individual Block Unlock (SBULK)	39H	V	V	ADD1	ADD2	ADD3	0	0
Read Block Lock (RDBLK)	3DH	V	V	ADD1	ADD2	ADD3	0	1
Global Block Lock (GBLK)	7EH	V	V				0	0
Global Block Unlock (GBULK)	98H	V	V				0	0
Set Burst with Warp (SET_BSTRD)	77H	V		ADD1(1)	ADD2(1)	ADD3(1)	0	1
Set Read Parameters (SET_PARAM)	C0H		V				0	1
命令描述	密码	精力	QPI	地址字节 1	地址字节 2	地址字节 3	假的循环	数据字节
读取状态寄存器 1 (RDSR1)	05H	V	V				0	一
读取状态寄存器 2 (RDSR2)	35 小时	V	V				0	一
读取状态寄存器 3 (RDSR3)	15 小时	V	V				0	一
写状态寄存器 1 (WRSR1)	01H	V	V				0	一
写状态寄存器 2 (WRSR2)	31H	V	V				0	一
写状态寄存器 3 (WRSR3)	11 小时	V	V				0	一
读取标识(RDID)	9FH	V	V				0	3
RDP 和读取设备 ID (RDI)	人身伤害	V	V	添加 1(1)	添加 2(1)	添加 3(1)	0	一

读取电子制造商和设备 ID (REMS)	90H	V	V	添加 1(1)	添加 2(1)	添加 3(2)	0	2
读取电子制造商和设备 ID 通过双 I/O (REMS2)	92H	V		添加 1(1)	添加 2(1)	添加 3(2)	0	2
读取电子制造商和设备 ID 通过四通道 I/O (REMS4)	94H	V		添加 1(1)	添加 2(1)	添加 3(2)	0	2
读取可发现的串行闪存参数(RDSFDP)	5AH	V	V	ADD1	ADD2	ADD3	8 或 4/6/8	1~
读取安全寄存器(RDSECR)	48 小时	V		ADD1	ADD2	ADD3	8	0
程序安全寄存器	42 小时	V		ADD1	ADD2	ADD3	0	1-256
擦除安全寄存器(ERSECR)	44H	V		ADD1	ADD2	ADD3	0	0
独立块锁(SBLK)	36 小时	V	V	ADD1	ADD2	ADD3	0	0
独立模块解锁(SBULK)	39H	V	V	ADD1	ADD2	ADD3	0	0
读取块锁(RDBLK)	3DH	V	V	ADD1	ADD2	ADD3	0	—
全局块锁(GBLK)	7EH	V	V				0	0
全局块解锁(GBULK)	98H	V	V				0	0
设置带扭曲的突发脉冲(SET_BSTRD)	77H	V		添加 1(1)	添加 2(1)	添加 3(1)	0	—
设置读取参数(SET_PARAM)	C0H		V				0	—

Note: (1) Input Address is ignored.

注意:(1)输入地址被忽略。

(2) If ADD3=8'h00, Manufacturer ID will be shifted out first; If ADD3=8'h01, Device ID will be shifted out first.

(2)如果 ADD3=8'h00，制造商 ID 将首先移出；如果 ADD3=8'h01，设备 ID 将首先移出。

17. REGISTER DESCRIPTION

18. 寄存器描述

9.1 Status Register

Status Register 1

9.1 状态寄存器状态寄存器 1

No	Bit name	Description	Default	Type
Bit 7	CMP	Complement protect bit (1)	0	Non-volatile bit
Bit 6	BP4	Level of protected block (1)	0	Non-volatile bit
Bit 5	BP3	Level of protected block (1)	0	Non-volatile bit
Bit 4	BP2	Level of protected block (1)	0	Non-volatile bit
Bit 3	BP1	Level of protected block (1)	0	Non-volatile bit
Bit 2	BP0	Level of protected block (1)	0	Non-volatile bit
Bit 1	WEL	Write enable latch 1=write enable 0=not write enable	0	Volatile bit (Read only)
Bit 0	WIP	Write in progress bit 1=write operation 0=not in write operation	0	Volatile bit (Read only)
不	位名	描述	默认	类型
第 7 位	金属波纹管 (Corrugated Metal Pipe)	互补保护位(1)	0	非易失性位
第 6 位	BP4	受保护块的级别(1)	0	非易失性位
第 5 位	BP3	受保护块的级别(1)	0	非易失性位
第 4 位	BP2	受保护块的级别(1)	0	非易失性位
第 3 位	BP1	受保护块的级别(1)	0	非易失性位
第 2 位	BP0	受保护块的级别(1)	0	非易失性位
第 1 位	WEL	写使能锁存器 1 =写使能 0 =不写 使能	0	易失位(只读)

第 0 位	半成品	写入进行中位 1 =写入操作 0 =不在写入操作中	0	易失位(只读)

Note: (1) Detail see the Table 3 "Protected Area Size".
注:(1)详情见 Table 3 “保护区大小”。

Status Register 2
状态寄存器 2

No	Bit name	Description	Default	Type
Bit 7	ESB	Erase Suspend bit 1=Erase is suspended 0=Erase is not suspended	0	Volatile bit (Read only)
Bit 6	PSB	Program Suspend bit 1=Program is suspended 0=Program is not suspended	0	Volatile bit (Read only)
Bit 5	Reserved	x	x	x
Bit 4	LB2	Security Register 2 Lock bit 1=Locked 0=Unlocked	0	OTP
Bit 3	LB1	Security Register 1 Lock bit 1=Locked 0=Unlocked	0	OTP
Bit 2	QE	Quad Enable bit 1=Quad enable 0=not Quad enable	0	Non-volatile bit
Bit 1	SRP1	The Status Register Protect bit (1)	0	Non-volatile bit
Bit 0	SRP0	The Status Register Protect bit (1)	0	Non-volatile bit

不	位名	描述	默认	类型
第 7 位	电存储电池（electric storage battery 的缩写）	擦除暂停位 1 =擦除暂停 0 =不暂停擦除	0	易失位(只读)
第 6 位	PSB	程序暂停位 1 =程序暂停 0 =程序未暂停	0	易失位(只读)
第 5 位	内向的；寡言少语的；矜持的	x	x	x
第 4 位	LB2	安全寄存器 2 锁定位 1 =锁定 0 =解锁	0	动态密码

第 3 位	LB1	安全寄存器 1 锁定位 1 =锁定 0 =解锁	0	动态密码
第 2 位	QE	四通道使能位 1 =四 通道使能 0 =非四通道使能	0	非易失性位
第 1 位	SRP1	状态寄存器保护位(1)	0	非易失性位
第 0 位	SRP0	状态寄存器保护位(1)	0	非易失性位

Note: (1) Detail see the Table 10 "Status Register Protect method".

注:(1)详情见 Table 10 “状态寄存器保护方法”。

Status Register 3

状态寄存器 3

No	Bit name	Description	Default	Type
Bit 7	HOLD/RST	Select HOLD# or RESET# function bit 0=SIO3 Pin acts as HOLD# 1=SIO3 Pin acts as RESET#	0	Non-Volatile bit
Bit 6	ODS1	Output Driver Strength bit (1)	0	Non-Volatile bit
Bit 5	ODS0	Output Driver Strength bit (1)	0	Non-Volatile bit
Bit 4	Reserved	x	x	x
Bit 3	Reserved	x	x	x
Bit 2	WPS	Write Protect Scheme bit 1=Individual Block Protect method 0=Block Protect method	0	Non-volatile bit
Bit 1	E_FAIL	Erase Fail bit 1=Indicate erase failed 0=Normal erase succeed	0	Volatile bit (Read only)
Bit 0	P_FAIL	Program Fail bit 1=Indicate program failed 0=Normal program succeed	0	Volatile bit (Read only)
不	位名	描述	默认	类型
第 7 位	霍尔德/RST	选择保持#或复位#功能位 0=SIO3 引脚 充当保持# 1=SIO3 引脚用作复位#	0	非易失性位
第 6 位	ODS1	输出驱动器强度位(1)	0	非易失性位
第 5 位	ODS0	输出驱动器强度位(1)	0	非易失性位
第 4 位	内向的；寡言少语的；矜持的	x	x	x
第 3 位	内向的；寡言少语的；矜持的	x	x	x
第 2 位	文字处理系统	写保护方案位 1 =单个块保护方法 0 =块保护方法	0	非易失性位
第 1 位	e _失败	擦除失败位 1 =表示擦 除失败 0 =正常擦除成功	0	易失位(只读)
第 0 位	p _失败	编程失败位 1 =表示编程 失败 0 =正常程序成功	0	易失位(只读)

Note: (1) Detail see the Table 11 "Output Driver Strength Table".

注:(1)详情见 Table 11 “输出驱动强度表”。

The definition of the status register bits is as below:

状态寄存器位的定义如下:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WIP 位。写入进行中(WIP)位是一个易失性位，指示器件在编程/擦除/写入状态寄存器过程中是否繁忙。当 WIP 位设置为 1 时，表示器件正忙于编程/擦除/写状态寄存器进程。当 WIP 位设置为 0 时，表示器件不在编程/擦除/写入状态寄存器周期中。

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register command. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register command. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

WEL 比特。写使能锁存(WEL)位是一个易失位，指示器件是否设置为内部写使能锁存。当 WEL 位设为 1 时，意味着内部写使能锁存器已置位，器件可以接受编程/擦除/写状态寄存器命令。当 WEL 位设置为 0 时，这意味着没有内部写使能锁存；该设备将不接受编程/擦除/写入状态寄存器命令。如果将编程/擦除命令应用于受保护的存储区，则该命令将被忽略。为了确保 WIP 位和 WEL 位都被设置为 0 且可用于下一个编程/擦除/操作，在轮询 WEL 位之前，需要确认 WIP 位为 0。WIP 位确认后，WEL 位需要确认为 0。

BP4, BP3, BP2, BP1, BP0 bits. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in Table 3) of the device to against the program/erase command without hardware protection mode being set. To write the Block Protect (BP4, BP3, BP2, BP1, BP0) bits requires the Write Status Register 1(WRSR1) command to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE/SE3B/SE4B), Block Erase (BE) and Chip Erase (CE) commands (only if Block Protect bits (BP3:BP0) set to 0, the CE command can be executed). The BP4, BP3, BP2, BP1, BP0 bits are "0" as default. Which is unprotected.

BP4、BP3、BP2、BP1、BP0 位。块保护(BP4、BP3、BP2、BP1、BP0)位是非易失性位，表示受保护区域(如中所定义 Table 3)来对抗编程/擦除命令，而不设置硬件保护模式。要写入块保护(BP4、BP3、BP2、BP1、BP0)位，需要执行写状态寄存器 1(WRSR1)命令。这些位定义了存储器的保护区域，以防止页面编程(PP)、扇区擦除(SE/SE3B/SE4B)、块擦除(BE)和芯片擦除(CE)命令(仅当块保护位(BP3:BP0)设置为 0 时，才能执行 CE 命令)。BP4、BP3、BP2、BP1、BP0 位默认为“0”。它没有保护。

Complement Protect (CMP) bit. The Complement Protect bit (CMP), a non-volatile bit, is used in conjunction with BP4, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by BP4, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top

互补保护(CMP)位。互补保护位(CMP)是一种非易失性位，与 BP4、BP3、BP2、BP1 和 BP0 位配合使用，为阵列保护提供更大的灵活性。一旦 CMP 设置为 1，以前由 BP4、BP3、BP2、BP1 和 BP0 设置的阵列保护将被反转。例如，当 CMP=0 时，顶部的 64KB 块可以受到保护，而阵列的其余部分则不受保护；当 CMP=1 时，顶部

64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

64KB 数据块将不受保护，而阵列的其余部分将变为只读。详情请参考状态寄存器存储器保护表。默认设置为 CMP=0。

SRP1, SRP0 bits. The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register 2. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1、SRP0 位。状态寄存器保护位(SRP1 和 SRP0)是状态寄存器 2 中的非易失性读/写位。SRP 位控制写保护的方法:软件保护、硬件保护、电源锁定或一次性可编程(OTP)保护。

Table 10. Status Register Protect Method
表 10。状态寄存器保护方法

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protected	WP# has no control. The Status Register can be written to after a Write Enable (WREN) instruction. (Default)
0	1	0	Hardware Protected	When WP# pin is low, the Status Register is locked and cannot be written to.
0	1	1	Hardware Unprotected	When WP# pin is high, the Status Register is unlocked and can be written to after a Write Enable (WREN) instruction.
1	0	X	Power Supply Lock-Down (1)	The Status Register is protected and cannot be written to again until the next power-down, power-up cycle.
1	1	X	One time Program (2)	The Status Register is permanently protected and can not be written to.
SRP1	SRP0	WP#	状态寄存器	描述
0	0	X	软件保护	WP#没有控件。写操作后，可以写入状态寄存器启用(WREN)指令。(默认)
0	一	0	五金器具保护	当 WP#引脚为低电平时，状态寄存器被锁定，无法写给。
0	一	一	五金器具无保护的	当 WP#引脚为高电平时，状态寄存器解锁，可以在写使能(WREN)指令后写入。
一	0	X	电源锁定(1)	状态寄存器受到保护，在下一个关断、上电周期。
一	一	X	一次性程序(2)	状态寄存器受到永久保护，不能写入。

Note: (1) When SRP1, SRP0=(1,0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0,0) state.
注意:(1)当 SRP1，SRP0=(1，0)时，一个关断、上电周期会将 SRP1，SRP0 变为(0，0)状态。
(2) This feature is available on special order. Please contact NORMEM for details.
(2)此功能可通过特殊订购获得。详情请联系 NORMEM。

QE bit. The Quad Enable (QE) bit is a non-volatile read/write bit that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state, the WP# pin and HOLD# are enabled. When the QE bit is set

to a 1, the Quad IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled.

QE 比特。四通道使能(QE)位是非易失性读/写位，允许四通道 SPI 和 QPI 操作。当 QE 位设置为 0 状态时，WP#引脚和 HOLD#使能。当 QE 位置 1 时，四通道 IO2 和 IO3 引脚使能，WP#和 HOLD#功能禁用。

LB2, LB1 bits. The Security Register Lock Bits (LB2, LB1) are non-volatile One Time Program (OTP) bits that provide the write protect control and status to the Security Registers. The default state of LB2-1 is 0, Security Registers are unlocked. LB2-1 can be set to 1 individually using the Write Status Register instruction. LB2-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 1K-Byte Security Register will become read-only permanently.

LB2、LB1 位。安全寄存器锁定位(LB2、LB1)是非易失性一次性编程(OTP)位，为安全寄存器提供写保护控制和状态。LB2-1 的默认状态为 0，安全寄存器解锁。可以使用写状态寄存器指令将 LB2-1 单独设置为 1。LB2-1 是一次性可编程(OTP)寄存器，一旦设置为 1，相应的 1K 字节安全寄存器将永久变为只读。

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

程序暂停位。程序暂停位(PSB)表示程序暂停操作的状态。用户可以使用 PSB 来识别闪存的状态。在闪存被程序挂起命令挂起后，PSB 被设置为“1”。在程序操作恢复后，PSB 被清除为“0”。

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

擦除挂起位。擦除挂起位(ESB)指示擦除挂起操作的状态。用户可以使用 ESB 来识别闪存的状态。在闪存被擦除挂起命令挂起后，ESB 被设置为“1”。擦除操作恢复后，ESB 被清除为“0”。

Program Fail bit. The Program Fail bit is a status flag, which shows the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

程序失败位。编程失败位是状态标志，其显示最后编程操作的状态。如果程序操作失败或程序区域被保护，它将被设置为“1”。如果最后一次操作成功，它将被设置为“0”。请注意，它不会中断或停止闪存中的任何操作。

Erase Fail bit. The Erase Fail bit is a status flag, which shows the status of last Erase operation. It will be set to "1", if the erase operation fails or the erase region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

擦除失败位。擦除失败位是一个状态标志，表示上一次擦除操作的状态。如果擦除操作失败或擦除区域受保护，它将被设置为“1”。如果最后一次操作成功，它将被设置为“0”。请注意，它不会中断或停止闪存中的任何操作。

Write Protect Selection (WPS) bit. The WPS bit is used to select which Write Protect scheme should be used. When WPS=0 (factory default), the device will use the combination of CMP, BP[4:0] bits to protect a

写保护选择(WPS)位。WPS 位用于选择应该使用哪种写保护方案。当 WPS=0(工厂默认值)时，器件将使用 CMP、BP[4:0]位的组合来保护 a

specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset

存储器阵列的特定区域。当 WPS=1 时，设备将利用单独的块锁来保护任何单独的扇区或块。器件上电时或复位后，所有单个块锁定位的默认值为 1

ODS1, ODS0 bits. The output driver strength (ODS1,ODS0) bits are volatile bits, which indicate the output driver level (as defined in "Output Driver Strength Table") of the device. To write the ODS bits requires the Write Status Register (WRSR3) command to be executed.

ODS1、ODS0 位。输出驱动器强度(ODS1、ODS0)位是易失性位，表示器件的输出驱动器电平(定义见“输出驱动器强度表”)。写入 ODS 位需要执行写状态寄存器(WRSR3)命令。

Table 11. Output Driver Strength Table
表 11。输出驱动器强度表

ODS1	ODS0	Output Driver Strength
0	0	50% (default)
0	1	25%
1	0	75%
1	1	100%
ODS1	ODS0	输出驱动器强度
0	0	50%(默认)
0	—	25%
—	0	75%
—	—	100%

HOLD/RST function bit. The HOLD/RST bit is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the HOLD# and RESET# functions are disabled, the pin acts as a dedicated data I/O pin.

保持/RST 功能位。保持/RST 位用于确定 8 引脚封装的硬件引脚上应实现保持#还是复位#功能。当 HOLD/RST=0(工厂默认)时，引脚充当/HOLD；当保持/RST=1 时，引脚用作/RESET。然而，/HOLD 或/RESET 功能仅在 QE=0 时可用。如果 QE 设为 1，保持#和复位#功能被禁用，该引脚用作专用数据 I/O 引脚。

19. COMMAND DESCRIPTION

20. 命令描述

10.1 Write Enable (WREN)
10.2 写使能(WREN)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP/4PP), Sector Erase (SE), Block Erase (BE/BE32K), Chip Erase (CE), Write Status Register (WRSR1/2/3) and Erase/Program Security Registers.

写使能(WREN)命令用于设置写使能锁存(WEL)位。在每个页面编程(PP/4PP)、扇区擦除(se)、块擦除(BE/BE32K)、芯片擦除(CE)、写状态寄存器(WRSR1/2/3)和擦除/编程安全寄存器之前，必须设置写使能锁存(WEL)位。

The Write Enable (WREN) command sequence: CS# goes low -> sending the Write Enable command -> CS# goes high.

写使能(WREN)命令序列:CS#变为低电平->发送写使能命令-> CS#变为高电平。

Figure 2. Write Enable (WREN) Sequence (SPI Mode)
图二。写使能(WREN)序列(SPI 模式)

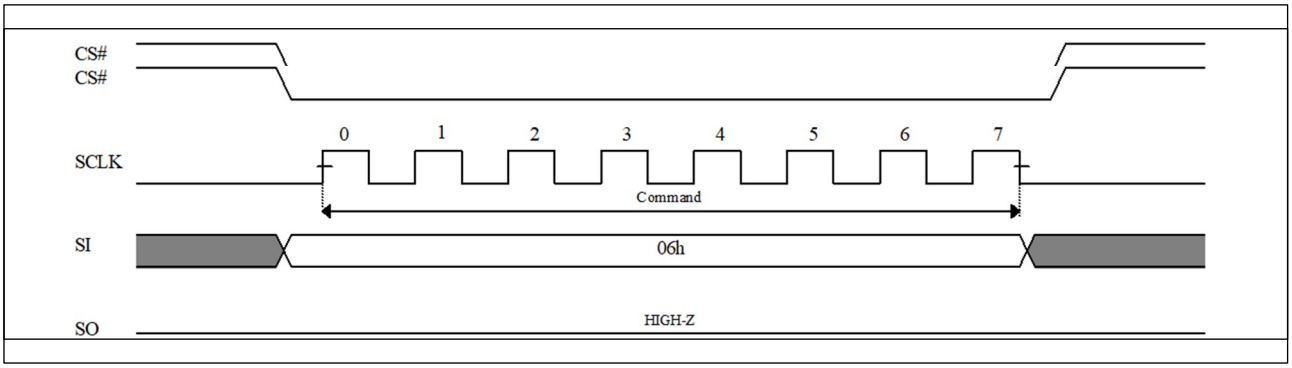
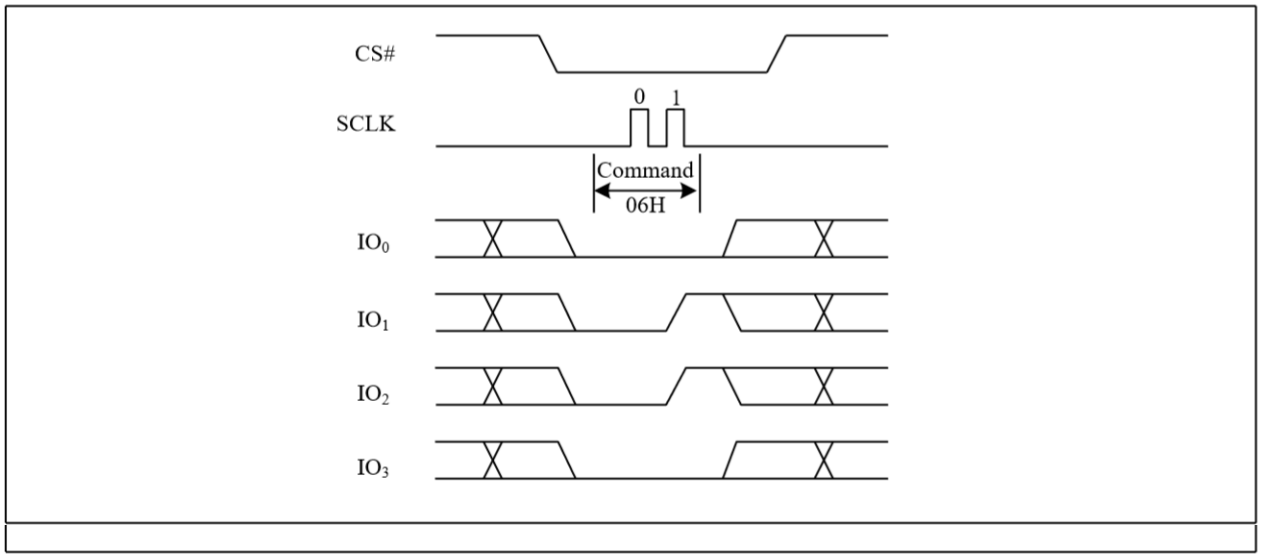


Figure 3. Write Enable (WREN) Sequence (QPI Mode)

图 3。写使能(WREN)序列(QPI 模式)



10.3 Write Disable (WRDI)
10.4 禁止写入(WRDI)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit

写禁止命令用于复位写允许锁存(WEL)位。用户可以使用 WRDI 命令来保护存储器区域，防止可能损坏存储器内容的无意写入。当 WIP 位时，WRDI 命令在嵌入式操作中被忽略

=1.

=1.

The WEL bit is reset by following situations:

WEL 位在以下情况下复位:

- Power-up
- 通电
- Reset# pin driven low
- Reset#引脚驱动至低电平
- WRDI command completion
- WRDI 命令完成
- WRSR1/ WRSR2/ WRSR3/WRCR command completion
- WRSR1/ WRSR2/ WRSR3/WRCR 命令完成
- PP/4PP command completion

- PP/4PP 命令完成
- SE/BE32K/BE/CE command completion
- SE/BE32K/BE/CE 命令完成
- PGM/ERS Suspend command completion
- PGM/ERS 暂停命令完成
- Soft-reset command completion
- 软复位命令完成
- Erase/Program security register completion
- 擦除/编程安全寄存器完成
- SBLK/SBULK/GBLK/GUBLK completion
- SBLK/SBULK/GBLK/GUBLK 完成
- SET_BSTRD/SET_PARAM completion
- SET_BSTRD/SET_PARAM 完成

The Write Disable command sequence: CS# goes low □Sending the Write Disable command □CS# goes high.

写禁用命令序列:CS#变为低电平发送写禁用命令 CS#变为高电平。

Figure 4. Write Disable (WRDI) Sequence (SPI Mode)

图 4。写禁用(WRDI)序列(SPI 模式)

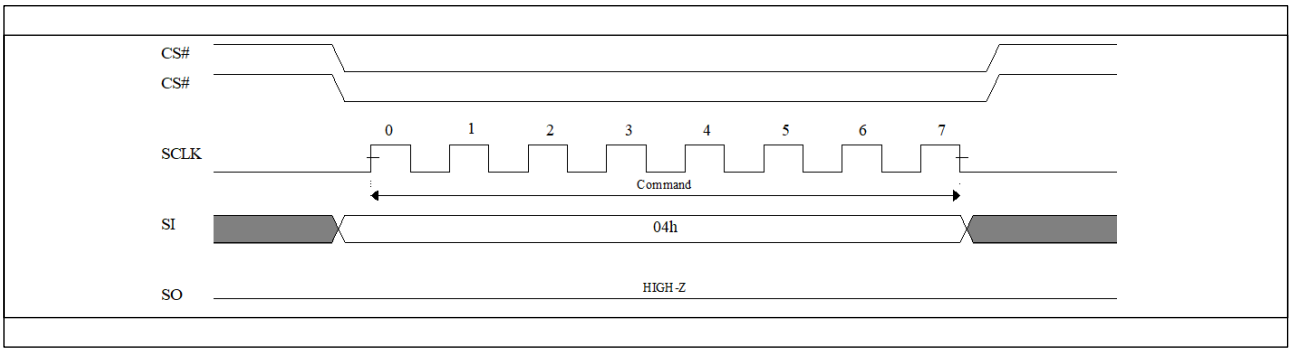
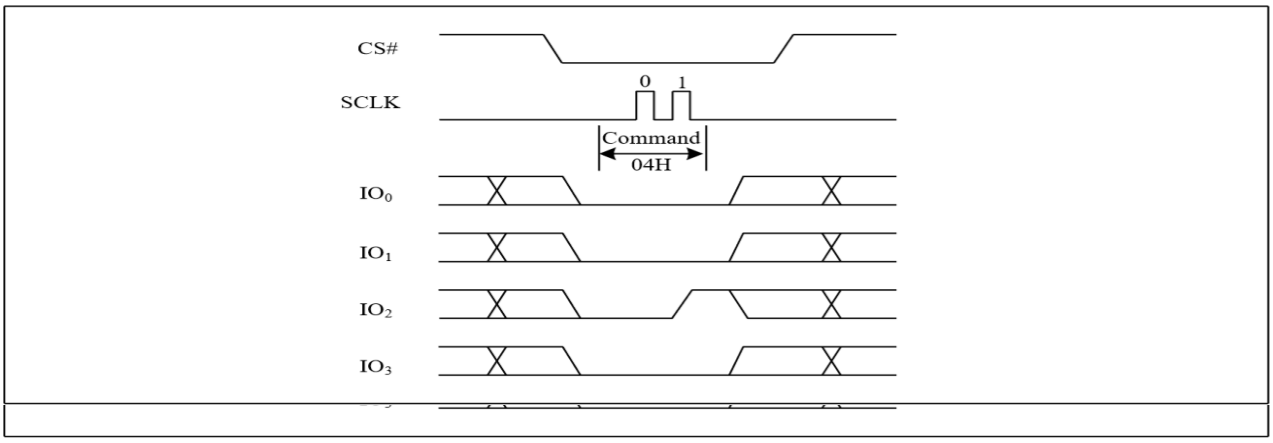


Figure 5. Write Disable (WRDI) Sequence (QPI Mode)

图 5。写禁用(WRDI)序列(QPI 模式)



10.5 Write Enable for Volatile Status Register
10.6 易失性状态寄存器的写使能

The non-volatile Status Register bits described can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 6) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

所述的非易失性状态寄存器位也可以作为易失性位写入。这为快速更改系统配置和存储器保护方案提供了更大的灵活性，而无需等待典型的非易失性位写入周期，也不会影响状态寄存器非易失性位的持久性。要将易失性值写入状态寄存器位，易失性状态寄存器的写使能(50h)指令必须先于写状态寄存器(01h)指令发出。易失性状态寄存器指令的写使能(图 6)不会设置写使能锁存(WEL)位，它仅对写状态寄

存器指令有效，以更改易失性状态寄存器位值。

Figure 6. Write Enable for Volatile Status Register Sequence (SPI Mode)
图 6。易失性状态寄存器序列的写使能(SPI 模式)

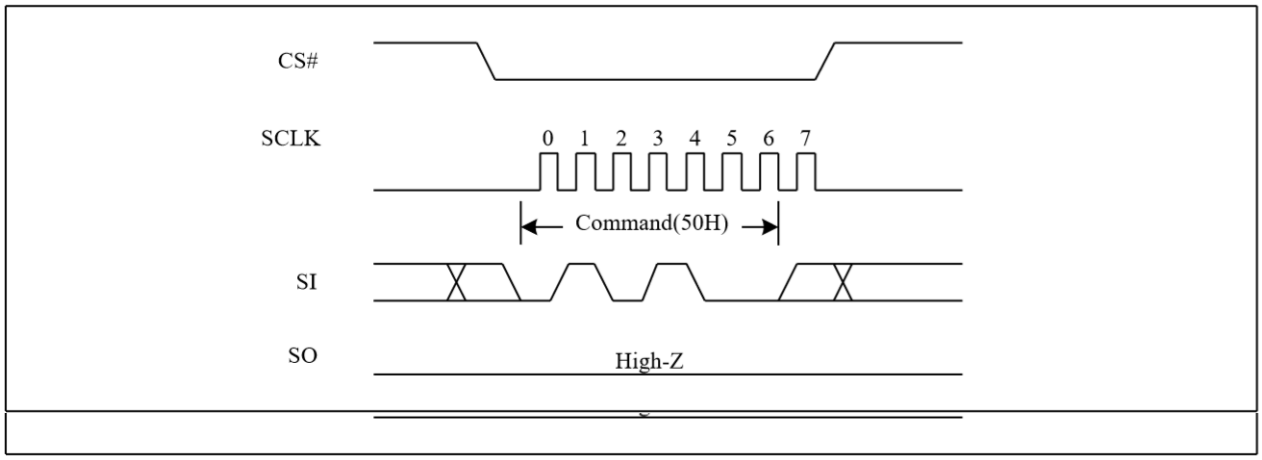
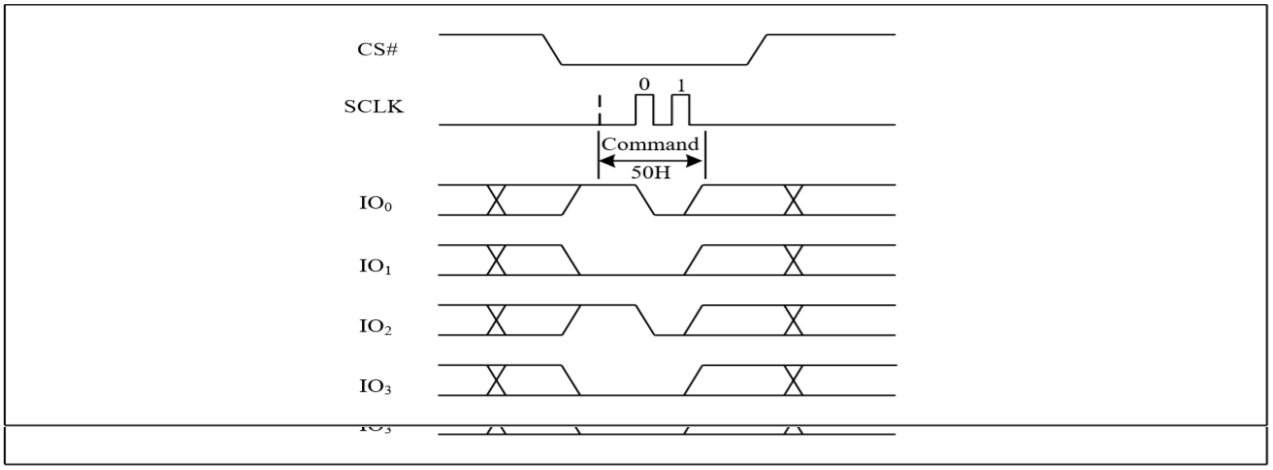


Figure 7. Write Enable for Volatile Status Register Sequence (QPI Mode)
图 7。易失性状态寄存器序列的写使能(QPI 模式)



10.7 Read Status Register (RDSR1/RDSR2/RDSR3)
10.8 读取状态寄存器(RDSR1/RDSR2/RDSR3)

The Read Status Register (RDSR1/RDSR2/RDSR3) command is for reading the Status Register. The Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new command when a program, erase, or write status register operation is in progress. For command code “05H” / “35H” / “15H”, the SO will output Status Register bits S7~S0 / S15-S8 / S16-S23.

读取状态寄存器(RDSR1/RDSR2/RDSR3)命令用于读取状态寄存器。可以随时读取状态寄存器(甚至在编程/擦除/写入状态寄存器条件下)。当编程、擦除或写状态寄存器操作正在进行时，建议在发送新命令之前检查正在写入(WIP)位。对于命令代码“05H”/“35H”/“15H”，SO 将输出状态寄存器位 S7~S0 / S15-S8 / S16-S23。

Figure 8. Read Status Register (RDSR1/RDSR2/RDSR3) Sequence (SPI Mode)
图 8。读取状态寄存器(RDSR1/RDSR2/RDSR3)序列(SPI 模式)

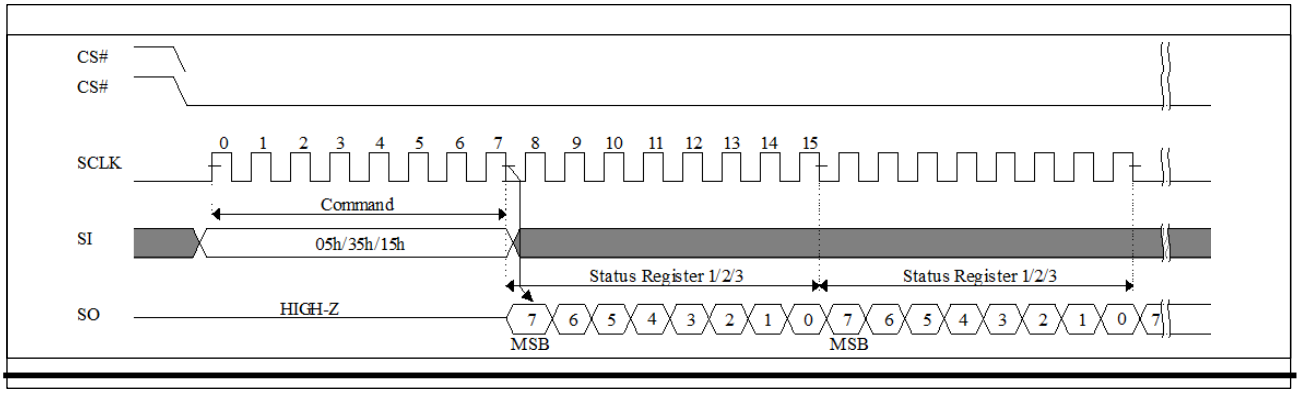
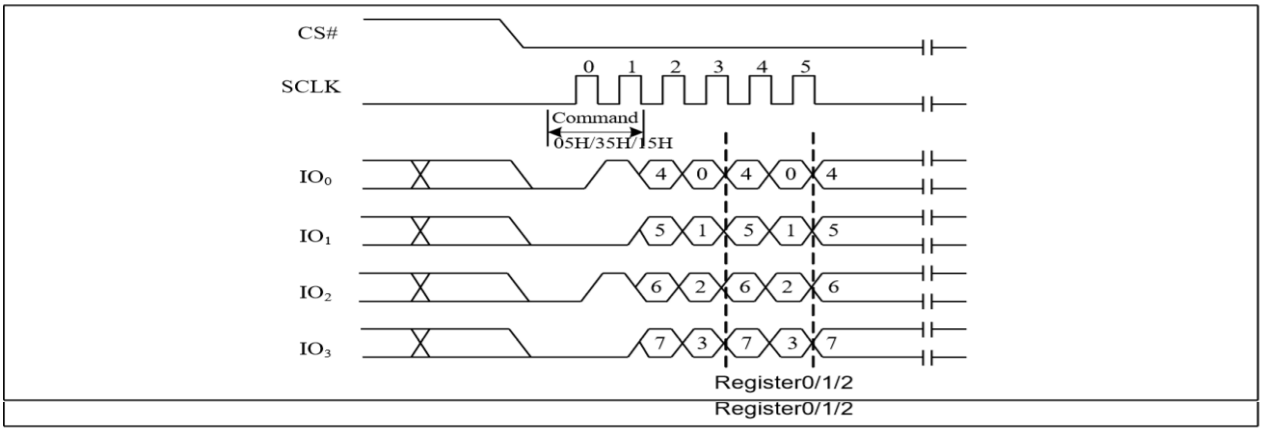


Figure 9. Read Status Register (RDSR1/RDSR2/RDSR3) Sequence (QPI Mode)
图 9。读取状态寄存器(RDSR1/RDSR2/RDSR3)序列(QPI 模式)



10.9 Write Status Register (WRSR1/WRSR2/WRSR3)

10.10 写状态寄存器(WRSR1/WRSR2/WRSR3)

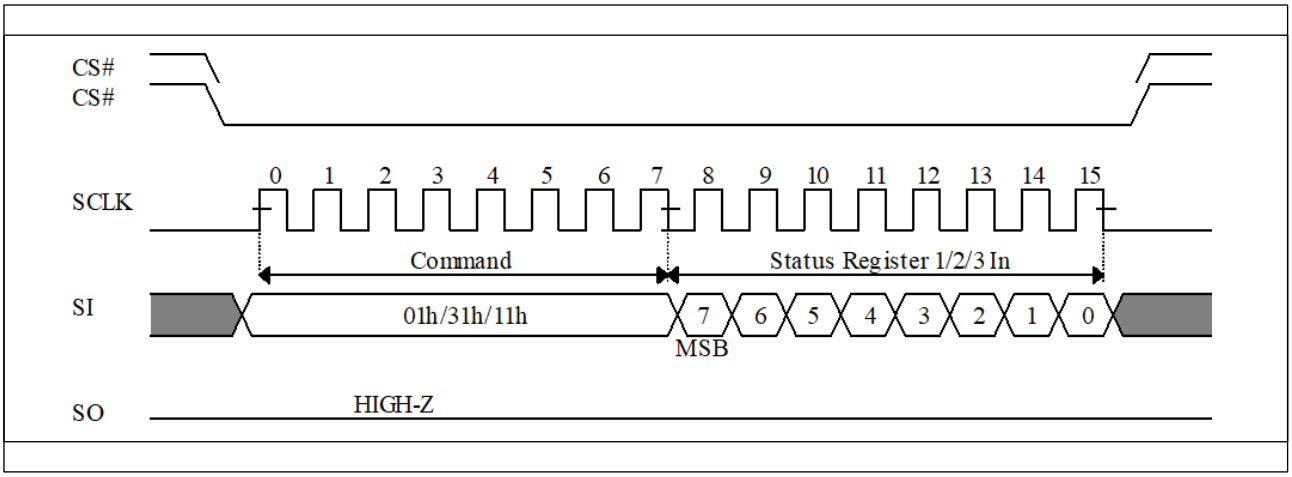
The Write Status Register (WRSR1/WRSR2/WRSR3) command allows new values to be written to the Status Register. Before sending WRSR1/WRSR2/WRSR3 command, the Write Enable (WREN) command must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR command can change the value of Block Protect (BP4, BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in "Table 3. Protected Area Sizes").

写状态寄存器(WRSR1/WRSR2/WRSR3)命令允许将新值写入状态寄存器。发送 WRSR1/WRSR2/WRSR3 命令之前，必须解码并执行写使能(WREN)命令，以预先设置写使能锁存(WEL)位。WRSR 命令可以更改块保护(BP4、BP3、BP2、BP1、BP0)位的值，以定义内存的受保护区域(如中所示)Table 3. 保护区大小”)。

In SPI, CS# must go high exactly at the 8 bits or 16 bits data boundary; In DOPI, CS# must go high while clock is low; otherwise, the command will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

在 SPI 中，CS#必须恰好在 8 位或 16 位数据边界处变为高电平；在 DOPI，CS#必须在时钟为低电平时变为高电平；否则，该命令将被拒绝并且不被执行。一旦片选(CS#)变为高电平，自定时写状态寄存器周期时间(tW)就会启动。在写入状态寄存器周期进行期间，仍可检出正在写入(WIP)位。WIP 在 tW 时序期间置 1，当写状态寄存器周期完成时置 0，并且写使能锁存器(WEL)位复位。

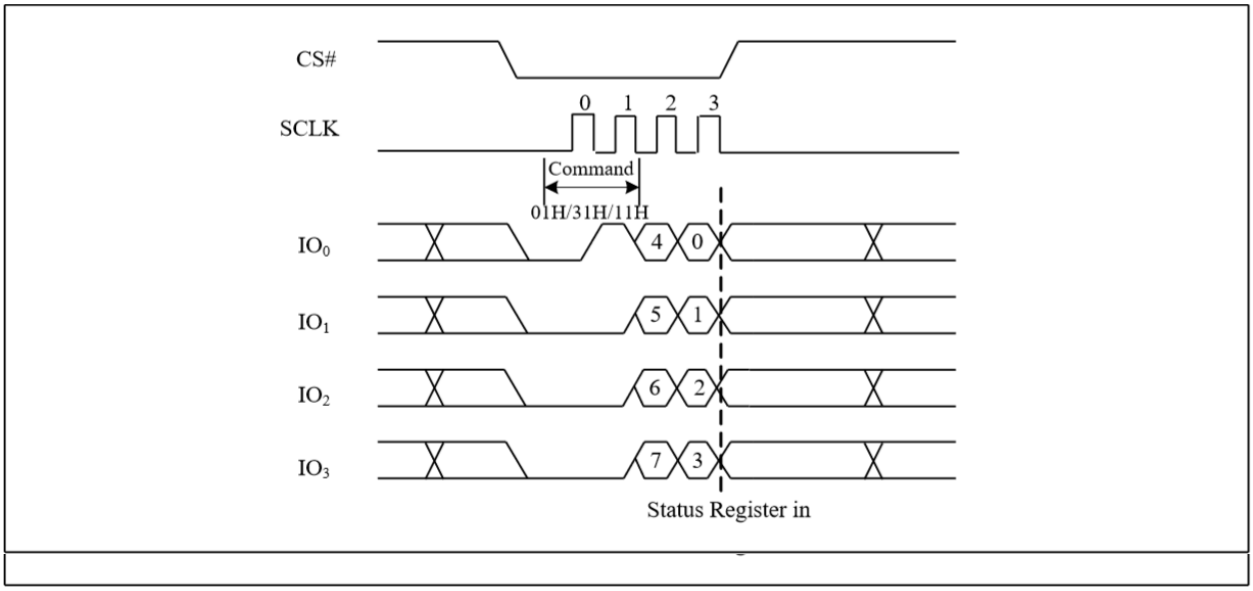
Figure 10. Write Status Register (WRSR) Sequence (SPI Mode)
图 10。写状态寄存器(WRSR)序列(SPI 模式)



Note: The CS# must go high exactly at 8 bits data boundary to completed the write register command.

注意:CS#必须恰好在 8 位数据边界变为高电平，才能完成写寄存器命令。

Figure 11. Write Status Register (WRSR) Sequence (QPI Mode)
图 11。写状态寄存器(WRSR)序列(QPI 模式)



10.11 Read Data Bytes (READ)
10.12 读取数据字节(Read)

The Read Data Bytes command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. The address counter rolls over to 0 when the highest address has been reached.

“读取数据字节”命令后是一个 3 字节的地址(A23-A0)，每个位在 SCLK 的上升沿被锁存。然后，在 SCLK 的下降沿期间，在该地址的存储器内容在 s0 上被移出，每个比特以最大频率 fR 被移出。寻址的第一个字节可以在任何位置。每移出一个字节的数据后，地址会自动递增到下一个更高的地址。因此，整个存储器可以用一个读数据字节(read)命令读取。当达到最高地址时，地址计数器翻转到 0。

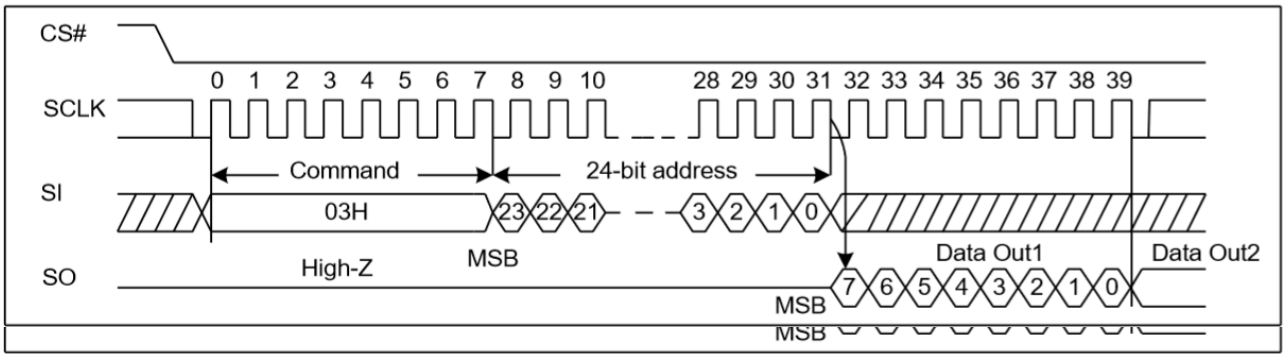
Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

当擦除、编程或写入周期正在进行时，读取数据字节 (Read)命令被拒绝，对正在进行的周期没有任何影响。

The READ command sequence: CS# goes low → sending READ command → 3-byte address on SI → data out on SO → to end READ operation can use CS# to high at any time during data out.

读取命令序列:CS#变为低电平→发送读取命令→SI 上的 3 字节地址→SO 上的数据输出→要结束读取操作，可以在数据输出期间随时使用 CS#变为高电平。

Figure 12. Read Data Bytes (READ) Sequence (SPI Mode only)
图 12。读取数据字节(读取)序列(仅限 SPI 模式)



10.13 Read Data Bytes at Higher Speed(FAST_READ)
10.14 以更高的速度读取数据字节(FAST_READ)

The Read Data Bytes at Higher Speed (Fast_Read) command is for quickly reading data out. It is followed by a 3-byte (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single FAST_READ command. The address counter rolls over to 0 when the highest address has been reached.

高速读取数据字节(Fast_Read)命令用于快速读取数据。其后是一个 3 字节(A23-A0)和一个虚拟字节，每个位在 SCLK 的上升沿被锁存。然后，在 SCLK 的下降沿期间，以最大频率 fC 将该地址的存储器内容移出 s0，每个比特被移出。寻址的第一个字节可以在任何位置。每移出一个字节的数据后，地址会自动递增到下一个更高的地址。因此，可以用一个 FAST_READ 命令读取整个存储器。当达到最高地址时，地址计数器翻转到 0。

The FAST_READ command sequence: CS# goes low→ sending FAST_READ command→ 3-byte address on SI→ 8 dummy cycles→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

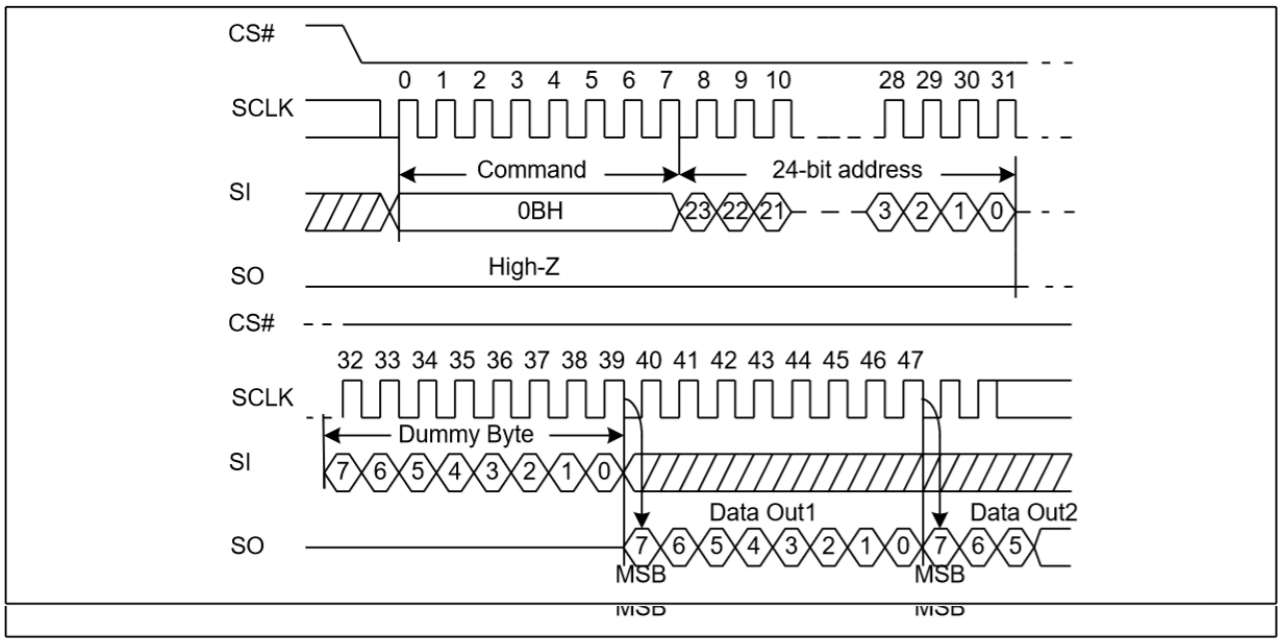
FAST_READ 命令序列:CS#变为低电平→发送 FAST_READ 命令→SI 上的 3 字节地址→ 8 个虚拟周期→SO 上的数据输出→要结束 FAST_READ 操作，可以在数据输出期间随时使用 CS#变为高电平。

While Program/ Erase/ Write Status Register cycle is in progress, FAST_READ command is rejected without any impact on the Program/Erase/Write Status Register current cycle.

当编程/擦除/写入状态寄存器周期正在进行时，FAST_READ 命令被拒绝，而对编程/擦除/写入状态寄存器当前周期没有任何影响。

Figure 13. Read at Higher Speed (FAST_READ) Sequence (SPI Mode)

图 13。高速读取(FAST_READ)序列(SPI 模式)



Fast Read in QPI mode

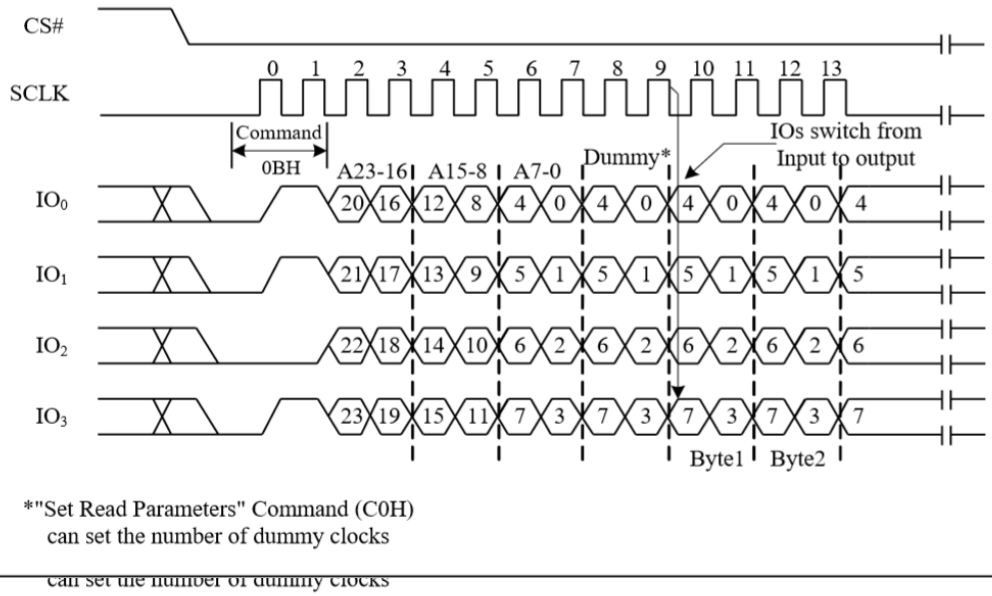
QPI 模式下的快速阅读

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the “Set Read Parameters (C0H)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8/8.

QPI 模式也支持快速读取命令。在 QPI 模式下，虚拟时钟的数量由“设置读取参数(C0H)”命令配置，以适应对最大快速读取频率或最小数据访问延迟有不同需求的各种应用。根据读取参数位 P[5:4]的设置，虚拟时钟的数量可以配置为 4/6/8/8。

Figure 14. Read at Higher Speed (FAST_READ) Sequence (QPI Mode)

图 14。以更高速度读取(FAST_READ)序列(QPI 模式)



*"Set Read Parameters" Command (C0H)
can set the number of dummy clocks

10.15 Dual Output Fast Read (DREAD)
10.16 双输出快速读取(DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

DREAD 指令使读取模式下串行 NOR 闪存的吞吐量加倍。地址在 SCLK 的上升沿锁存，每两位数据(在 2 个 I/O 引脚上交错)在 SCLK 的下降沿以最大频率 ft 移出。第一个地址字节可以在任何位置。每个字节数据移出后，地址自动增加到下一个更高的地址，因此整个存储器可以在一个单独的指令中读出。当达到最高地址时，地址计数器翻转到 0。一旦写入恐惧指令，随后的数据输出将作为 2 位执行，而不是之前的 1 位。

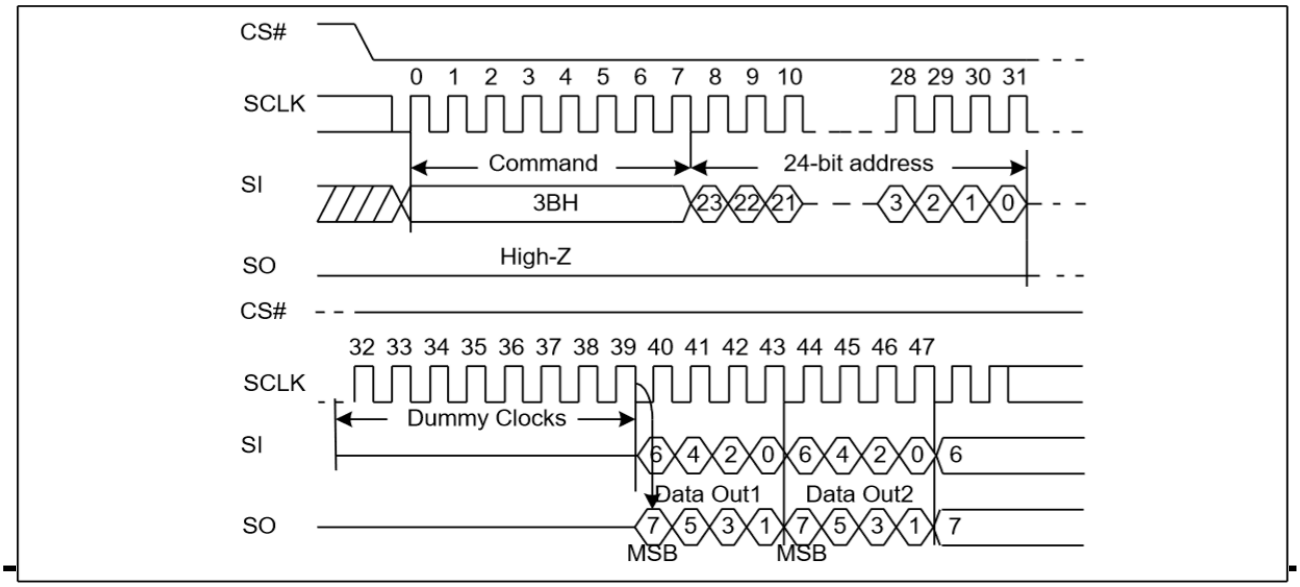
The sequence of issuing DREAD instruction is: CS# goes low→ sending DREAD instruction→ 3-byte address on SIO0→ 8 dummy cycles on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation can use CS# to high at any time during data out.

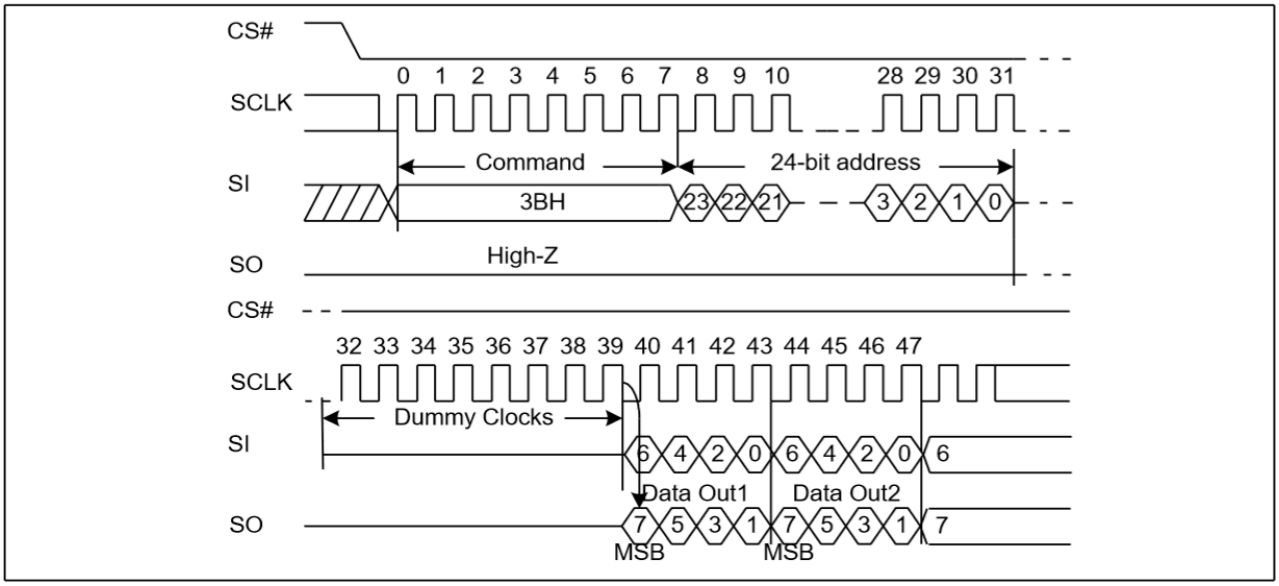
发出 DREAD 指令的顺序是:CS#变低→发送 DREAD 指令→SiO 0 上的 3 字节地址→SiO 0 上的 8 个虚拟周期 SIO1 & SIO0 上的数据输出交错→要结束 DREAD 操作可以在数据输出期间的任何时候使用 CS#变高。

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

当编程/擦除/写入状态寄存器周期正在进行时，DREAD 指令被拒绝，而对编程/擦除/写入状态寄存器当前周期没有任何影响。

Figure 15. Dual Output Fast Read (DREAD) Sequence (SPI Mode only)
图 15。双路输出快速读取(DREAD)序列(仅限 SPI 模式)





10.17 Quad Output Fast Read (QREAD)

10.18 四路输出快速读取(QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register 2 must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

QREAD 指令在读取模式下启用串行 NOR 闪存的四倍吞吐量。发送 QREAD 指令之前，状态寄存器 2 的四通道使能(QE)位必须设为“1”。地址在 SCLK 的上升沿锁存，每四位数据(在 4 个 I/O 引脚上交错)在 SCLK 的下降沿以最大频率 fQ 移出。第一个地址字节可以在任何位置。每个字节数据移出后，地址会自动增加到下一个更高的地址，因此可以通过一条 QREAD 指令读出整个存储器。当达到最高地址时，地址计数器翻转到 0。一旦写入 QREAD 指令，随后的数据输出将作为 4 位执行，而不是之前的 1 位。

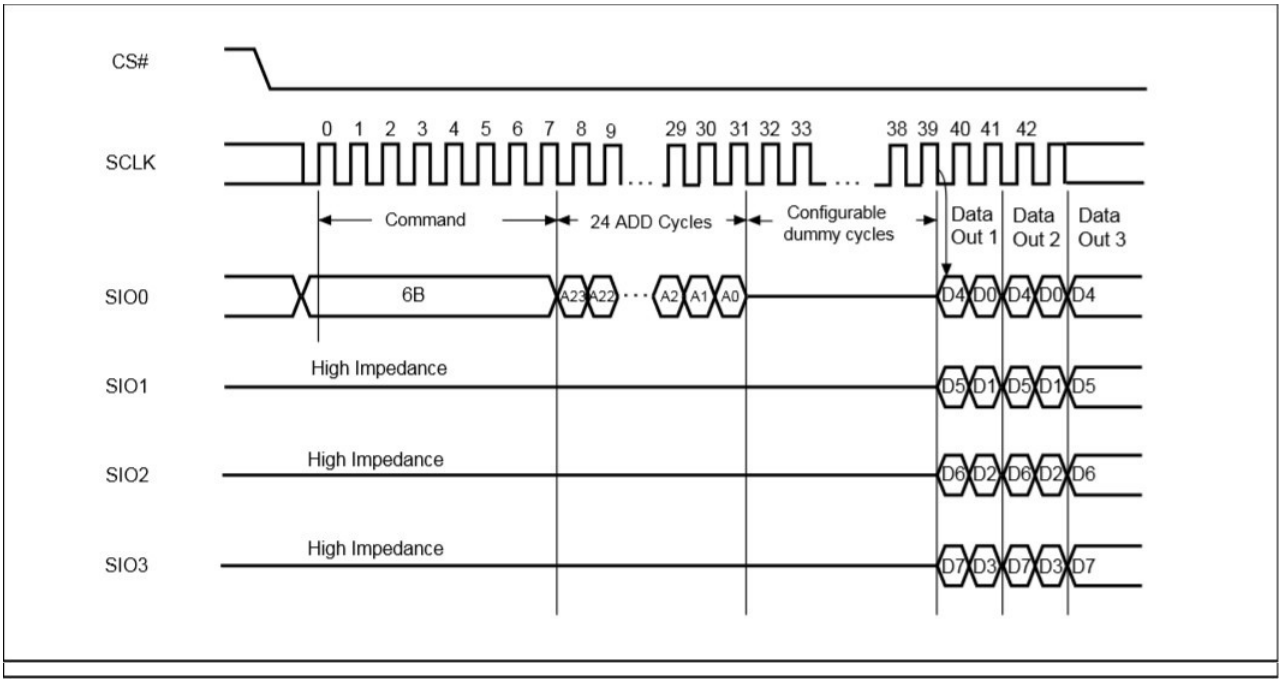
The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8 dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

发出 QREAD 指令的顺序是:CS#变低→发送 QREAD 指令→SI 上的 3 字节地址→ 8 个伪周期 SIO3、SIO2、SIO1 & SIO0 上的数据输出交错→要结束 QREAD 操作可以在数据输出期间的任何时候使用 CS#变高。

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

当编程/擦除/写入状态寄存器周期正在进行时，QREAD 指令被拒绝，而对编程/擦除/写入状态寄存器当前周期没有任何影响。

Figure 16. Quad Output Fast Read (QREAD) Sequence (SPI Mode only)
图 16。四路输出快速读取(QREAD)序列(仅限 SPI 模式)



10.19 Dual I/O Fast Read (2READ)

10.20 双 I/O 快速读取(2 个读取)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by

SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure17. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

双 I/O 快速读取命令类似于双输出快速读取命令，但能够输入 3 字节地址(A23-0)和“连续读取模式”字节，SI 和 SO 每时钟 2 位，每一位在 SCLK 上升沿锁存，然后存储器内容从 SI 和 SO 每时钟周期移出 2 位。命令序列如下图 17 所示。寻址的第一个字节可以在任何位置。每移出一个字节的数据后，地址会自动递增到下一个更高的地址。

Dual I/O Fast Read with “Continuous Read Mode”
具有“连续读取模式”的双 I/O 快速读取

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-4) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure18. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

双 I/O 快速读取命令可以通过在输入 3 字节地址(A23-A0)后设置“连续读取模式”位(M7-4)来进一步减少命令开销。如果“连续读取模式”位(M5-4) = (1，0)，则下一个双 I/O 快速读取命令(在 CS#升高然后降低之后)不需要 BBH 命令代码。命令序列如下图 18 所示。如果“连续读取模式”位(M5-4)不等于(1，0)，则下一个命令需要第一个 BBH 命令代码，从而返回正常操作。建议为下一条指令(16 个时钟)在 IO0 上输入 FFFFh，以确保 M4 = 1，并使器件返回正常工作状态。

Figure 17. Dual I/O Fast Read (2READ) Sequence (M5-4≠(1, 0))

图 17。双 I/O 快速读取(2READ)序列(M5-4≦(1，0))

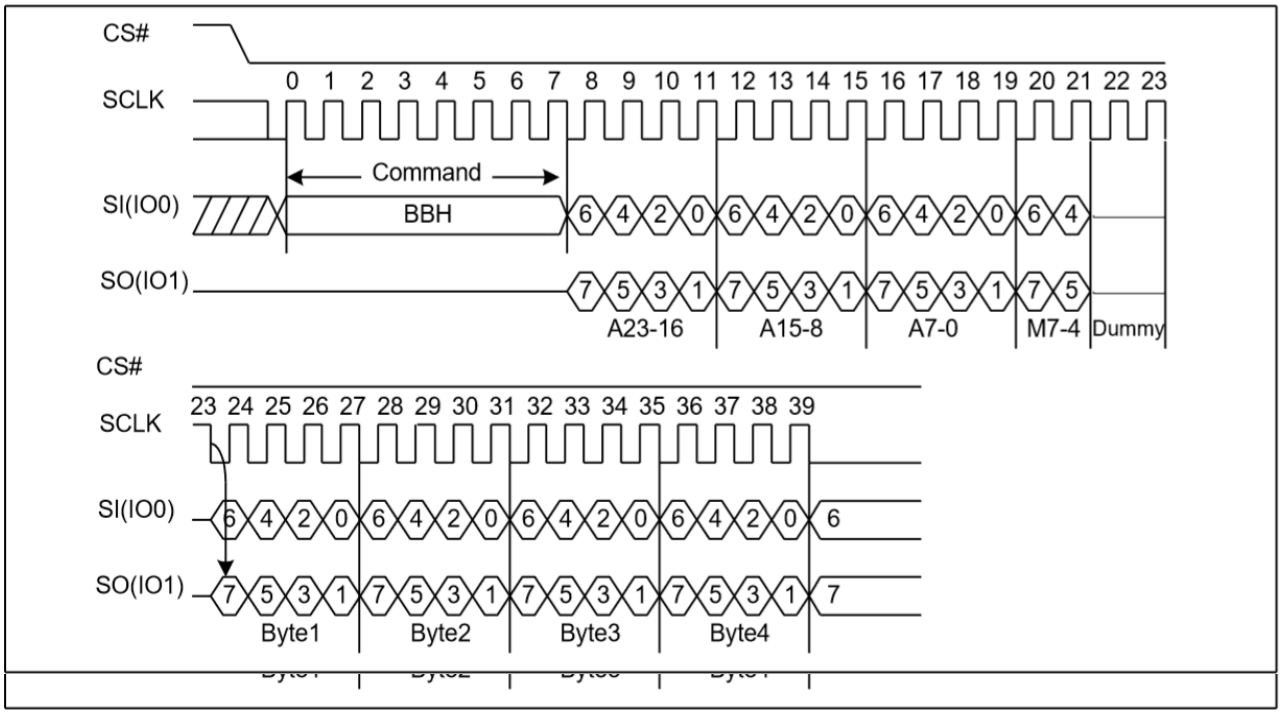
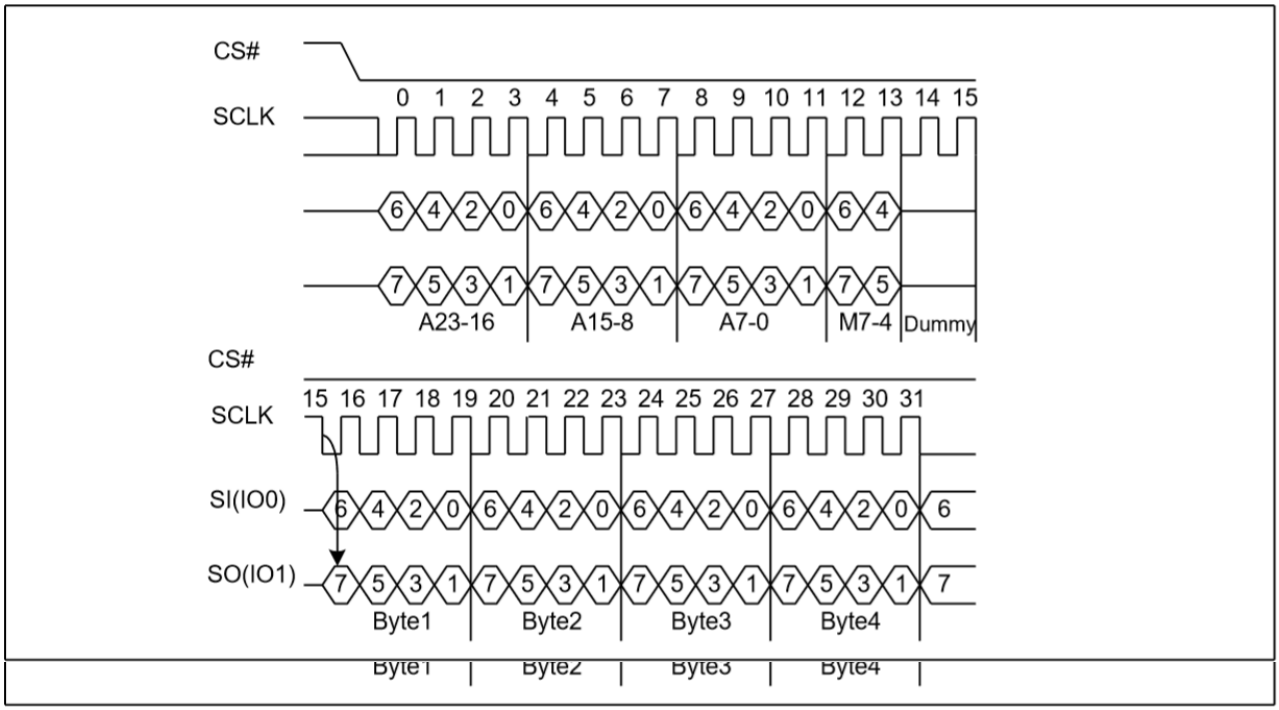


Figure 18. Dual I/O Fast Read (2READ) Sequence (M5-4=(1, 0))

图 18。双 I/O 快速读取(2READ)序列(M5-4=(1，0))



10.21 Quad I/O Fast Read (4READ)

10.22 四路 I/O 快速读取(4 路)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure19. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

四路 I/O 快速读取命令类似于双路 I/O 快速读取命令，但能够通过 IO0、IO1、IO2、IO3 输入 3 字节地址(A23-0)和一个“连续读取模式”字节以及 4 个伪时钟(每个时钟 4 位),每个位在 SCLK 上升沿期间被锁存，然后存储器内容在每个时钟周期从 IO0、IO1、IO2、IO3 移出 4 位。命令序列如下图 19 所示。寻址的第一个字节可以在任何位置。每移出一个字节的数据后，地址会自动递增到下一个更高的地址。对于四通道 I/O 快速读取命令，状态寄存器(S9)的四通道使能位(QE)必须设置为使能。

Quad I/O Fast Read with “Continuous Read Mode”

具有“连续读取模式”的四通道 I/O 快速读取

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure20. If the “Continuous Read Mode” bits (M5-4) do not equal to (1, 0), the next command requires the first EBH command code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

通过在输入 3 字节地址(A23-A0)后设置“连续读取模式”位(M7-0)，四通道 I/O 快速读取命令可以进一步降低命令开销。如果“连续读取模式”位(M5-4) = (1，0)，则下一个四通道 I/O 快速读取命令(在 CS#升高然后降低之后)不需要 EBH 命令代码。命令序列如下面的图 20 所示。如果“连续读取模式”位(M5-4)不等于(1，0)，则下一个命令需要第一个 EBH 命令代码，从而返回正常操作。建议为下一条指令(8 个时钟)在 IO0 上输入 FFh，以确保 M4 = 1，并使器件返回正常工作状态。

Figure 19. Quad I/O Fast Read (4READ) Sequence (M5-4≠(1, 0))
图 19。四通道 I/O 快速读取(4 读)序列(M5-4≦(1，0))

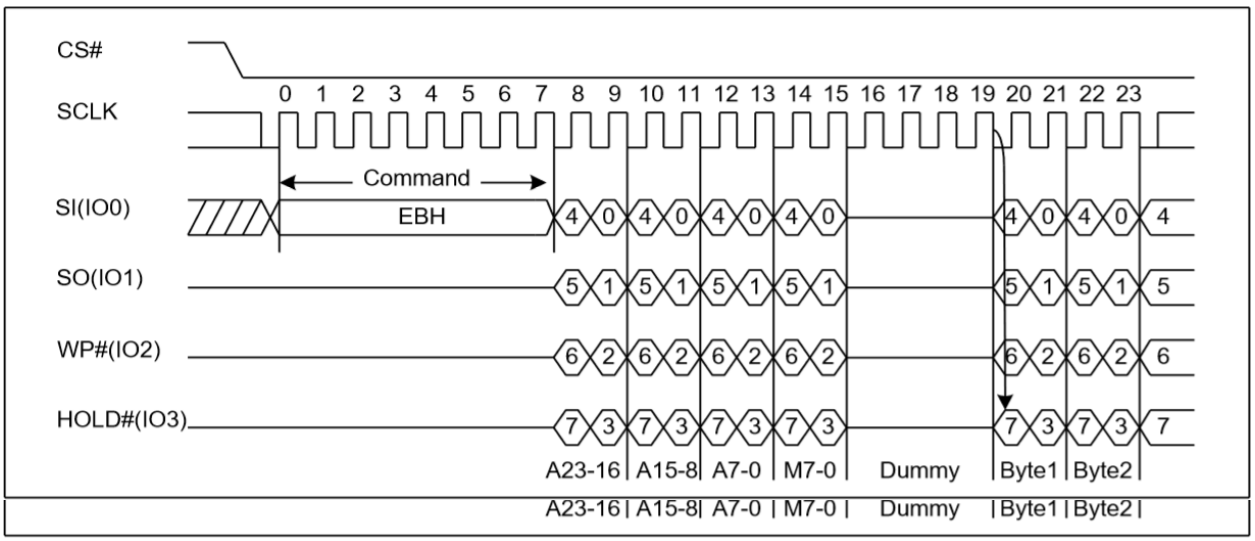
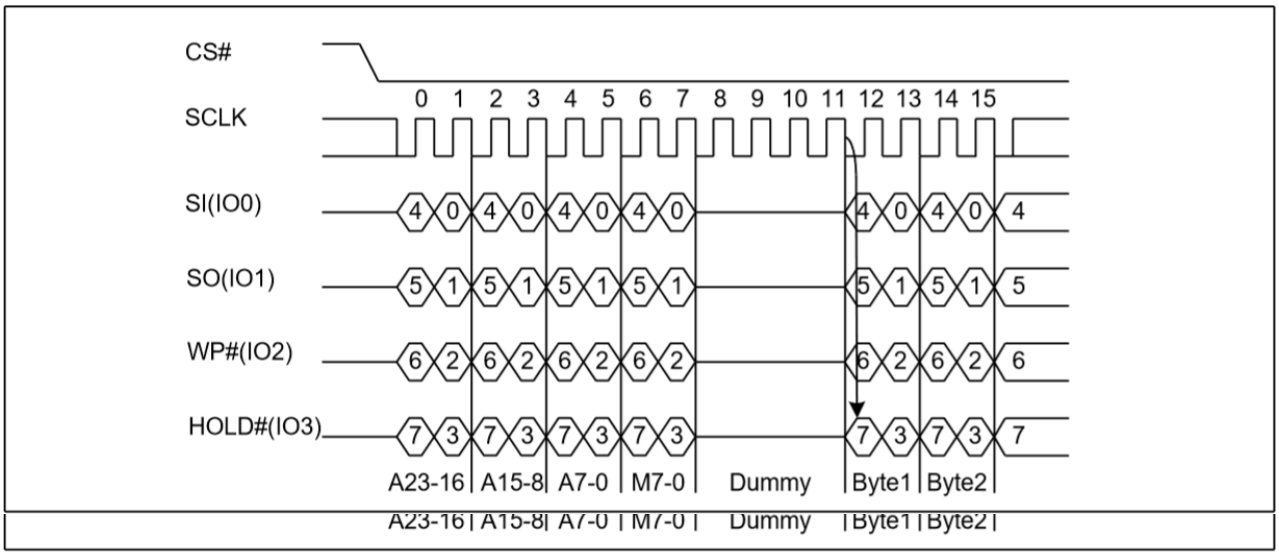

CS#
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
Command
SI(IO0)
EBH
SO(IO1)
WP#(IO2)
HOLD#(IO3)
A23-16
A15-8
A7-0
M7-0
Dummy
Byte1
Byte2

Figure 20. Quad I/O Fast Read (4READ) Sequence (M5-4=(1, 0))

图 20。四通道 I/O 快速读取(4 读)序列(M5-4=(1，0))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

标准 SPI 模式下的四通道 I/O 快速读取，带"8/16/32/64 字节回绕"

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command. The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

四 I/O 快速读取命令可用于访问页面内的特定部分，方法是在 EBH 之前发出"带回绕的设置突发"(77H)命令。"设置带回绕的脉冲串"(77H)命令可以启用或停用以下 EBH 命令的"回绕"功能。启用"回绕"时，被访问的数据可以被限制在 256 字节页面的 8/16/32/64 字节部分。输出数据从命令中指定的初始地址开始，一旦到达 8/16/32/64 字节部分的结束边界，输出将自动绕过开始边界，直到 CS#被拉高以终止命令。具有回绕功能的突发允许使用高速缓存的应用快速获取关键地址，然后在固定长度(8/16/32/64 字节)的数据内填充高速缓存，而无需发出多个读取命令。"设置带回绕的脉冲串"命令允许设置三个"回绕位"W6-W4。W4 位用于启用或禁用"回绕"操作，而 W6-W5 用于指定页面内回绕部分的长度。

Quad I/O Fast Read in QPI mode

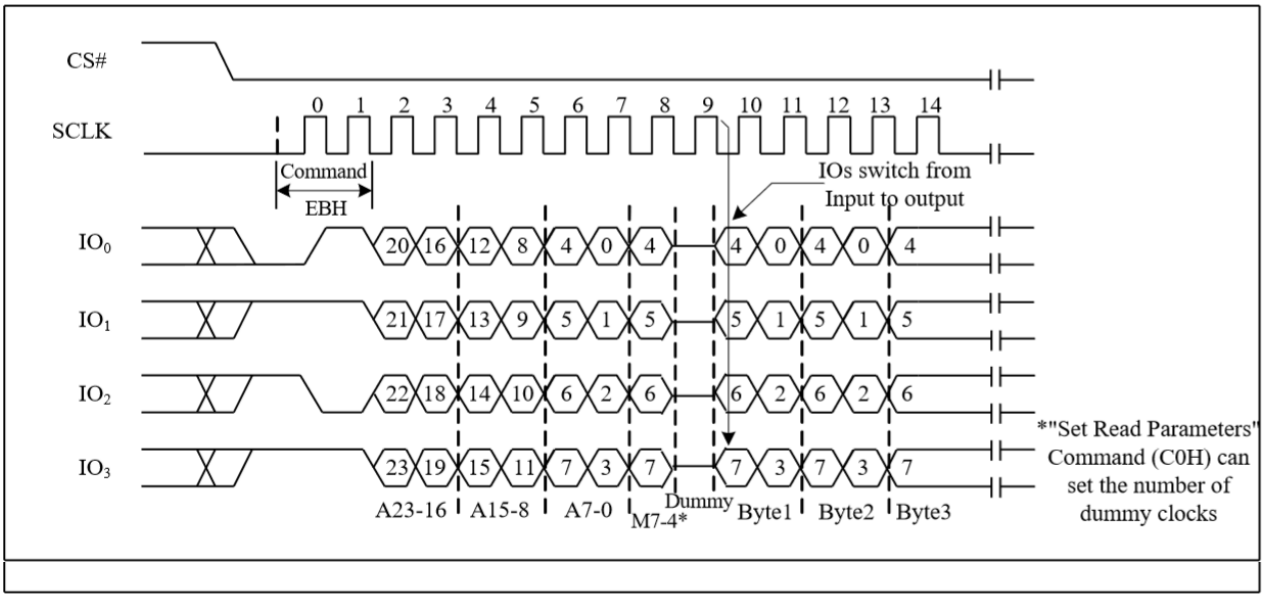
QPI 模式下的四路 I/O 快速读取

The Quad I/O Fast Read command is also supported in QPI mode. See Figure21. In QPI mode, the number of dummy clocks is configured by the “ Set Read Parameters (C0H) ” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8/8. In QPI mode, the “Continuous Read Mode” bits M7-M0 are also considered as dummy clocks. “Continuous Read Mode” feature is also available in QPI mode for Quad I/O Fast Read command. “Wrap Around” feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0CH) command must be used.

QPI 模式下也支持四 I/O 快速读取命令。参见图 21。在 QPI 模式下，虚拟时钟的数量由“设置读取参数(C0H)”命令配置，以适应对最大快速读取频率或最小数据访问延迟有不同需求的各种应用。根据读取参数位 P[5:4]的设置，虚拟时钟的数量可以配置为 4/6/8/8。在 QPI 模式下，“连续读取模式”位 M7-M0 也被视为虚拟时钟。“连续读取模式”功能在 QPI 模式下也可用于四 I/O 快速读取命令。“回绕”功能在四 I/O 快速读取命令的 QPI 模式下不可用。要在 QPI 模式下执行具有固定数据长度回绕的读取操作，必须使用专用的“带回绕的突发读取”(0CH)命令。

Figure 21. Quad I/O Fast Read (4READ) Sequence (M5-4=(1, 0) QPI)

图 21。四通道 I/O 快速读取(4 读)序列(M5-4=(1，0) QPI)



10.23 Quad I/O Word Fast Read (4READ_WD)
10.24 四路 I/O 字快速读取(4READ_WD)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure22. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command. Quad I/O Word Fast Read can only support SPI mode.

四通道 I/O 字快速读取命令与四通道 I/O 快速读取命令类似，只是最低地址位(A0)必须等于 0，并且只有 2 个伪时钟。命令序列如下面的图 22 所示。寻址的第一个字节可以在任何位置。每移出一个字节的数据后，地址会自动递增到下一个更高的地址。对于四通道 I/O 字快速读取命令，状态寄存器(S9)的四通道使能位(QE)必须设置为使能。四通道 I/O 字快速读取仅支持 SPI 模式。

Quad I/O Word Fast Read with “Continuous Read Mode”
“连续读取模式”下的四路 I/O 字快速读取

The Quad I/O Word Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure23. If the “Continuous Read Mode” bits (M5-4) do not equal

to (1, 0), the next command requires the first E7H command code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

通过在输入 3 字节地址(A23-A0)后设置“连续读取模式”位(M7-0)，四通道 I/O 字快速读取命令可以进一步降低命令开销。如果“连续读取模式”位(M5-4) = (1，0)，则下一个四通道 I/O 字快速读取命令(在 CS#升高然后降低之后)不需要 E7H 命令代码。命令序列如下面的图 23 所示。如果“连续读取模式”位(M5-4)不等于(1，0)，下一个命令需要第一个 E7H 命令代码，从而返回正常操作。建议为下一条指令(8 个时钟)在 IO0 上输入 FFh，以确保 M4 = 1，并使器件返回正常工作状态。

Figure 22. Quad I/O Word Fast Read (4READ_WD) Sequence (M5-4≠(1, 0))
图 22。四通道 I/O 字快速读取(4READ_WD)序列(M5-4≦(1，0))

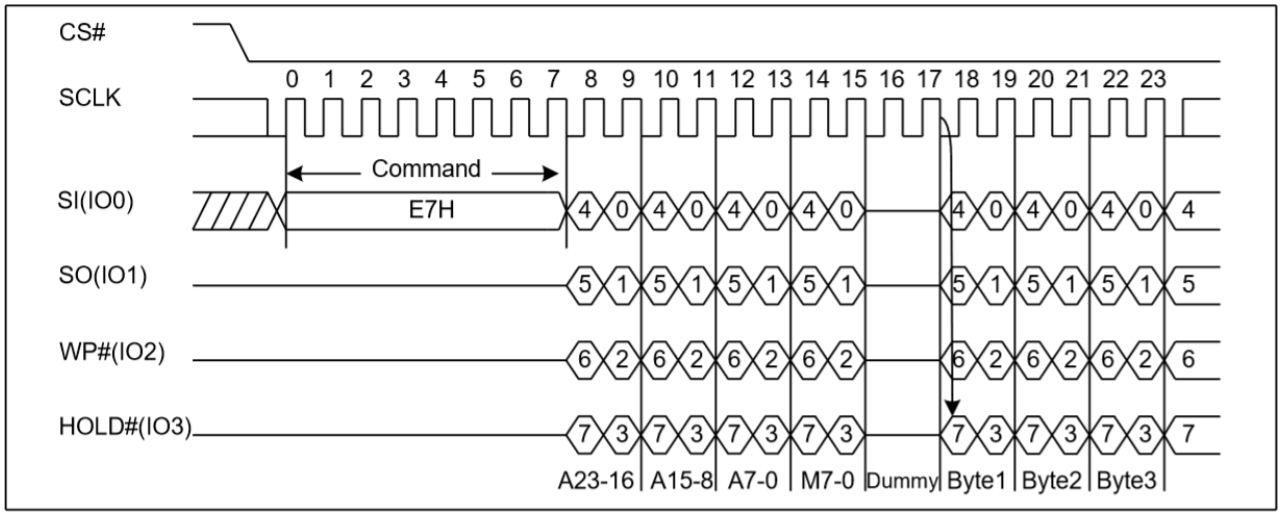
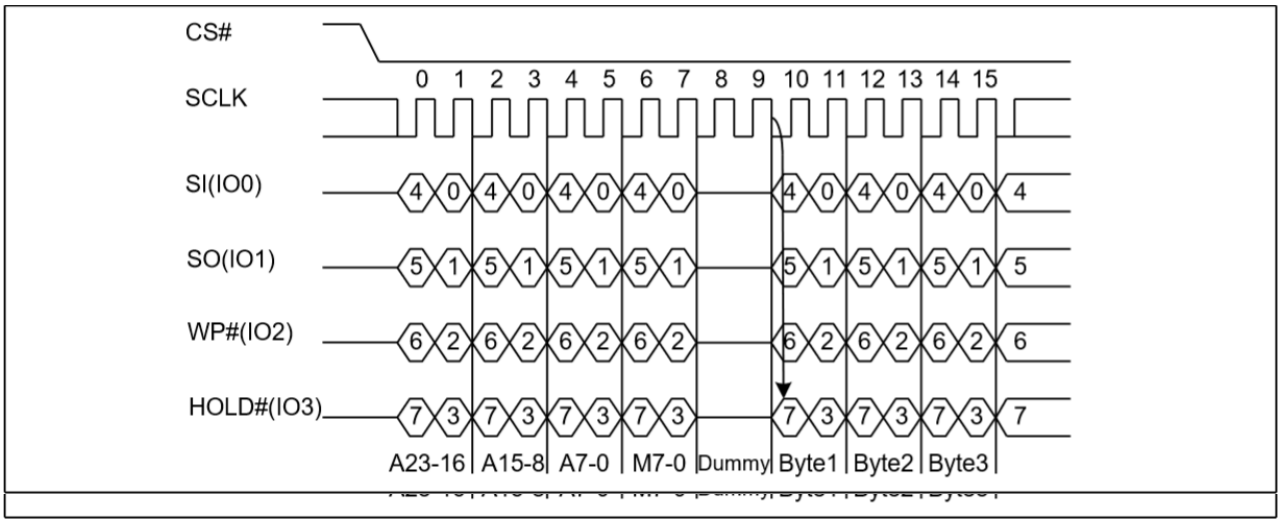


Figure 23. Quad I/O Word Fast Read (4READ_WD) Sequence (M5-4=(1, 0))
图 23。四通道 I/O 字快速读取(4READ_WD)序列(M5-4=(1，0))



Quad I/O Word Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode
标准 SPI 模式下的四路 I/O 字快速读取，带“8/16/32/64 字节回绕”

The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77H) commands prior to E7H. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following E7H commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

四 I/O 字快速读取命令可用于访问页面内的特定部分，方法是在 E7H 之前发出“带换行的组突发”(77H)命令。“设置带回绕的脉冲串”(77H)命令可以启用或禁用以下 E7H 命令的“回绕”功能。启用“回绕”时，被访问的数据可以被限制在 256 字节页面的 8/16/32/64 字节部分。输出数据从命令中指定的初始地址开始，一旦到达 8/16/32/64 字节部分的结束边界，输出将自动绕过开始边界，直到 CS#被拉高以终止命令。

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

具有回绕功能的突发允许使用高速缓存的应用快速获取关键地址，然后在固定长度(8/16/32/64 字节)的数据内填充高速缓存，而无需发出多个读取命令。“设置带回绕的脉冲串”命令允许设置三个“回绕位”W6-W4。W4 位用于启用或禁用“回绕”操作，而 W6-W5 用于指定页面内回绕部分的长度。

10.25 Set Burst with Wrap (SET_BSTRD)

10.26 设置带换行的突发(SET_BSTRD)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

在标准 SPI 模式下，Set Burst with Wrap 命令与"四通道 I/O 快速读取"和"四通道 I/O 字快速读取"命令配合使用，可访问 256 字节页面内固定长度的 8/16/32/64 字节部分。

The Set Burst with Wrap command sequence: CS# goes low→ sending SET_BSTRD command→

带 Wrap 命令序列的 Set 突发:CS#变为低电平→发送 SET_BSTRD 命令→

Send 24 dummy bits on SI→ Send 8 bits "Wrap bits" → data out on SO→ CS# goes high.

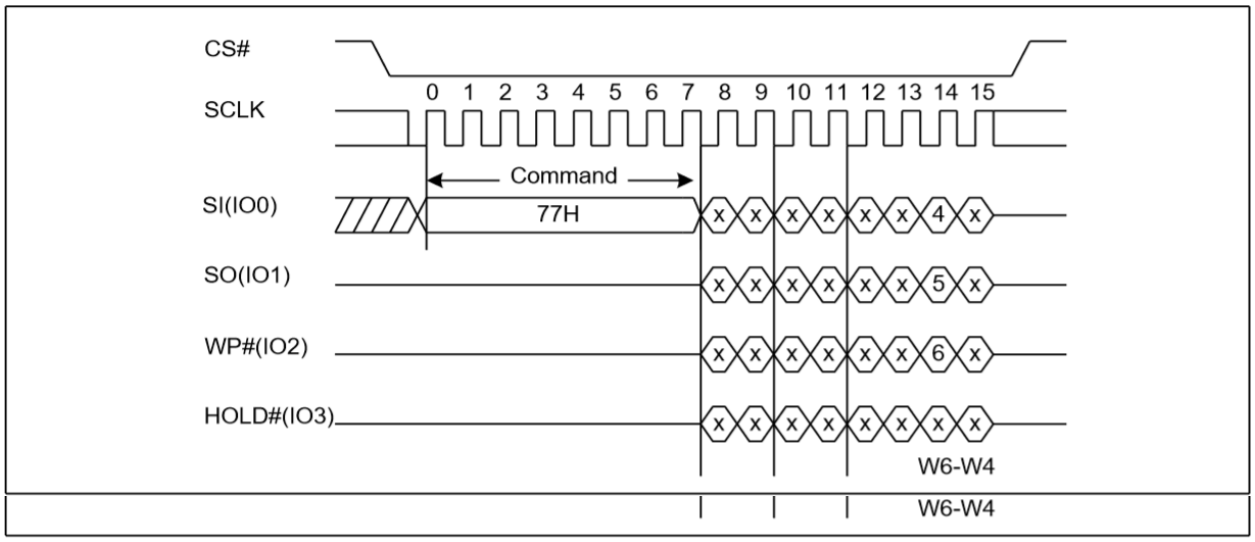
在 SI 上发送 24 个虚拟位→发送 8 位"回绕位"→在 SO 上输出数据→ CS#变为高电平。

W6, W5	W4=0		W4=1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A
W6，W5	W4=0		W4=1(默认)	
	环绕的	包装长度	环绕的	包装长度
0，0	是	8 字节	不	不适用的
0，1	是	16 字节	不	不适用的
1，0	是	32 字节	不	不适用的
1，1	是	64 字节	不	不适用的

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1. In QPI mode, the "Burst Read with Wrap (0CH)" command should be used to perform the Read Operation with "Wrap Around" feature. The Wrap Length set by W5-W6 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0H) command.

如果 W6-W4 位是由带回绕的突发设置命令设置的，所有随后的"四 I/O 快速读取"和"四 I/O 字快速读取"命令将使用 W6-W4 设置来访问任何页面内的 8/16/32/64 字节部分。要退出"回绕"功能并返回正常读取操作，应发出另一个带回绕命令的设置突发，以设置 W4=1。在 QPI 模式下，应使用"带回绕的突发读取(0CH)"命令来执行带"回绕"功能的读取操作。W5-W6 在标准 SPI 模式下设置的回绕长度在 QPI 模式下仍然有效，也可以通过"设置读取参数(C0H)命令"重新配置。

Figure 24. Set Burst with Wrap Sequence
图 24。设置带回绕序列的突发


CS#
SCLK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Command
SI(IO0)
77H
SO(IO1)
WP#(IO2)
HOLD#(IO3)
W6-W4
W6-W4

10.27 Page Program (PP)

10.28 页面程序

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending each Page Program command. The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (32-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

页面编程(PP)命令用于对存储器进行编程。在发送每个页面编程命令之前，必须先执行写使能(WREN)命令，以设置写使能锁存(WEL)位。该器件仅对发送至器件的最后 256 个数据字节进行编程。对于 256 字节页面编程，最后一个地址字节(8 个最低有效地址位 A7-A0)应设置为 0。如果 A7-A0 不全为 0，则超过页面长度的传输数据从当前所选页面的起始地址(最后 8 位全为 0 的 32 位地址)开始编程。如果发送到器件的数据字节超过 256，则最后 256 个数据字节在请求页面进行编程，之前的数据将被忽略。如果发送到器件的数据字节未超过 256，数据将被编程到页面的请求地址。对同一页的其他数据字节没有影响。

The Page Program command sequence: CS# goes low→ sending PP command →3-byte address

页面编程命令序列:CS#变为低电平→发送 PP 命令→3 字节地址

→ at least 1-byte data → CS# goes high.

→至少 1 字节数据→ CS#变为高电平。

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary in SPI (the latest eighth bit of data being latched in), otherwise the command will be rejected and will not be executed.

在整个页面编程周期中，CS#必须保持为低；CS#必须恰好在 SPI 中的字节边界处变为高电平(被锁存数据的最新第八位)，否则命令将被拒绝且不会执行。

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

一旦 CS#变为高电平，就会启动自定时页面编程周期(持续时间为 tPP)。当页面编程周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时页面编程周期期间，正在写入(WIP)位为 1，当它完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

不执行应用于受块保护(BP4、BP3、BP2、BP1 和 BP0)保护的页面的页面编程(PP)命令。

Figure 25. Page Program (PP) Sequence (SPI Mode)
图 25。页面编程(PP)序列(SPI 模式)

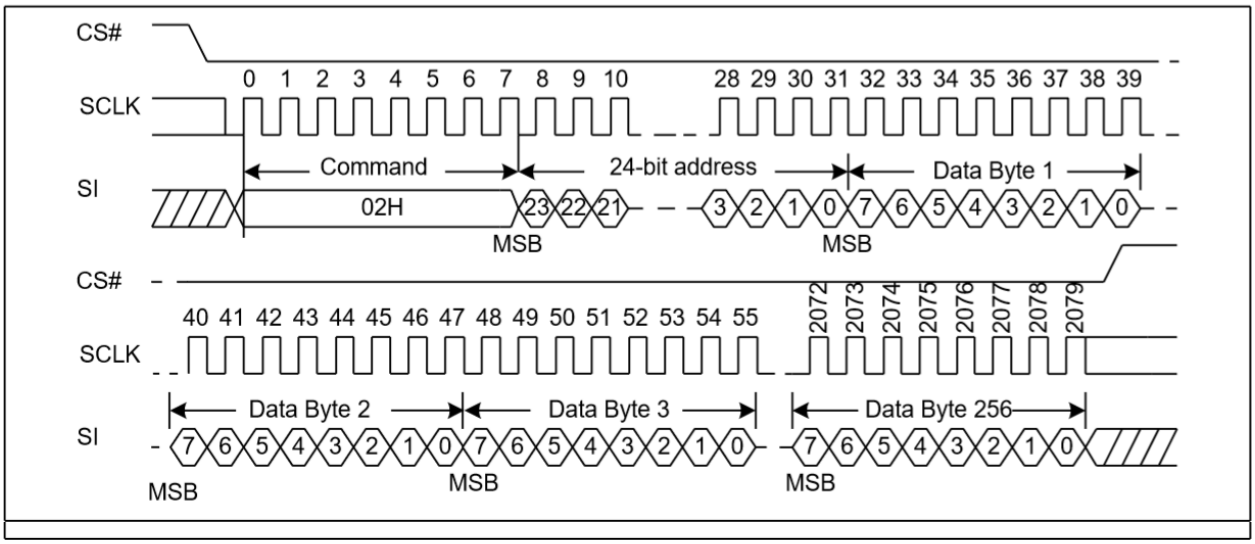
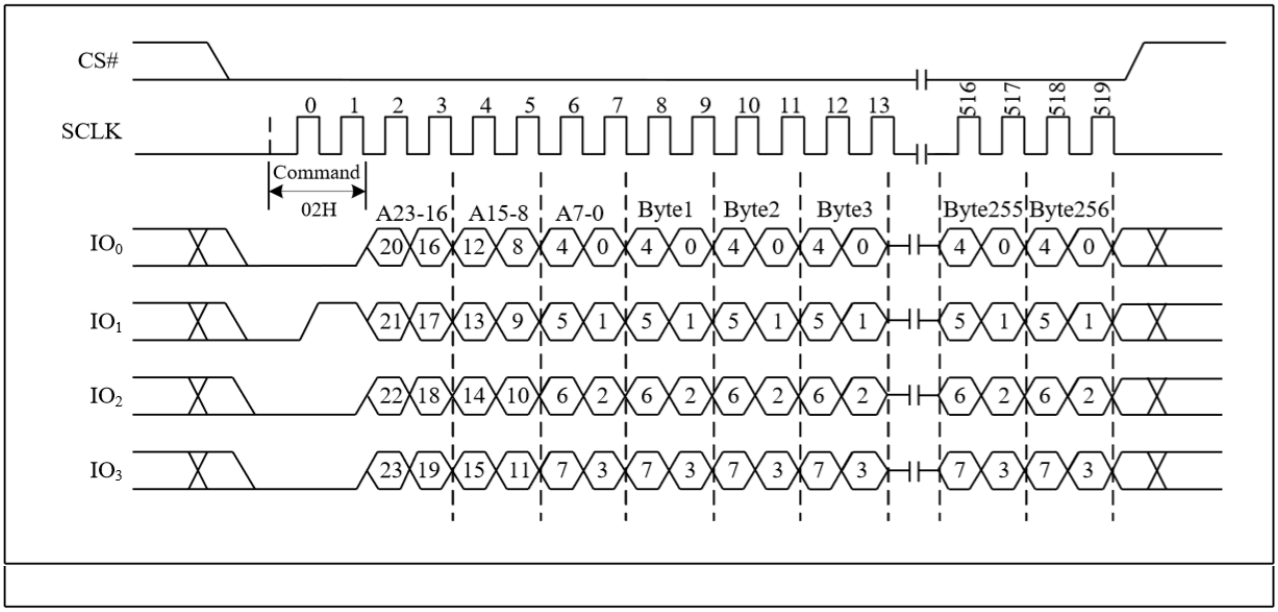


Figure 26. Page Program (PP) Sequence (QPI Mode)

图 26。页面程序(PP)序列(QPI 模式)



10.29 Quad Page Program (QPP)

10.30 四页程序(QPP)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins. Quad Page Program can only support SPI mode.

四页编程命令用于使用四个引脚对存储器进行编程:IO0、IO1、IO2 和 IO3。要使用四重页编程，必须设置状态寄存器位 9 中的四重使能(QE=1)。在发送页面编程命令之前，必须先执行写使能(WREN)命令来设置写使能锁存(WEL)位。将 CS#拉低，输入四页编程命令，然后输入命令代码(32H)、三个地址字节和 IO 引脚上的至少一个数据字节。四页程序只能支持 SPI 模式。

The command sequence is shown in Figure27. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (QPP) command is not executed.

命令序列如图 27 所示。如果发送到器件的数据超过 256 个字节，先前锁存的数据将被丢弃，最后

256 个数据字节保证在同一页内正确编程。如果发送到器件的数据字节少于 256 个，它们将被正确编程到所请求的地址，而不会对同一页面的其他字节产生任何影响。最后一个数据字节的第八位锁存后，CS#必须变为高电平；否则，不执行四页编程(QPP)命令。

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

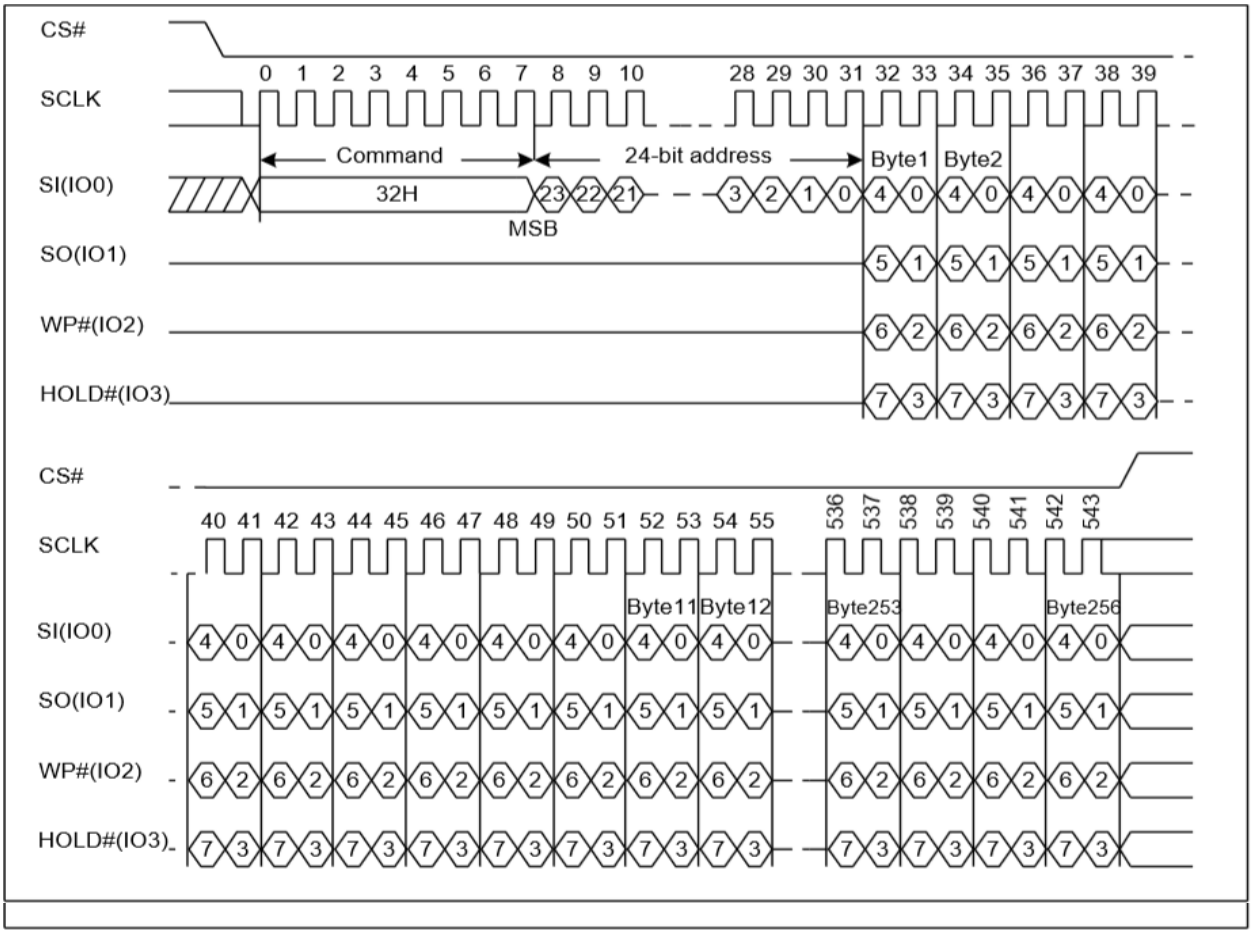
一旦 CS#变为高电平，就会启动自定时四页编程周期(持续时间为 tPP)。当四页编程周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时四页编程周期期间，正在写入(WIP)位为 1，完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

不执行应用于受块保护(BP4、BP3、BP2、BP1 和 BP0)保护的页面的四页面编程命令。

Figure 27. Quad Page Program (QPP) Sequence

图 27。四页程序(QPP)序列



10.31 Sector Erase (SE)
10.32 扇区擦除

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. Any address of the sector (Please refer to "5. MEMORY ORGANIZATION") is a valid address for Sector Erase (SE) command. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the command will be rejected and not executed.

扇区擦除(se)命令擦除所选扇区的所有数据。必须先执行写使能(WREN)命令来设置写使能锁存(WEL)位。扇区的任何地址(请参考“5。存储器组织”)是扇区擦除(se)命令的有效地址。CS#必须恰好在字节边界处变为高电平(地址字节的最低有效位被锁存)；否则，该命令将被拒绝并且不被执行。

The Sector Erase (SE) command sequence: CS# goes low→ sending SE command→ 3-byte address → CS# goes high.

扇区擦除(se)命令序列:CS#变为低电平→发送 SE 命令→ 3 字节

地址→ CS#变高。

As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The WIP sets 1 during the self-timed Sector Erase cycle, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (Block Protect Mode), the Sector Erase (SE) command will not be executed on the block. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit is not executed.

一旦 CS#变为高电平，便会启动自定时扇区擦除周期(持续时间为 tSE)。当扇区擦除周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时扇区擦除周期期间，WIP 置 1，并且当扇区擦除周期完成时，WIP 清零，并且写使能锁存器(WEL)位被清零。如果块受 BP 位保护(块保护模式)，则不会在块上执行扇区擦除(se)命令。不执行应用于受块保护(BP4、BP3、BP2、BP1 和 BP0)位保护的扇区的扇区擦除(se)命令。

Figure 28. Sector Erase (SE) Sequence (SPI Mode)

图 28。扇区擦除(se)序列(SPI 模式)

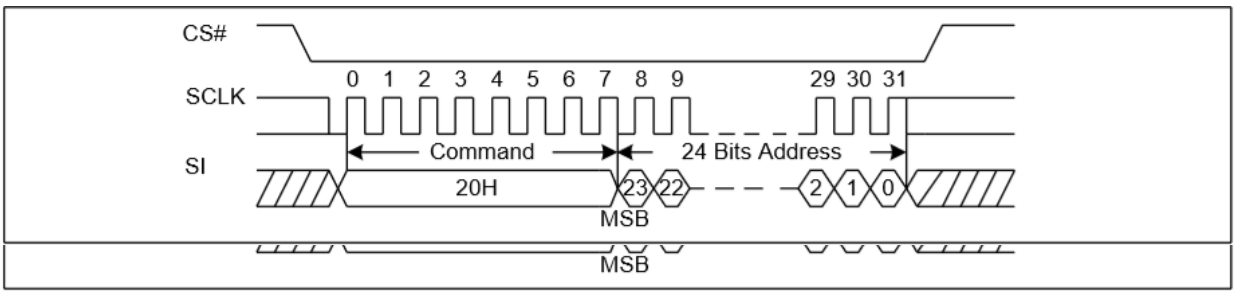
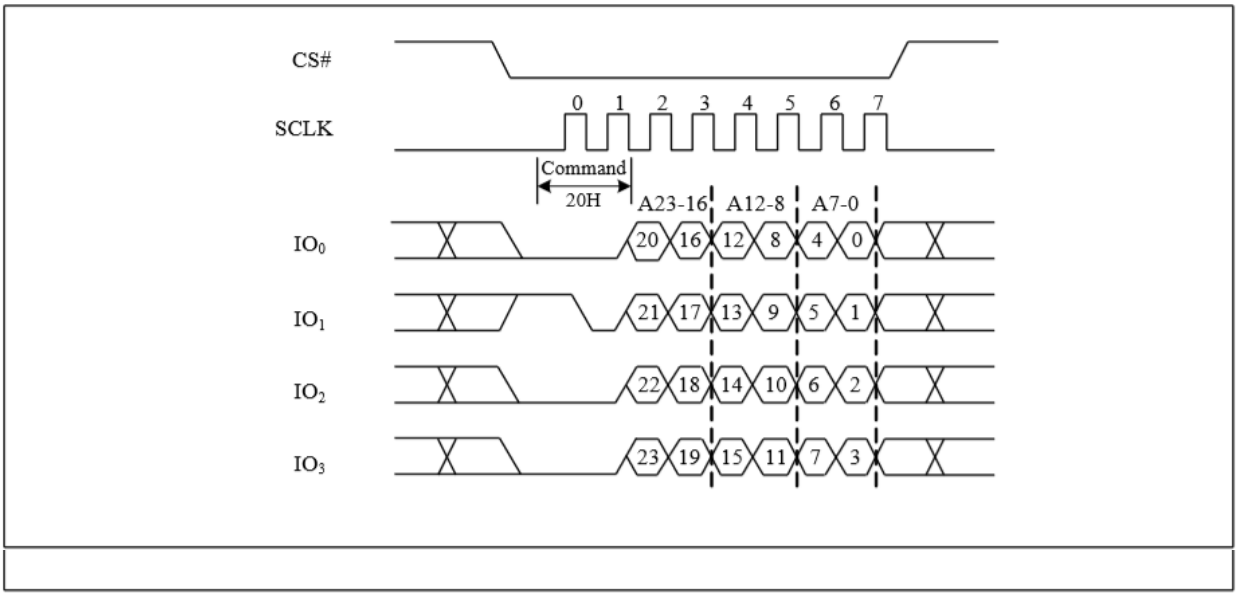


Figure 29. Sector Erase (SE) Sequence (QPI Mode)

图 29。扇区擦除(se)序列(QPI 模式)



10.33 Block Erase for 32K-byte (BE32K)
10.34 32K 字节的块擦除(BE32K)

The Block Erase for 32K-byte (BE32K) command is erased the all data of the chosen block. The command is used for 4M-byte block erase operation. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. Any address of the block (Please refer to "5. MEMORY ORGANIZATION") is a valid address for Block Erase for 32KB (BE32K) command. The CS# must go high exactly at the byte boundary (the least significant bit of address byte

been latched-in); otherwise, the command will be rejected and not executed.

32K 字节块擦除(BE32K)命令擦除所选块的所有数据。该命令用于 4M 字节的块擦除操作。必须先执行写使能(WREN)命令来设置写使能锁存(WEL)位。块的任何地址(请参考″5。存储器组织”)是 32KB (BE32K)命令的块擦除的有效地址。CS#必须恰好在字节边界处变为高电平(地址字节的最低有效位被锁存)；否则，该命令将被拒绝并且不被执行。

The Block Erase for 32KB (BE32K) command sequence: CS# goes low→ sending BE32K command→ 3-byte address → CS# goes high.

32KB 块擦除(BE32K)命令序列:CS#变为低电平→发送 BE32K 命令→ 3 字节地址→ CS#变为高电平。

As soon as CS# is driven high, the self-timed Block Erase for 32KB cycle (whose duration is tBE32K) is initiated. While the Block Erase for 32KB cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase for 32KB cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Block Erase for 32KB (BE32K) command is not executed if any sector is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

一旦 CS#变为高电平，就会启动 32KB 周期的自定时块擦除(持续时间为 tBE32K)。当 32KB 周期的块擦除正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在 32KB 周期的自定时块擦除期间，正在写入(WIP)位为 1，完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。如果任何扇区受块保护(BP4、BP3、BP2、BP1 和 BP0)位保护，则不执行 32KB 块擦除(BE32K)命令。

Figure 30. Block Erase for 32KB (BE32K) Sequence (SPI Mode)

图 30。32KB (BE32K)序列的块擦除(SPI 模式)

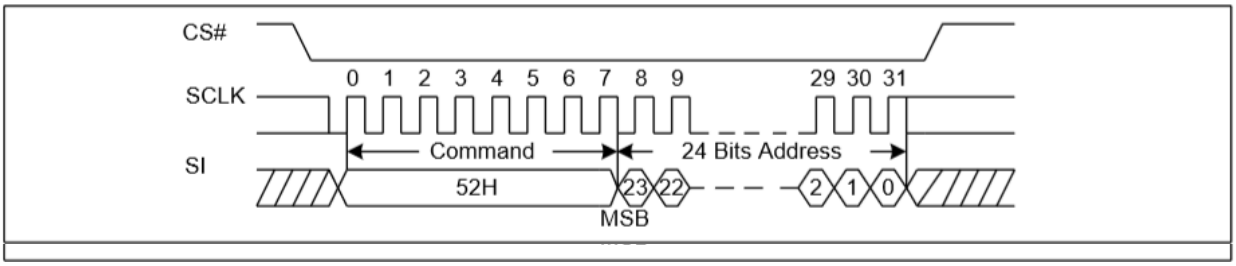
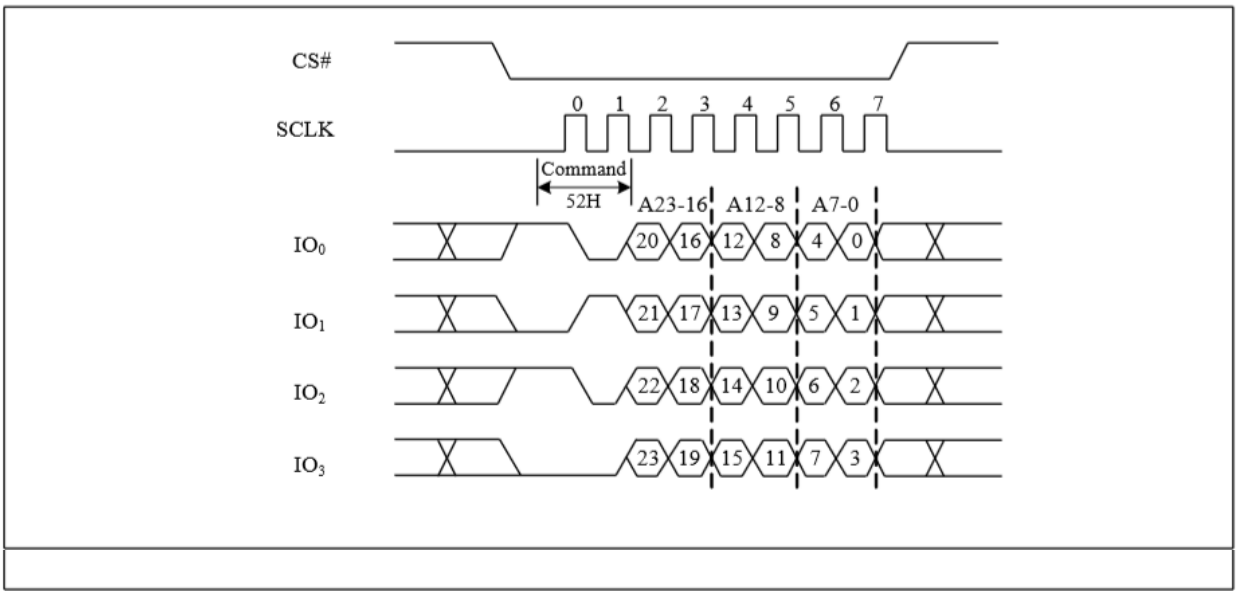


Figure 31. Block Erase for 32KB (BE32K) Sequence (QPI Mode)

图 31。32KB (BE32K)序列的块擦除(QPI 模式)



10.35 Block Erase (BE)
10.36 块擦除

The Block Erase (BE) command is erased the all data of the chosen block. The command is used for 8M-byte block erase operation. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. Any address of the block (Please refer to "5. MEMORY ORGANIZATION") is a valid address for Block Erase (BE) command. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the command will be rejected and not executed.

块擦除(BE)命令擦除所选块的所有数据。该命令用于 8M 字节的块擦除操作。必须先执行写使能(WREN)命令来设置写使能锁存(WEL)位。块的任何地址(请参考"5。存储器组织")是块擦除(BE)命令的有效地址。CS#必须恰好在字节边界处变为高电平(地址字节的最低有效位被锁存)；否则，该命令将被拒绝并且不被执行。

The Block Erase (BE) command sequence: CS# goes low→ sending BE command→ 3-byte address → CS# goes high.

块擦除(BE)命令序列:CS#变为低电平→发送 BE 命令→ 3 字节地址→ CS#变高。

As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Block Erase (BE) command is not executed if any sector is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

一旦 CS#变为高电平，就会启动自定时块擦除周期(持续时间为 tBE)。当块擦除周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时块擦除周期期间，正在写入(WIP)位为 1，完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。如果任何扇区受到块保护(BP4、BP3、BP2、BP1 和 BP0)位的保护，则不会执行块擦除(BE)命令。

Figure 32. Block Erase (BE) Sequence (SPI Mode)

图 32。块擦除(BE)序列(SPI 模式)

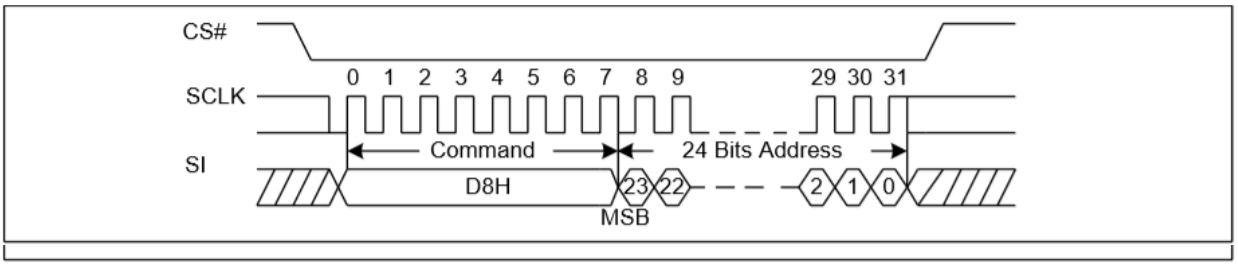
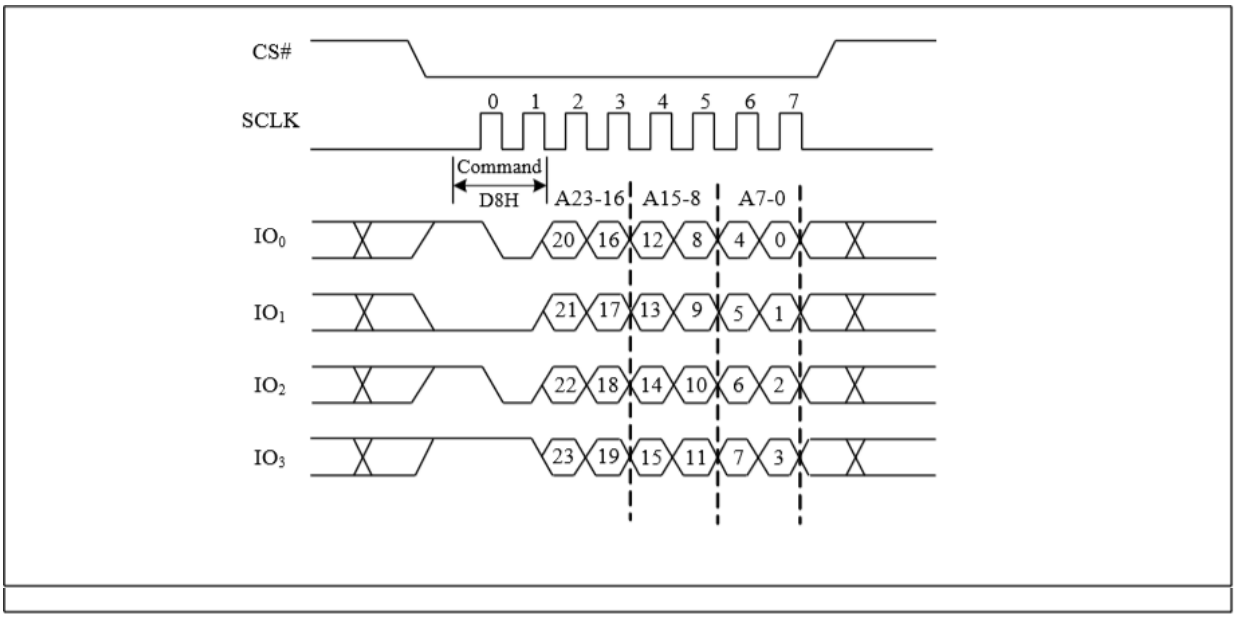


Figure 33. Block Erase (BE) Sequence (QPI Mode)

图 33。块擦除(BE)序列(QPI 模式)



10.37 Chip Erase (CE)
10.38 芯片擦除

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The CS# must go high exactly at the byte boundary, otherwise the command will be rejected and not executed.

芯片擦除(CE)命令擦除芯片的所有数据。必须先执行写使能(WREN)命令来设置写使能锁存(WEL)位。CS#必须恰好在字节边界处变为高电平，否则命令将被拒绝且不执行。

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes

high.

芯片擦除命令序列:CS#变为低电平发送芯片擦除命令 CS#变为高电平。

As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is not executed if any sector is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits. It will be only executed when BP4-BP0 all set to "0".

一旦 CS#变为高电平，便会启动自定时芯片擦除周期(持续时间为 tCE)。当芯片擦除周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时芯片擦除周期期间，写入进行中(WIP)位为 1，完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。如果任何扇区受到块保护(BP4、BP3、BP2、BP1 和 BP0)位的保护，则不会执行芯片擦除(CE)命令。只有当 BP4-BP0 都设置为“0”时，它才会被执行。

Figure 34. Chip Erase (CE) Sequence (SPI Mode)
图 34。芯片擦除(CE)序列(SPI 模式)

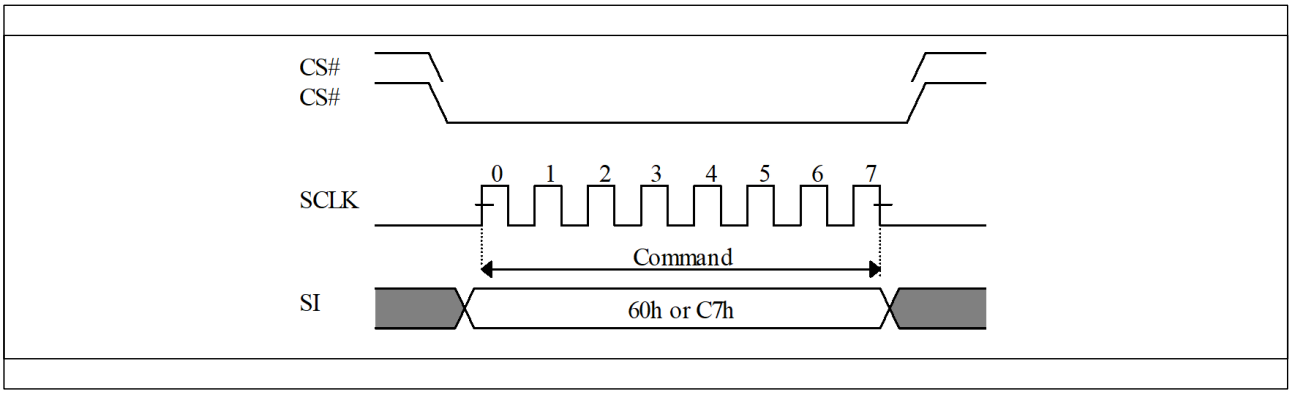
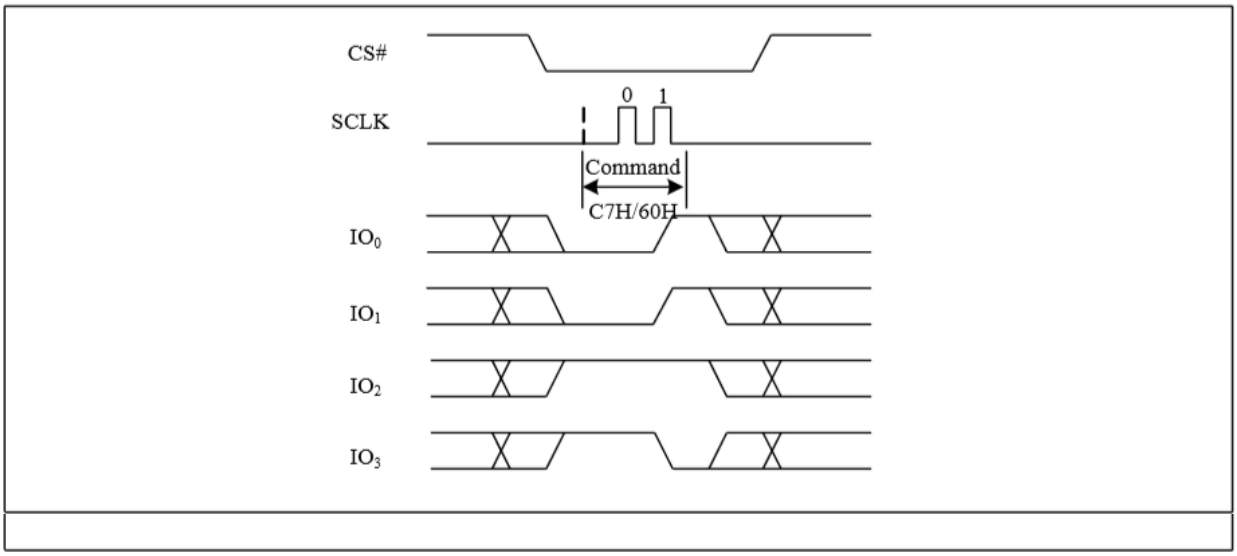


Figure 35. Chip Erase (CE) Sequence (QPI Mode)
图 35。芯片擦除(CE)序列(QPI 模式)



10.39 Deep Power-down (DP)
10.40 深度掉电(DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

深度掉电(DP)指令用于将器件设置为最小功耗(待机电流从 ISB1 降低到 ISB2)。深度掉电模式要求进入深度掉电(DP)指令，在深度掉电模式期间，器件不活动，所有写入/编程/擦除指令都被忽略。当 CS#变为高电平时，它仅处于深度掉电模式，而不是待机模式。和待机模式不一样。

The sequence of issuing DP instruction is: CS# goes low → sending DP instruction code → CS# goes high.

发出 DP 指令的顺序是:CS#变低→发送 DP 指令代码→ CS#变高。

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Device ID (RDI) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

一旦 DP 指令被设置，除了从深度掉电模式(RDP)释放和读取设备 ID (RDI)指令之外，所有指令都将被忽略。(这些指令允许读取 ID)。关断时，深度关断模式自动停止，上电时，器件自动进入待机模式。对于 DP 指令，CS#必须恰好在字节边界变高(指令代码的最后第八位被锁存)；否则，指令不会被执行。一旦片选(CS#)变为高电平，在进入深度掉电模式之前需要一个 tDP 延迟。

Figure 36. Deep Power-down (DP) Sequence (SPI Mode)
图 36。深度掉电(DP)序列(SPI 模式)

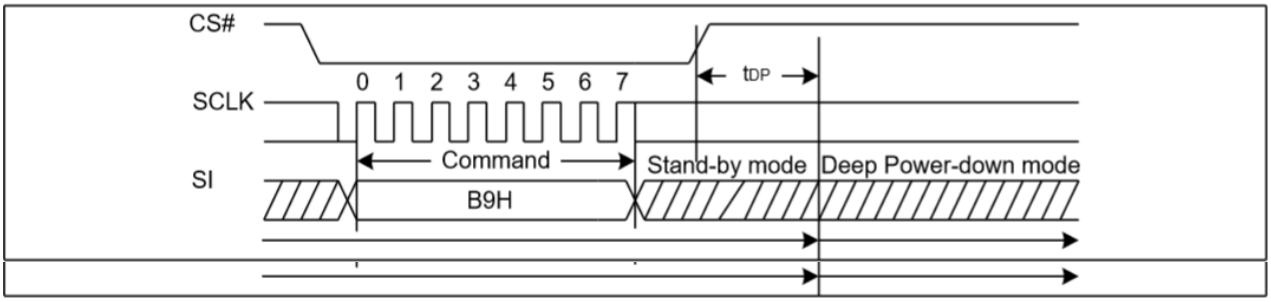
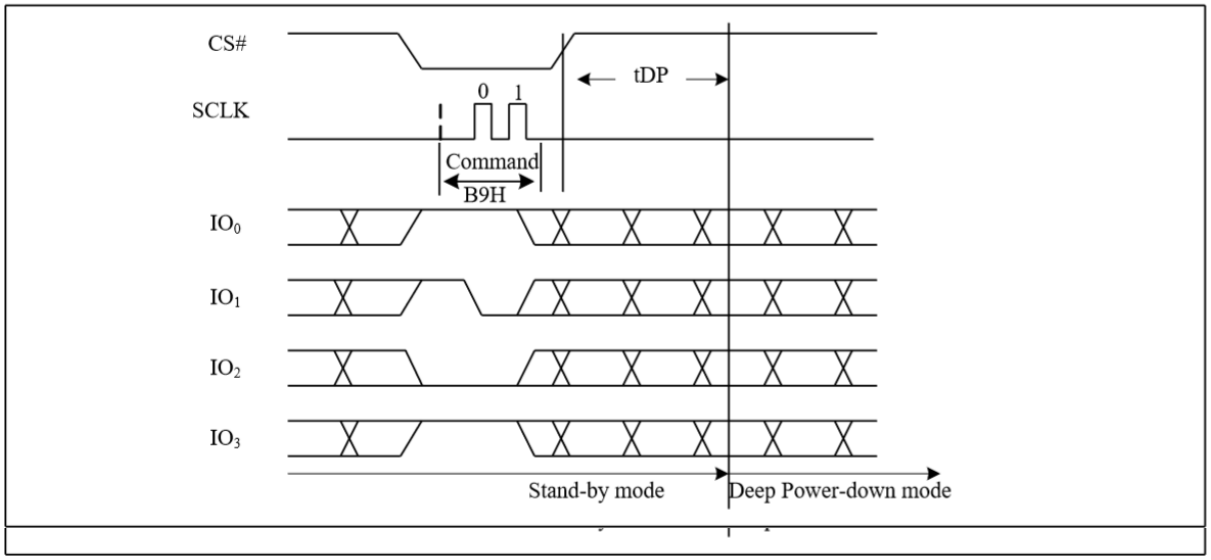


Figure 37. Deep Power-down (DP) Sequence (QPI Mode)
图 37。深度掉电(DP)序列(QPI 模式)



10.41 Release from Deep Power-Down (RDP) and Read Device ID (RDI)
10.42 从深度掉电释放(RDP)并读取设备 ID (RDI)

The Release from Power-Down (RDP) and Read Device ID (RDI) command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

释放掉电(RDP)和读取设备 ID (RDI)命令是一个多用途命令。它可用于解除设备的断电状态或获取设备的电子标识(ID)号。

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure38. Release from

Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

要解除器件的关断状态，可以通过将 CS#引脚拉低、移位指令代码“ABH”并将 CS#拉高来发出命令，如图 38 所示。在器件恢复正常工作并接受其它命令之前，从掉电状态释放将需要 tRES1 的持续时间(见交流特性)。在 tRES1 期间，CS#引脚必须保持高电平。

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure40. The Device ID value for the NM25Q64EVB is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

当仅用于在非关断状态下获取器件 ID 时，该命令通过将 CS#引脚拉低并移位指令代码“ABH ”,后跟 3 个虚拟字节来启动。然后，器件 ID 位在 SCLK 的下降沿移出，最高有效位(MSB)优先，如图 40 所示。制造商和设备标识表中列出了 NM25Q64EVB 的设备 ID 值。可以连续读取设备 ID。该命令通过将 CS#拉高来完成。

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure40, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration

当用于将器件从关断状态释放并获取器件 ID 时，该命令与前面所述相同，如图 40 所示，只是在 CS#被拉高后，它必须在 tRES2 的持续时间内保持高电平(参见交流特性)。在这段时间之后

the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

该设备将恢复正常操作，且其它命令将被接受。如果在擦除、编程或写入周期正在进行时发出从掉电/器件 ID 释放命令(当 WIP 等于 1 时),该命令将被忽略，不会对当前周期产生任何影响。

Figure 38. Release From Power-down (RDP) Sequence (SPI Mode)
图 38。从掉电(RDP)序列中释放(SPI 模式)

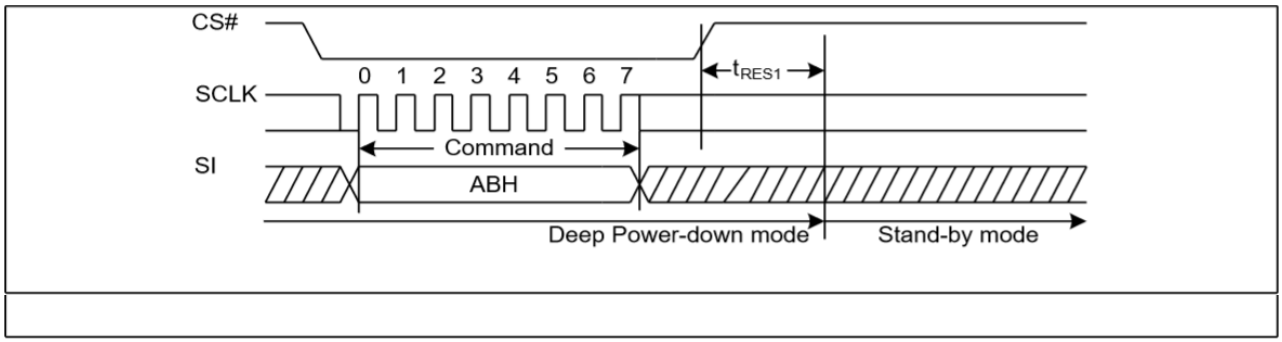


Table 12. ID Definitions for NM25Q64EVB

表 12。NM25Q64EVB 的 ID 定义

Command Type		NM25Q64		
RDID	9FH	Manufacturer ID	Memory Type	Memory Density
		52	22	17
RDI	ABH	Device ID		
		16		
REMS/REMS2/REMS4	90H/92H/94H	Manufacturer ID	Device ID	
		52	16	
命令类型		NM25Q64		
RDID	9FH	制造商 ID	记忆类型	存储密度
		52	22	17
推荐的日摄入量	人身伤害	设备 ID		
		16		
REMS/REMS2/REMS4	90 小时/92 小时/94 小时	制造商 ID	设备 ID	
		52	16	

Figure 39. Release From Deep Power-down (RDP) Sequence (QPI Mode)
图 39。从深度掉电(RDP)序列中释放(QPI 模式)

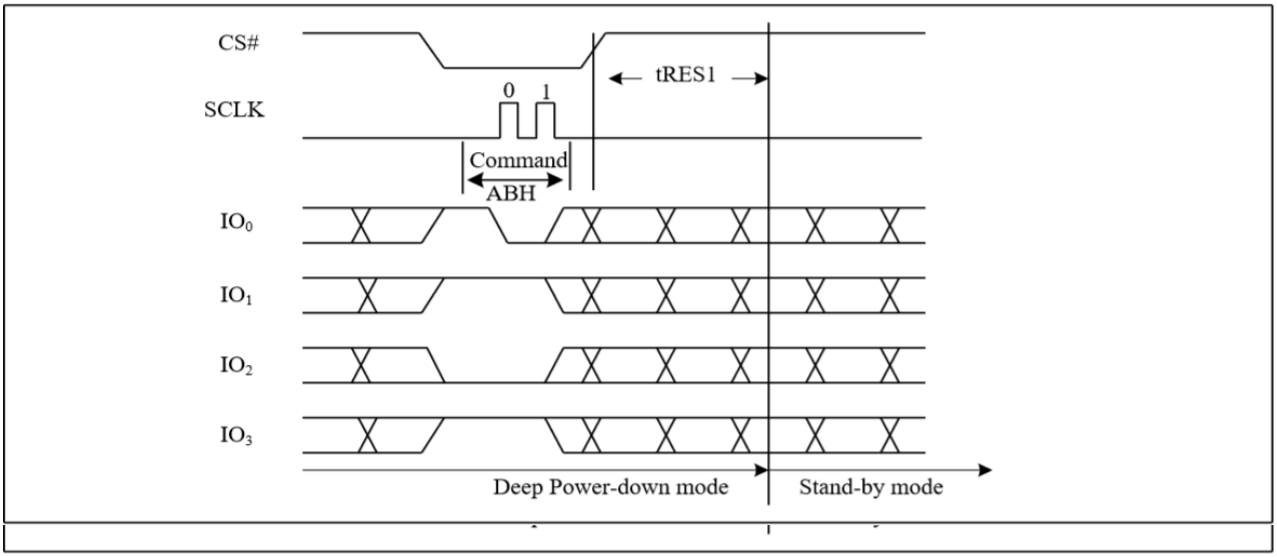

CS#
SCLK
0
1
tRES1
Command
ABH
IO0
IO1
IO2
IO3
Deep Power-down mode
Stand-by mode

Figure 40. Release From Power-down/Read Device ID (RDI) Sequence (SPI Mode)

图 40。释放关断/读取器件 ID (RDI)序列(SPI 模式)

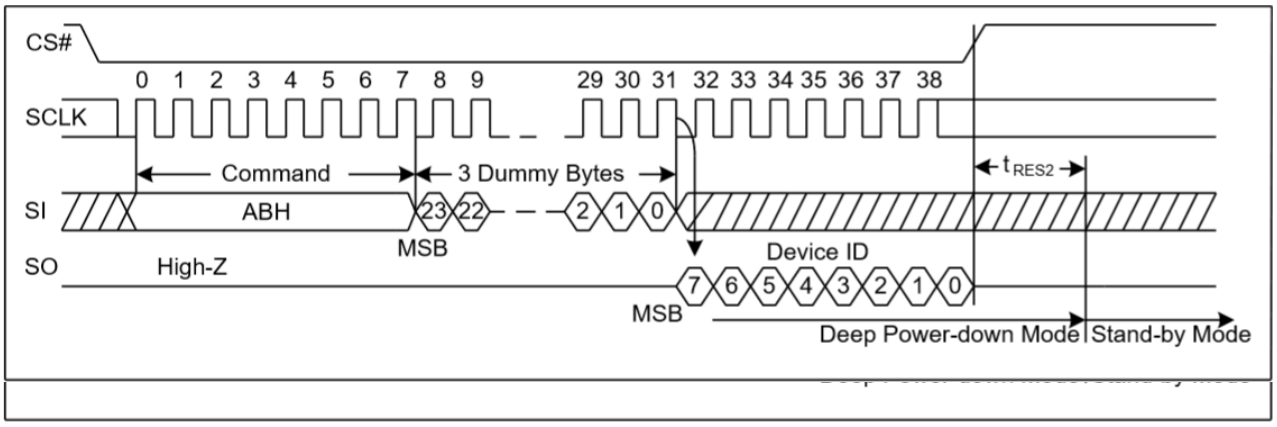
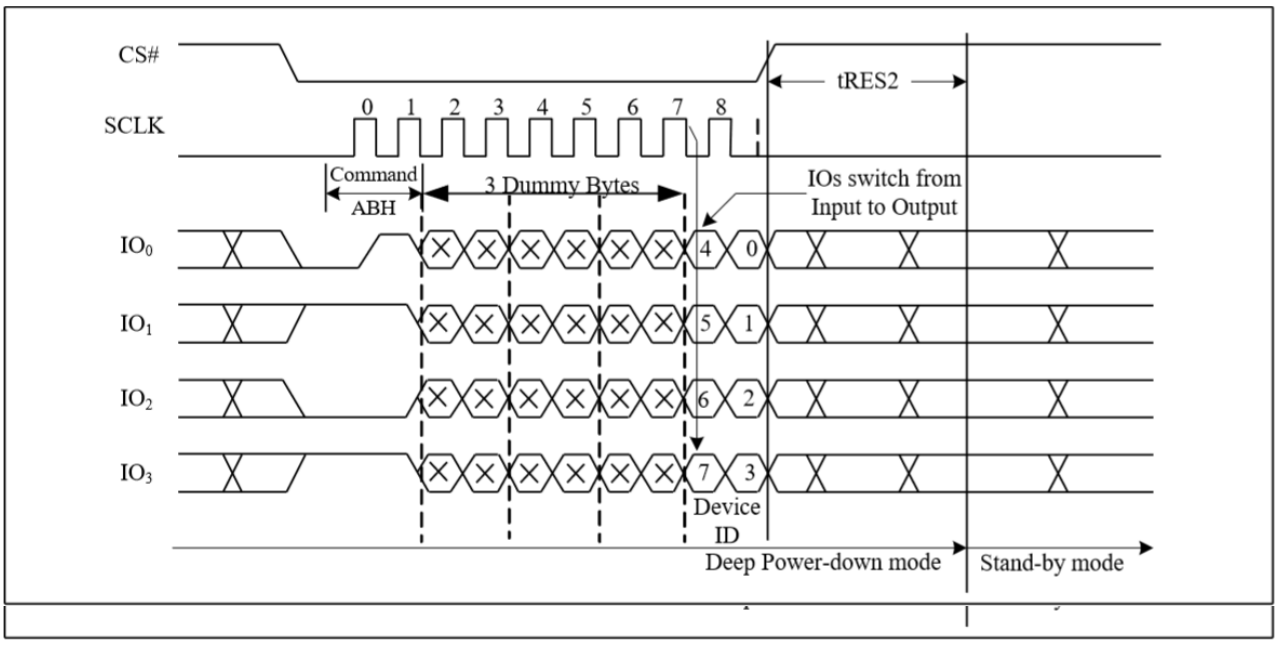


Figure 41. Release From Power-down/Read Device ID (RDI) Sequence (QPI Mode)

图 41。从关断/读取器件 ID (RDI)序列中释放(QPI 模式)



10.43 Read Manufacture ID/ Device ID (REMS)
10.44 读取制造商 ID/设备 ID (REMS)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device

ID.

读取制造商/器件 ID 命令是释放掉电/器件 ID 命令的替代命令，它提供 JEDEC 分配的制造商 ID 和特定器件 ID。

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID (defined in table 12)are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure42. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

该命令通过将 CS#引脚拉低并移位命令代码“90H ”,后跟 000000H 的 24 位地址(A23-A0)来启动。之后，制造商 ID 和设备 ID(在 table 12)在 SCLK 的下降沿移出，最高有效位(MSB)优先，如图 42 所示。如果 24 位地址最初设置为 000001H，将首先读取器件 ID。

Figure 42. Read Manufacture ID/Device ID Sequence (SPI Mode)

图 42。读取制造商 ID/器件 ID 序列(SPI 模式)

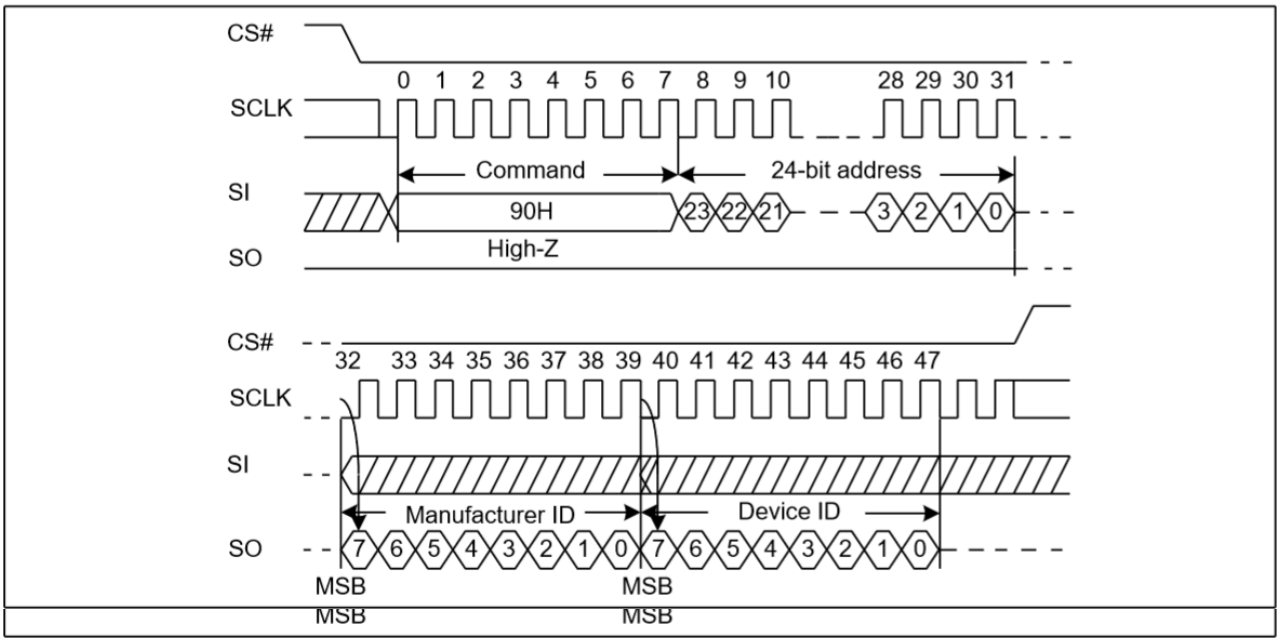
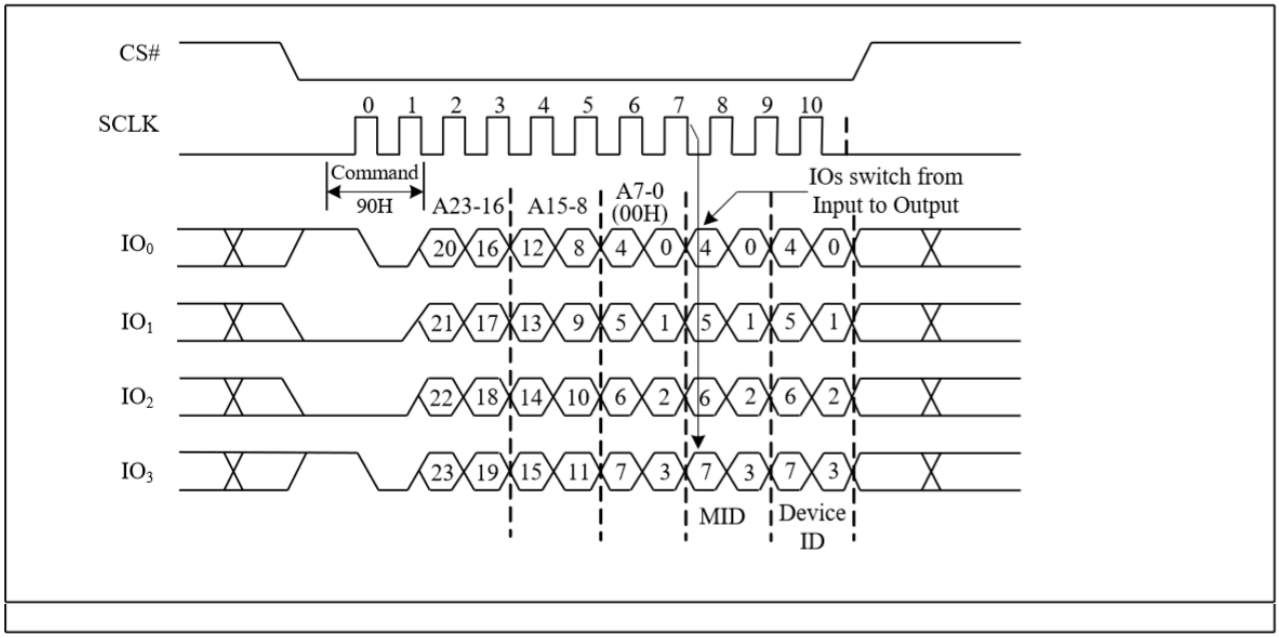


Figure 43. Read Manufacture ID/Device ID Sequence (QPI Mode)

图 43。读取制造商 ID/设备 ID 序列(QPI 模式)



10.45 Read Manufacture ID/ Device ID with Dual I/O (REMS2)

10.46 使用双 I/O 读取制造商 ID/设备 ID(rems 2)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

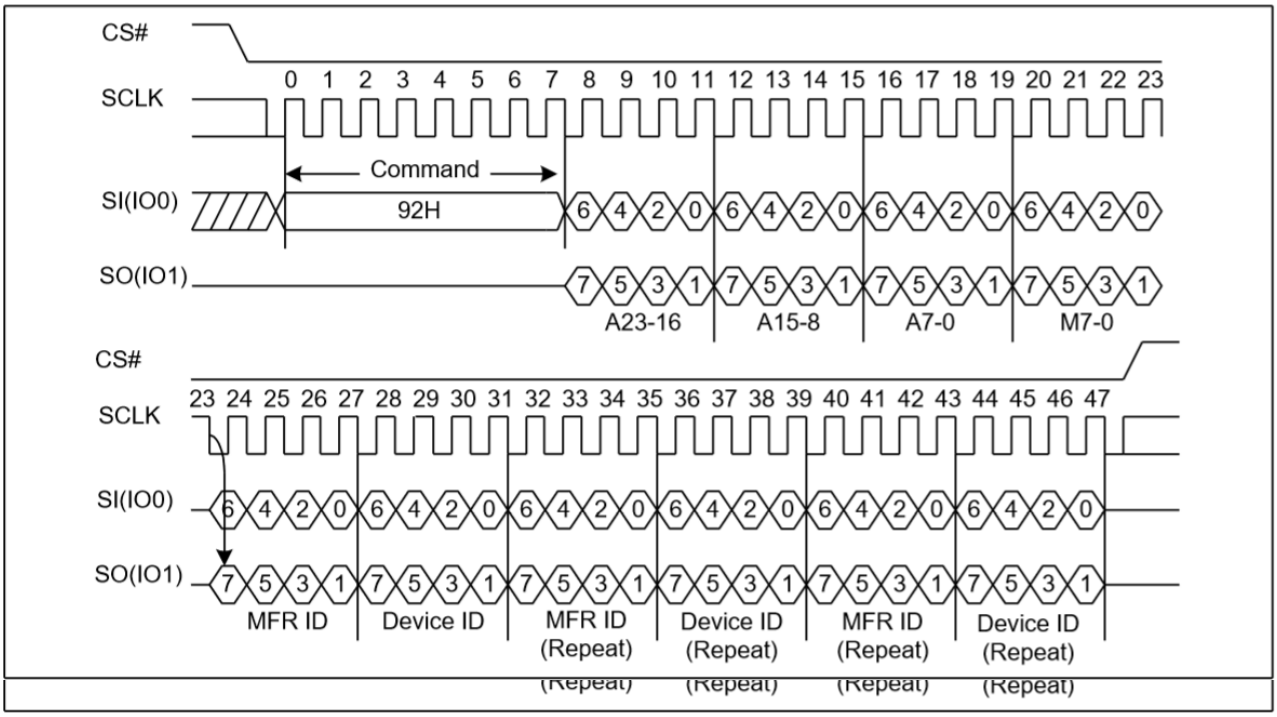
读取制造商/器件 ID 双 I/O 命令是释放掉电/器件 ID 命令的替代命令，它通过双 I/O 提供 JEDEC 分配的制造商 ID 和特定器件 ID。

The command is initiated by driving the CS# pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID (defined in table 12) are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure44. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

该命令通过将 CS#引脚拉低并移位命令代码“92H”后跟随 24 位地址(A23-A0)000000h 来启动。之后，制造商 ID 和设备 ID(在 table 12)在 SCLK 的下降沿移出，最高有效位(MSB)优先，如图 44 所示。如果 24 位地址最初设置为 000001H，将首先读取器件 ID。

Figure 44. Read Manufacture ID/Device ID Sequence with Dual I/O (SPI Mode only)

图 44。利用双 I/O 读取制造商 ID/器件 ID 序列(仅限 SPI 模式)



10.47 Read Manufacture ID/ Device ID with Quad I/O (REMS4)

10.48 使用四通道 I/O (REMS4)读取制造商 ID/设备 ID

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

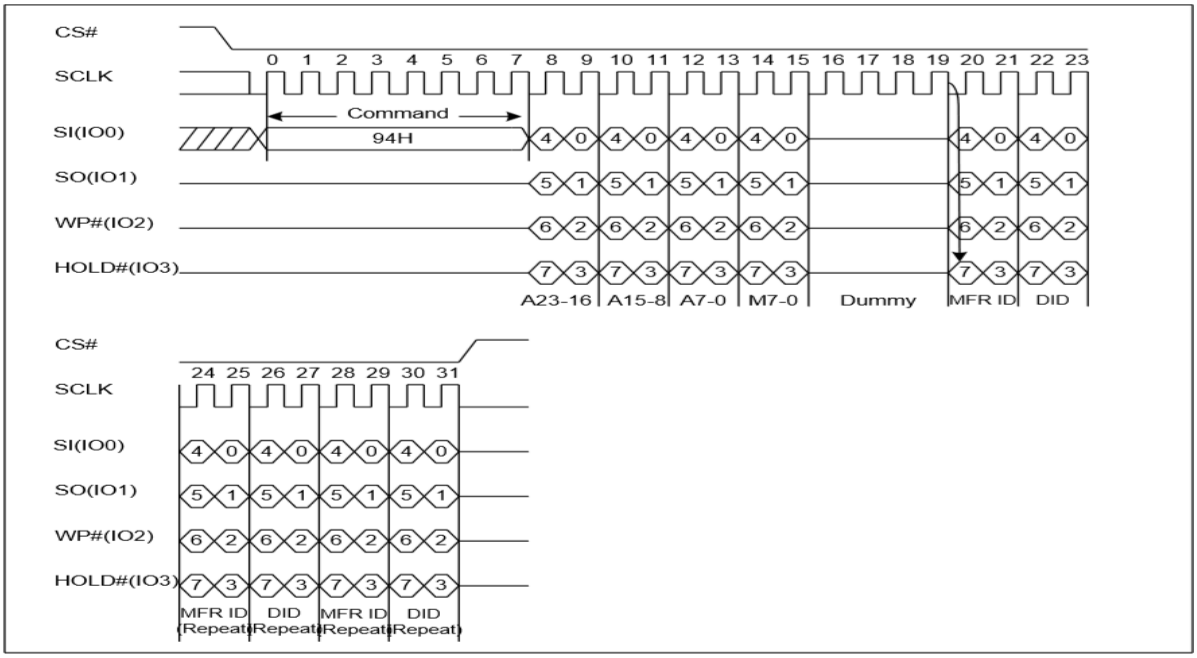
读取制造商/器件 ID 四通道 I/O 命令是释放掉电/器件 ID 命令的替代命令，它通过四通道 I/O 提供 JEDEC 分配的制造商 ID 和特定器件 ID。

The command is initiated by driving the CS# pin low and shifting the command code “94H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID (defined in table 12) are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure45. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

该命令通过将 CS#引脚拉低并移位命令代码“94H”后跟随 24 位地址(A23-A0)000000h 来启动。之后，制造商 ID 和设备 ID(在 table 12)在 SCLK 的下降沿移出，最高有效位(MSB)优先，如图 45 所示。如果 24 位地址最初设置为 000001H，将首先读取器件 ID。

Figure 45. Read Manufacture ID/Device ID with Quad I/O Sequence (SPI Mode only)

图 45。利用四通道 I/O 序列读取制造商 ID/器件 ID(仅限 SPI 模式)



10.49 Read Identification (RDID)

10.50 读取标识(RDID)

The RDID command is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte.

RDID 命令用于读取 1 字节的制造商 ID，后跟 2 字节的设备 ID。

The Read Identification (RDID) command sequence: CS# goes low→ sending RDID command→24-bits ID data out on SO (defined in table 12) → to end RDID operation can drive CS# to high at any time during data out.

读取识别(RDID)命令序列:CS#变为低电平→发送 RDID 命令→SO 上的 24 位 ID 数据输出(定义见 table 12)→要结束 RDID 操作，可在数据输出期间随时将 CS#驱动至高电平。

While Program/Erase operation is in progress, it will not decode the RDID command, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

当编程/擦除操作正在进行时，它不会解码 RDID 命令，因此对当前正在进行的编程/擦除操作的周期没有影响。当 CS#变为高电平时，器件处于待机状态。

Figure 46. Read Identification (RDID) Sequence (SPI mode)
图 46。读取识别(RDID)序列(SPI 模式)

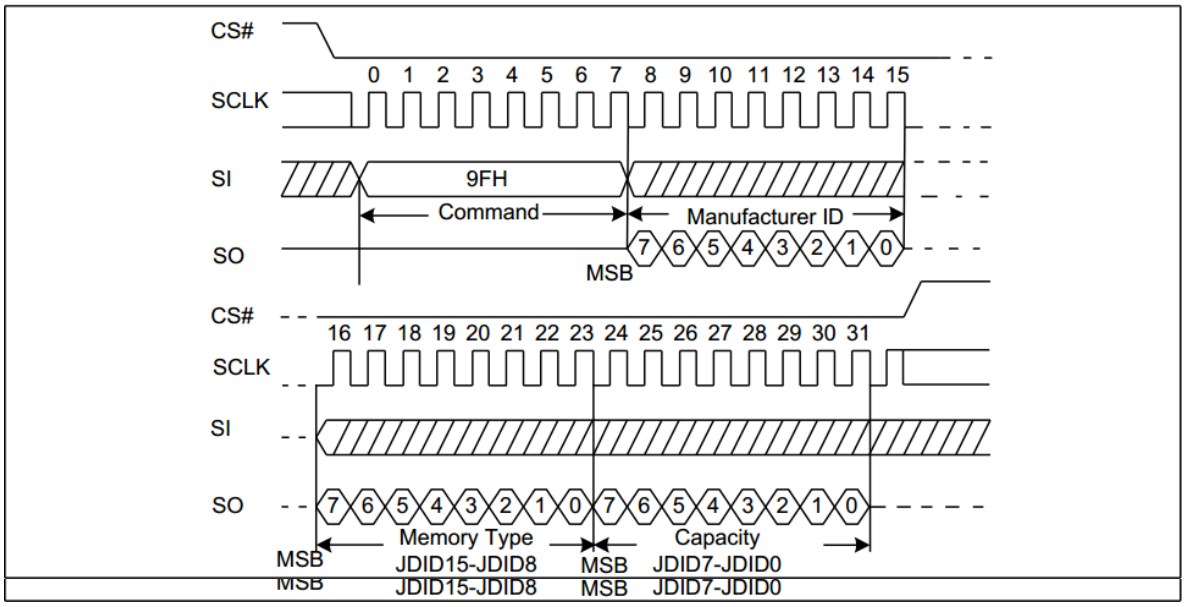
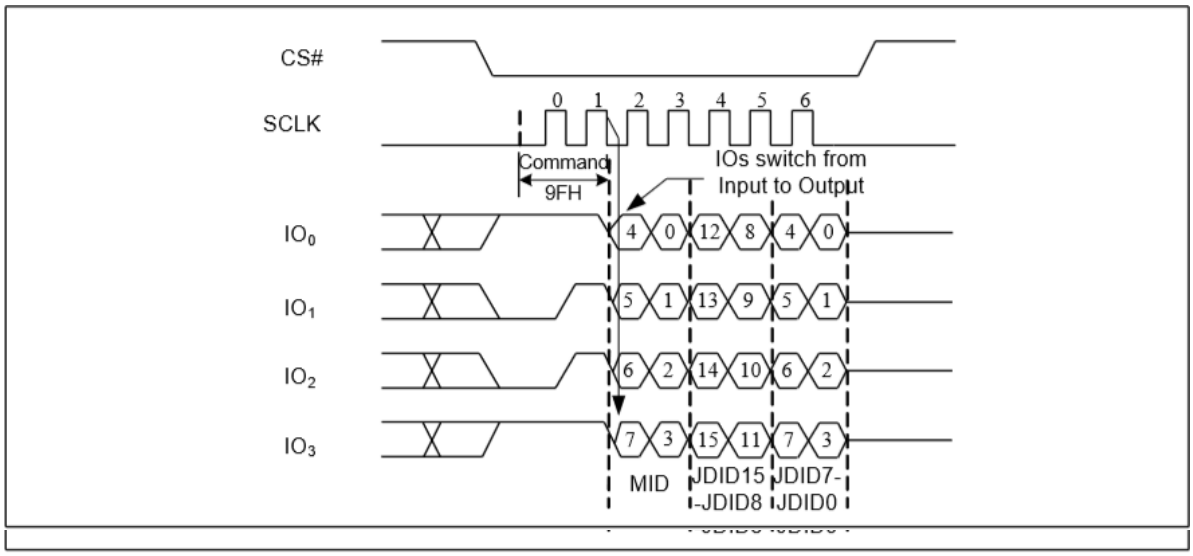

CS#
SCLK
SI
SO
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
9FH
Command
Manufacturer ID
7 6 5 4 3 2 1 0
MSB
CS#
SCLK
SI
SO
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
Memory Type
Capacity
MSB
JDID15-JDID8
MSB
JDID7-JDID0
MSB
JDID15-JDID8
MSB
JDID7-JDID0

Figure 47. Read Identification (RDID) Sequence (QPI Mode)

图 47。读取识别(RDID)序列(QPI 模式)



10.51 Program/Erase Suspend (Suspend)
10.52 编程/擦除暂停(暂停)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H/31H/11H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H / 32H) are not allowed during Program/Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

编程/擦除暂停命令“75H”允许系统中断页面编程或扇区/块擦除操作，然后从任何其他扇区或块读取数据。在编程/擦除暂停期间，不允许写状态寄存器命令(01H/31H/11H)和擦除/编程安全寄存器命令(44H、42H)和擦除命令(20H、52H、D8H、C7H、60H)和页面编程命令(02H / 32H)。编程/擦除暂停仅在页面编程或扇区/块擦除操作期间有效。暂停编程/擦除操作最长需要“tsus”时间(见交流特性)。

The Program/Erase Suspend command will be accepted by the device only if the ESB/PSB bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the ESB/PSB bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the ESB/PSB bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show in Figure48.

只有在页面编程或扇区或块擦除操作正在进行时，状态寄存器中的 ESB/PSB 位等于 0 且 WIP 位等于 1，设备才会接受编程/擦除挂起命令。如果 ESB/PSB 位等于 1 或 WIP 位等于 0，设备将忽略挂起命令。在“tsus”内，WIP 位将从 1 清除到 0，并且在编程/擦除暂停后，ESB/PSB 位将立即从 0 设置到 1。挂起期间的断电将重置设备并解除挂起状态。命令序列如图 48 所示。

Figure 48. Program/Erase Suspend Sequence (SPI Mode)
图 48。编程/擦除挂起序列(SPI 模式)

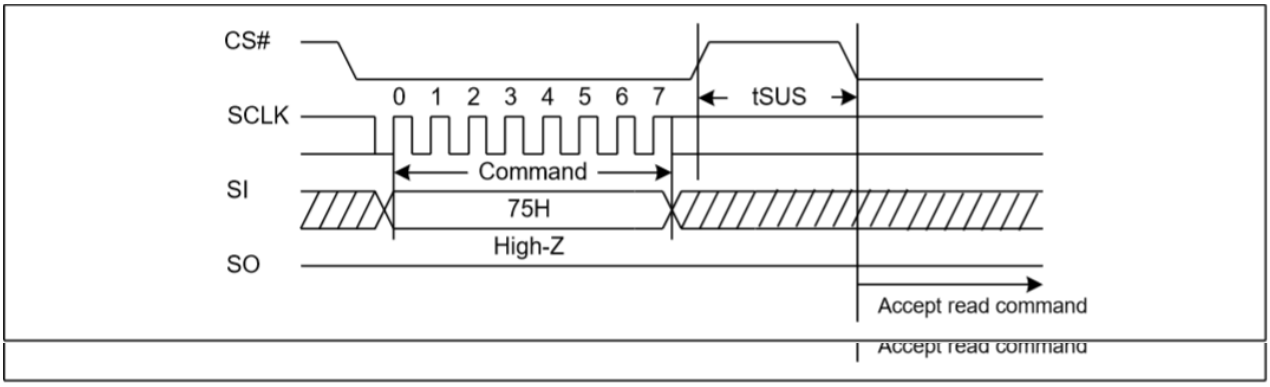
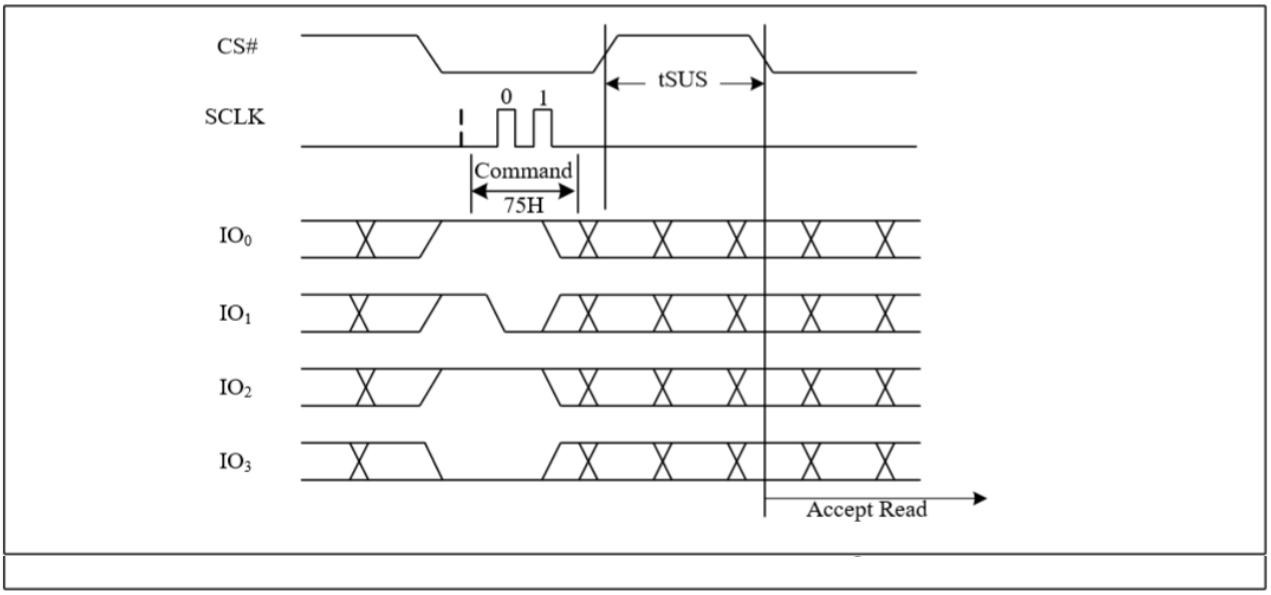


Figure 49. Program/Erase Suspend Sequence (QPI Mode)

图 49。编程/擦除暂停序列(QPI 模式)



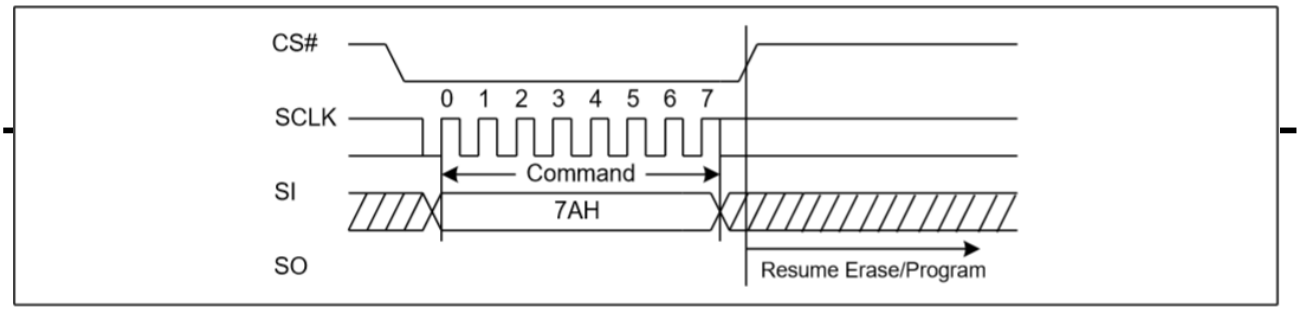
10.53 Program/Erase Resume (Resume)
10.54 编程/擦除恢复(恢复)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the ESB/PSB bit equal to 1 and the WIP bit equal to 0. After issued the ESB/PSB bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show in Figure50.

在编程/擦除暂停命令之后，必须写入编程/擦除恢复命令以恢复编程或扇区/块擦除操作。只有当 ESB/PSB 位等于 1 且 WIP 位等于 0 时，设备才会接受编程/擦除恢复命令。发出后，状态寄存器中的 ESB/PSB 位将立即从 1 清除到 0，WIP 位将在 200ns 内从 0 设置到 1，并且扇区或块将完成擦除操作，或者页面将完成编程操作。除非编程/擦除暂停被激活，否则编程/擦除恢复命令将被忽略。命令序列如图 50 所示。

Figure 50. Program/Erase Resume Sequence (SPI Mode)

图 50。编程/擦除恢复序列(SPI 模式)



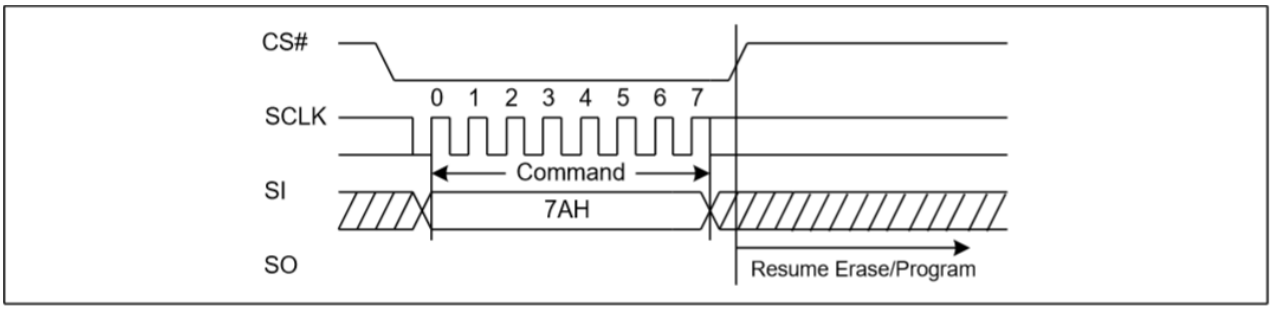
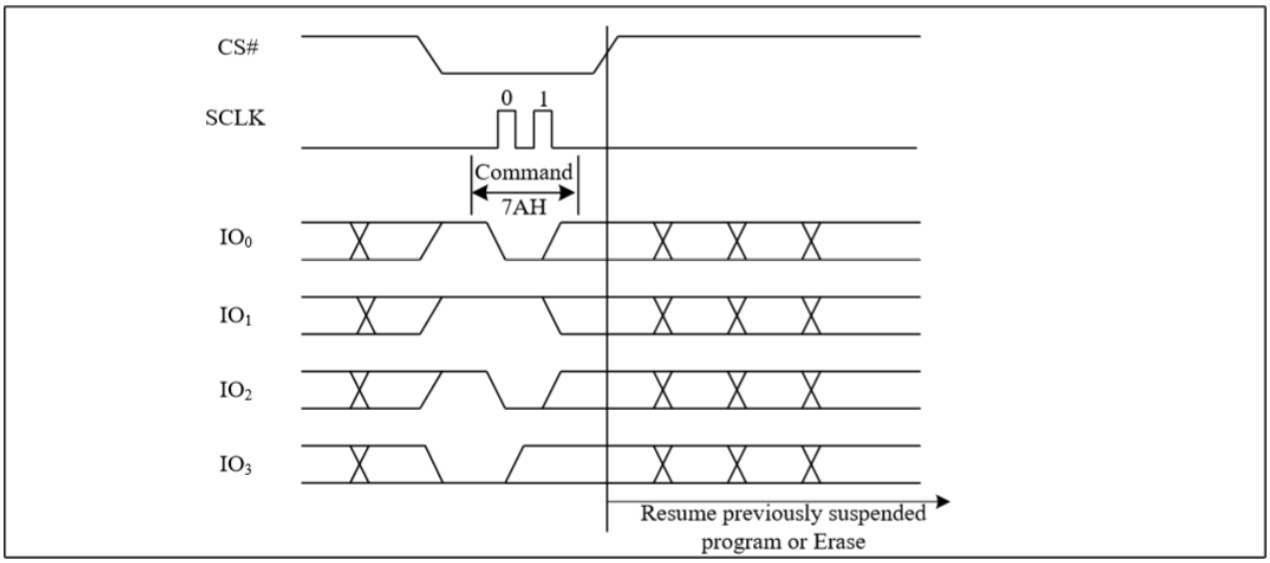


Figure 51. Program/Erase Resume Sequence (SPI Mode)
图 51。编程/擦除恢复序列(SPI 模式)



10.55 Erase Security Registers (ERSECR)

10.56 擦除安全寄存器(ERSECR)

The NM25Q64EVB provides two 1K-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

NM25Q64EVB 提供两个 1K 字节的安全寄存器，可以单独擦除和编程。系统制造商可以使用这些寄存器来存储独立于主存储器阵列的安全和其他重要信息。

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

擦除安全寄存器命令类似于扇区/块擦除命令。必须先执行写使能(WREN)命令来设置写使能锁存(WEL)位。

The Erase Security Registers command sequence: CS# goes low→ sending Erase Security Registers command→ CS# goes high.

擦除安全寄存器命令序列:CS#变为低电平→发送擦除安全寄存器命令→ CS#变为高电平。

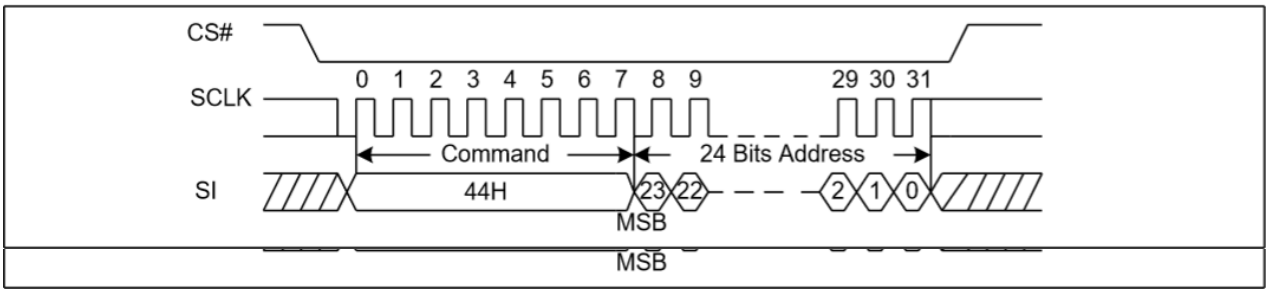
The command sequence is shown in Figure52. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB2-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security

Registers command will be ignored. Security registers region refer to “Table 6. Secured Register Definition”.

命令序列如图 52 所示。命令代码的第八位锁存后，CS#必须变为高电平；否则，不执行擦除安全寄存器命令。一旦 CS#变为高电平，自定时擦除安全寄存器周期(持续时间为 tSE)就会启动。当擦除安全寄存器周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时擦除安全寄存器周期期间，正在写入(WIP)位为 1，完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。状态寄存器中的安全寄存器锁定位(LB2-1)可用于 OTP 保护安全寄存器。一旦 LB 位被设置为 1，安全寄存器将被永久锁定；擦除安全寄存器命令将被忽略。安全寄存器区域请参考"Table 6. 安全寄存器定义”。

Figure 52. Erase Security Registers Sequence (SPI mode only)

图 52。擦除安全寄存器序列(仅限 SPI 模式)



10.57 Program Security Registers (PGSECR)
10.58 程序安全寄存器(PGSECR)

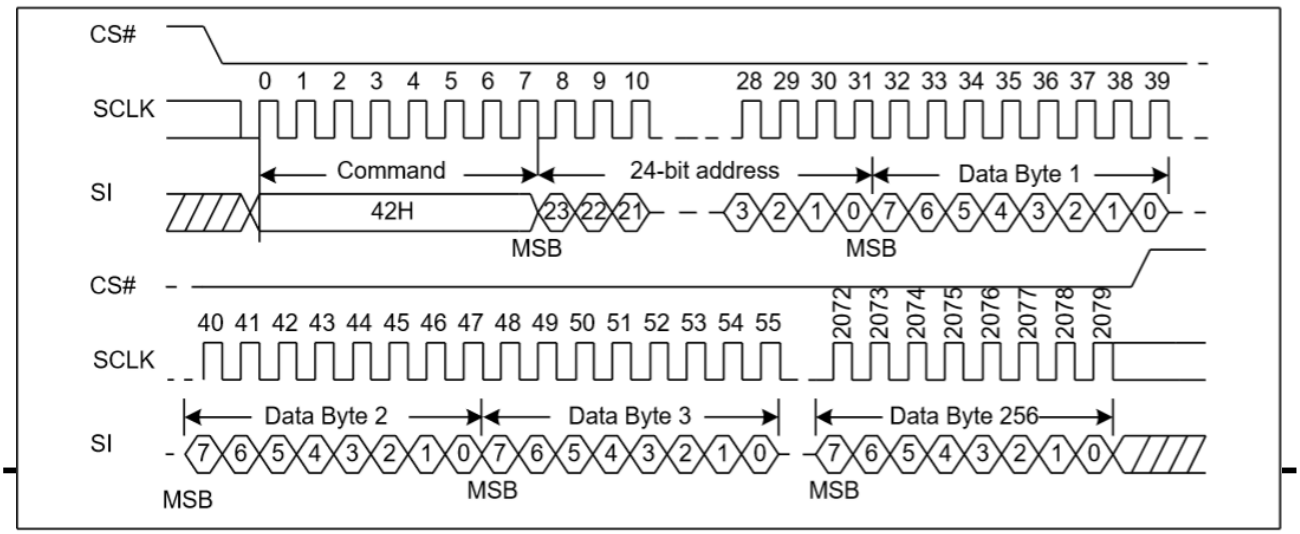
The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1K bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command.

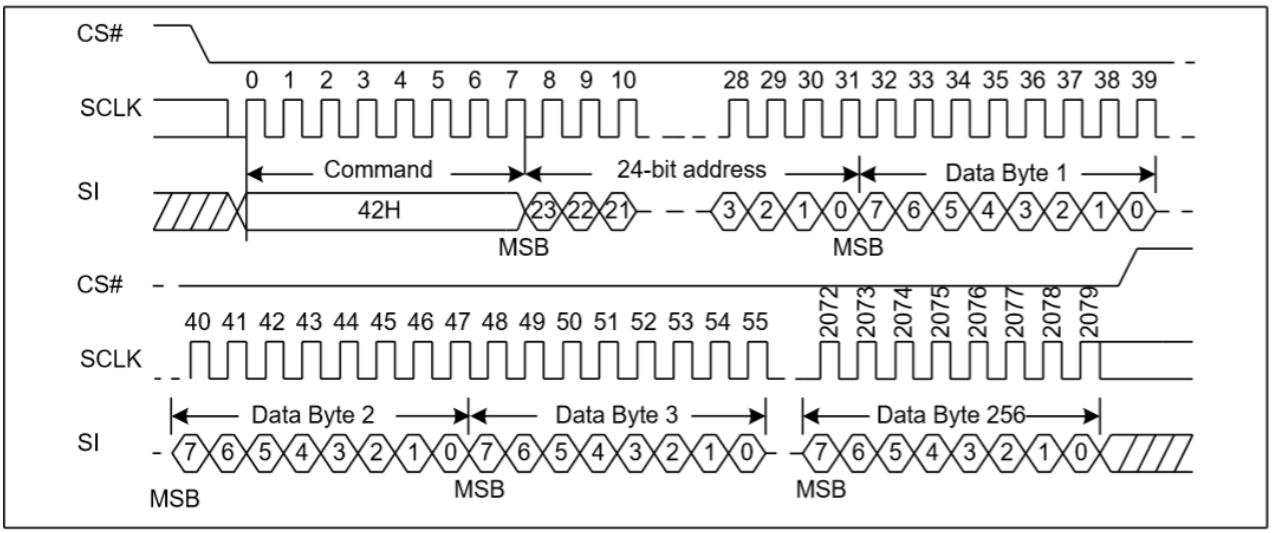
“程序安全性寄存器”命令类似于“页面程序”命令。它允许对 1 至 1K 字节的安全寄存器数据进行编程。在发送程序安全寄存器命令之前，必须先执行写使能(WREN)命令，以设置写使能锁存(WEL)位。

The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. If the Security Registers Lock Bit (LB2-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

将 CS#拉低，输入程序安全寄存器命令，然后输入命令代码(42H)、三个地址字节和 SI 上的至少一个数据字节。一旦 CS#变为高电平，自定时程序安全寄存器周期(持续时间为 tPP)就会启动。当程序安全寄存器周期正在进行时，可以读取状态寄存器来检查正在写入(WIP)位的值。在自定时程序安全寄存器周期期间，正在写入(WIP)位为 1，完成时为 0。在周期完成之前的某个未指定时间，写使能锁存(WEL)位被复位。如果安全寄存器锁定位(LB2-1)设为 1，安全寄存器将被永久锁定。程序安全寄存器命令将被忽略。

Figure 53. Program Security Registers Sequence (SPI mode only)
图 53。程序安全寄存器序列(仅限 SPI 模式)



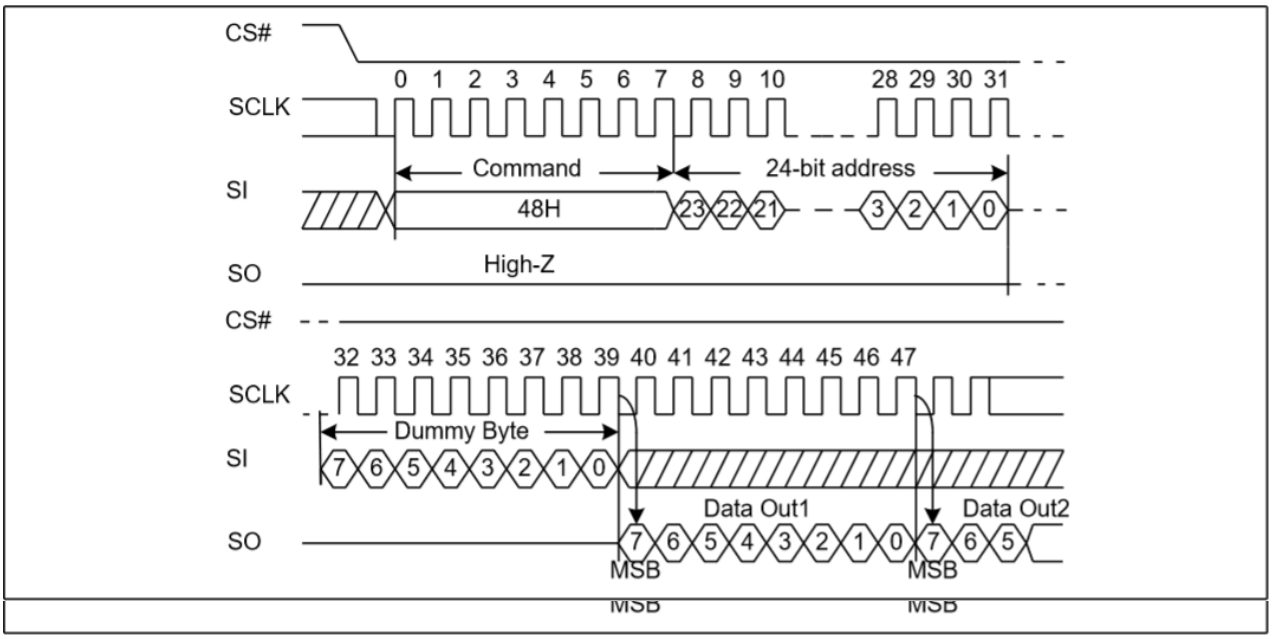


10.59 Read Security Registers (RDSECR)
10.60 读取安全寄存器(RDSECR)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

读取安全寄存器命令类似于快速读取命令。该命令后跟一个 3 字节的地址(A23-A0)和一个虚拟字节，每个位在 SCLK 的上升沿被锁存。然后，在 SCLK 的下降沿期间，以最大频率 fC 将该地址的存储器内容移出 s0，每个比特被移出。寻址的第一个字节可以在任何位置。每移出一个字节的数据后，地址会自动递增到下一个更高的地址。一旦 A9-A0 地址到达寄存器的最后一个字节(字节 3FFH)，它将复位至 000H，通过将 CS#拉高来完成命令。

Figure 54. Read Security Registers Sequence (SPI mode only)
图 54。读取安全寄存器序列(仅限 SPI 模式)



10.61 Individual Block/Sector Lock (SBLK)
10.62 独立块/扇区锁(SBLK)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP[4:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

单独的块/扇区锁提供了保护存储器阵列免受不利擦除/编程的替代方式。为了使用单独的块/扇区锁，状态寄存器-2 中的 WPS 位必须置 1。如果 WPS=0，写保护将由状态寄存器中的 CMP、BP[4:0]位决定。各个块/扇区锁定位是易失性位。器件加电或复位后的默认值为 1，因此整个存储器阵列受到保护。

To lock a specific block or sector as illustrated in Figure 55, an Individual Block/Sector Lock instruction must be issued by driving CS# low, shifting the instruction code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

如图 55 所示，要锁定特定模块或扇区，必须通过将 CS#拉低，在 CLK 的上升沿将指令代码“36h”移入数据输入(DI)引脚，后跟一个 24 位地址，然后将 CS#拉高，来发出单独的模块/扇区锁定指令。

Figure 55. Individual Block/Sector Lock Sequence (SPI mode)
图 55。单个块/扇区锁定序列(SPI 模式)

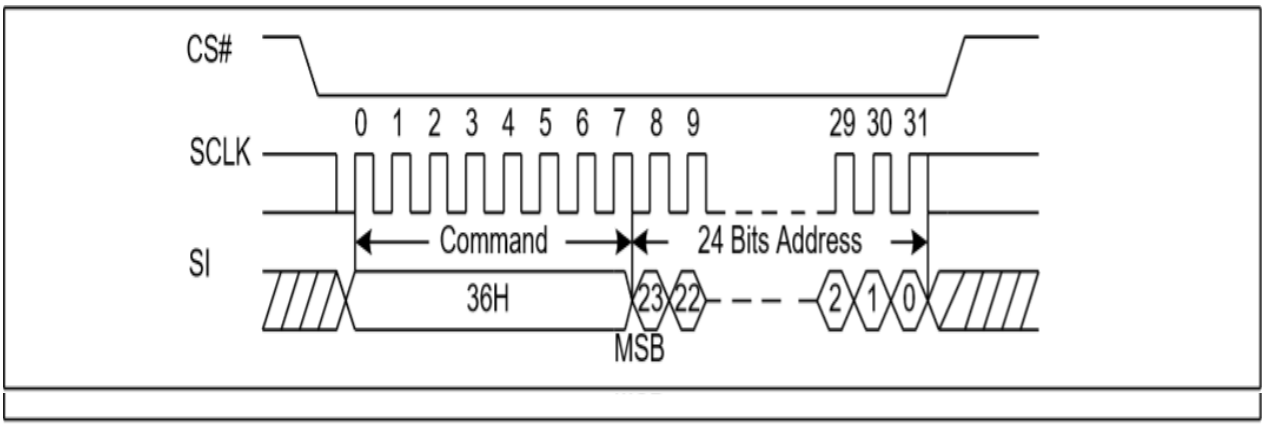
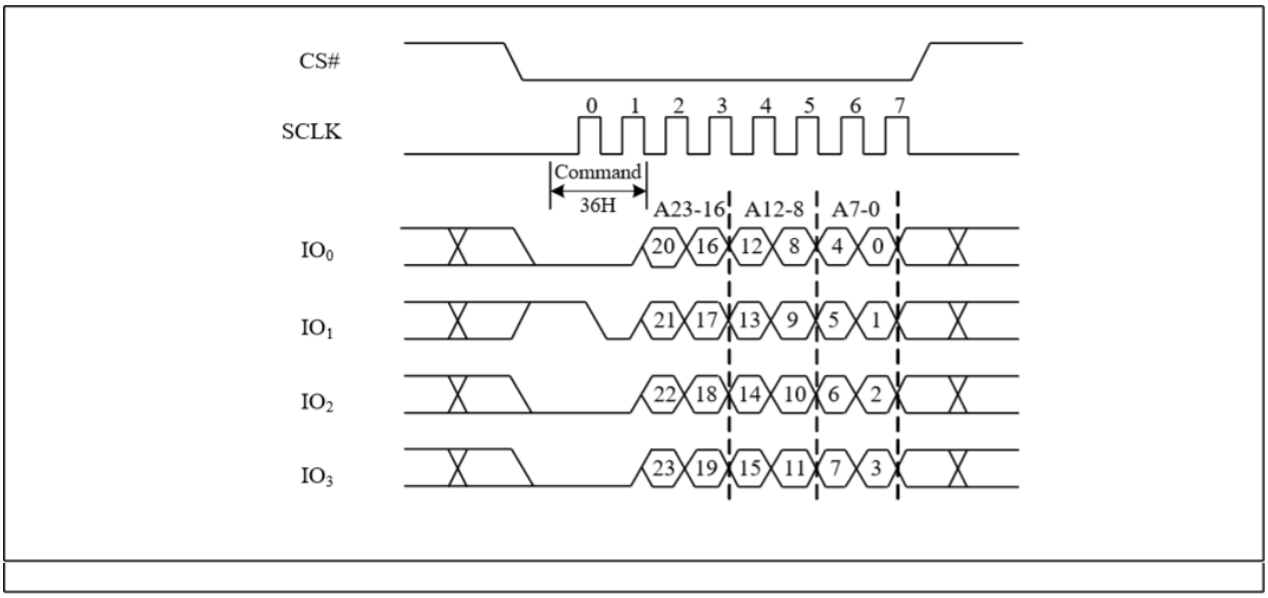

CS#
SCLK
SI
0 1 2 3 4 5 6 7 8 9
29 30 31
Command
24 Bits Address
36H
23 22
2 1 0
MSB

Figure 56. Individual Block/Sector Lock Sequence (QPI mode)
图 56。单个块/扇区锁定序列(QPI 模式)



10.63 Individual Block/Sector Unlock (SBULK)
10.64 独立块/扇区解锁(SBULK)

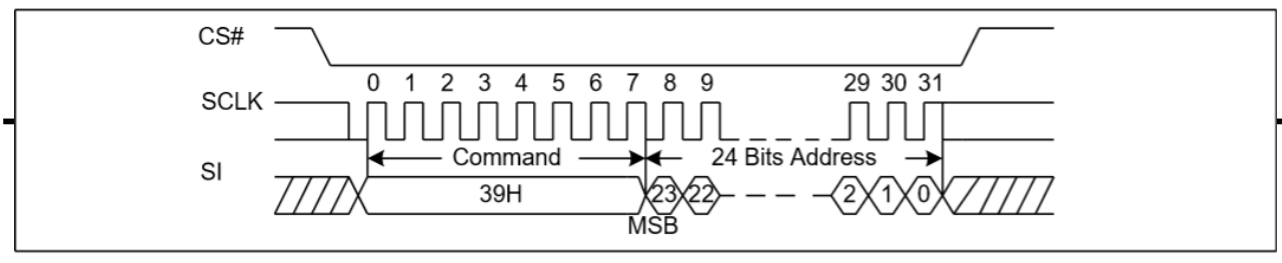
The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP[4:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

单独的块/扇区锁提供了保护存储器阵列免受不利擦除/编程的替代方式。为了使用单独的块/扇区锁，状态寄存器-2 中的 WPS 位必须置 1。如果 WPS=0，写保护将由状态寄存器中的 CMP、BP[4:0]位决定。各个块/扇区锁定位是易失性位。器件加电或复位后的默认值为 1，因此整个存储器阵列受到保护。

To unlock a specific block or sector as illustrated in Figure 57, an Individual Block/Sector Unlock instruction must be issued by driving CS# low, shifting the instruction code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

要解锁图 57 所示的特定模块或扇区，必须通过将 CS#拉低，在 CLK 的上升沿将指令代码“39h”移入数据输入(DI)引脚，后跟一个 24 位地址，然后将 CS#拉高，来发出单独的模块/扇区解锁指令。

Figure 57. Individual Block/Sector Unlock Sequence (SPI mode)
图 57。单个块/扇区解锁序列(SPI 模式)



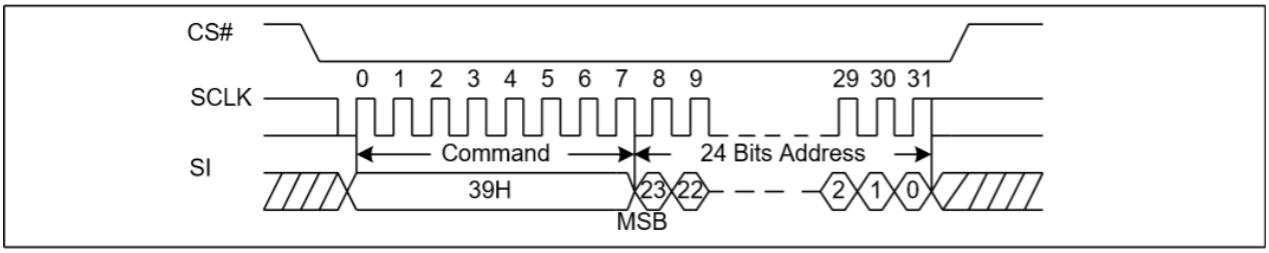
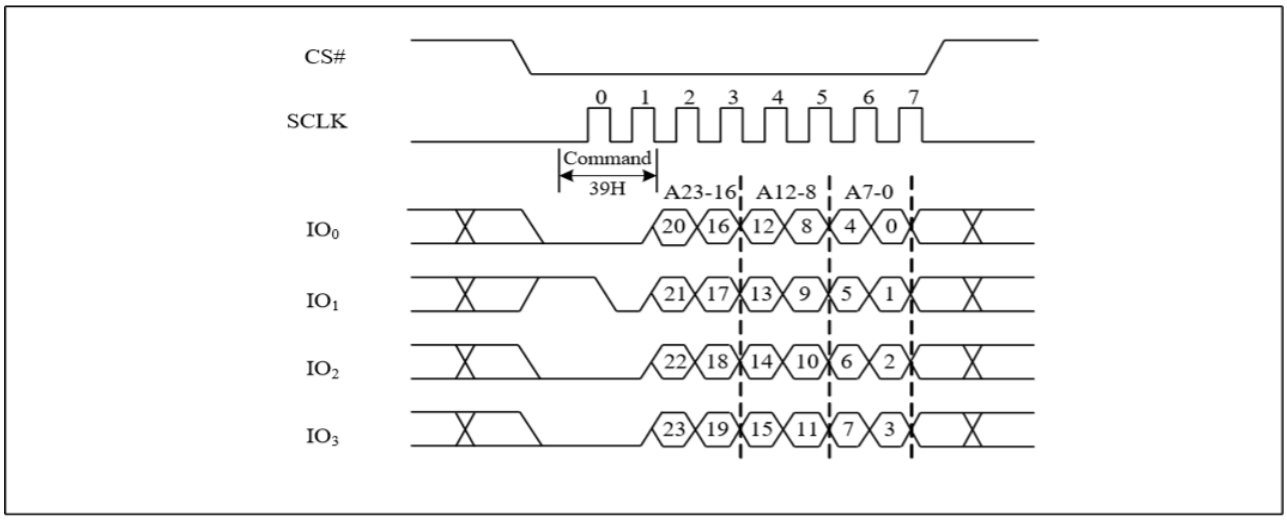


Figure 58. Individual Block/Sector Unlock Sequence (QPI mode)

图 58。单个块/扇区解锁序列(QPI 模式)



10.65 Read Block/Sector Lock (RDBLK)

10.66 读取块/扇区锁(RDBLK)

The Individual Block/Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-2 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP[4:0] bits in the Status Registers. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

单独的块/扇区锁提供了保护存储器阵列免受不利擦除/编程的替代方式。为了使用单独的块/扇区锁，状态寄存器-2 中的 WPS 位必须置 1。如果 WPS=0，写保护将由状态寄存器中的 CMP、BP[4:0]位决定。各个块/扇区锁定位是易失性位。器件加电或复位后的默认值为 1，因此整个存储器阵列受到保护。

To read out the lock bit value of a specific block or sector as illustrated in Figure 59, a Read Block/Sector Lock instruction must be issued by driving CS# low, shifting the instruction code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address. The Block/Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. If the least significant bit (LSB) is 1, the corresponding block/sector is locked; if LSB=0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

要读取特定模块或扇区的锁定位值，如图 59 所示，必须通过拉低 CS#来发出读取模块/扇区锁定指令，在 CLK 的上升沿将指令代码“3Dh”移入数据输入(DI)引脚，后跟一个 24 位地址。块/扇区锁定位值将在 CLK 的下降沿通过 DO 引脚移出，最高有效位(MSB)优先。如果最低有效位(LSB)为 1，则相应的块/扇区被锁定；如果 LSB=0，则相应的块/扇区解锁，可以执行擦除/编程操作。

Figure 59. Read Block/Sector Lock Sequence (SPI mode)
图 59。读取块/扇区锁定序列(SPI 模式)

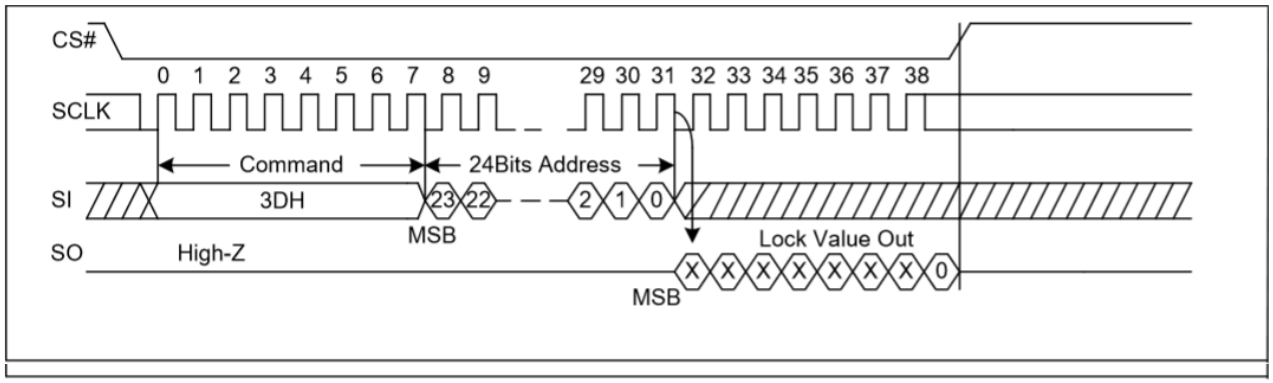
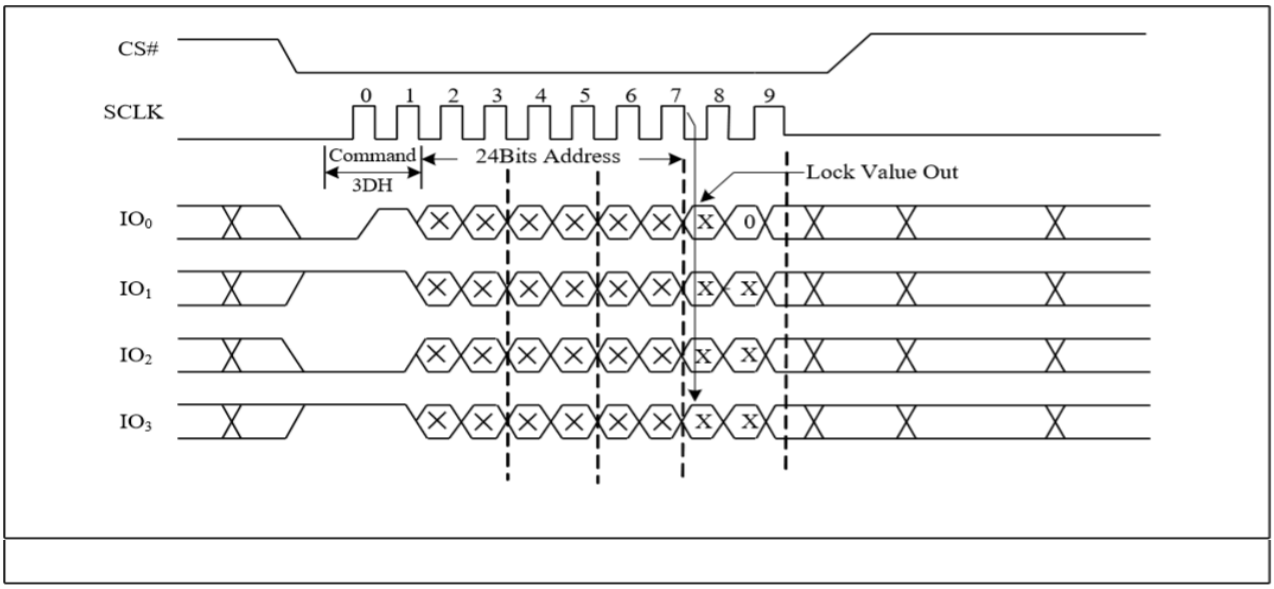

CS#
SCLK
SI
SO
0 1 2 3 4 5 6 7 8 9
29 30 31 32 33 34 35 36 37 38
Command
24Bits Address
3DH
23 22
2 1 0
MSB
High-Z
Lock Value Out
X X X X X X X 0
MSB

Figure 60. Read Block/Sector Lock Sequence (QPI mode)

图 60。读取块/扇区锁定序列(QPI 模式)



10.67 Global Block/Sector Lock (GBLK)

10.68 全局块/扇区锁(GBLK)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock instruction. The instruction must be issued by driving CS# low, shifting the instruction code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

全局块/扇区锁定指令可以将所有块/扇区锁定位设置为 1。必须通过将 CS#拉低，在 CLK 的上升沿将指令代码“7Eh”移入数据输入(DI)引脚，然后将 CS#拉高来发出指令。

Figure 61. Global Block Lock Sequence (SPI Mode)

图 61。全局块锁定序列(SPI 模式)

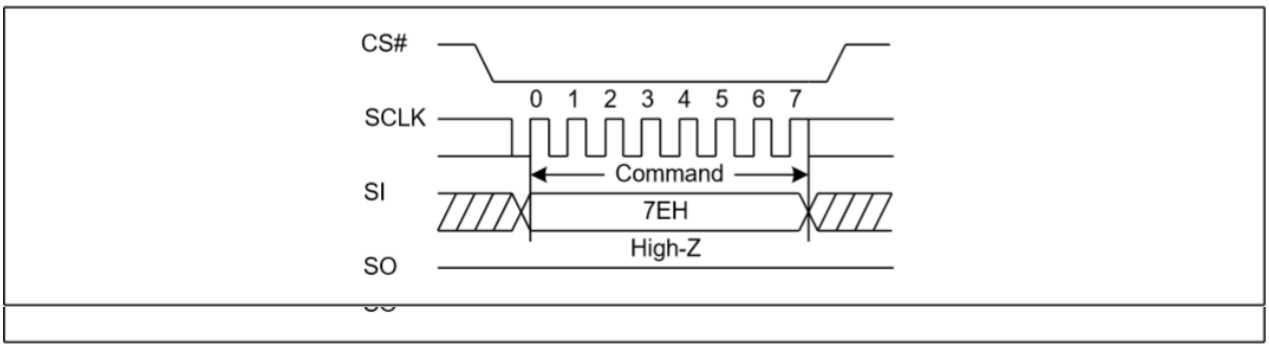
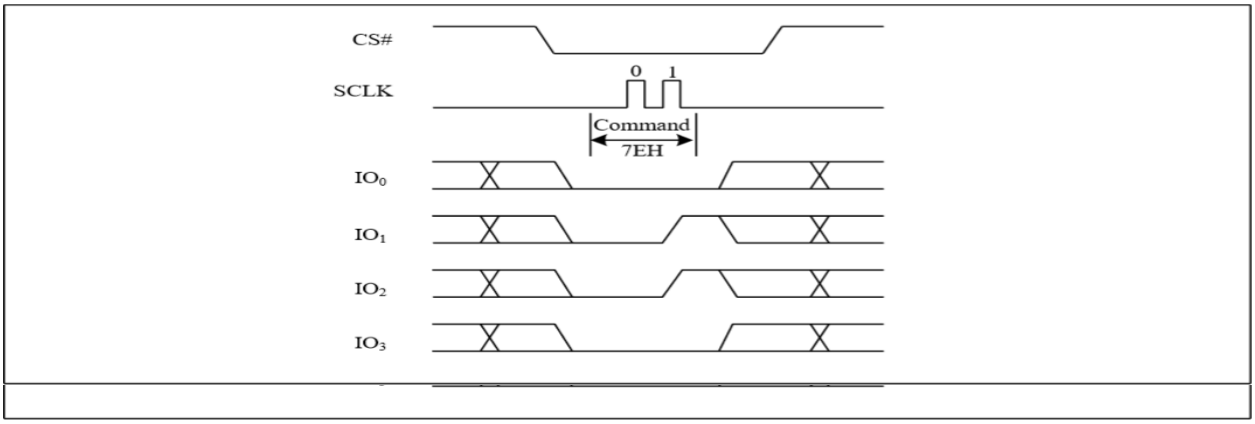


Figure 62. Global Block Lock Sequence (QPI Mode)
图 62。全局块锁定序列(QPI 模式)



10.69 Global Block/Sector Unlock (GBULK)

10.70 全局块/扇区解锁(GBULK)

All Block/Sector Lock bits can be set to 0 by the Global Block/Sector Unlock instruction. The instruction must be issued by driving CS# low, shifting the instruction code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

全局块/扇区解锁指令可以将所有块/扇区锁定位设置为 0。必须通过将 CS#拉低，在 CLK 的上升沿将指令代码“98h”移入数据输入(DI)引脚，然后将 CS#拉高来发出指令。

Figure 63. Global Block Unlock Sequence (SPI Mode)
图 63。全局模块解锁序列(SPI 模式)

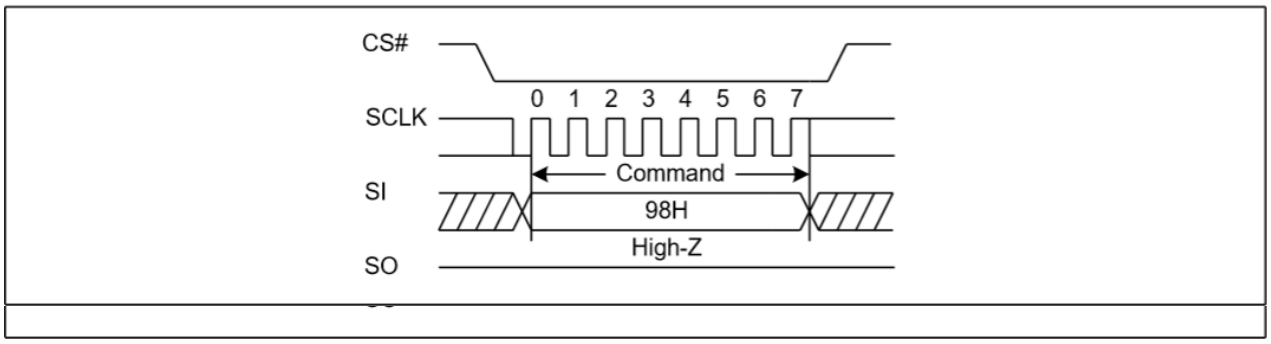
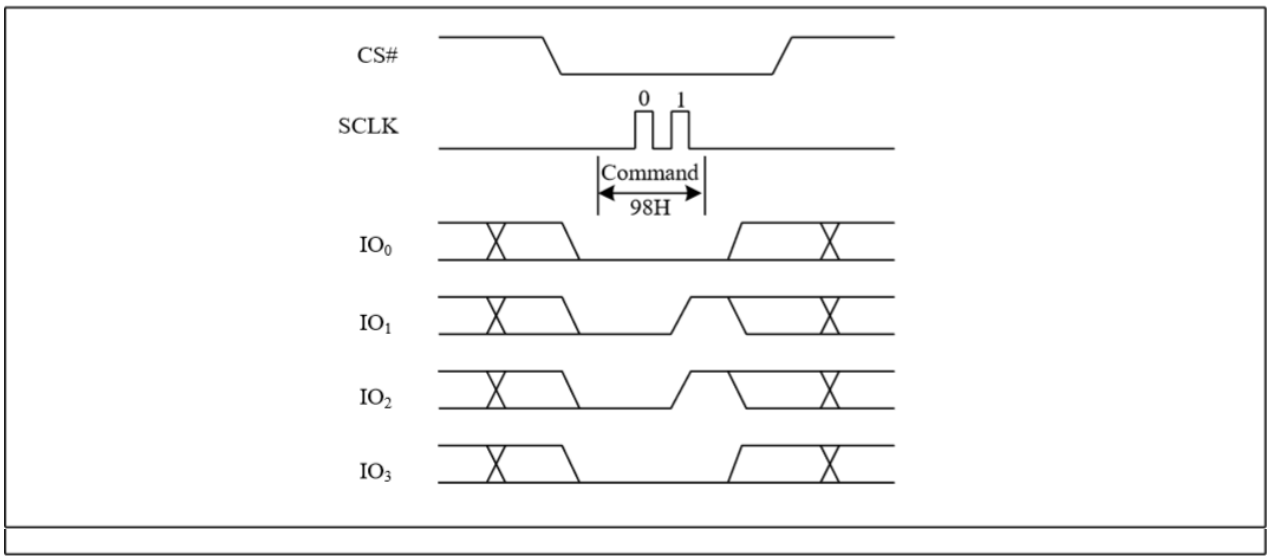


Figure 64. Global Block Unlock Sequence (QPI Mode)

图 64。全局块解锁序列(QPI 模式)



10.71 Set Read Parameter (SET_PARAM)
10.72 设置读取参数(SET_PARAM)

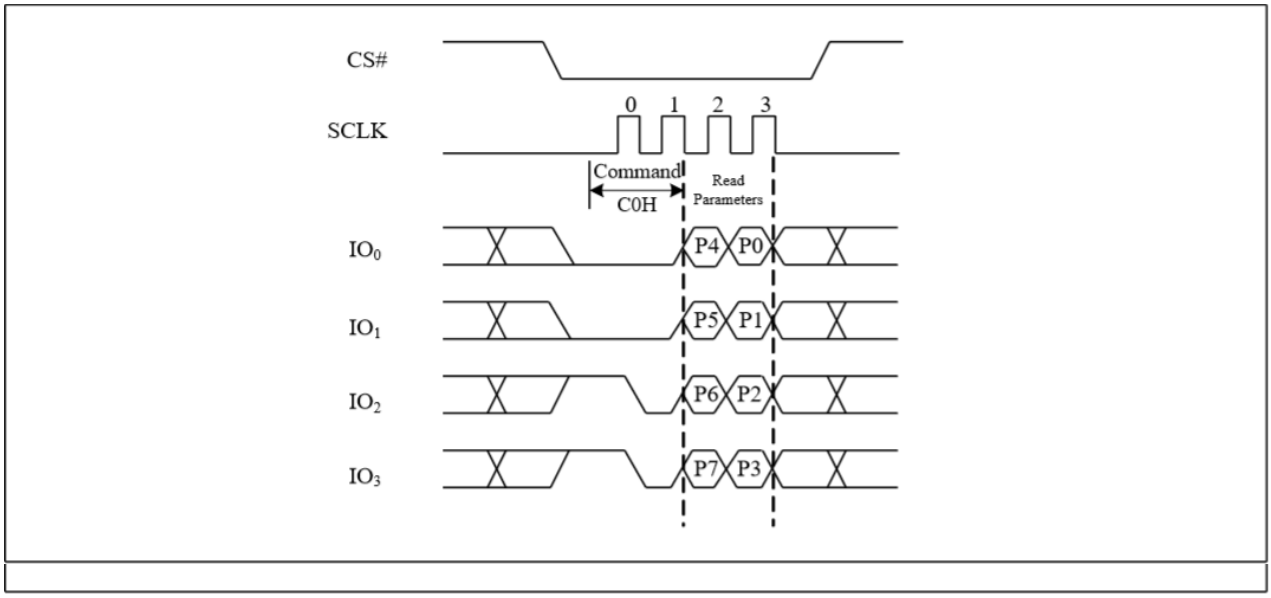
In QPI mode the “Set Read Parameters (C0H)” command can be used to configure the number of dummy clocks for “Fast Read (0BH)”, “Quad I/O Fast Read (EBH)” and “Burst Read with Wrap (0CH)” command, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0CH)” command. In standard SPI mode, the “Wrap Length” is set by W5-6 bit in the “Set Burst with Wrap (77H)” command. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

在 QPI 模式下，“设置读取参数(C0H)”命令可用于配置“快速读取(0BH)”、“四通道 I/O 快速读取(EBH)”和“带回绕的突发读取(0CH)”命令的虚拟时钟数，以及配置“带回绕的突发读取(0CH)”命令的“回绕长度”的字节数。在标准 SPI 模式下，“换行长度”由“设置带换行的突发(77H)”命令中的 W5 6 位设置。当器件从标准 SPI 模式切换到 QPI 模式时，该设置将保持不变。

P5, P4	Dummy Cycle	Max. Read Freq.	P1, P0	Wrap Length
0, 0	4	60MHz	0, 0	8-byte
0, 1	6	80MHz	0, 1	16-byte
1, 0	8	104MHz	1, 0	32-byte
1, 1	8	104MHz	1, 1	64-byte
P5，P4	虚拟循环	最大值阅读频率。	P1，P0	包装长度
0，0	四	60 兆赫	0，0	8 字节
0，1	6	80 兆赫	0，1	16 字节
1，0	8	104 兆赫	1，0	32 字节
1，1	8	104 兆赫	1，1	64 字节

Figure 65. Set Read Parameter Sequence (QPI mode only)

图 65。设置读取参数序列(仅 QPI 模式)

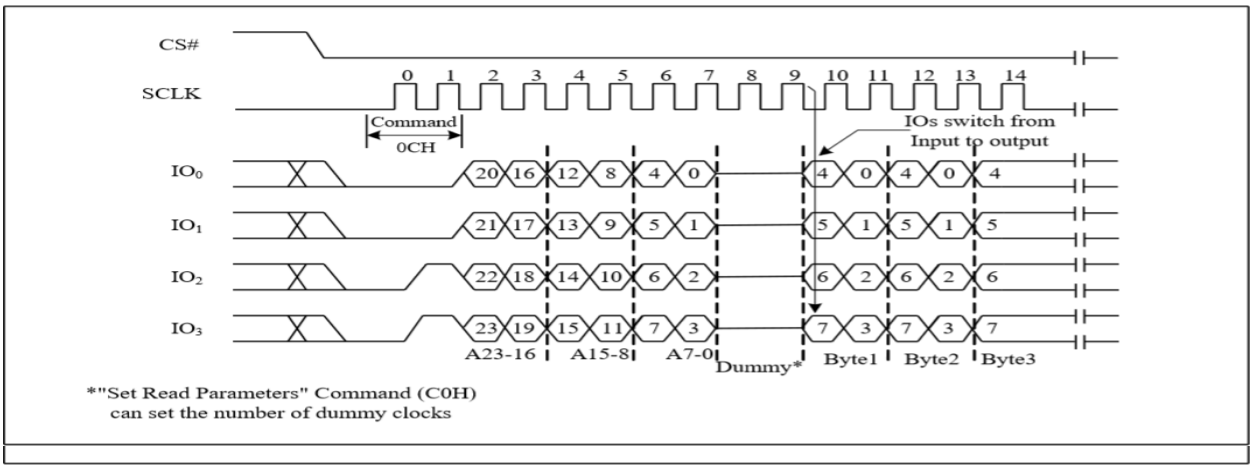


10.73 Quad I/O Burst Read with Wrap (4READ_BST)
10.74 带回绕的四路 I/O 突发读取(4READ_BST)

The Quad I/O Burst Read command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

四通道 I/O 突发读命令提供了一种在 QPI 模式下使用“回绕”执行读操作的替代方法。该命令类似于 QPI 模式中的“快速读取(0BH)”命令，除了一旦到达结束边界，读取操作的寻址将“回绕”到“回绕”的开始边界。“回绕长度”和虚拟时钟的数量可通过“设置读取参数(C0H)”命令进行配置。

Figure 66. Quad I/O Burst Read with Wrap Sequence (QPI mode only)
图 66。带回绕序列的四路 I/O 突发读取(仅限 QPI 模式)

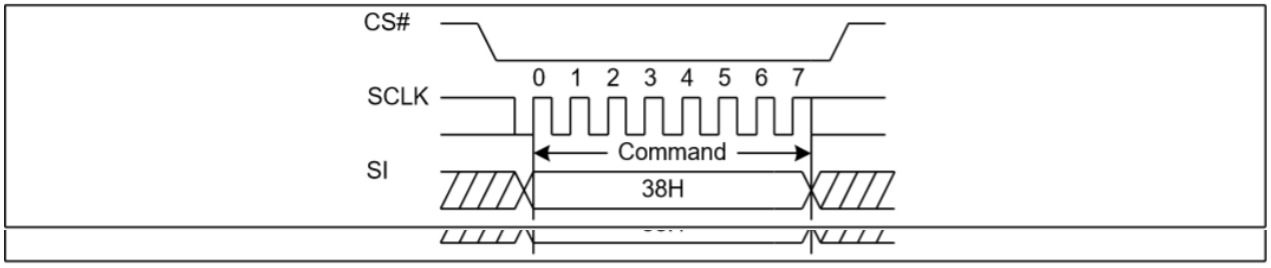


10.75 Enable QPI (EQIO)
10.76 启用 QPI (EQIO)

The device support both Standard/Dual/Quad SPI and QPI mode. The "Enable QPI (38H)" command can switch the device from SPI mode to QPI mode. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and "Enable QPI (38H)" command must be issued. If the QE bit is 0, the "Enable QPI (38H)" command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

该器件支持标准/双通道/四通道 SPI 和 QPI 模式。"启用 QPI (38H)"命令可以将器件从 SPI 模式切换到 QPI 模式。为了将设备切换到 QPI 模式，必须首先将状态寄存器-2 中的四通道使能(QE)位设置为 1，并且必须发出"使能 QPI (38H)"命令。如果 QE 位为 0，"使能 QPI (38H)"命令将被忽略，器件将保持 SPI 模式。当器件从 SPI 模式切换到 QPI 模式时，现有的写使能锁存和编程/擦除挂起状态以及卷绕长度设置将保持不变。

Figure 67. Enable QPI Sequence (SPI mode only)
图 67。使能 QPI 序列(仅限 SPI 模式)



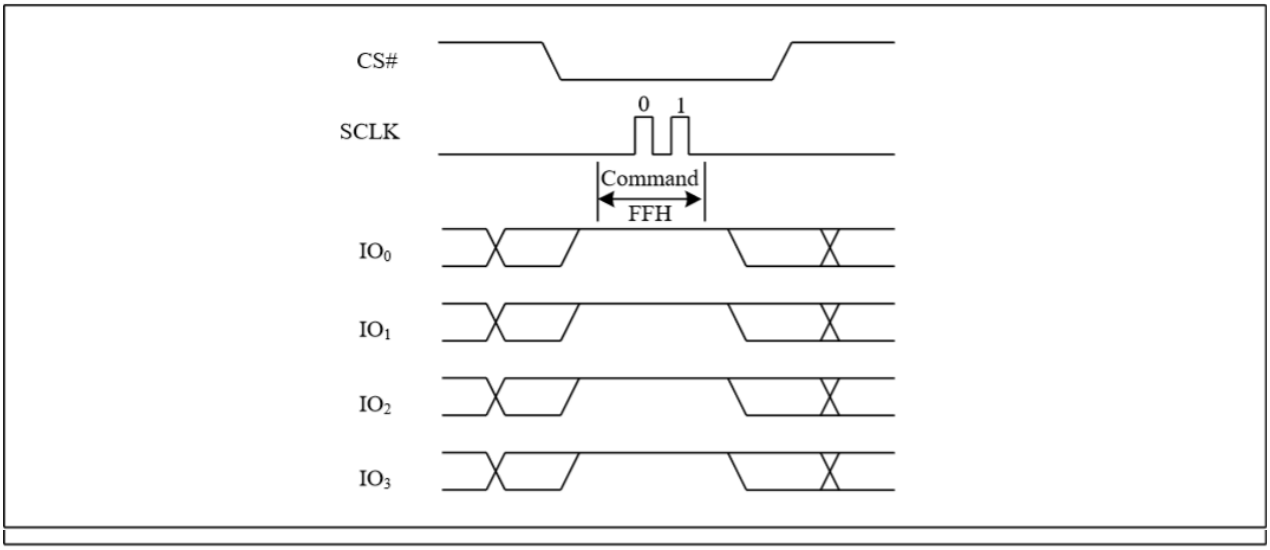
10.77 Reset QPI (RSTQIO)
10.78 复位 QPI (RSTQIO)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the "Reset QPI (FFH)" command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

要退出 QPI 模式并返回标准/双通道/四通道 SPI 模式，必须发出"复位 QPI (FFH)"命令。当器件从 QPI 模式切换到 SPI 模式时，现有的写使能锁存和编程/擦除挂起状态以及卷绕长度设置将保持不变。

Figure 68. Reset QPI Sequence (QPI mode only)

图 68。重置 QPI 序列(仅 QPI 模式)



10.79 Software Reset (Reset-Enable (RSTEN) and Reset (RST))
10.80 软件复位(复位使能(RSTEN)和复位(RST))

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

如果复位命令被接受，任何正在进行的内部操作将被终止，并且设备将返回到其默认通电状态，并且丢失所有当前易失性设置，例如易失性状态寄存器位、写使能锁存状态(WEL)、编程/擦除暂停状态、读取参数设置(P7-P0)、连续读取模式位设置(M7-M0)和回绕位设置(W6-W4)。

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in either SPI or QPI mode. The “Reset (99H)” command sequence as follow: CS# goes low→ Sending Erase Security Registers command→ CS# goes high→ CS# goes low→ Sending Reset command→ CS# goes high.

“使能复位(66H)”和“复位(99H)”命令可以在 SPI 或 QPI 模式下发出。“复位(99H)”命令序列如下:CS#变低→发送擦除安全寄存器命令→ CS#变高→ CS#变低→发送复位命令→ CS#变高。

Once the Reset command is accepted by the device, the device will take approximately tRST to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the ESB/PSB bit in Status Register before issuing the Reset command sequence.

一旦设备接受复位命令，设备将需要大约 tRST 的时间来复位。在此期间，不接受任何命令。当设备接受复位命令序列时，如果存在正在进行或暂停的内部擦除或编程操作，可能会发生数据损坏。建议在发出复位命令序列之前，检查状态寄存器中的 BUSY 位和 ESB/PSB 位。

Figure 69. Software Reset Sequence (SPI mode)
图 69。软件复位序列(SPI 模式)

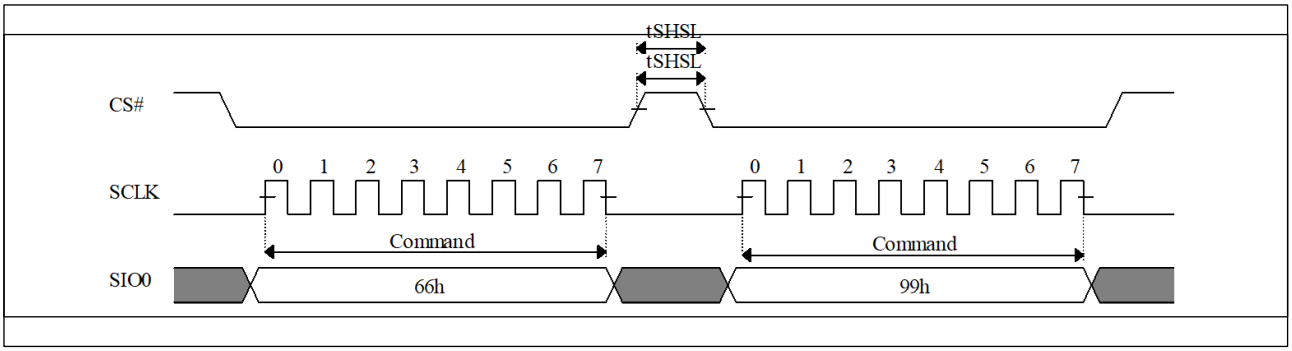
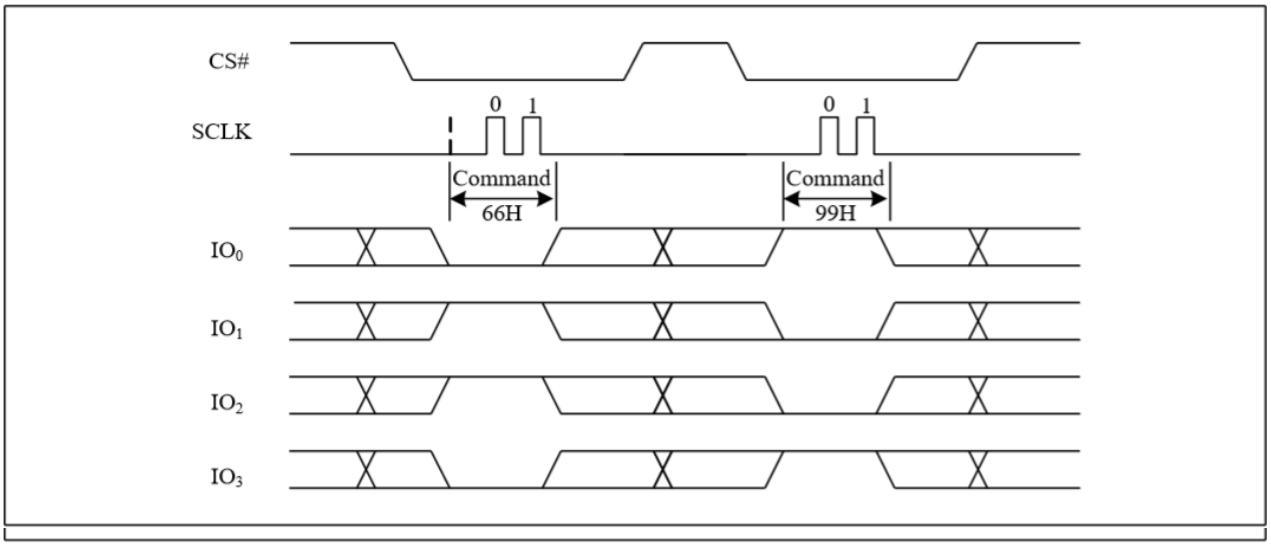


Figure 70. Software Reset Sequence (QPI mode)
图 70。软件复位序列(QPI 模式)


CS#
SCLK
0
1
0
1
Command
66H
Command
99H
IO0
IO1
IO2
IO3

10.81 Read SFDP Mode (RDSFDP)

10.82 读取 SFDP 模式(RDSFDP)

The NM25Q64 features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011.

NM25Q64 具有一个 256 字节的串行闪存可发现参数(SFDP)寄存器，其中包含有关设备配置、可用指令和其他功能的信息。SFDP 参数存储在一个或多个参数识别(PID)表中。目前只指定了一个 PID 表，但将来可能会添加更多。读取 SFDP 寄存器指令兼容 2010 年针对 PC 和其它应用制定的 SFDP 标准，以及 2011 年发布的 JEDEC 标准 JESD216。

The sequence of issuing RDSFDP command is CS# goes low→ send RDSFDP command (5Ah)→ send 3 address bytes on SI pin→ send 8 dummy cycles → read SFDP code on SO →to end RDSFDP operation can use CS# to high at any time during data out.

RDSFDP 命令的发出顺序为 CS#变为低电平→发送 RDSFDP 命令(5Ah)→在 SI 引脚上发送 3 个地址字节→发送 8 个虚拟周期→在 SO 上读取 SFDP 码→要结束 RDSFDP 操作，可在数据输出期间随时使用 CS#变为高电平。

Figure 71. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence
图 71。读取串行闪存可发现参数(RDSFDP)序列

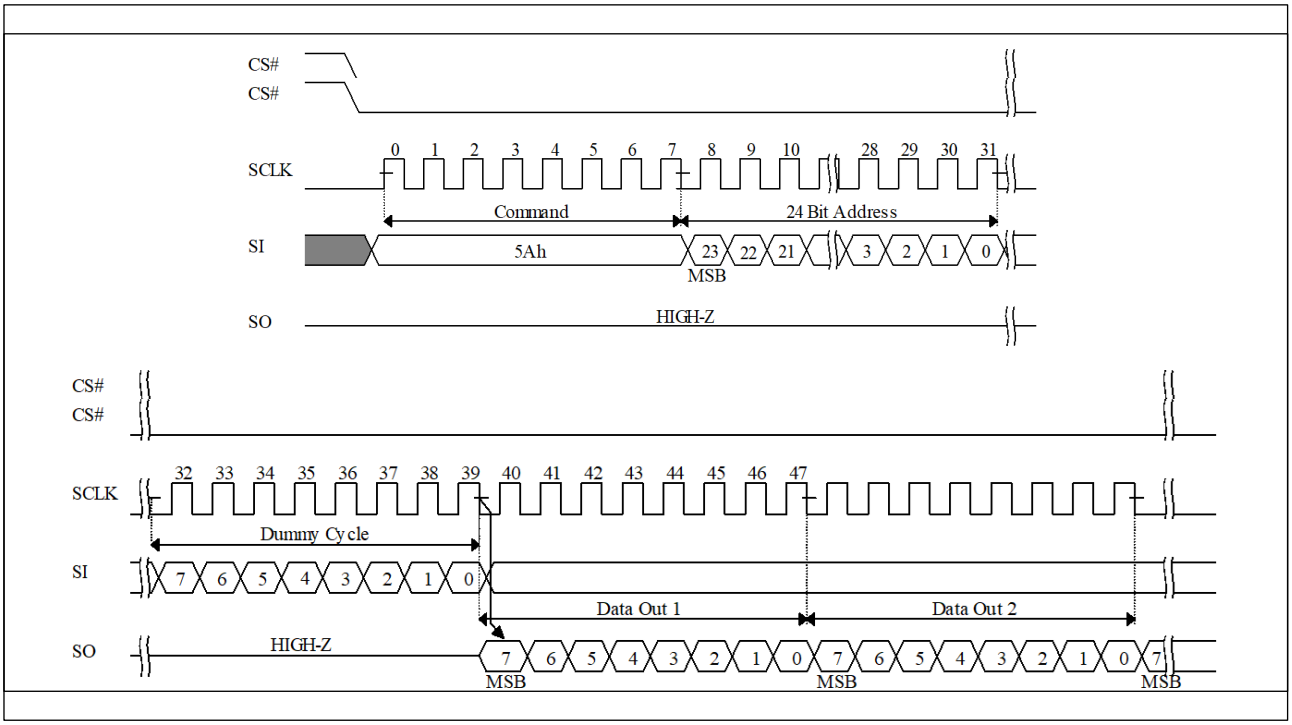
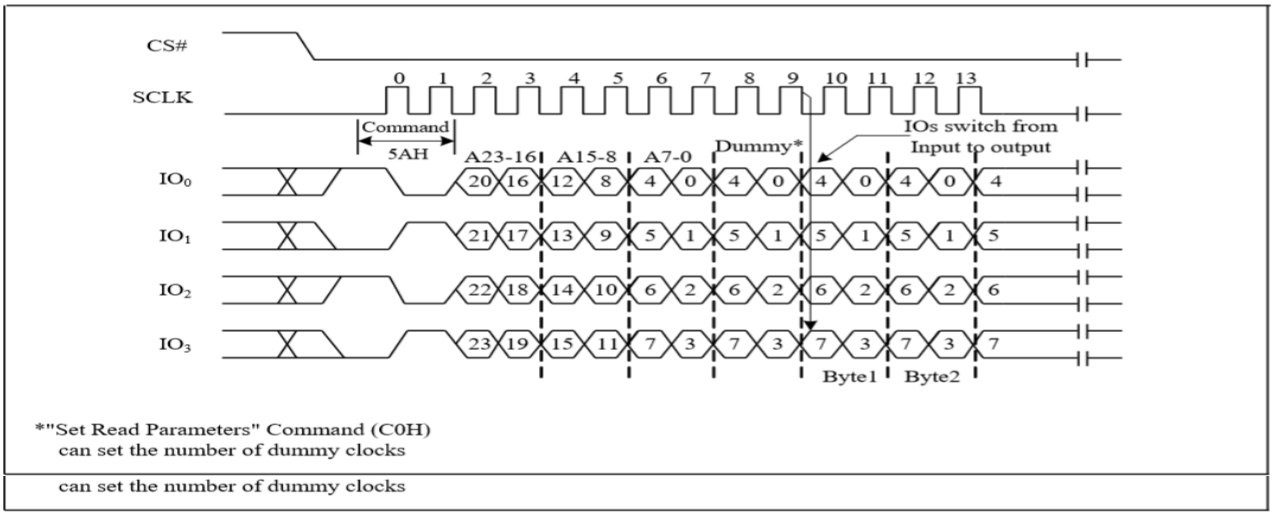


Figure 72. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence (QPI Mode)
图 72。读取串行闪存可发现参数(RDSFDP)序列(QPI 模式)



can set the number of dummy clocks

21. RESET

22. 重置

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:

将 RESET#引脚拉低 tRLRH 或更长时间将复位器件。复位周期后，设备处于以下状态:

- Standby mode
- 备用方式
- All the volatile bits such as WEL/WIP will return to the default status as power on.
- 所有易失位(如 WEL/WIP)将在通电时返回默认状态。
- All the volatile bits in SR1/SR2/SR3/CR will return to the default status as power on.

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SIO data becomes high impedance

- 上电时，SR1/SR2/SR3/CR 中的所有易失位将返回默认状态。如果器件正在编程或擦除，将 RESET#引脚拉低也会终止操作，数据可能会丢失。在复位周期中，SIO 数据变为高阻态

and the current will be reduced to minimum.

并且电流将被减小到最小。

Figure 73. RESET Timing

图 73。重置时序

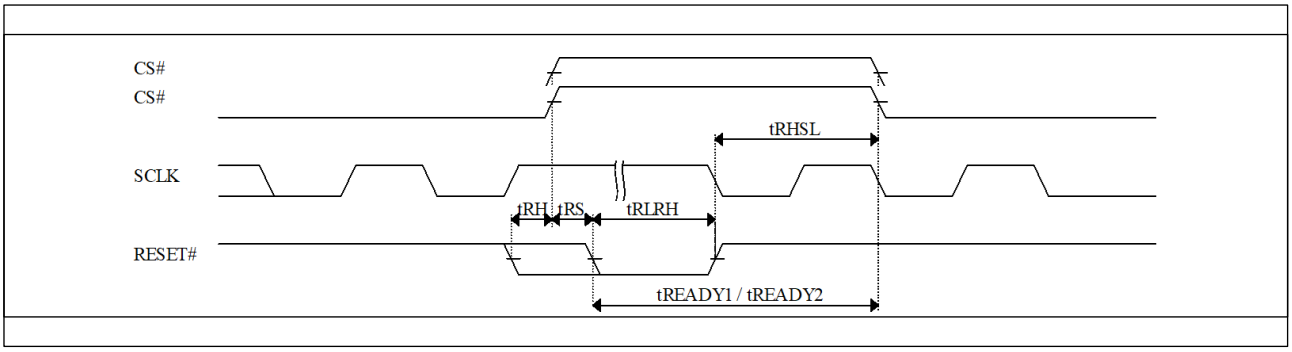


Table 13. Reset Timing-(Standby)

表 13。重置时间-(待机)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time	35			us

标志	参数	量滴	典型。	最大值	单位
tRHSL	在 CS#低之前复位#高	10			我们
tRS	重置#设置时间	15			纳秒
殿下	重置#保持时间	15			纳秒
tRLRH	重置#低脉冲宽度	10			我们
踏板 1	重置恢复时间	35			我们

Table 14. Reset Timing-(Other Operation)
表 14。重置定时-(其他操作)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (During command decoding)	40			us
	Reset Recovery time (for read operation)	40			us
标志	**参数**	**量滴**	**典型。**	**最大值**	**单位**
tRHSL	在 CS#低之前复位#高	10			我们
tRS	重置#设置时间	15			纳秒
殿下	重置#保持时间	15			纳秒
tRLRH	重置#低脉冲宽度	10			我们
踏板 2	复位恢复时间(命令解码期间)	40			我们
	复位恢复时间(用于读取操作)	40			我们

	Reset Recovery time (for program operation)	310			us
	Reset Recovery time(for SE4KB operation)	12			ms
	Reset Recovery time (for BE64K operation)	25			ms
	Reset Recovery time (for Chip Erase operation)	100			ms
	Reset Recovery time (for WRSR operation)	40			ms
	复位恢复时间(用于程序运行)	310			我们
	复位恢复时间(针对 SE4KB 操作)	12			女士
	复位恢复时间(用于 BE64K 操作)	25			女士
	复位恢复时间(芯片擦除操作)	100			女士
	重置恢复时间(适用于 WRSR 操作)	40			女士

23. POWER-ON STATE
24. 通电状态

The device is at below states when power-up:
通电时，设备处于以下状态:

- Standby mode (please note it is not deep power-down mode)
- 待机模式(请注意，这不是深度掉电模式)
- Write Enable Latch (WEL) bit is reset
- 写使能锁存(WEL)位复位

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

除非 VCC 达到正确水平以下，否则在加电和断电阶段不得选择器件:

- VCC minimum at power-up stage and then after a delay of Tvsl

- 通电阶段和 Tvsl 延迟后的 VCC 最小值
- GND at power-down
- 掉电时的 GND

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

请注意，CS#上的上拉电阻可以确保安全和适当的上电/关断电平。

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

内部上电复位(POR)电路可以防止器件在上电状态下出现数据损坏和意外数据更改。当 VCC 低于 VWI (POR 阈值电压值)时，内部逻辑复位，闪存设备对任何命令无响应。

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

为了进一步保护设备，如果 VCC 没有达到 VCC 最低水平，则不能保证正确操作。写入、擦除和编程命令应在以下时间延迟后发送:

- tVSL after VCC reached VCC minimum level
- VCC 达到 VCC 最低水平后的 tVSL

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the ""Power-up Timing"".

该设备可以在 VCC 达到 VCC 最小值和 tVSL 的时间延迟之后接受读取命令。请参考“通电时间”。

Note:
注意:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- 为了稳定 VCC 电平，建议使用靠近封装引脚的合适电容对 VCC 供电轨进行去耦。(一般在 0.1uF 左右)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.
- 在断电阶段，VCC 降至 VWI 电平以下，所有操作均被禁用，设备对任何命令均无响应。当写入、编程、擦除循环正在进行时，数据损坏可能发生在该阶段。

25. ELECTRICAL SPECIFICATIONS

26. 电气规格

Table 15. ABSOLUTE MAXIMUM RATINGS
表 15。绝对最大额定值

RATING	VALUE	
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 2.5V
等级	**价值**	
环境工作温度	技术等级	-40 摄氏度至 85 摄氏度
储存温度		-65 摄氏度至 150 摄氏度
施加的输入电压		-0.5V 至 VCC+0.5V
施加的输出电压		-0.5V 至 VCC+0.5V
VCC 到地电位		-0.5V 至 2.5V

NOTICE:

注意:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied.

2. 超过绝对最大额定值的应力可能会对器件造成永久性损坏。这只是压力等级，并不暗示本规范的功能操作部分。

Exposure to absolute maximum rating conditions for extended period may affect reliability.
长时间暴露在绝对最大额定值条件下可能会影响可靠性。

3. Specifications contained within the following tables are subject to change.

4. 下表中包含的规格可能会更改。

5. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

6. 在电压转换期间，所有引脚可能会过冲至 VCC+1.0V 或-1.0V 长达 20 纳秒。

Figure 74. Maximum Negative Overshoot Waveform
图 74。最大负过冲波形

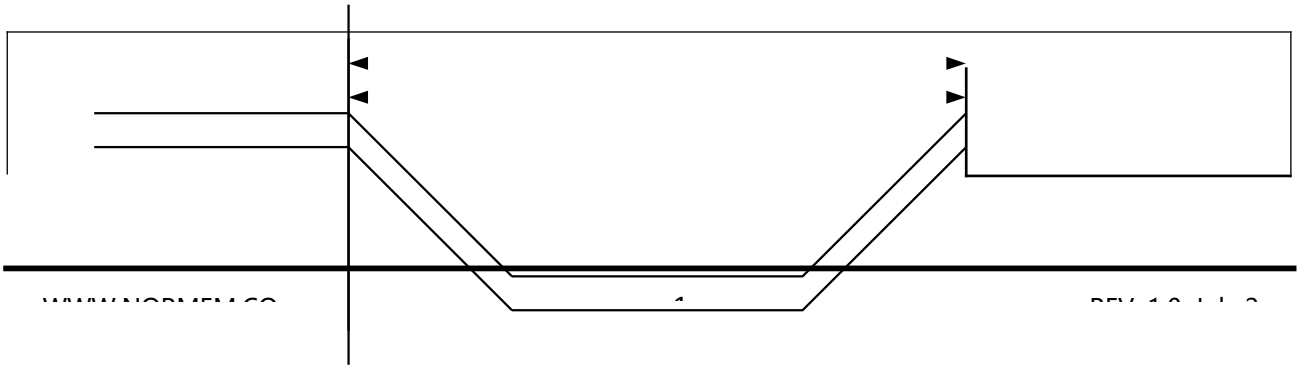


Figure 75. Maximum Positive Overshoot Waveform
图 75。最大正过冲波形

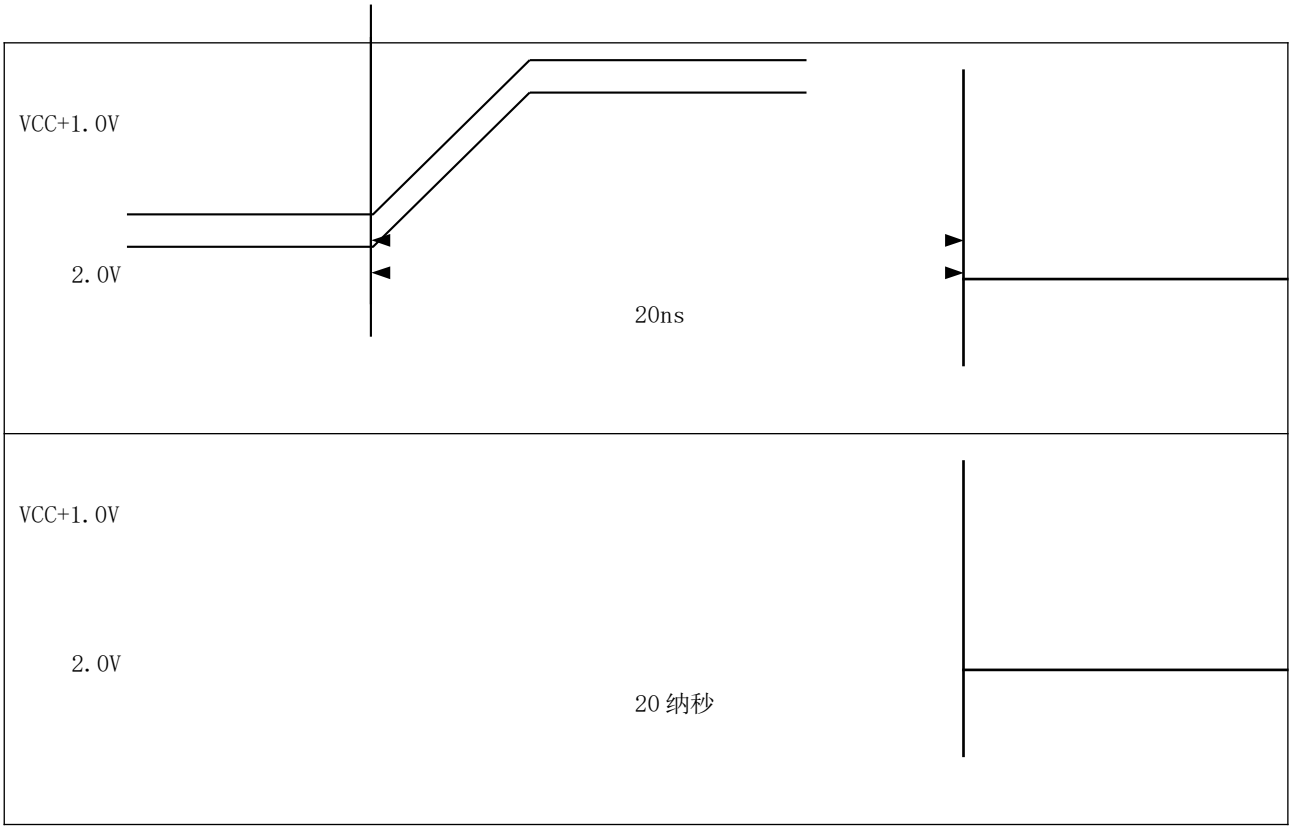


Table 16. CAPACITANCE TA = 25°C, f = 1.0 MHz

表 16。电容 TA = 25° C，f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V
标志	参数	量滴	典型。	最大值	单位	情况
CIN	输入电容			6	性能因素 (Performance Factor)	VIN = 0V
标准输出	输出电容			8	性能因素 (Performance Factor)	VOUT = 0V

Figure 75. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

图 75。输入测试波形和测量电平

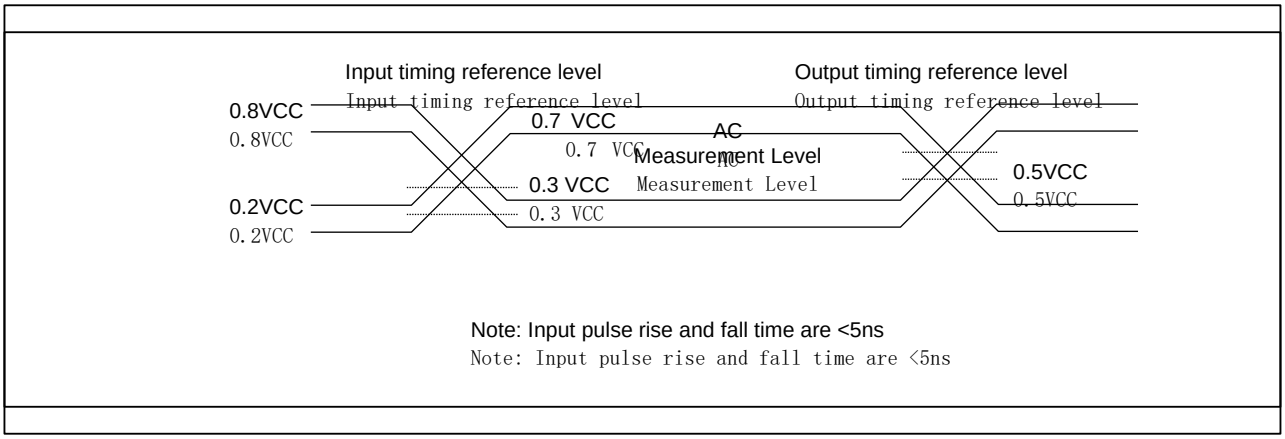
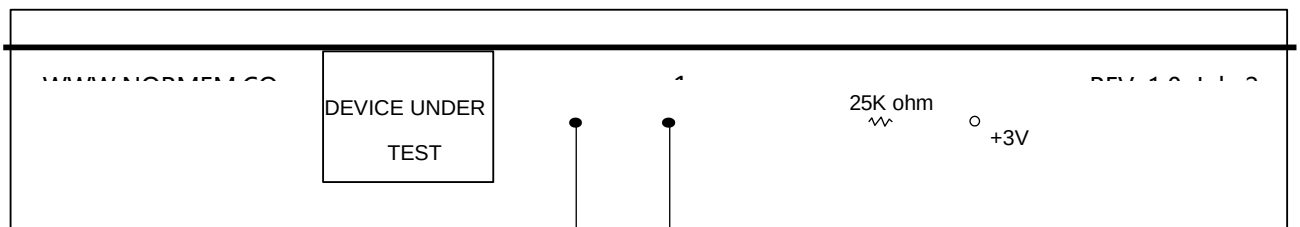
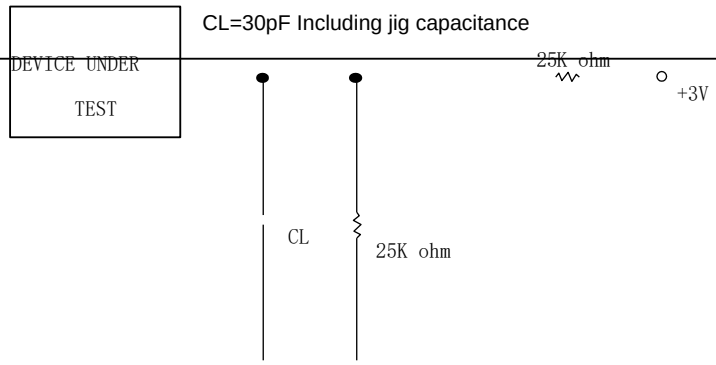


Figure 76. OUTPUT LOADING

图 76。输出负载





CL=30pF Including jig capacitance

13.1 DC CHARACTERISTICS

13.2 DC特色

Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V

温度= -40 摄氏度至 85 摄氏度，VCC = 2.7 伏至 3.6 伏

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		20	180	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			3	50	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		20	40	mA	100MHz 4IO STR (SIO floating)
				25	50	mA	133MHz 4IO STR (SIO floating)
ICC2	VCC Program Current	1		30	40	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	40	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		20	40	mA	Erase in Progress, CS#=VCC
ICC4	VCC Block Erase Current (BE)	1		30	40	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	40	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.4		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL=100uA
VOH	Output High Voltage		VCC-0.2			V	IOH=-100uA
标志	**参数**	**笔记**	**量滴**	**典型。**	**最大值**	**单位**	**试验条件**
ILI	输入负载电流	一			2	美国联合航空公司	VCC = VCC • 马克斯，VIN = VCC 或 GND
国际劳	输出泄漏	一			2	美国	VCC = VCC • 马克斯，

工组织	目前的					联合航空公司	VOUT = VCC 或 GND
ISB1	VCC 待命 目前的	一		20	180	美国联合航空公司	VIN = VCC 或 GND， CS# = VCC
ISB2	深度关断 目前的			3	50	美国联合航空公司	VIN = VCC 或 GND， CS# = VCC
ICC1	VCC 读道	一		20	40	妈	100MHz 4IO 字符串 (SIO 浮动)
				25	50	妈	133MHz 4IO 字符串 (SIO 浮动)
ICC2	VCC 计划 目前的	一		30	40	妈	程序正在进行中， CS# = VCC
ICC3	VCC 写状态寄存器 (WRSR)当前			20	40	妈	程序状态寄存器进行中，CS#=VCC
ICC4	VCC 扇区擦除电流 (东南)	一		20	40	妈	正在擦除，CS#=VCC
ICC4	VCC 块擦除电流 (是)	一		30	40	妈	正在擦除，CS#=VCC
ICC5	VCC 芯片擦除 电流(CE)	一		20	40	妈	正在擦除， CS#=VCC
垂直注入逻辑	输入低电压		-0.4		0.3 伏交流电压	V	
VIH	输入高电压		0.7VCC		VCC+0.4	V	
卷（volume 的缩写）	输出低电压				0.2	V	IOL=100uA
VOH	输出高电平 电压		VCC-0.2			V	IOH=-100uA

Notes:

注意事项:

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. VCC = 3.3V、温度= 25° c 时的典型值，这些电流对所有产品版本(封装和速度)都有效。
3. Typical value is calculated by simulation.
4. 典型值通过模拟计算。

13.3 AC CHARACTERISTICS

13.4 交流特性

Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V
温度= -40 摄氏度至 85 摄氏度，VCC = 2.7 伏至 3.6 伏

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock frequency for SPI commands except Read				104	MHz
fRSCLK	fR	Clock Frequency for READ, REMS, RDID commands				80	MHz
fQSCLK	fQ	Clock Frequency for 4READ				104/80	MHz
tCH(1)	tCH	Clock High Time		0.45*T			ns
tCL(1)	tCL	Clock Low Time		0.45*T			ns
tCLCH(2)		Clock Rise Time (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHSL	tCSH	CS# Deselect Time (read/write)		20			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		2			ns
tSHQZ(2)	tDIS	Output Disable Time				8	ns
tCLQV / tCHQV	tV	Clock transient to Output Valid	Loading: 30pF			8	ns
			Loading: 20pF			6	
tCLQX	tHO	Output Hold Time		1			ns
tHLCH		HOLD# Low Setup Time (relative to SCLK)		5			
tHHCH		HOLD# High Setup Time (relative to SCLK)		5			
tCHHL		HOLD# High High Time (relative to SCLK)		5			
tCHHH		HOLD# High Low Time (relative to SCLK)		5			
tHLQZ		HOLD# Low To High-Z Output				8	
tHHQX		HOLD# High To Low-Z Output				8	
tWHSL		Write Protect Setup Time Before CS# Low		20			
tSHWL		Write Protect Hold Time After CS# High		100			
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode				30	us
tRES2(2)		CS# High to Standby Mode with RDI				30	us
tSUS		CS# High to Next Command After Suspend				20	us
tRST_R		CS# High to Standby Mode with Reset (From Read)				20	us
tRST_P		CS# High to Standby Mode with Reset (From Program)				20	us
tRST_E		CS# High to Standby Mode with Reset (From Erase)				12	us
tW		Write Status/Configuration Register Cycle Time			5	30	ms
tBP(3)		Byte Program Cycle Time			30	50	us
tPP(3)		Page Program Cycle Time			0.6	2.4	ms
tSE		Sector Erase Cycle Time			25	400	ms

tBE32		Block Erase (32KB) Cycle Time		0.11	1.6	s
tBE		Block Erase (64KB) Cycle Time		0.22	2	s

标志	表示“另类的”	参数		量滴	典型。	最大值	单位
fSCLK	足球俱乐部（Football Club）	除读取以外的SPI命令的时钟频率				104	兆赫
fRSCLK	神父	读取、REMS、RDID命令的时钟频率				80	兆赫
fQSCLK	会计季度(fiscal quarter)	4读取的时钟频率				104/80	兆赫
tCH(1)	哼	时钟高电平时间		0.45*T			纳秒
tCL(1)	TCL集团股份有限公司（TCL Corporation的缩写）	时钟低电平时间		0.45*T			纳秒
tCLCH(2)		时钟上升时间(峰峰值)		0.1			V/ns
tCHCL(2)		时钟下降时间(峰峰值)		0.1			V/ns
tSLCH	tCSS	CS#活动设置时间(相对于SCLK)		5			纳秒
tCHSL		CS#非活动保持时间(相对于SCLK)		5			纳秒
tSHCH		CS#非活动设置时间(相对于SCLK)		5			纳秒
tCHSH		CS#活动保持时间(相对于SCLK)		5			纳秒
tSHSL	tCSH	CS#取消选择时间(读/写)		20			纳秒
tDVCH	tDSU	设置时间内的数据		2			纳秒
tCHDX	tDH	数据保持时间		2			纳秒
东方神起(2)	tDIS	输出禁用时间				8	纳秒
tCLQV / tCHQV	电视	时钟瞬变至输出有效	负载:30pF			8	纳秒
			负载:20pF			6	
tCLQX	可是	输出保持时间		一			纳秒
tHLCH		保持#低设置时间(相对于SCLK)		5			
tHHCH		保持#高设置时间(相对于SCLK)		5			
tCHHL		保持# High High时间(相对于SCLK)		5			
tCHHH		保持#高/低时间(相对于SCLK)		5			
tHLQZ		保持#低至高Z输出				8	
tHHQX		保持#高到低Z输出				8	
tWHSL		CS#低电平前的写保护建立时间		20			
tSHWL		CS#高电平后的写保护保持时间		100			
tDP(2)		CS#高电平至深度掉电模式				10	我们
tRES1(2)		CS#高电平至待机模式				30	我们
tRES2(2)		CS#高电平至带RDI的待机模式				30	我们

tSUS		暂停后CS#高电平至下一个命令			20	我们
tRST_R		CS#高电平至带复位的待机模式(从读取)			20	我们
tRST_P		CS#高电平至带复位的待机模式(来自程序)			20	我们
tRST_E		CS#高电平至带复位的待机模式(从擦除)			12	我们
tW		写状态/配置寄存器周期时间		5	30	女士
tBP(3)		字节程序周期时间		30	50	我们
tPP(3)		页面程序周期时间		0.6	2.4	女士
试验辅助设备		扇区擦除周期时间		25	400	女士
tBE32		块擦除(32KB)周期时间		0.11	1.6	s
四溴乙烷(tetrabromoethane)		块擦除(64KB)周期时间		0.22	2	s

tCE		Chip Erase Cycle Time		22	60	s
总综合误差（Total Composite Error 的缩写）		芯片擦除周期时间		22	60	s

Notes:

注意事项:

1. tCH + tCL must be greater than or equal to 1/ Frequency.

2. tCH + tCL 必须大于或等于 1/频率。

3. Typical values given for TA=25°C. Not 100% tested.

4. TA = 25° c 时给出的典型值，未经 100%测试。

5. While programming consecutive bytes, Page Program command provides optimized timings by selecting to program the whole 256 bytes or only a few bytes between 1~256 bytes.

6. 当编程连续字节时，页面编程命令通过选择编程整个 256 字节或仅编程 1~256 字节之间的几个字节来提供优化的时序。

Figure 77. Input Timing (STR mode)
图 77。输入时序(STR 模式)

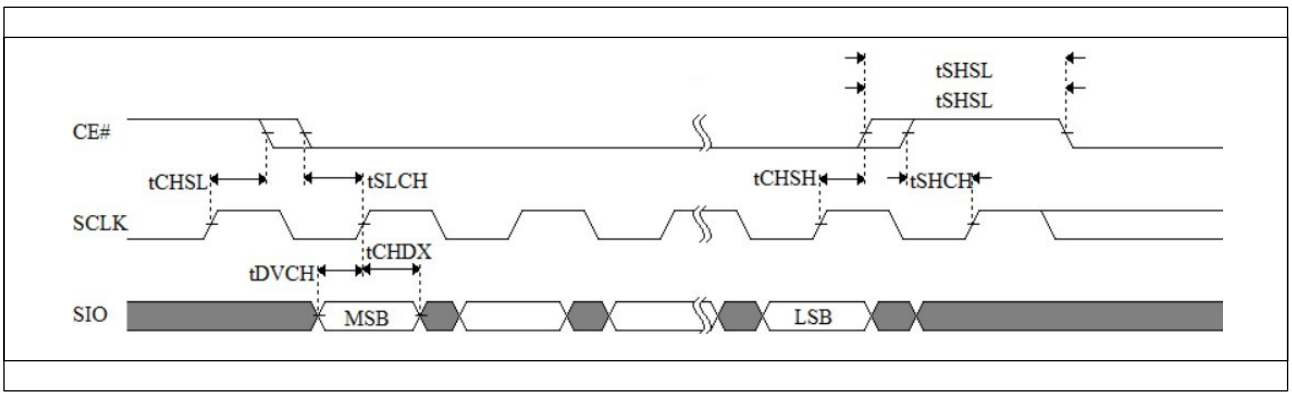
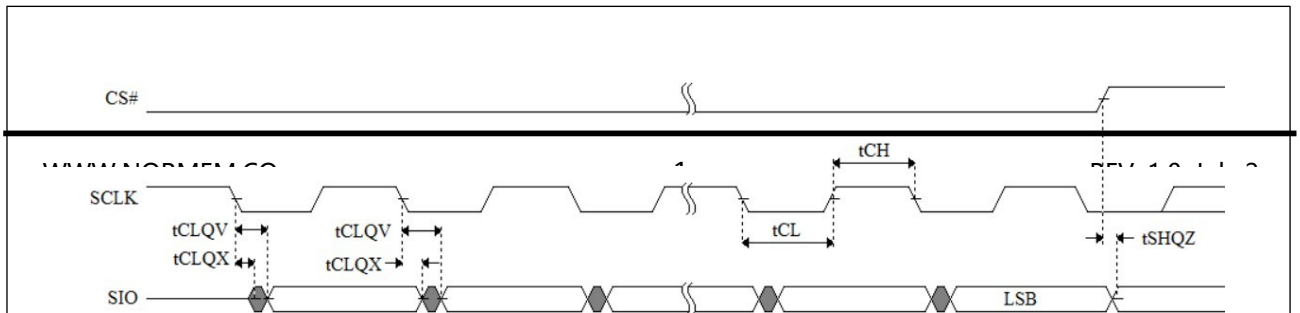


Figure 78.Output Timing (STR mode)
图 78。输出时序(STR 模式)



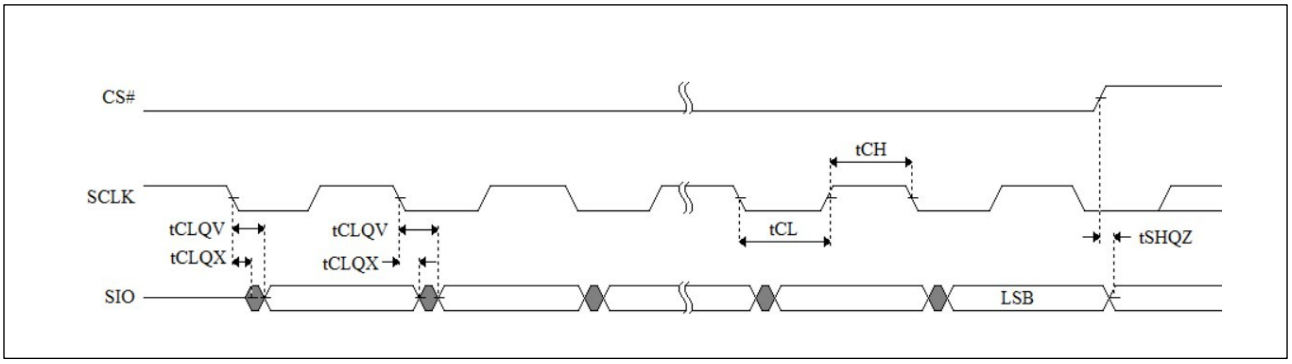
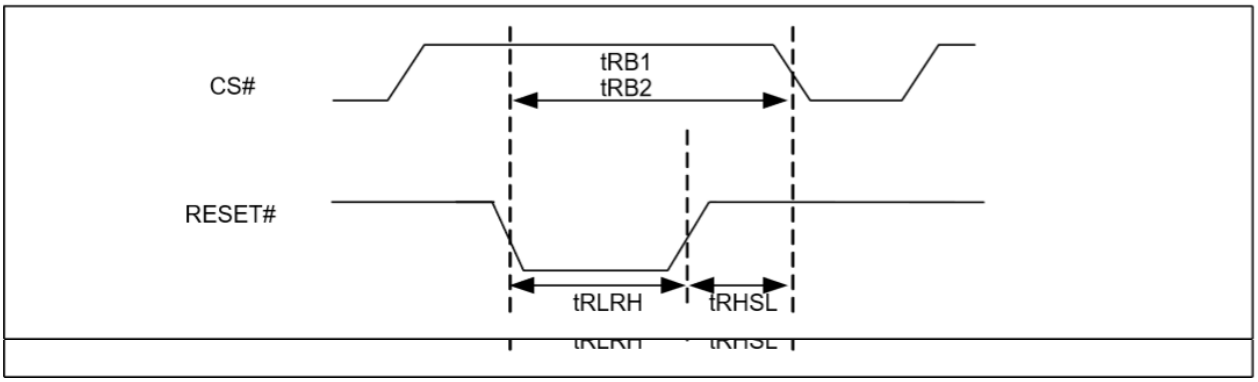


Figure 79.Reset Timing
图 79。重置时序

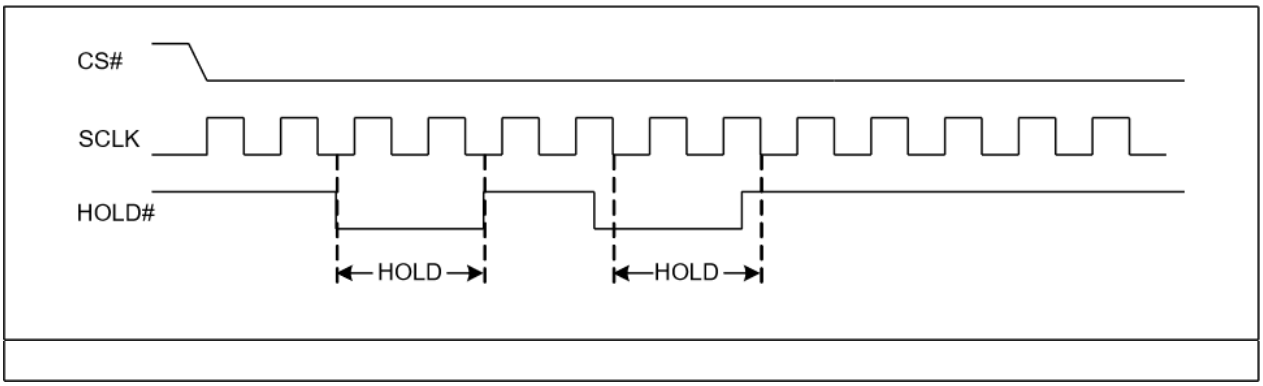


Reset Timing

重置时序

Symbol	Parameter	Setup	Speed	Unit
tRLRH	Reset Pulse Width	MIN	1	us
tRHSL	Reset High Time Before Read	MIN	50	ns
tRB1	Reset Recovery Time (For not busy mode)	MAX	5	us
tRB2	Reset Recovery Time (For busy mode)	MAX	60	us
标志	参数	设置	速度	单位
tRLRH	复位脉冲宽度	部	一	我们
tRHSL	读取前复位高电平时间	部	50	纳秒
tRB1	复位恢复时间(非繁忙模式)	马克斯(男子名,等于Maximilian)	5	我们
tRB2	复位恢复时间(繁忙模式)	马克斯(男子名,等于Maximilian)	60	我们

Figure 80. Hold Timing
图 80。保持计时



27. OPERATING CONDITIONS

28. 操作件

14.1 At Device Power-Up and Power-Down
14.2 在器件上电和断电时

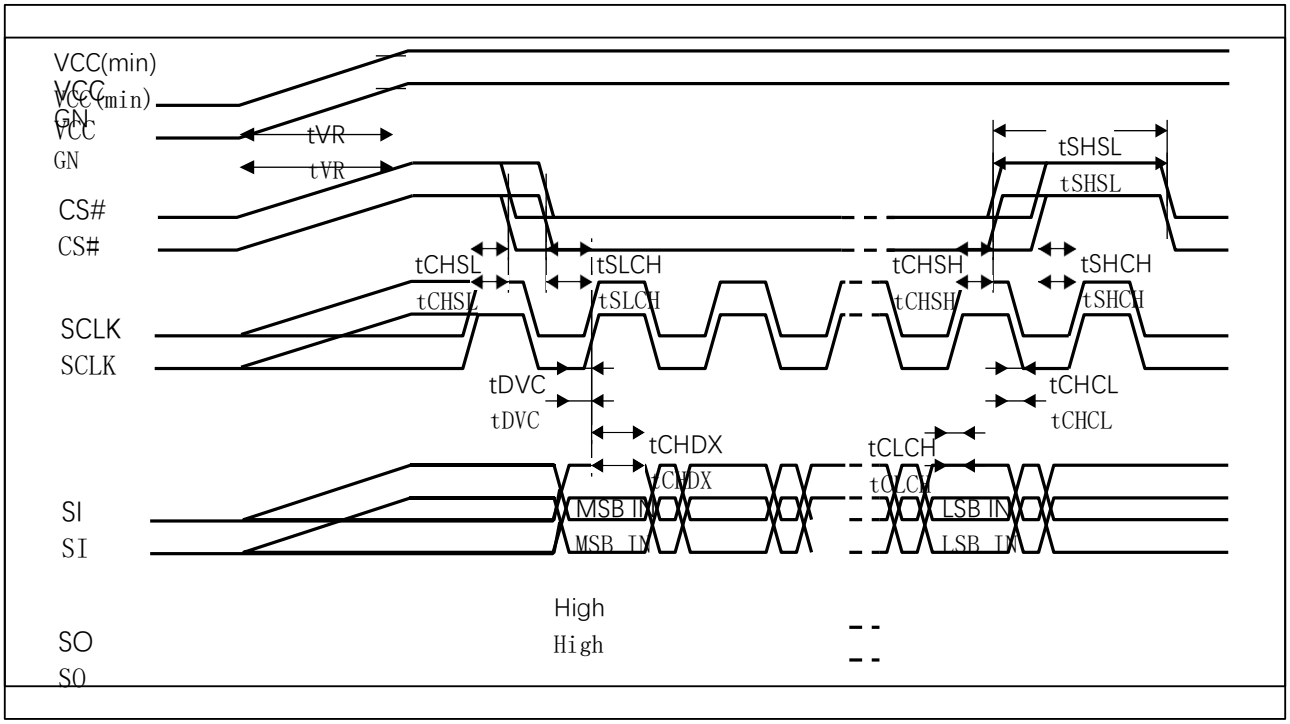
AC timing illustrated in Figure 84 and Figure 85 are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

图 84 和图 85 所示的交流时序针对器件上电和关断时的电源电压和控制信号。如果忽略图中的时序，设备将无法正常工作。

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

在上电和关断期间，CS#需要跟随 VCC 上施加的电压，以防止器件被选中。当 VCC 达到 Vcc(最小值)时，CS#可以被驱动为低。)再等一段 tVSL。

Figure 81. AC Timing at Device Power-Up
图 81。器件上电时的交流时序



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V
标志	**参数**	**笔记**	**量滴**	**最大值**	**单位**
tVR	VCC 上升时间	一	20	500000	美国/V

Notes:
注意事项:

1. Sampled, not 100% tested.
2. 取样，不是 100%测试。
3. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to
4. 对于图中的交流规格 tCHSL、tSLCH、tDVCH、tCHDX、tSHSL、tCHSH、tSHCH、tCHCL、tCLCH，请参考

"AC CHARACTERISTICS".
"交流特性"。

Figure 82. Power-Down Sequence
图 82。掉电序列

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.
关断期间，CS#需要跟随 VCC 上的电压降，以避免误操作。

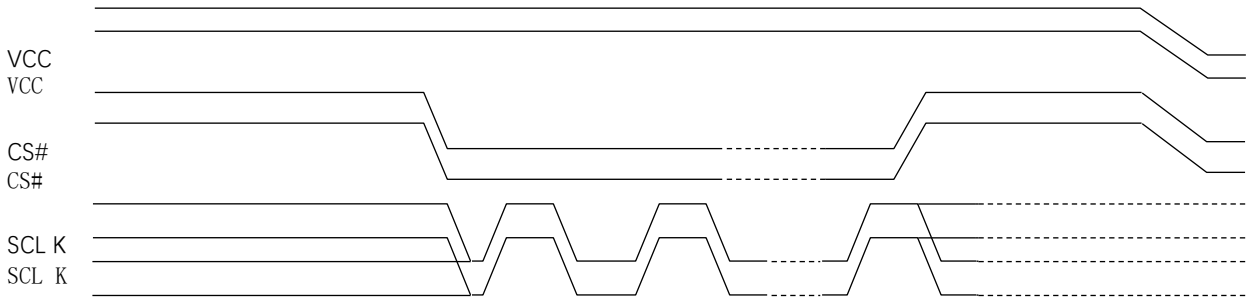


Figure 83. Power-up Timing
图 83。上电时序

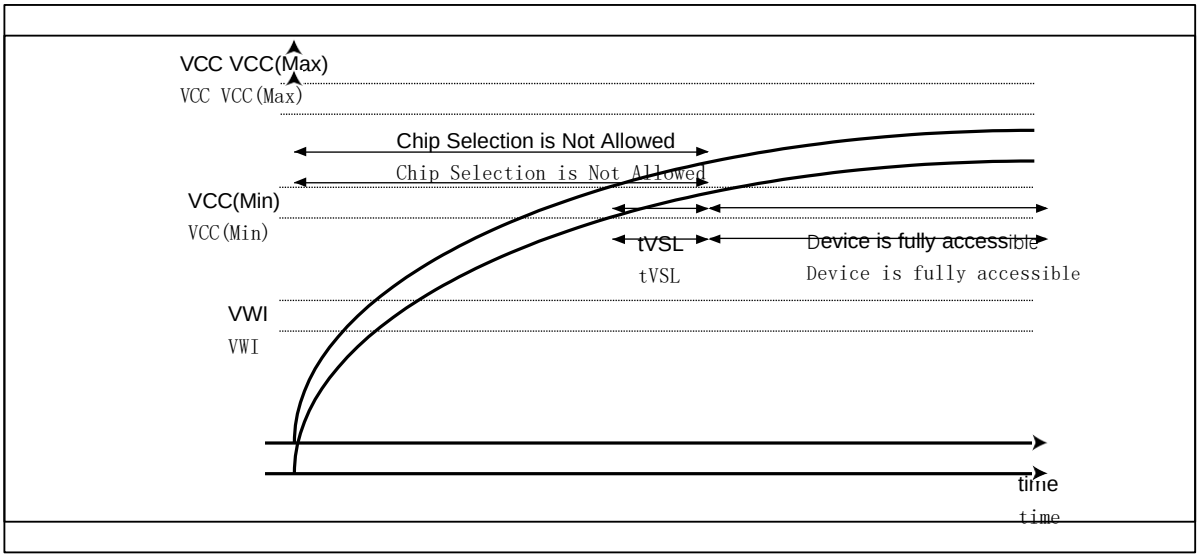
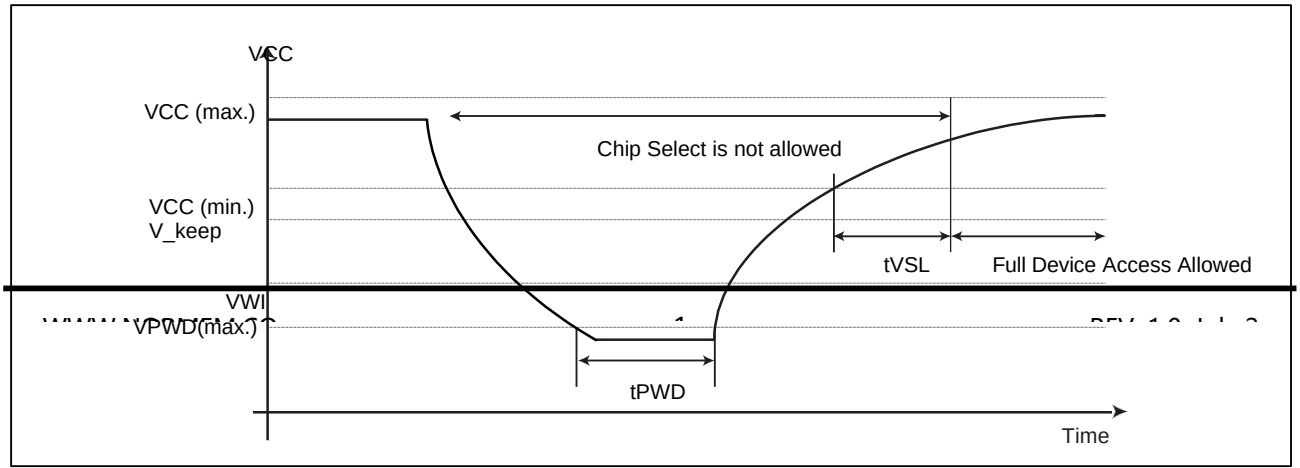
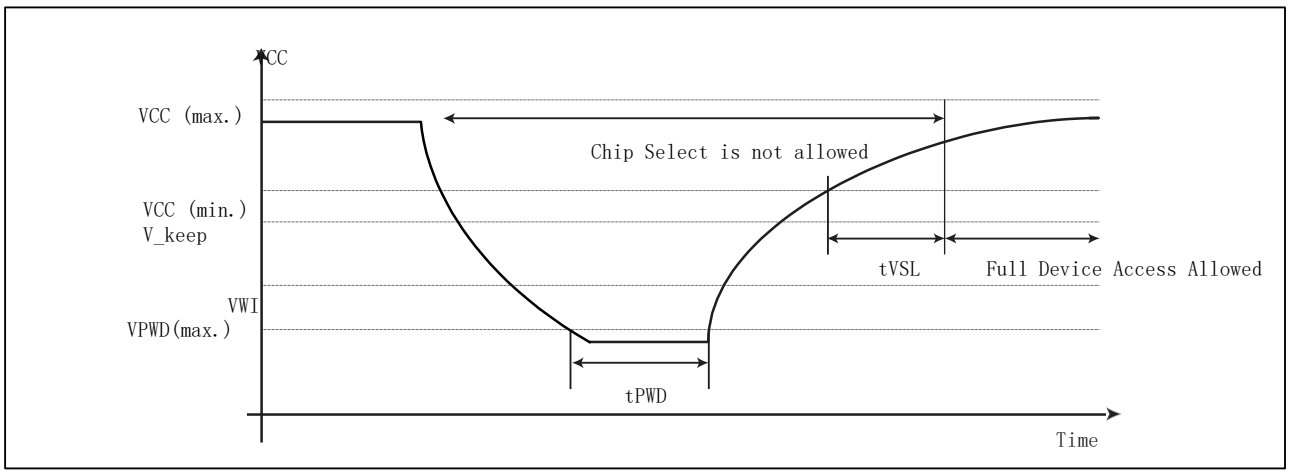


Figure 84. Power Up/Down and Voltage Drop
图 84。上电/断电和压降




VCC
VCC (max.)
VCC (min.)
V_keep
VWI
VPWD(max.)
Chip Select is not allowed
tVSL
Full Device Access Allowed
tPWD
Time

For Power-down to Power-up operation, the VCC of flash device must below V_{PWD} for at least tPWD timing. Please check the table below for more detail.

对于关断到上电操作，闪存器件的 VCC 必须低于 VPWD 至少 tPWD 时序。请查看下表了解更多详情。

Table 17. Power-Up/Down Voltage and Timing
表 17。上电/关断电压和时序

Symbol	Parameter	Min.	Max.	Unit
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		0.9	V
V_keep	Voltage that a re-initialization is necessary if VDD drop below to VKEEP	2.4		V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	3		ms
tVR	VCC Rise Time	20	500000	us/V
VCC	VCC Power Supply	2.7	3.6	V
VWI	Write Inhibit Voltage	2.0	2.3	V
标志	**参数**	**量滴**	**最大值**	**单位**
VPWD	VCC 电压需要低于 VPWD，以确保 将进行初始化		0.9	V
v _保持	如果 VDD 下降，则需要重新初始化的电压 下面到 VKEEP	2.4		V
tPWD	确保初始化发生的最短持续时间	300		我们
tVSL	VCC(最小。)到设备操作	3		女士
tVR	VCC 上升时间	20	500000	美 国/V
VCC	VCC 电源	2.7	3.6	V
VWI	写入禁止电压	2.0	2.3	V

14.3 INITIAL DELIVERY STATE
14.4 初始交付状态

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0). DEFDOPI# in SR2 depends on shipping device model.

器件交付时，存储器阵列已擦除:所有位均设置为 1(每个字节包含 FFh)。状态寄存器包含 00h(所有状态寄存器位均为 0)。SR2 的 DEFDOPI#取决于装运设备型号。

29. ERASE AND PROGRAMMING PERFORMANCE

30. 擦除和编程性能

Parameter	Min.	Typ. *(1)*	Max. *(2)*	Unit
Write Status Register Cycle Time			30	ms
Sector Erase Cycle Time (4KB)		25	400	ms
Block Erase Cycle Time (64KB)		220	2000	ms
Chip Erase Cycle Time		22	60	s
Page Program Time		0.6	2.4	ms
Erase/Program Cycle	100,000			cycles
参数	**量滴**	**典型。(1)**	**最大值(2)**	**单位**
写状态寄存器周期时间			30	女士
扇区擦除周期时间(4KB)		25	400	女士
块擦除周期时间(64KB)		220	2000	女士
芯片擦除周期时间		22	60	s
页面编程时间		0.6	2.4	女士
擦除/编程周期	100,000			周期

Note:
注意:

1. Typical program and erase time assumes the following conditions: 25°C, 3V, and checkboard pattern.
2. 典型的编程和擦除时间假设以下条件:25° C、3V 和 checkboard 模式。
3. Under worst conditions of 2.7V.
4. 在 2.7V 的最差条件下。
5. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
6. 系统级开销是执行编程命令的第一个总线周期序列所需的时间。
7. The maximum chip programming time is evaluated under the worst conditions of 0°C, VCC=3.3V, and 100K cycle with 90% confidence level.
8. 最大芯片编程时间是在 0° C、VCC=3.3V、100K 周期、90%置信度的最差条件下评估的。

31. DATA RETENTION

32. 数据保持

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years
参数	**情况**	**量滴**	**最大值**	**单位**
数据保持	55 摄氏度	20		年

33. LATCH-UP CHARACTERISTICS

34. 闩锁特性

	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input current with respect to GND on all non-power pins	-100mA	+100mA
Test conditions are compliant to JEDEC JDESD78 standard		
	量滴	**最大值**
所有电源引脚上相对于 GND 的输入电压		1.5 VCCmax
所有非电源引脚上相对于 GND 的输入电流	-100 毫安	+100 毫安
测试条件符合 JEDEC JDESD78 标准		

35. ORDERING INFORMATION

36. 订购须知

Please contact our regional sales for the latest product selection and available form factors.
请联系我们的区域销售人员，了解最新的产品选择和可用的外形规格。

PART NO.	TEMPERATURE	PACKAGE	Remark
NM25Q64EVBSIG	-40°C to 85°C	8-SOP (208mil)	Default x1I/O
NM25Q64EVBVIG	-40°C to 85°C	8-VSOP (208mil)	Default x1I/O
NM25Q64EVBFIG	-40°C to 85°C	16-SOP(300mil)	Default x1I/O
NM25Q64EVBBIG	-40°C to 85°C	8-DIP(300mil)	Default x1I/O
NM25Q64EVBPIG	-40°C to 85°C	8-WSON (6x5mm)	Default x1I/O
NM25Q64EVBWIG	-40°C to 85°C	8-WSON (8x6mm)	Default x1I/O
NM25Q64EVBTIG	-40°C to 85°C	24-Ball BGA (5x5 ball array)	Default x1I/O
零件号	**温度**	**包裹**	**注意**
NM25Q64EVBSIG	-40 摄氏度至 85 摄氏度	8-SOP(208 毫升)	默认 x1I/O
NM25Q64EVBVIG	-40 摄氏度至 85 摄氏度	8-VSOP (208mil)	默认 x1I/O
NM25Q64EVBFIG	-40 摄氏度至 85 摄氏度	16-SOP(300 毫升)	默认 x1I/O
NM25Q64EVBBIG	-40 摄氏度至 85 摄氏度	8-DIP(300 毫升)	默认 x1I/O
NM25Q64EVBPIG	-40 摄氏度至 85 摄氏度	8 英寸 WSON (6x5mm)	默认 x1I/O
NM25Q64EVBWIG	-40 摄氏度至 85 摄氏度	8 英寸 WSON (8x6mm)	默认 x1I/O
NM25Q64EVBTIG	-40 摄氏度至 85 摄氏度	24 引脚 BGA (5x5 引脚阵列)	默认 x1I/O

37. PART NAME DESCRIPTION

38. 零件名称描述

NM 25 Q 64E V B P I G

NM 25 Q 64E V B P I G

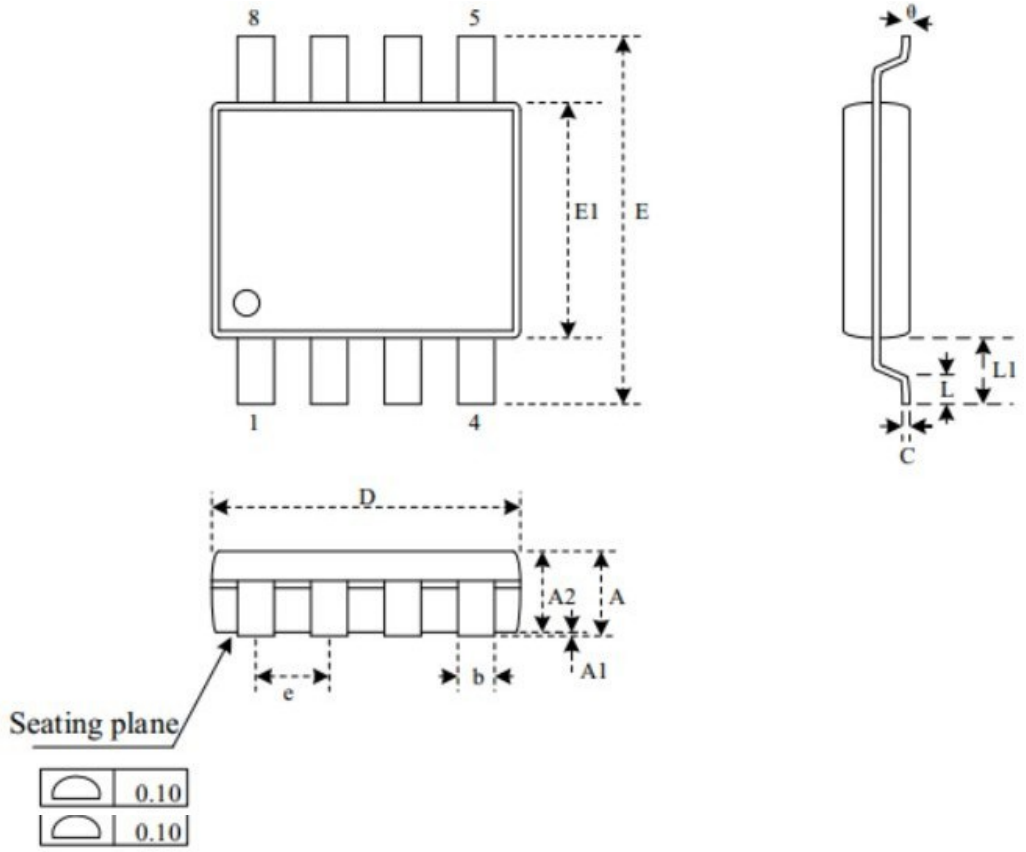
Green Code:
绿色代码：
G:Pb Free & Halogen Free Green Package
g:无铅无卤绿色包装
TEMPERATURE RANGE:
温度范围：
I:Industrial = -40℃to 85℃
M:Mobile = -40℃to 85℃
I:工业=-40℃至85℃ M:移动=-40℃至85℃
A:Automotive=-40℃ to 105℃ (Grade2 AEC-Q100)
答:汽车=-40℃至105℃(2级 AEC-Q100)
PACKGE
包装
S: 8-SOP(208 mil) V: 8-VSOP (208mil) F: 16-SOP(300 mil) B: 8-DIP(300mil)
s:8-SOP(208密耳)V:8-VSOP(208密耳)F:16-SOP(300密耳)B:8-DIP(300密耳)
P: 8-WSON (6x5mm) BW: 8-WSON (8x6mm)
p:8-WSON(6x 5毫米)BW:8-WSON(8x 6毫米)
T: 24-ball BGA(5×5 ball array)
T: 24球BGA(5×5球阵列)
Generation:
世代：
A: 1st generation
B: 2nd generation
Voltage：
a:第一代B:第二代电压:
V: 2.7V~3.6V
电压:2.7V~3.6V
Density:
密度：
64E: 64Mb (8MB)
64E: 64Mb (8MB)
128E: 128Mb (16MB)
128E: 128Mb (16MB)
256E: 256Mb (32MB)
256E: 256Mb (32MB)
512E: 512Mb (64MB)
512E: 512Mb (64MB)
TYPE:
类型：
L: Octal I/O
1:八进制输入输出
Q: QUAD / DUAL/Single I/O
问:四/双/单I/O
DEVICE:
设备：
25: Serial Nor Flash
25:串行或非闪存

39. PACKAGE INFORMATION

40. 包装信息

Package SOP8 208MIL

SOP8 208MIL 封装



Dimensions (Inch dimensions are derived from original mm dimensions)

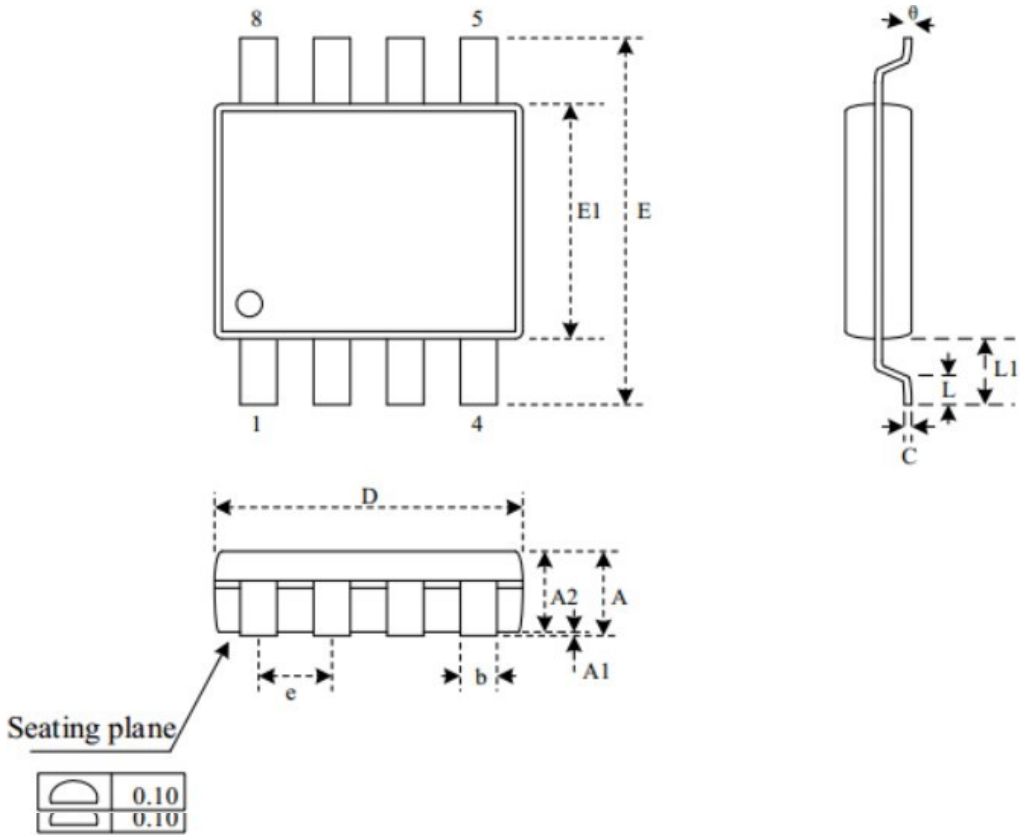
尺寸(英寸尺寸源自原始毫米尺寸)

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
	Min		0.05	1.70	0.31	0.18	5.13	7.70	5.18		0.50	1.21	0

mm	Nom		0.15	1.80	0.41	0.21	5.23	7.90	5.28	1.27	0.67	1.31	5
	Max	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.85	1.41	8
Inch	Min		0.002	0.067	0.012	0.007	0.202	0.303	0.204		0.020	0.048	0
	Nom		0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	5
	Max	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.033	0.056	8
标志 单位		A	一流的	主动脉第二声	b	C	D	E	E1	e	L	腰神经2	θ
毫米	福建话		0.05	1.70	0.31	0.18	5.13	7.70	5.18		0.50	1.21	0
	提名		0.15	1.80	0.41	0.21	5.23	7.90	5.28	1.27	0.67	1.31	5
	最大	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.85	1.41	8
英寸	福建话		0.002	0.067	0.012	0.007	0.202	0.303	0.204		0.020	0.048	0
	提名		0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	5
	最大	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.033	0.056	8

Package VSOP8 208MIL

封装 VSOP8 208MIL



Dimensions (Inch dimensions are derived from original mm dimensions)

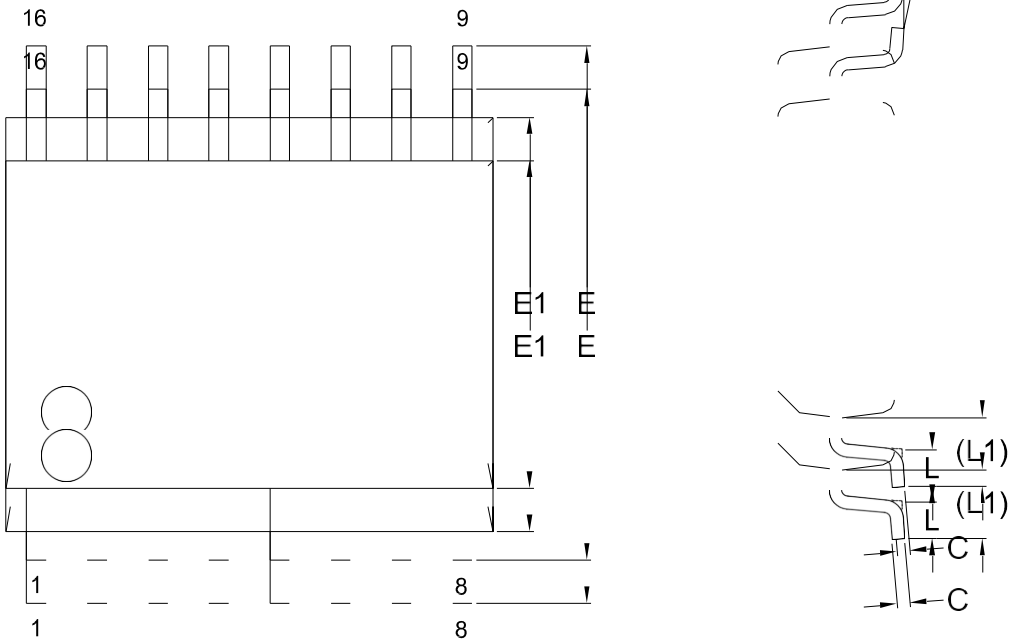
尺寸(英寸尺寸源自原始毫米尺寸)

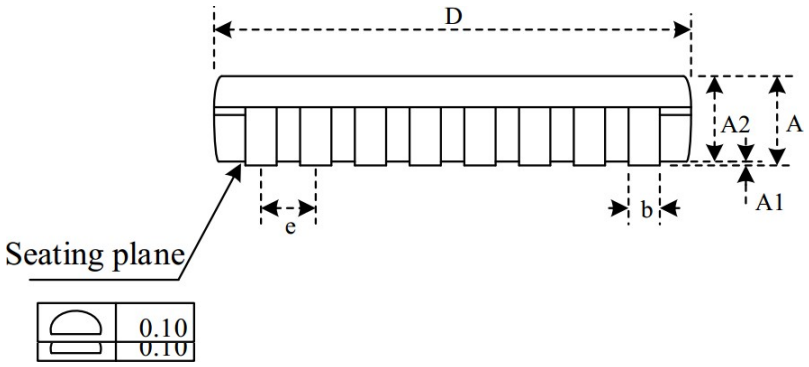
Symbol / Unit		A	A1	A2	b	D	E	E1	e	L	L1	C	θ
mm	Min	-	0.05	0.75	0.35	5.18	7.70	5.18	-	0.50	1.31REF	0.09	0°
	Nom	-	0.10	0.80	0.42	5.28	7.90	5.28	1.27BSC	0.65		-	-
	Max	1.00	0.15	0.85	0.48	5.38	8.10	5.38	-	0.80		0.2	10°
Inch	Min	-	0.002	0.030	0.014	0.204	0.303	0.204	-	0.020	0.052REF	0.004	0°
	Nom	-	0.004	0.031	0.017	0.208	0.311	0.208	0.050BSC	0.026		0	-
	Max	0.04	0.006	0.033	0.019	0.212	0.319	0.212	-	0.031		0.008	10°

标志 / 单位		A	一流的	主动脉第二声	b	D	E	E1	e	L	腰神经 2	C	θ
毫米	福建话	-	0.05	0.75	0.35	5.18	7.70	5.18	-	0.50	1.31 参考	0.09	0
	提名	-	0.10	0.80	0.42	5.28	7.90	5.28	1.27BSC	0.65		-	-
	最大	1.00	0.15	0.85	0.48	5.38	8.10	5.38	-	0.80		0.2	10
英寸	福建话	-	0.002	0.030	0.014	0.204	0.303	0.204	-	0.020	0.052 参考	0.004	0
	提名	-	0.004	0.031	0.017	0.208	0.311	0.208	0.050BSC	0.026		0	-
	最大	0.04	0.006	0.033	0.019	0.212	0.319	0.212	-	0.031		0.008	10

Package SOP16 300MIL

SOP16 300MIL 封装





Dimensions (Inch dimensions are derived from original mm dimensions)

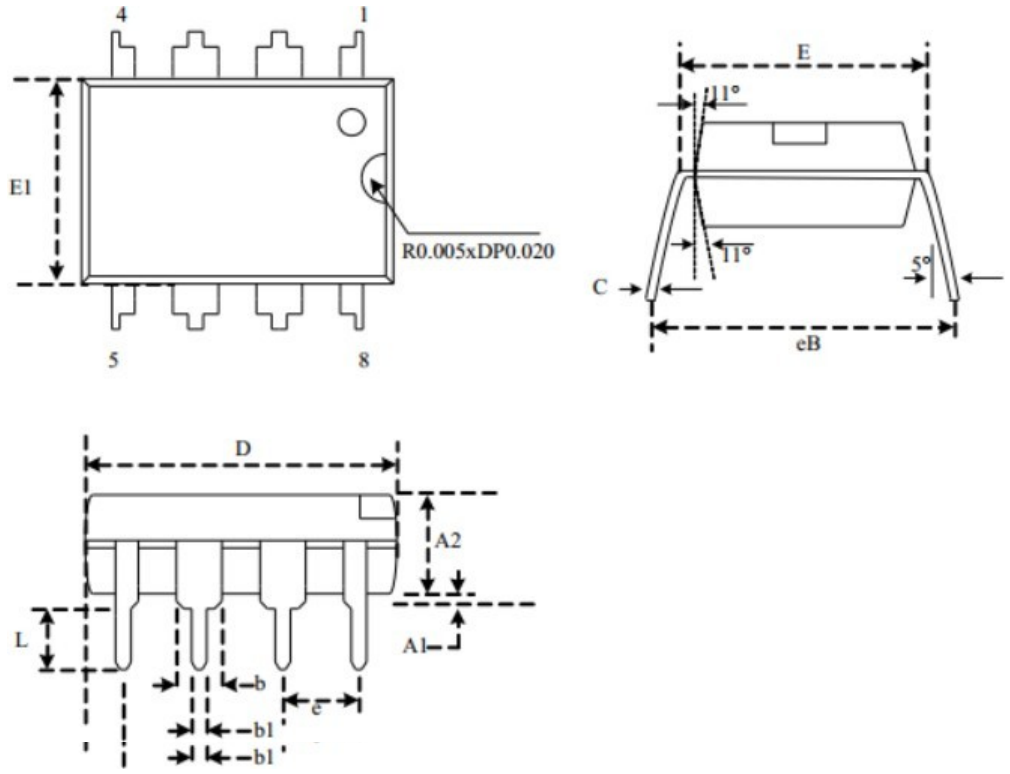
尺寸(英寸尺寸源自原始毫米尺寸)

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27	0.84	1.44	5

	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050	0.033	0.057	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8
标志 单位		A	一流的	主动脉第二声	b	C	D	E	E1	e	L	腰神经 2	θ
毫米	福建话	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	提名	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27	0.84	1.44	5
	最大	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
英寸	福建话	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	提名	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050	0.033	0.057	5
	最大	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8

Package DIP8 300MIL

包装 dip 8 300 毫升



Dimensions (Inch dimensions are derived from original mm dimensions)

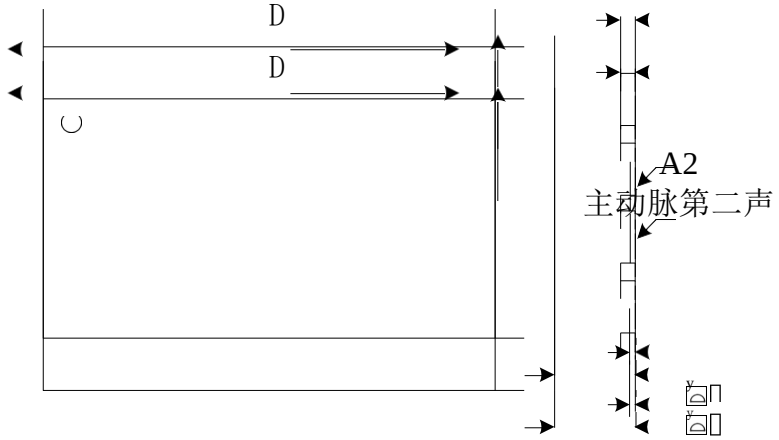
尺寸(英寸尺寸源自原始毫米尺寸)

Symbol / Unit		A1	A2	b	b1	C	D	E	E1	e	eB	L
mm	Min	0.38	3.00	1.27	0.38	0.20	9.05	7.62	6.12		7.62	3.04
	Nom	0.72	3.25	1.46	0.46	0.28	9.32	7.94	6.38	2.54	8.49	3.30
	Max	1.05	3.50	1.65	0.54	0.34	9.59	8.26	6.64		9.35	3.56
Inch	Min	0.015	0.118	0.05	0.015	0.008	0.356	0.300	0.242		0.333	0.12
	Nom	0.028	0.128	0.058	0.018	0.011	0.367	0.313	0.252	0.1	0.345	0.13
	Max	0.041	0.138	0.065	0.021	0.014	0.378	0.326	0.262		0.357	0.14
标志												

单位		一流的	主动脉第二声	b	b1	C	D	E	E1	e	eB	L
毫米	福建话	0.38	3.00	1.27	0.38	0.20	9.05	7.62	6.12		7.62	3.04
	提名	0.72	3.25	1.46	0.46	0.28	9.32	7.94	6.38	2.54	8.49	3.30
	最大	1.05	3.50	1.65	0.54	0.34	9.59	8.26	6.64		9.35	3.56
英寸	福建话	0.015	0.118	0.05	0.015	0.008	0.356	0.300	0.242		0.333	0.12
	提名	0.028	0.128	0.058	0.018	0.011	0.367	0.313	0.252	0.1	0.345	0.13
	最大	0.041	0.138	0.065	0.021	0.014	0.378	0.326	0.262		0.357	0.14

Package WSON 8 (6*5mm)

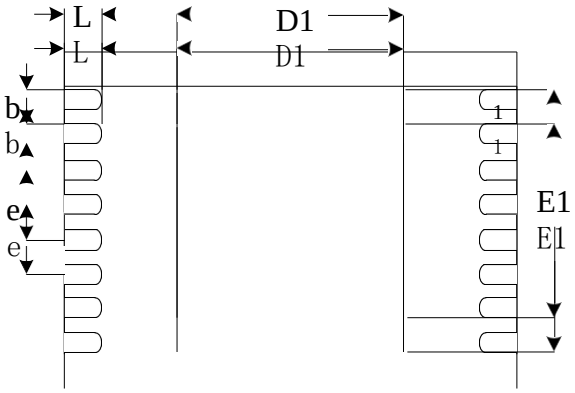
包装 WSON 8(6 * 5 毫米)



Top View
顶视图

一个 A1

Side View
侧景



Bottom View
仰视图

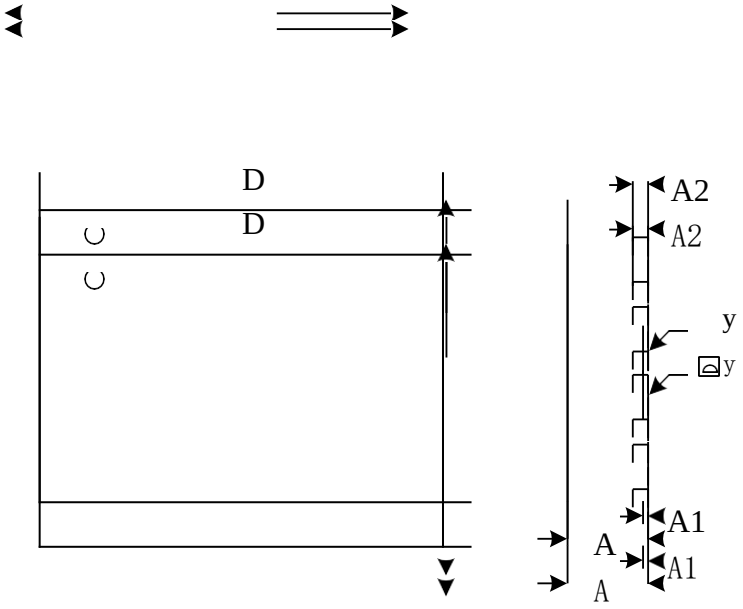
Dimensions (Inch dimensions are derived from original mm dimensions)
尺寸(英寸尺寸源自原始毫米尺寸)

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.70			0.35	5.90	3.30	4.90	3.90		0.00	0.55
	Nom	0.75		0.2REF	0.40	6.00	3.40	5.00	4.00	1.27BSC	0.04	0.60
	Max	0.80	0.05		0.45	6.10	3.50	5.10	4.10		0.08	0.65
Inch	Min	0.028			0.014	0.232	0.130	0.193	0.154		0.000	0.022
	Nom	0.030		0.008	0.016	0.236	0.134	0.197	0.157	0.05BSC	0.001	0.024
	Max	0.032	0.002		0.018	0.240	0.138	0.201	0.161		0.003	0.026
标志 / 单位		A	一流的	主动脉第二声	b	D	D1	E	E1	e	y	L
毫米	福建话	0.70			0.35	5.90	3.30	4.90	3.90		0.00	0.55
	提名	0.75		0.2 参考	0.40	6.00	3.40	5.00	4.00	1.27BSC	0.04	0.60
	最大	0.80	0.05		0.45	6.10	3.50	5.10	4.10		0.08	0.65

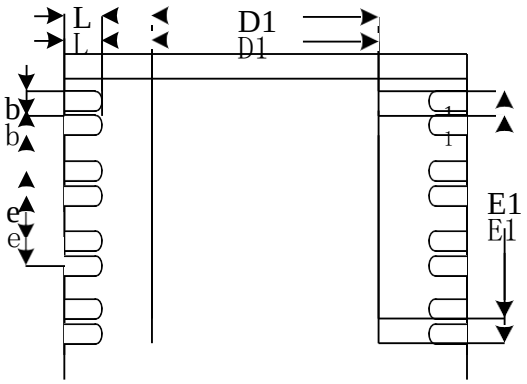
英寸	福建话	0.028			0.014	0.232	0.130	0.193	0.154		0.000	0.022
	提名	0.030		0.008	0.016	0.236	0.134	0.197	0.157	0.05BSC	0.001	0.024
	最大	0.032	0.002		0.018	0.240	0.138	0.201	0.161		0.003	0.026

Package WSON 8 (8*6mm)

包装 WSON 8(8 * 6 毫米)



Top View Side View
俯视图侧视图



Bottom View
仰视图

Dimensions (Inch dimensions are derived from original mm dimensions)

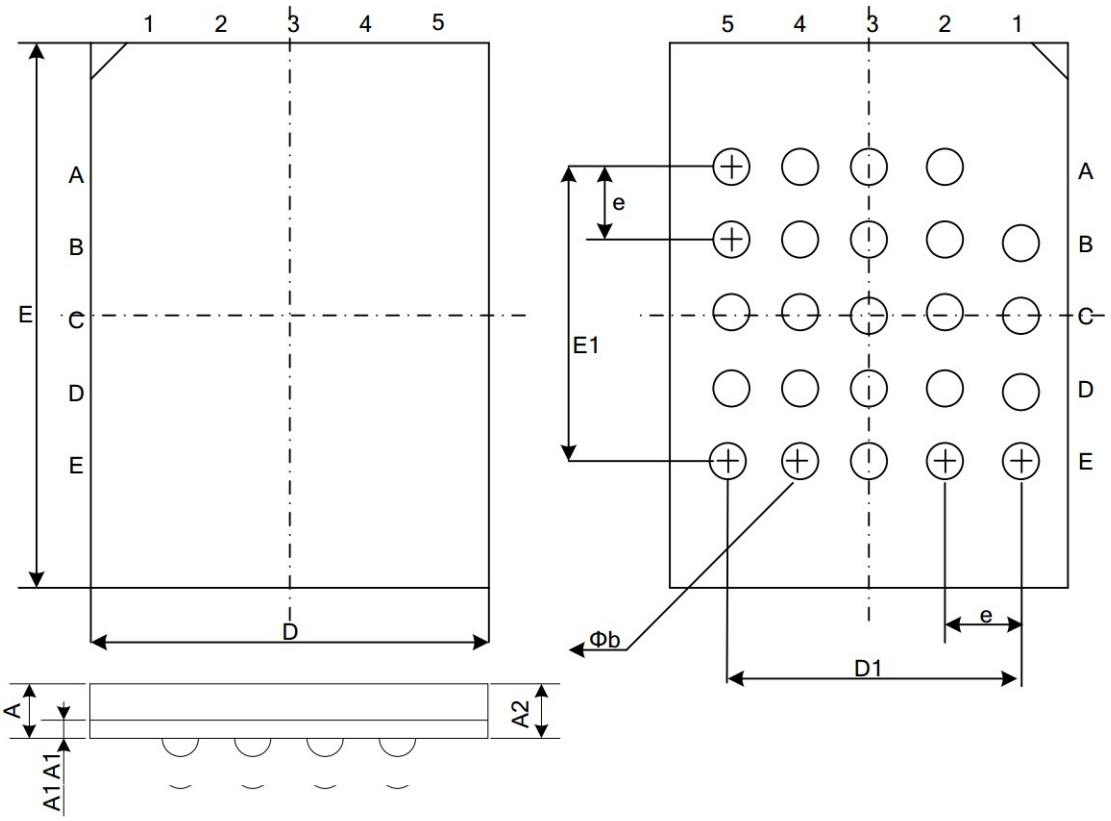
尺寸(英寸尺寸源自原始毫米尺寸)

Symbol / Unit	A	A1	A2	b	D	D1	E	E1	e	y	L

mm	Min	0.70			0.35	7.90	3.25	5.90	4.15		0.00	0.55
	Nom	0.75		0.20BSC	0.40	8.00	3.42	6.00	4.30	1.27BSC	0.04	0.60
	Max	0.80	0.05		0.45	8.10	3.50	6.10	4.40		0.08	0.65
Inch	Min	0.028			0.014	0.311	0.128	0.232	0.163		0.000	0.022
	Nom	0.030		0.008BSC	0.016	0.315	0.135	0.236	0.169	0.050BSC	0.001	0.024
	Max	0.031	0.002		0.018	0.319	0.138	0.240	0.173		0.003	0.027
标志 单位		A	一流的	主动脉第二声	b	D	D1	E	E1	e	y	L
毫米	福建话	0.70			0.35	7.90	3.25	5.90	4.15		0.00	0.55
	提名	0.75		0.20BSC	0.40	8.00	3.42	6.00	4.30	1.27BSC	0.04	0.60
	最大	0.80	0.05		0.45	8.10	3.50	6.10	4.40		0.08	0.65
英寸	福建话	0.028			0.014	0.311	0.128	0.232	0.163		0.000	0.022
	提名	0.030		0.008BSC	0.016	0.315	0.135	0.236	0.169	0.050BSC	0.001	0.024
	最大	0.031	0.002		0.018	0.319	0.138	0.240	0.173		0.003	0.027

Package TFBGA-24BALL (5*5 ball array)

封装 TFBGA-24 球(5*5 球阵列)



Dimensions (Inch dimensions are derived from original mm dimensions)

尺寸(英寸尺寸源自原始毫米尺寸)

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30		0.40	6.00	4.00	8.00	4.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010	0.033	0.014	0.232		0.311		
	Nom		0.012		0.016	0.236	0.157	0.315	0.157	0.039
	Max	0.047	0.014		0.018	0.240		0.319		
标志 / 单位		A	一流的	主动脉第二声	b	D	D1	E	E1	e
	福建话		0.25		0.35	5.90		7.90		
	提名		0.30		0.40	6.00	4.00	8.00	4.00	1.00

毫米	最大	1.20	0.35		0.45	6.10		8.10		
英寸	福建话		0.010	0.033	0.014	0.232		0.311		
	提名		0.012		0.016	0.236	0.157	0.315	0.157	0.039
	最大	0.047	0.014		0.018	0.240		0.319		

41. REVISION HISTORY

42. 修订历史

Version No	Description	Page	Date
1.0	Initial Preliminary Release		2019-07-02
版本号	**描述**	**页**	**日期**
1.0	初始初步发布		2019-07-02