Weekly Project Report

1. Introduction

The brief given to the team for this project was to design a digital system to implement a video game using the Basys3. The board has a VGA output which will connect to a monitor for the signal display. Use the following PMODs from digitlentinc: Pmod KYPD: 16-button Keypad as an input device, Pmod SF3: 32 MB Serial NOR Flash as EEPROM memory to hold user settings, Pmod JSTK2: Two-axis Joystick. It is not necessary to design the actual game. The goal is to design a hardware platform that that would allow different games to be created.

2. Project Scope

The goal for this project is to develop an FPGA based platform which can be used to run different games though it is important to set a base line for which to work from. As a form of project scope we didn't want to jump right into the deep end and design a system that can run a very resource heavy game. Instead we decided this week to pick a game to work towards and from there we could decide if we could implement other games based on the progress towards our initial idea. The game we decided on for the basis of our design was Tetris. It is a simple enough game which still allows for an easy user experience.

The peripherals that will be used for this project are as seen below:

- Pmod KYPD – a 16-button keypad
- Pmod JSTK2 – a two-axis joystick
- Pmod SF3 – 32 MB serial flash memory
- VGA Output – the video output from the FPGA board

3. Design Decisions

The team agreed on five main subsystems:

1. **VGA Display Subsystem**
    - Generates VGA timing (HSYNC, VSYNC)
    - Converts game object/sprite data into pixel colors
    - Reads graphical data from BRAM-based tilemap or sprite memory
2. **Input Subsystem**
    - Keypad scanning and debouncing (Pmod KYPD)
    - Joystick SPI interface (Pmod JSTK2)
    - Button and switch handling
    - Produces clean signals for the Game Core
3. **Flash Memory Subsystem**
    - SPI controller for Pmod SF3
    - Reads/writes small blocks of configuration data
    - Used for high scores, difficulty settings, etc.

4. **Game Core / System Controller**
    - Central logic module
    - Contains game selection state machine
    - Arbitrates between input, video memory, and flash access
    - Defines the internal register/API system games will use
5. **Clock/Reset & Top-Level Integration**
    - Derives 25 MHz pixel clock from the 100 MHz system clock
    - Distributes system reset
    - Connects all subsystems together
    - Manages PMOD and VGA I/O assignments

This structure ensures each module is cleanly separated and testable.

4. Division of Work

Member A — VGA Display + Clock/Reset (Video Lead)

Responsibilities

- Generate the VGA timing signals (HSYNC, VSYNC)
- Implement pixel pipeline and color output
- Design the tilemap/sprite system using BRAM
- Implement BRAM read paths for background and sprites
- Generate 25 MHz pixel clock using MMCM/Clock Wizard
- Ensure video pipeline meets timing requirements
- Document VGA interface and required signal timing

Member B — Input System + Flash Storage (Input/Memory Lead)

Responsibilities

1. **Input**

- Implement keypad row/column scan FSM
- Debounce keypad presses
- Build SPI protocol for Pmod JSTK2
- Parse joystick X/Y positions and button states
- Handle on-board buttons and switches

2. **Flash (Pmod SF3)**

- Build SPI master for flash memory
- Implement read/write sequences
- Provide settings data to Game Core
- Write updated scores/settings to flash

Member C — Game Core + Top-Level Integration (System Lead)

Responsibilities

- Design the central system controller FSM
- Manage system states (RESET → MENU → GAME RUNNING → SAVE SETTINGS)
- Define the internal "API" for future game modules
- Coordinate sprite data updates to the video system
- Communicate with flash controller for load/save
- Connect all modules at the top level (`top.v`)
- Manage all pin assignments and .xdc constraint file

This division of work is still in the works since as a team it works out better if each system can communicate better with in put from each of the other team members.

5. Work Completed

Work Completed This Week

- Read and discussed project brief
- Identified hardware requirements for Basys3 and PMODs
- Drafted top-level block architecture
- Assigned subsystem blocks to each team member
- Reviewed VGA timing specs and SPI protocols
- Outlined communication registers between subsystems
- Created early plan for tilemap use

6. Issues/Questions raised

- Clarification needed on exact electrical interface for Pmod JSTK2 (analog vs digital)
- VGA tilemap memory size needs to be confirmed based on BRAM availability
- Team will need the lecturer's guidance on expectations for flash storage complexity