Weekly Project Report – Week 2

Work Completed This Week (17/Nov/2025 – 24/Nov/2025)

Overall Team Progress

During this week the team transitioned from planning into active development of each subsystem. All members have started implementation and testing of their assigned modules, while also coordinating interface requirements with the rest of the group so that integration can begin in the coming week.

VGA Display & Clock System

Progress Achieved

Successfully generated VGA timing signals (HSYNC, VSYNC) at the correct frequencies.

Implemented a basic colour output pipeline.
The VGA display now successfully shows alternating colours, confirming:

- Pixel clock works correctly
- Timing generator meets the monitor's requirements
- VGA output path is operational

Began drafting memory layout for tilemap-based rendering.

Notes

- The progress provides a functioning video output pathway, allowing the Game Core to eventually draw objects on screen.

Input System (Keypad + Joystick)

Progress Achieved

Completed research into keypad row/column scanning requirements and debouncing approaches.

Designed the keypad scanning FSM structure: 4-column cycling, row sampling, keycode encoding

Developed the first version of the keypad Verilog module, including state sequencing and output decoding.

Created a testbench for keypad simulation and verified key detection logic.

Confirmed pin requirements for the XDC file.

Notes

- Keypad module now provides clean digital outputs suitable for Game Core input.
- Currently focused on finishing input stabilisation and preparing final port definitions for integration.

Game Core & Top-Level Integration

Progress Achieved

Drafted the initial top-level structure (top.v) including placeholder wires and module stubs.

Defined the expected input signals from the input modules.

Started preparing the .xdc constraint file:

- Clock pin
- VGA pins
- Partial PMOD assignments
- Created draft memory map for Game Core <→ VGA communication.

Notes

- Full integration cannot be completed until the port lists for the modules are finalised, but the framework is prepared so integration later will be straightforward.