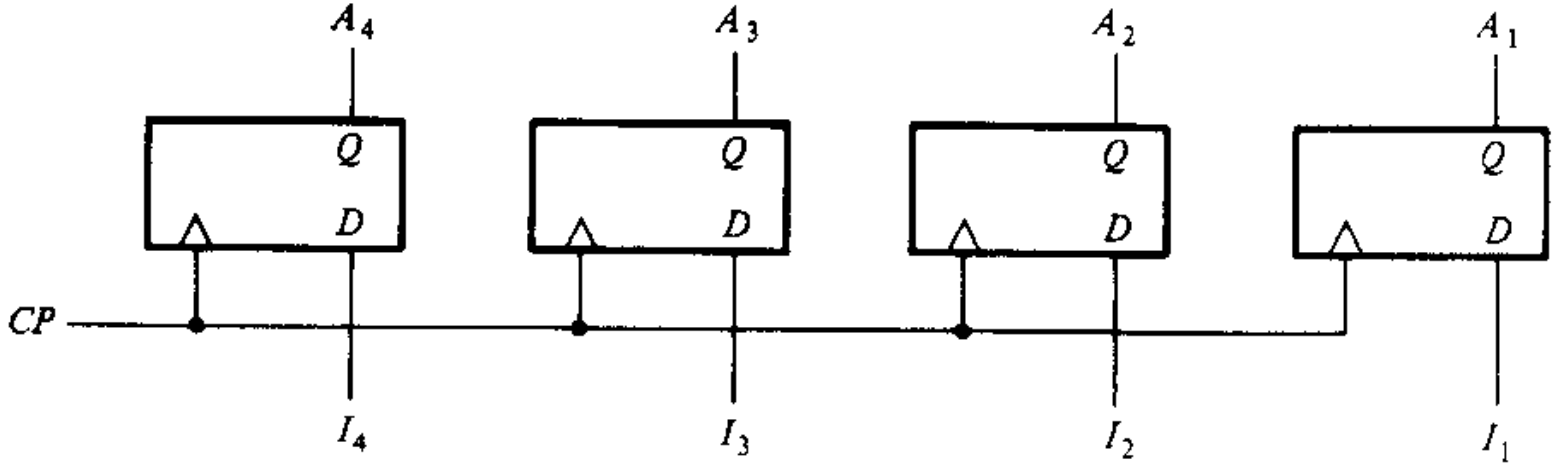
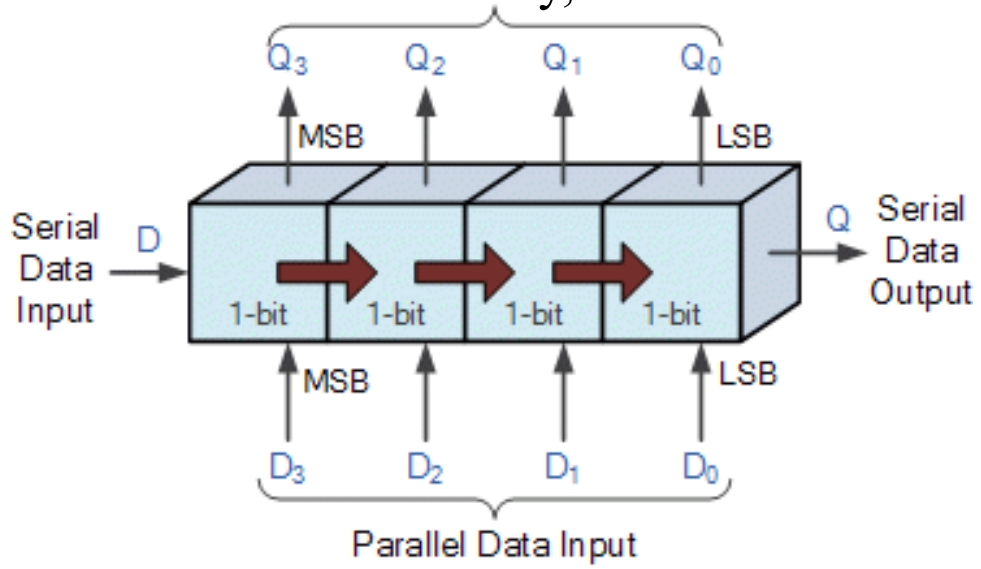
Registers

- A *register* is a group of flip-flops, each one of which shares a common clock and is capable of storing one bit of information.
- An *n* -bit register consists of a group of *n* flip-flops capable of storing *n* bits of binary information. In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks.
- In its broadest definition, a register consists of a group of flip-flops together with gates that affect their operation.
- The flip-flops hold the binary information, and the gates determine how the information is transferred into the register.



Shift Registers

- The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data
- In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, "shifting in" the data present at its input and 'shifting out' the last bit in the array, at each transition of the clock input.



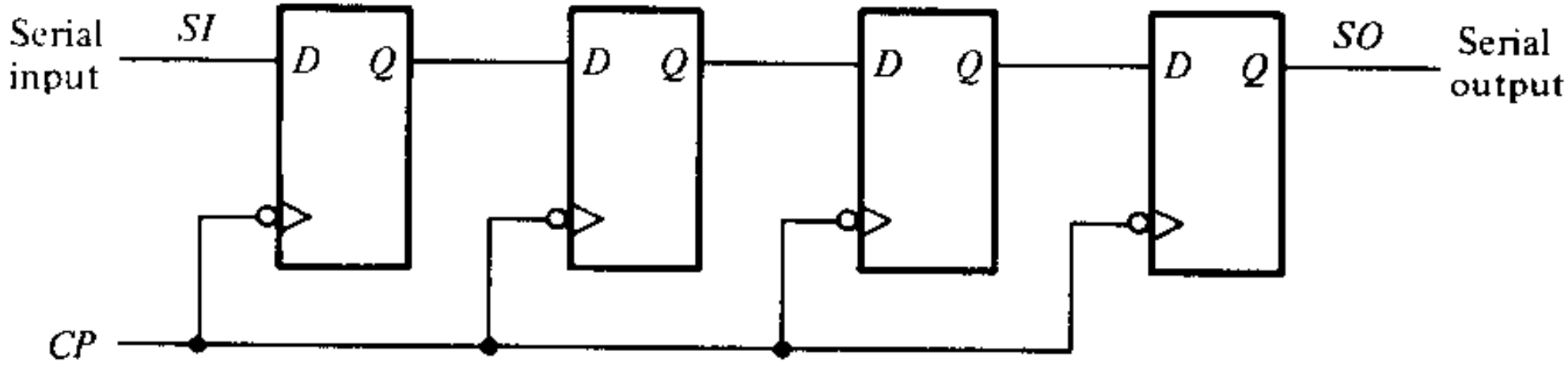
Shift Registers

- The register is capable of shifting bits either towards right hand side or towards left hand side in a shift register.
- An ‘N’ bit shift register contains ‘N’ flip-flops.

- Following are the four types of shift registers based on applying inputs and accessing of outputs.

    - Serial In − Serial Out shift register (SISO)
    - Serial In − Parallel Out shift register (SIPO)
    - Parallel In − Serial Out shift register (PISO)
    - Parallel In − Parallel Out shift register (PIPO)

Shift Register



- A register capable of shifting in one direction only is a *unidirectional* shift register.
- One that can shift in both directions is a *bidirectional* shift register.
- If the register has both shifts and parallel-load capabilities, it is referred to as a *universal shift register.*

Shift Register Counters

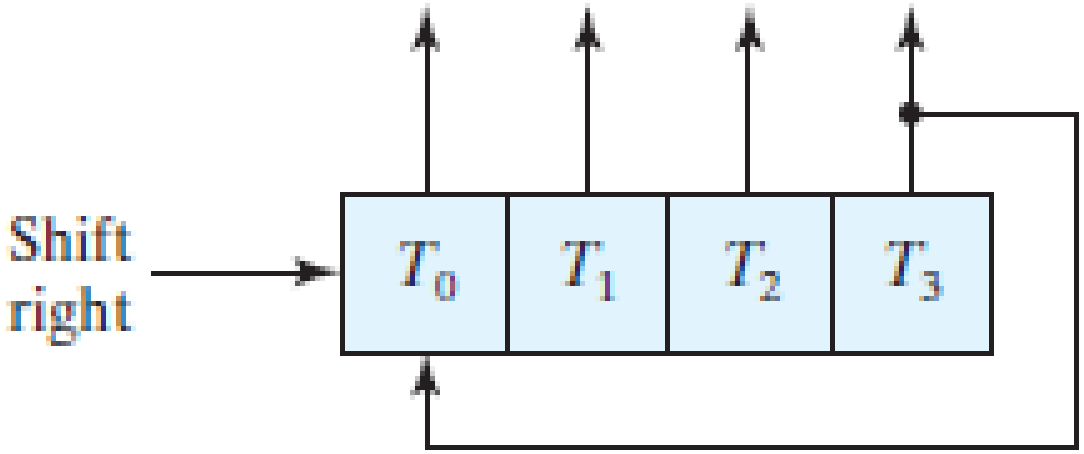
- A Shift Register Counter is basically a Shift Register with the serial output connected back to the serial input in order to produce **Special Sequences.**

- These devices are often classified as counters, because they exhibit a specified sequence of states.

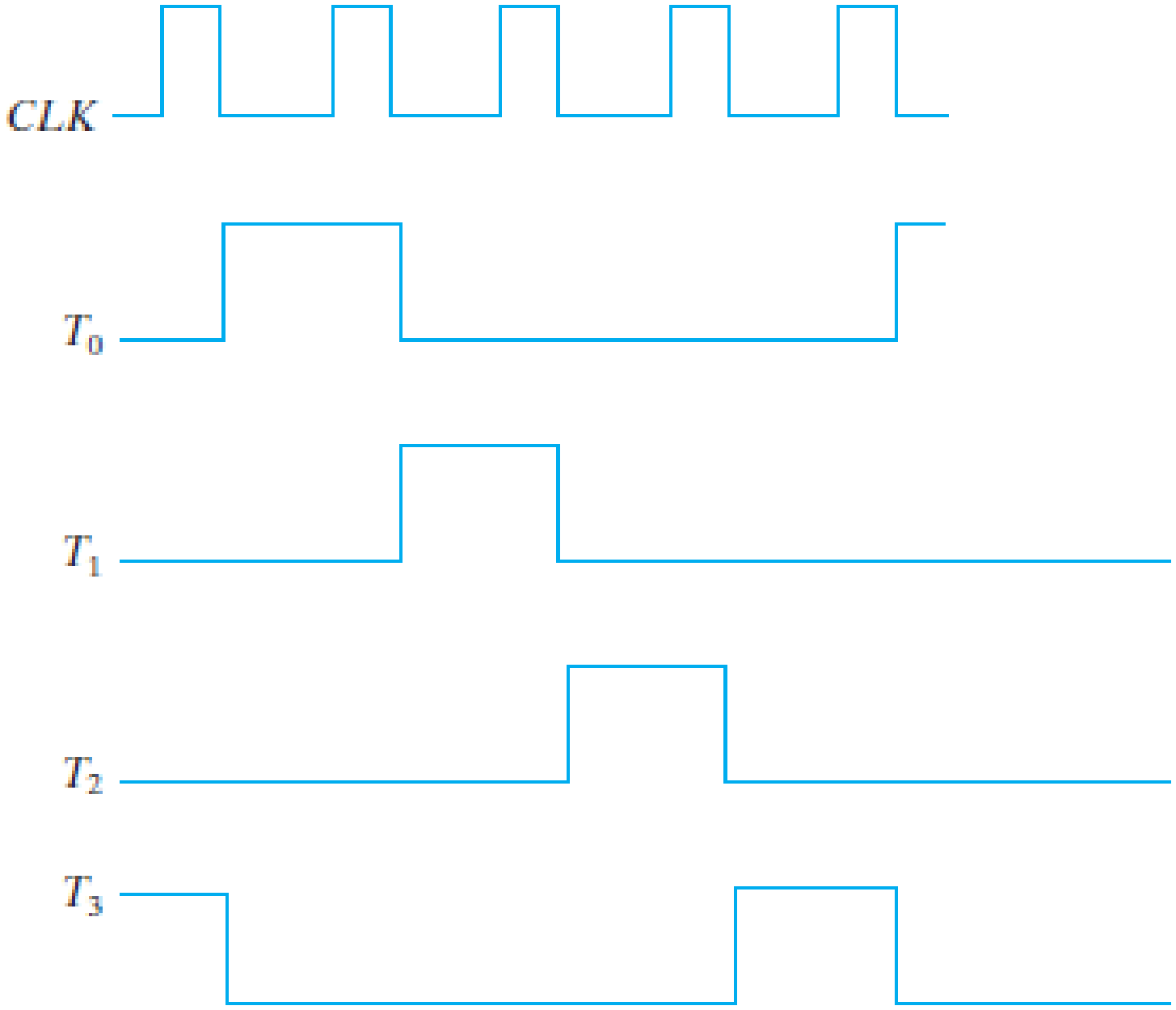
- Two of the most common types of Shift Register Counters are
  - Twisted Ring Counter
  - Ring Counter

Ring Counter

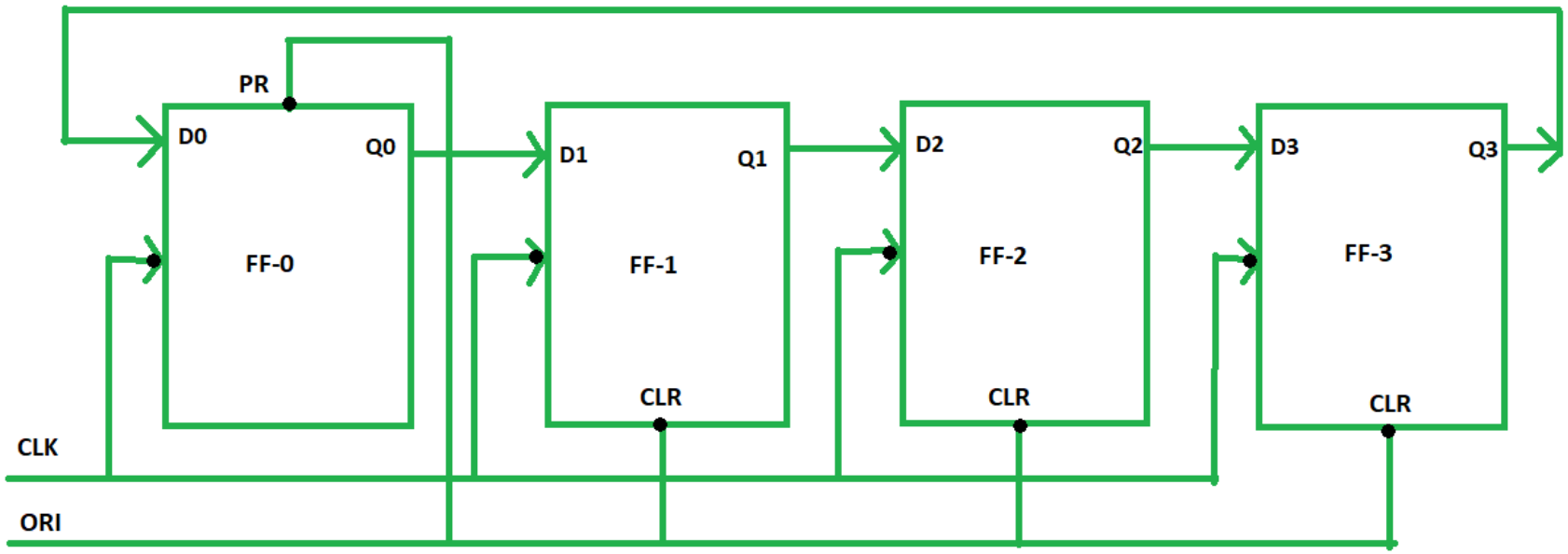
Timing signals that control the sequence of operations in a digital system can be generated by a shift register or by a counter with a decoder. A *ring counter* is a circular shift register with only one flip-flop being set at any particular time; all others are cleared. The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals.



This Figure shows a four-bit shift register connected as a ring counter. The initial value of the register is 1000 which produces the variable T0. The single bit is shifted right with every clock pulse and circulates back from T3 to T0. Each flip-flop is in the 1 state once every four clock cycles and produces one of the four timing signals Each output becomes a 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock cycle.


CLK
T_0
T_1
T_2
T_3

Ring Counter

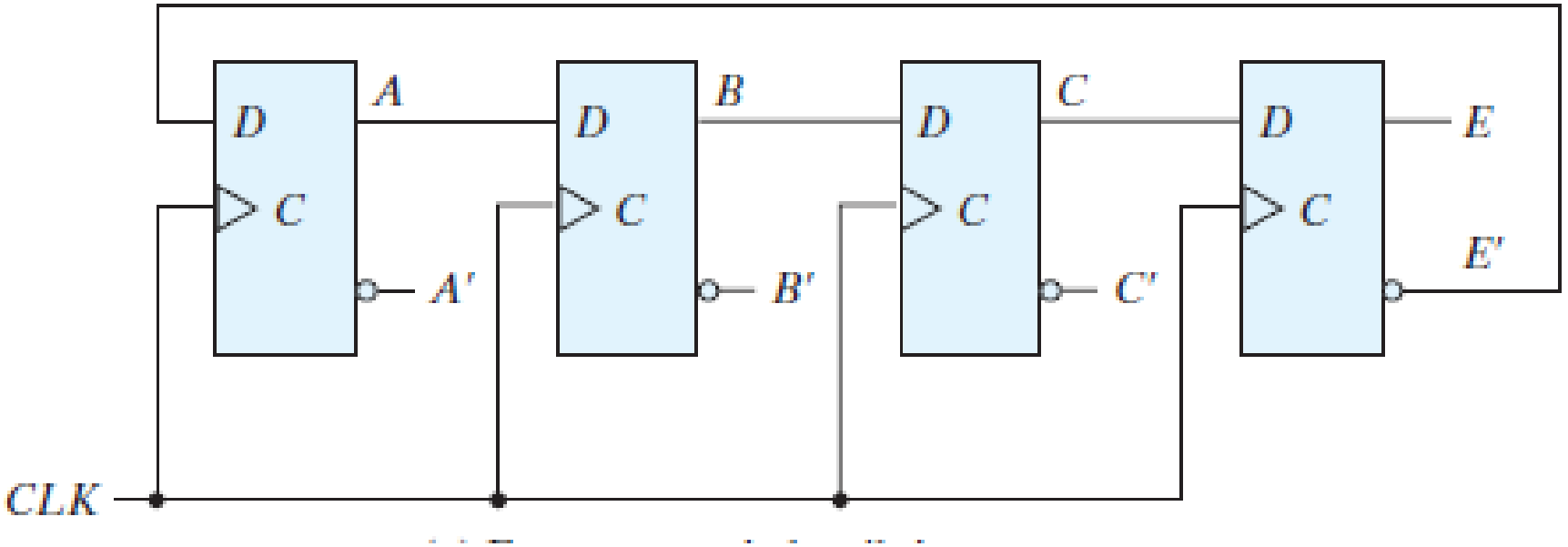


Ring Counter

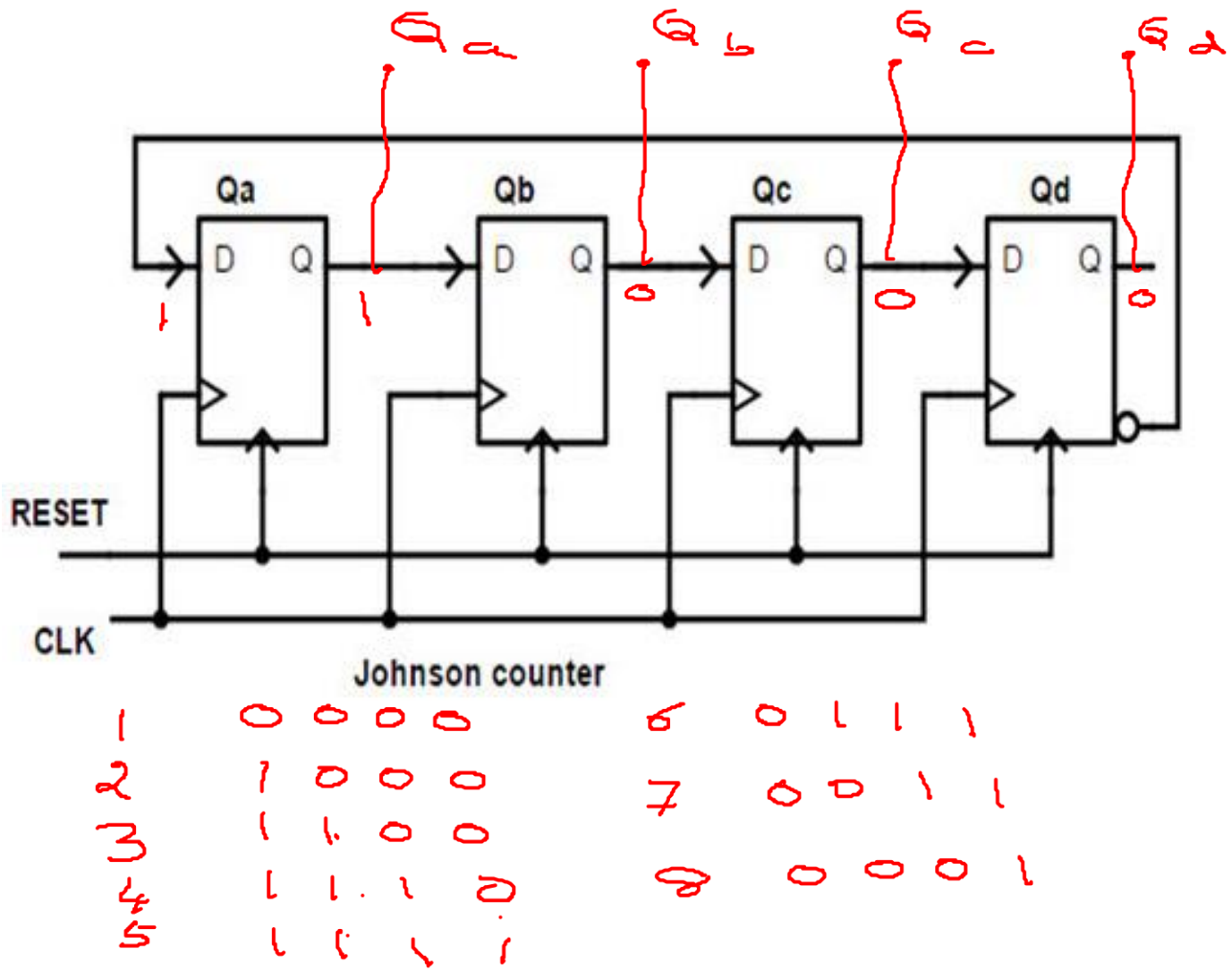
Q_0	Q_1	Q_2	Q_3
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

Johnson Counter

A Johnson Counter or a switch-tail ring counter is a circular shift register with the complemented output of the last flip-flop connected to the input of the first flip-flop.



Johnson Counter (Twisted Ring Counter, Moebius Counter)



Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Sequence number	Flip-flop outputs				AND gate required for output
	A	B	C	E	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

Starting from a cleared state, the Johnson counter goes through a sequence of eight states. In general, a k -bit Johnson counter will go through a sequence of $2k$ states. Starting from all 0's, each shift operation inserts 1's from the left until the register is filled with all 1's. In the next sequences, 0's are inserted from the left until the register is again filled with all 0's.

A k-bit Johnson counter with $2k$ decoding gates to provide $2k$ timing signals. The eight AND gates listed in the table, when connected to the circuit, will complete the construction of the Johnson counter. Since each gate is enabled during one particular state sequence, the outputs of the gates generate eight timing signals in succession.

The decoding of a k -bit Johnson counter to obtain $2k$ timing signals follows a regular pattern. The all-0's state is decoded by taking the complement of the two extreme flip-flop outputs. The all-1's state is decoded by taking the normal outputs of the two extreme flip-flops. All other states are decoded from an adjacent 1, 0 or 0, 1 pattern in the sequence.

For example, sequence 7 has an adjacent 0, 1 pattern in flip-flops B and C . The decoded output is then obtained by taking the complement of B and the normal output of C, or $B'C$.