

# Question Paper

Exam Date & Time: 25-Sep-2024 (10:45 AM - 12:15 PM)



## MANIPAL ACADEMY OF HIGHER EDUCATION

Department of Information and Communication Technology  
Mid Term Examination

### DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2123]

Marks: 30

Duration: 90 mins.

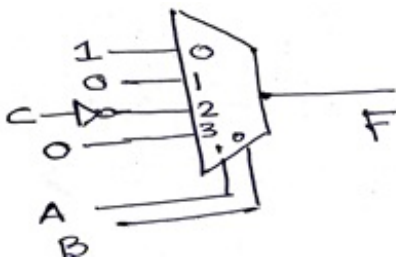
A

Answer all the questions.

Section Duration: 20 mins

Select the correct answer for the following questions

- 1) The following circuit realizes the function  $F(A,B,C) = \underline{\hspace{2cm}}$ . (0.5)



[m0+m2+m7](#) [M0.M2.M7](#) [m1+m2+m6+m7](#) [m0+m1+m4](#)

Correct option is: 4

- 2) The number of product terms in the minimized sum-of-product expression obtained through the following K-map is (where "d" denotes don't care states). (0.5)

A \ B	CD			
	00	01	11	10
00	1	0	0	1
01	0	d	0	0
11	0	0	d	1
10	1	0	0	1

[2](#) [3](#) [4](#) [5](#)

Correct option is: 1

- 3) Which of the following statement is FALSE ? (0.5)

[1. A 4-bit parallel adder can be constructed using two 2-bit parallel adders.](#) [2. A 4-bit parallel adder can be constructed using two 2-bit parallel adders.](#) [3. A 4-bit parallel adder can be constructed using two 2-bit parallel adders.](#) [4. A 4-bit parallel adder can be constructed using two 2-bit parallel adders.](#)

[Excess-3 is non-weighted code](#)

[Gray code is unit distance code](#)

[2 4 2 1 is a weighted code](#)

[8 4 2 1 is self complimenting BCD code](#)

**Correct option is: 4**

- 4) Convert binary number into Gray code: 100101. (0.5)

[101101](#) [001110](#) [110111](#) [111001](#)

**Correct option is: 3**

- 5) A Binary multiplier is designed to multiply two numbers:  $(B)_{16}$  and  $(101)_2$ . What is the minimum required number of 4-bit adders to perform the multiplication? (0.5)

[3](#) [2](#) [4](#) [1](#)

**Correct option is: 2**

- 6) 8 bit Carry look ahead adder is \_\_\_\_\_ times faster than 8 bit ripple carry adder. (0.5)

[8](#) [3](#) [6](#) [10](#)

**Correct option is: 1**

- 7) A BCD digit is represented in excess - 3 as 7 (in hexadecimal). What is the excess 3 representation of 9's complement for this BCD digit? (0.5)

[2](#) [8](#) [5](#) [A](#)

**Correct option is: 2**

- 8) The minimum number of Half adders used to realise Full adder if it is realised using only half adders, are: (0.5)

[2](#) [3](#) [4](#) [5](#)

**Correct option is: 2**

- 9) The number of output lines for a decimal to BCD encoder are (0.5)

[9](#) [10](#) [4](#) [15](#)

**Correct option is: 3**

- 10) the output  $(A > B)$  of a 2-bit comparator is logic 1 for \_\_\_\_\_ number of combinations. (0.5)

[6](#) [4](#) [7](#) [5](#)

**Correct option is: 1**

## B

### Answer all the questions.

Answer all the questions. Any missing data can be assumed suitably with proper reasoning.

- 11) Design a full subtractor using minimum number of 4:1 and 2:1 multiplexers. Using this as a block and with minimum 2:1 multiplexers, design a 4-bit magnitude comparator. (4)

- 12) If the functions W, X, Y, and Z are as follows (3)

$$W = R + \bar{P}Q + \bar{R}S$$

$$X = PQ\bar{R}\bar{S} + \bar{P}\bar{Q}R\bar{S} + P\bar{Q}R\bar{S}$$

$$Y = RS + \overline{PR + P\bar{Q} + \bar{P}\bar{Q}}$$

$$Z = R + S + \overline{PQ + \bar{P}\bar{Q}R + P\bar{Q}\bar{S}}$$

Then, apply the K-map method and show that  $W = Z$ .

- 13) Design a code converter using NOR gates only to convert a decimal digit represented in 8 4 2 1 code to a decimal digit represented in 8 4 -2 -1 code. (3)

- 14) Design a 4-bit by 4-bit binary multiplier using 7483 ICs and minimum external gates, detailing partial product generation, carry propagation, and logic gate usage. (3)

- 15) Design a 4-bit decimal adder using 7483 ICs and external NAND gates. (3)

- 16) Design the following combinational circuit using 74138 ICs and minimum external gates. (3)

$$F(A,B,C,D) = \sum_m(1,3,6,7,9,14)$$

- 17) Design a combinational circuit using 7485 IC, 7483 IC and minimum external gates to perform the following: (2)

If  $A > B$ ,  $F = A - B$

Else  $F = A + B$

Where A and B are two 4-bit binary numbers.

- 18) Design a 4 to 2 priority encoder, using basic gates. (2)

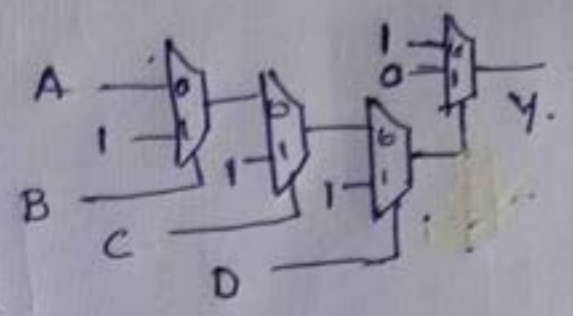
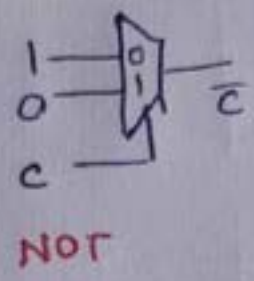
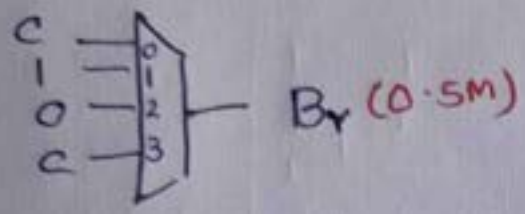
- 19) Design a 1-bit magnitude comparator with cascading inputs. (2)

-----End-----

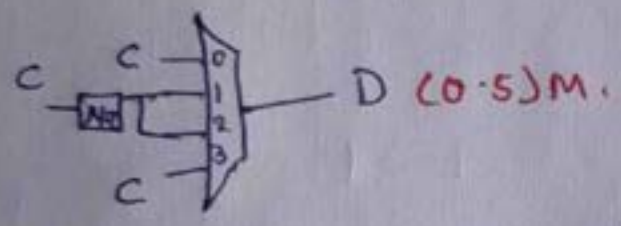
Q1.

# Full Subtractor

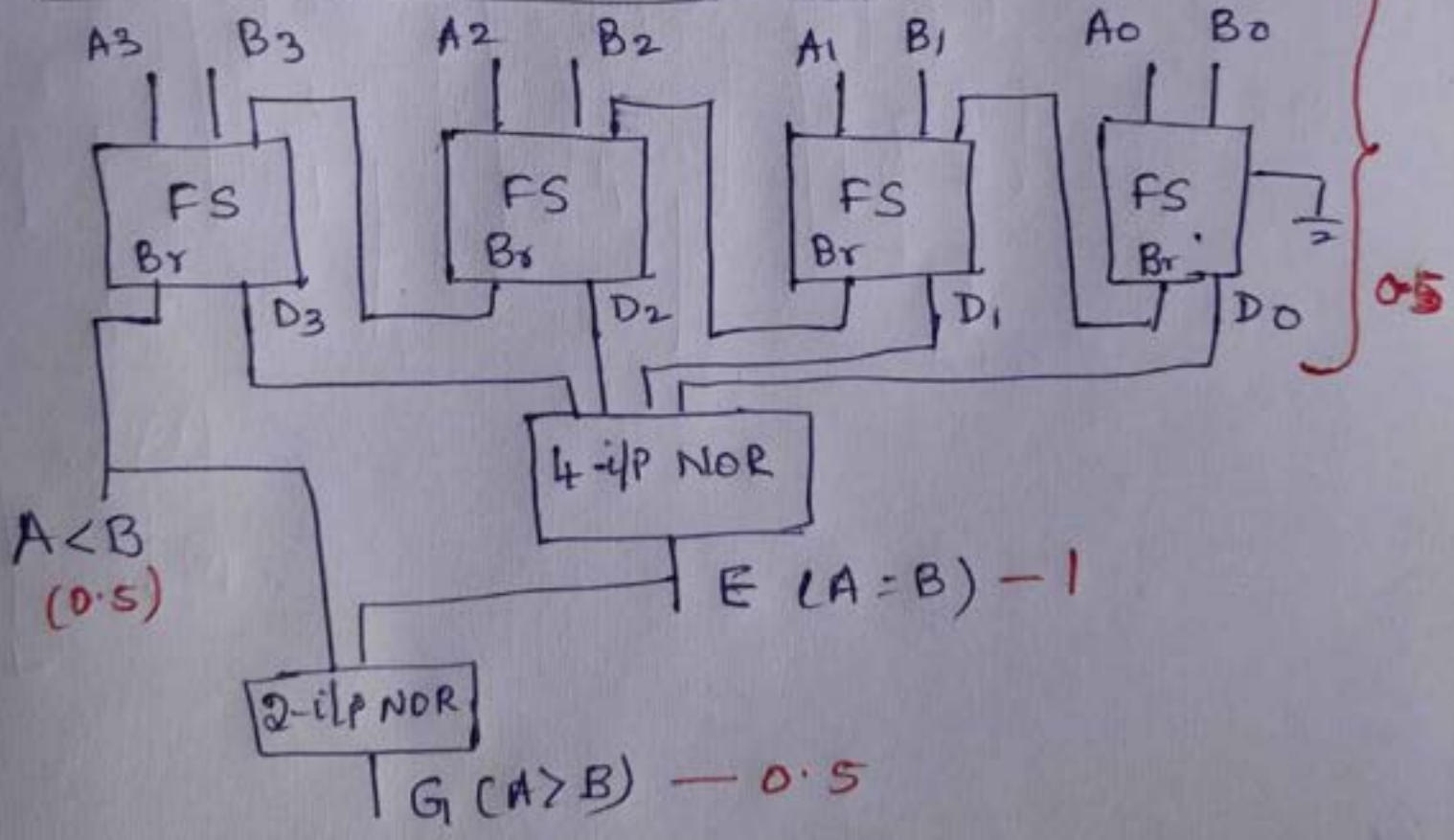
Truth table - 0.5



$$Y = \overline{A+B+C+D}$$
  
NOR



## 4-bit magnitude comparator



Q. Show  $W = Z$

$$W = R + \overline{P}Q + \overline{R}S$$

1 mark

PQ \ R	00	01	11	10
00		1	1	1
01	1	1	1	1
11		1	1	1
10		1	1	1

Simplification of

Z →

$$(Q+S) = X$$

$$(\overline{P} + \overline{Q})(\overline{P} + X)$$

$$\overline{P} + \overline{Q}X$$

$$\overline{P} + \overline{Q}(Q+S)$$

$$Z = R + S + \overline{P}Q + \overline{P}\overline{Q}\overline{R} + \overline{P}\overline{Q}\overline{S}$$

$$= R + S + \overline{P}Q + \overline{P}\overline{Q}\overline{R} + \overline{P}\overline{Q}\overline{S}$$

$$= R + S + (\overline{P} + \overline{Q})(P + Q + R)(\overline{P} + Q + S)$$

$$= R + S + (\overline{P} + \overline{Q})(\overline{P} + Q + S)(P + Q + R)$$

$$= R + S + \overline{P} + \overline{Q}(Q + S) + (P + Q + R)$$

$$= R + S + (\overline{P} + \overline{Q}(Q + S)) + (P + Q + R)$$

$$= R + S + (\overline{P} + \overline{Q} + \overline{Q}S) + (P + Q + R)$$

$$= R + S + (\overline{P} + \overline{Q}S)(P + Q + R)$$



$$= R + S + \bar{P}A + \bar{P}R + \bar{A}PS + \bar{A}RS.$$

PA	RS	00	01	11	10
00			1	1	1
01		1	1	1	1
11			1	1	1
10			1	1	1

2 kmap  
1 mark

RS	PA	00	01	11	10
00			1		
01		1	1	1	1
11		1	1	1	1
10		1	1	1	1

$$(\bar{A} + B)(\bar{A} + C) = (\bar{A} \cdot \bar{A}) + (\bar{A} \cdot C) + (\bar{A} \cdot B) + B \cdot C$$

$$= \bar{A}(\bar{A} + C + B) + B \cdot C$$

$$= \bar{A} + \bar{A}C + \bar{A}B + BC$$

$$= \bar{A}(1 + C) + \bar{A}B + BC$$

$$= \bar{A} + \bar{A}B + BC$$

$$= \bar{A}(1 + B) + BC$$

$$= \bar{A} + BC$$

if they  
check the k-map  
Give 1.5 mark

Ans. Attending  
0.5

$$\bar{P} + \bar{Q}R + \bar{Q}S(\bar{P} + \bar{Q}R)$$

$$\bar{P} + \bar{Q}R$$

	P	Q	R	S	Z
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

0	1	1	1
1	1	1	1
0	1	1	1
0	1	1	1

$$Z = R + S + \bar{P}Q$$

$$W = R + \bar{P}Q + \bar{R}S$$

$$= \cancel{R} + \bar{R}S + \bar{P}Q$$

$$= \underline{\underline{R + S + \bar{P}Q}}$$



$$Z = R + S + \overline{PQ} + \overline{PQR} + \overline{PQS}$$

$$\overline{PQ} + \overline{PQR} + \overline{PQS} = \overline{PQ} \cdot \overline{PQR} \cdot \overline{PQS}$$

$$= \overline{PQ} (P+Q+R) (\overline{P}+Q+S)$$

$$= (\overline{PQ}) (P+Q+R) (\overline{P}+Q+S)$$

$$= (\overline{PQ} + \overline{P}R + P\overline{Q} + \overline{Q}R) (\overline{P}+Q+S)$$

$$= \overline{PQ} + \overline{P}Q + \overline{P}QS + \overline{P}R + \overline{P}RQ + \overline{P}RS + P\overline{Q}S + \overline{Q}PR + QRS$$

$$= \overline{PQ}(1+S) + \overline{P}R(1+Q) + \overline{P}RS + P\overline{Q}S + \overline{Q}RS$$

$$= \overline{PQ} + \overline{P}R + \overline{P}RS + \overline{Q}S$$

$$= \overline{PQ} + \overline{P}R + \overline{Q}S$$

~~$R+S$~~  from eqn.

~~$PQ$~~

$$Z = \overline{PQ} + \overline{P}R + \overline{Q}S + R + S$$

$$= \overline{PQ} + R + S$$

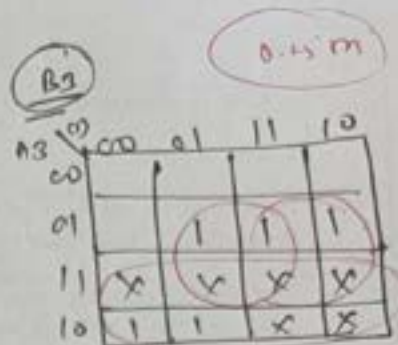
$$\begin{aligned} W &= R + \overline{PQ} + \overline{RS} \\ &= R + \overline{RS} + \overline{PQ} \\ &= R + S + \overline{PQ} \end{aligned}$$

1+0=1  
0+1=1

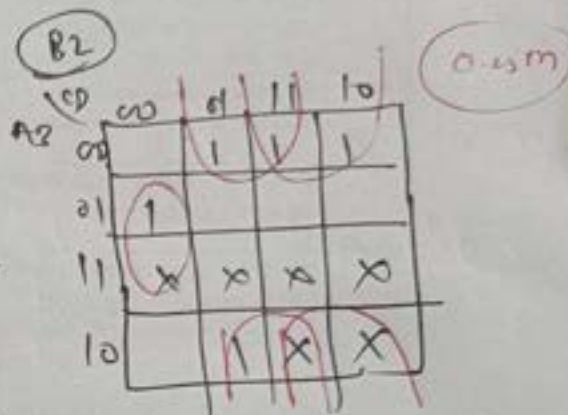


Q.13 scheme (1 mark)

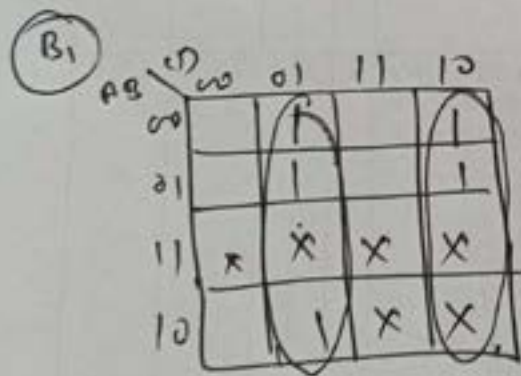
	8	4	2	1		8	4	2	1
	A	B	C	D		B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>
0	0	0	0	0		0	0	0	0
1	0	0	0	1		0	1	1	1
2	0	0	1	0		0	1	1	0
3	0	0	1	1		0	1	0	1
4	0	1	0	0		0	1	0	0
5	0	1	0	1		1	0	1	1
6	0	1	1	0		1	0	1	0
7	0	1	1	1		1	0	0	1
8	1	0	0	0		1	0	0	0
9	1	0	0	1		1	1	1	1
10	1	0	1	0		x	x	x	x
11	1	0	1	1		x	x	x	x
12	1	1	0	0		x	x	x	x
13	1	1	0	1		x	x	x	x
14	1	1	1	0		x	x	x	x
15	1	1	1	1		x	x	x	x



$$B_3 = A + BD + BC$$

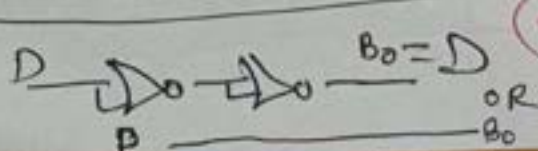
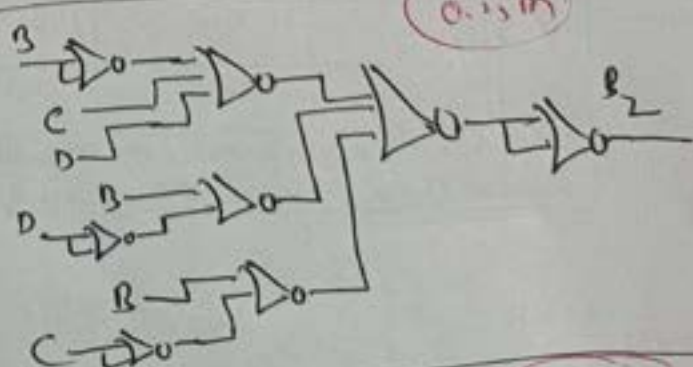
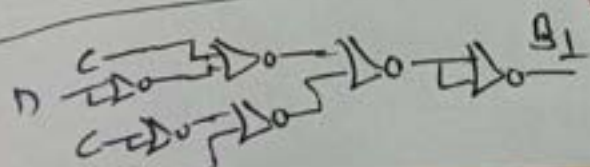
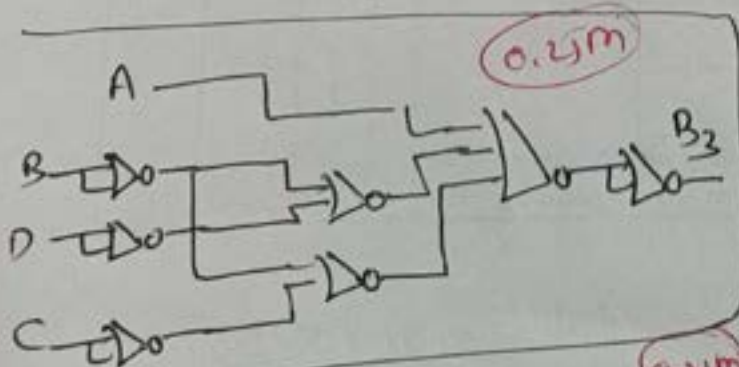


$$B_2 = B\bar{C}\bar{D} + \bar{D}D + \bar{B}C$$



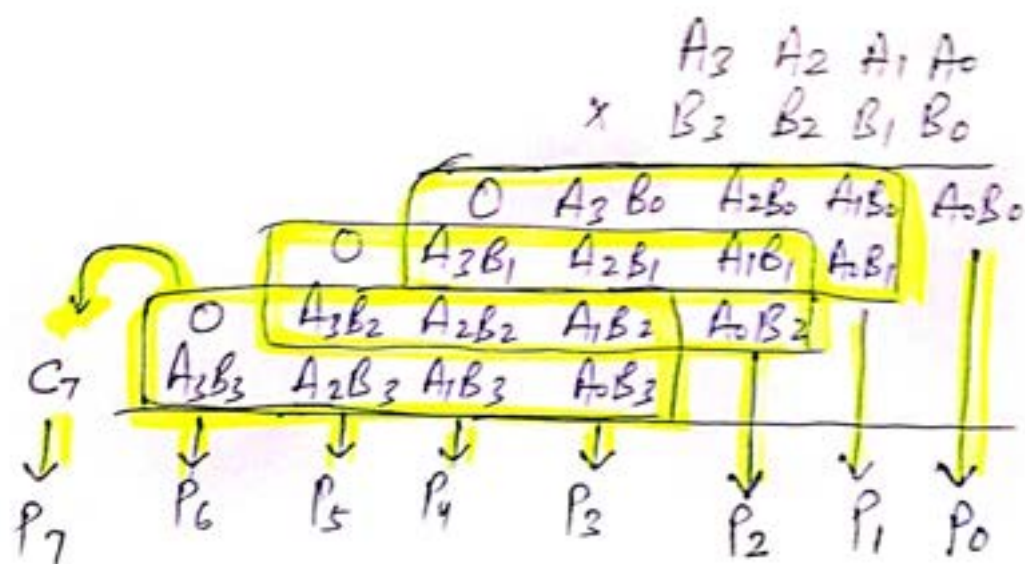
$$B_1 = \bar{C}D + C\bar{D}$$

$$B_0 = D$$

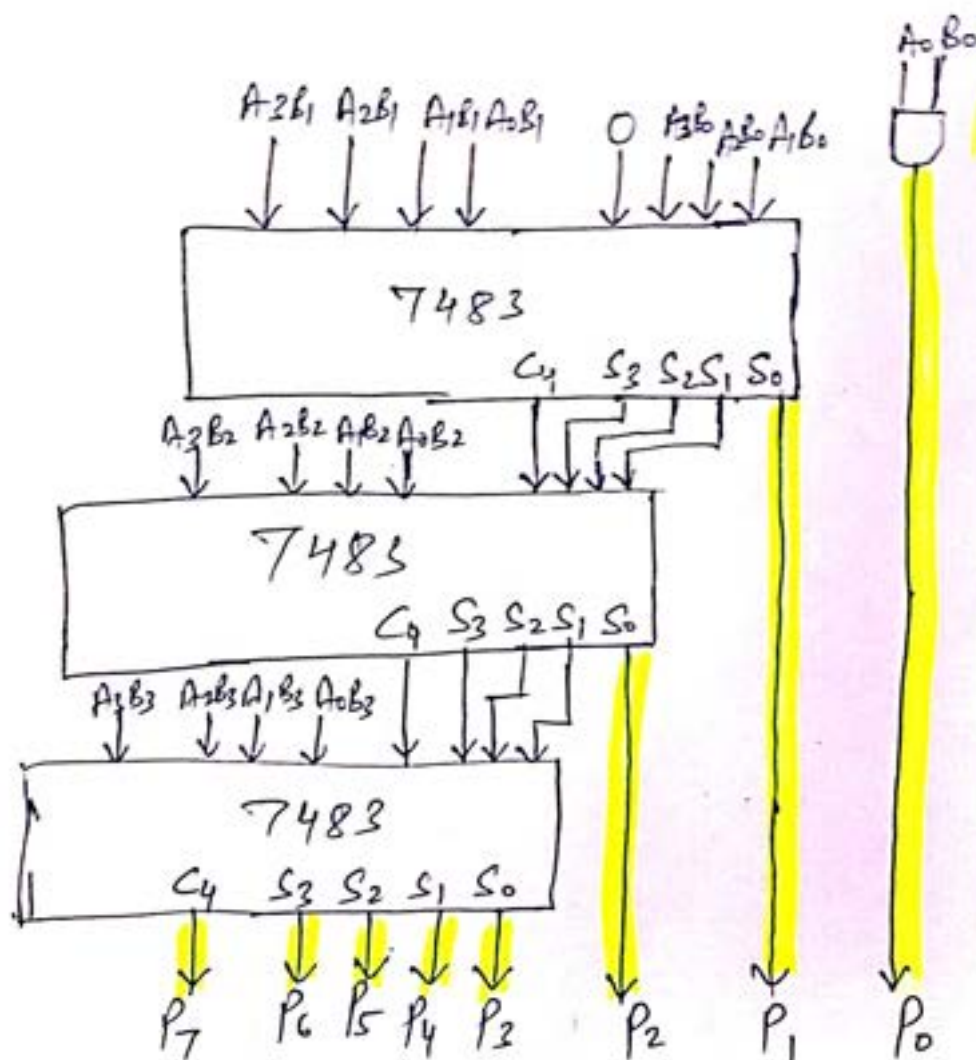


Ques

4x4 Bit Multiplier

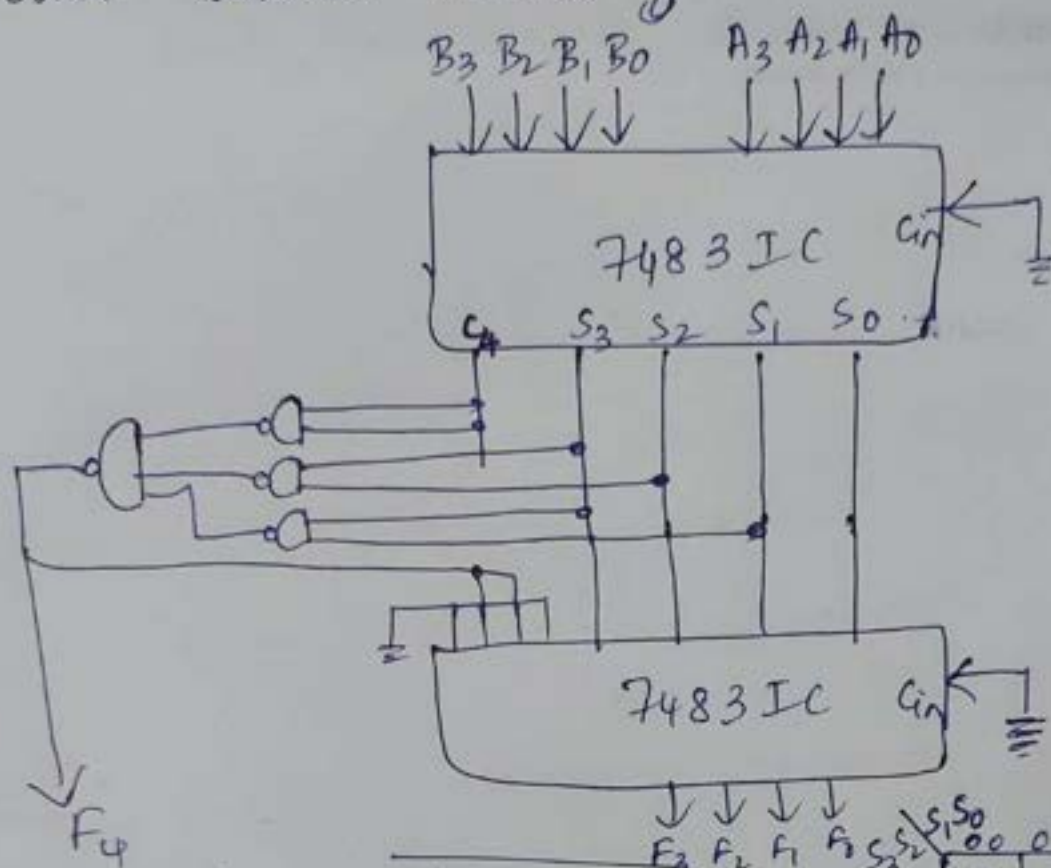


1.5 Marks



1.5 Marks

⑮. Design a 4-bit decimal adder using 7483 IC and external NAND gates.



$$Y = C_4 + S_3 S_2 + S_3 S_1$$

$$= \overline{C_4} \cdot \overline{S_3} S_2 \cdot \overline{S_3} S_1$$

	$S_1 S_0$	00	01	11	10
00	0	0	0	0	0
01	0	0	0	0	0
11	1	1	1	1	1
10	0	0	1	1	1

Equation: - 1 Mark.

1<sup>st</sup> Addition: -  $\frac{1}{2}$  Mark

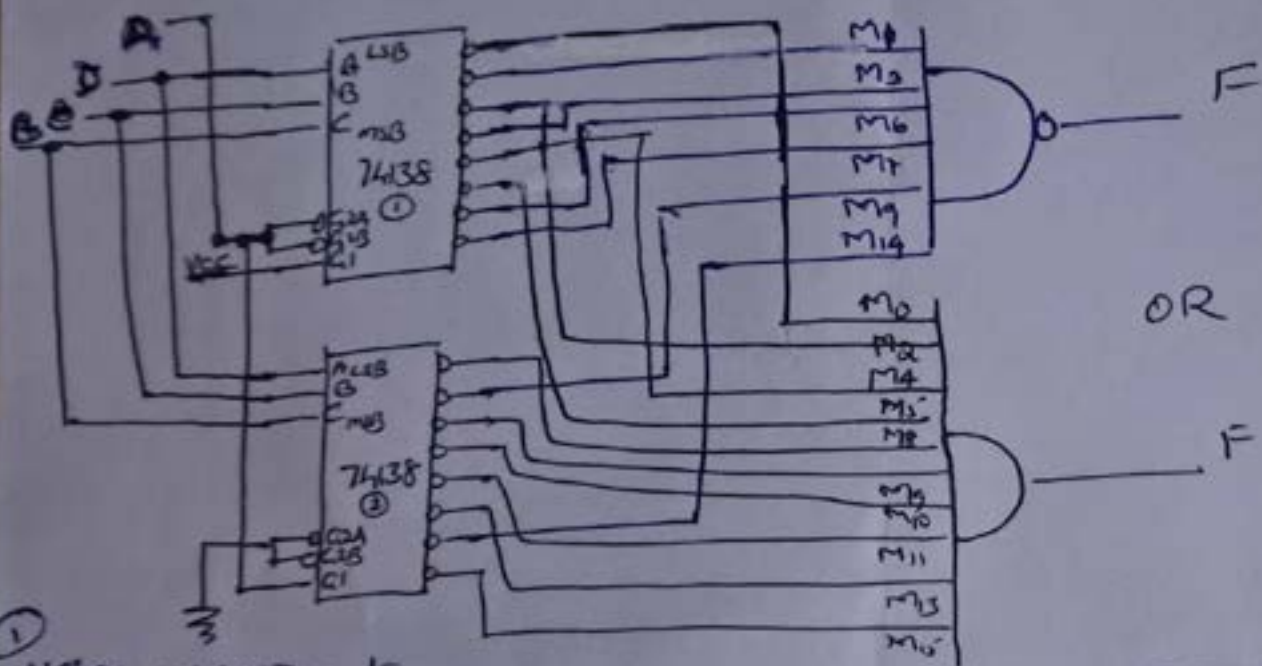
ckt for Y: -  $\frac{1}{2}$  Mark.

2<sup>nd</sup> Addition: -  $\frac{1}{2}$  Mark.

Final carry: -  $\frac{1}{2}$  Mark.



$$F = \sum_m (ABCD) \quad 1, 3, 6, 7, 9, 14 = \prod_M 0, 2, 4, 5, 8, 10, 11, 12, 13, 15$$



①

using NAND gate

$$F = m_1 + m_3 + m_6 + m_7 + m_9 + m_{14} = \overline{\overline{m_1} \cdot \overline{m_3} \cdot \overline{m_6} \cdot \overline{m_7} \cdot \overline{m_9} \cdot \overline{m_{14}}} \\ = \overline{M_1 \cdot M_3 \cdot M_6 \cdot M_7 \cdot M_9 \cdot M_{14}}$$

② using AND gate

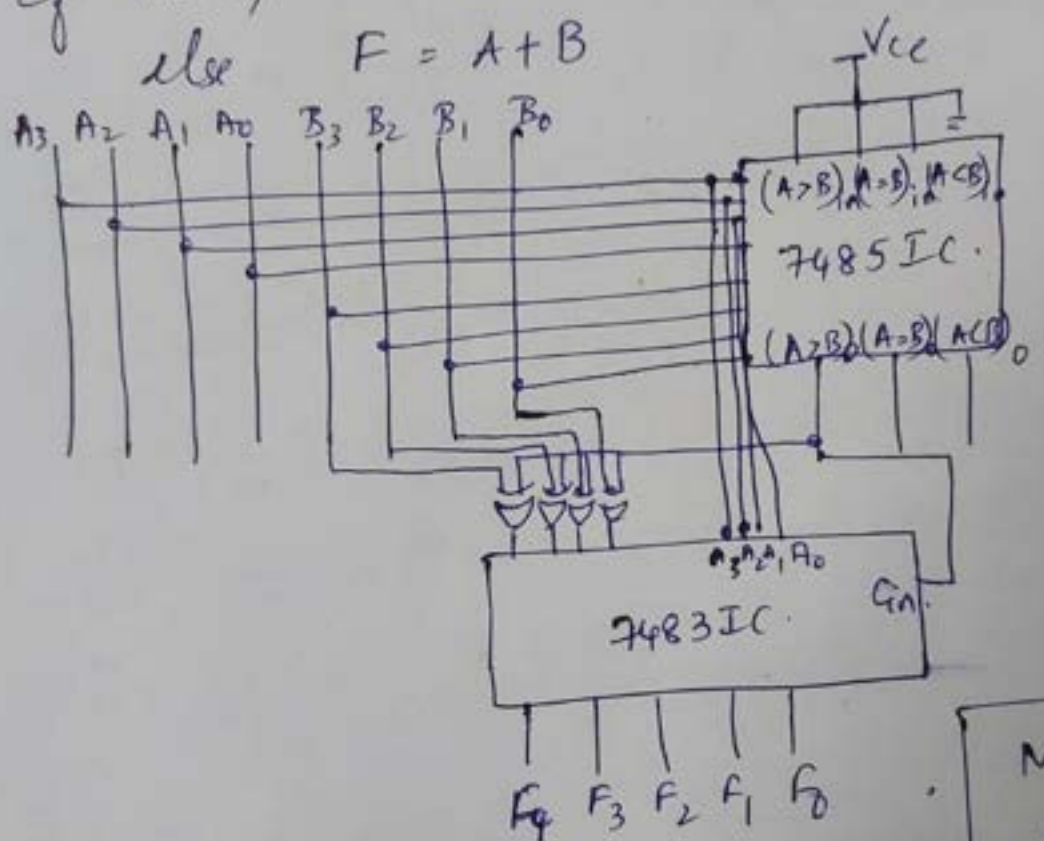
$$F = M_0 \cdot M_2 \cdot M_4 \cdot M_5 \cdot M_8 \cdot M_{10} \cdot M_{11} \cdot M_{12} \cdot M_{13} \cdot M_{15}$$



(A)

Design a Combinational Circuit using 7485 IC, 7483 IC & min ent gates to perform.

If  $A > B$ ,  $F = A - B$ .  $A$  &  $B$  are 4-bit numbers.  
else  $F = A + B$



Mag Comp  $\Rightarrow \frac{1}{2}$  Mark  
 ADDER  $\Rightarrow \frac{1}{2}$  Mark.  
 XOR  $\Rightarrow \frac{1}{2}$  Mark.  
 Mag initial cond }  $\frac{1}{2}$  Mark.  
 Cin

Q.18 4:2 priority encoder

9.9

$D_3$	$D_2$	$D_1$	$D_0$	A	B	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

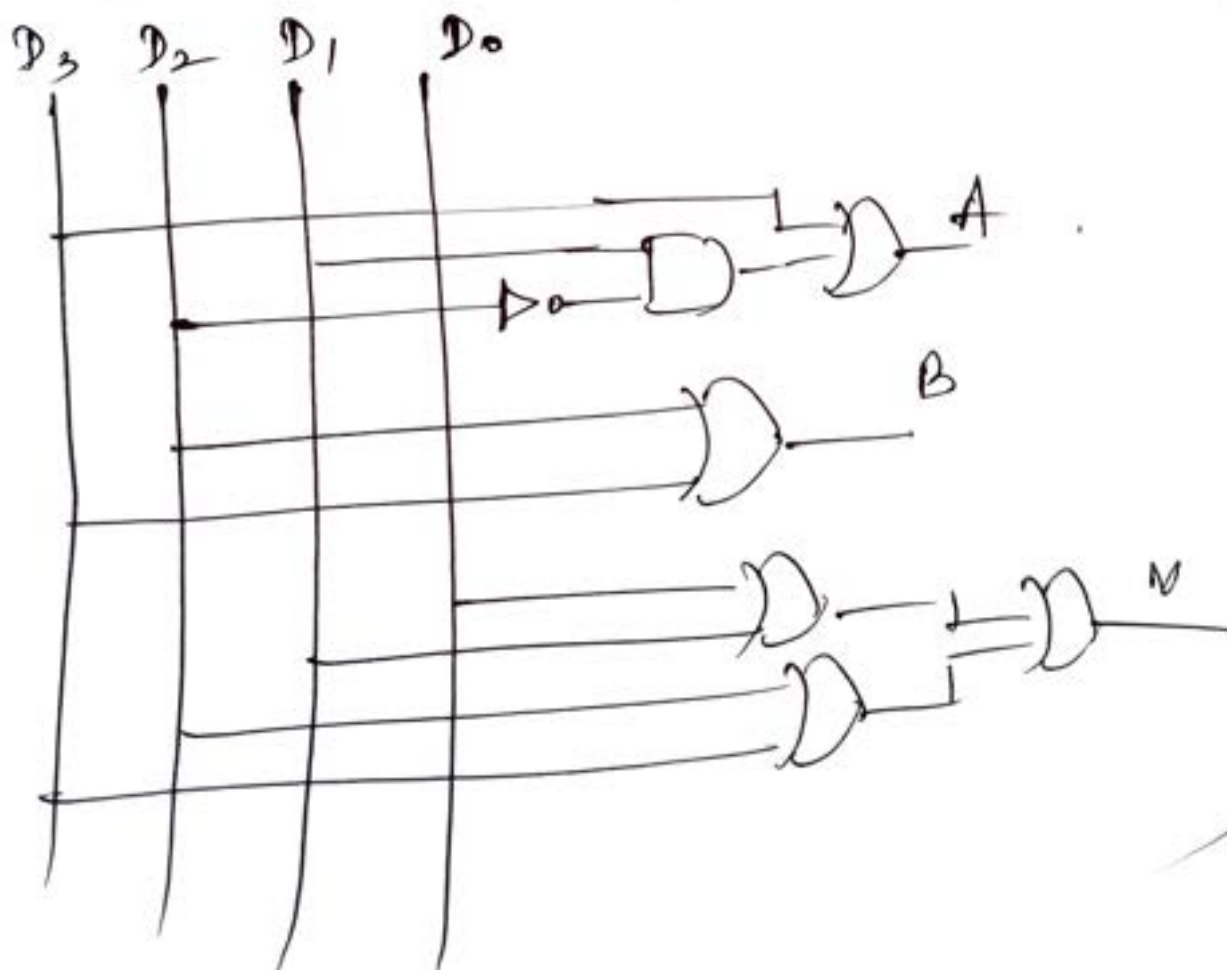
→ 1 mark

$$A = D_3 + D_1 D_2'$$

$$B = D_2 + D_3$$

$$V = D_0 + D_1 + D_2 + D_3$$

1 mark



19. 1-bit Mag Comp with Cascading inputs.

A	B	(A > B)	(A = B)	(A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$$(A > B) = A \bar{B}$$

$$(A < B) = \bar{A} B$$

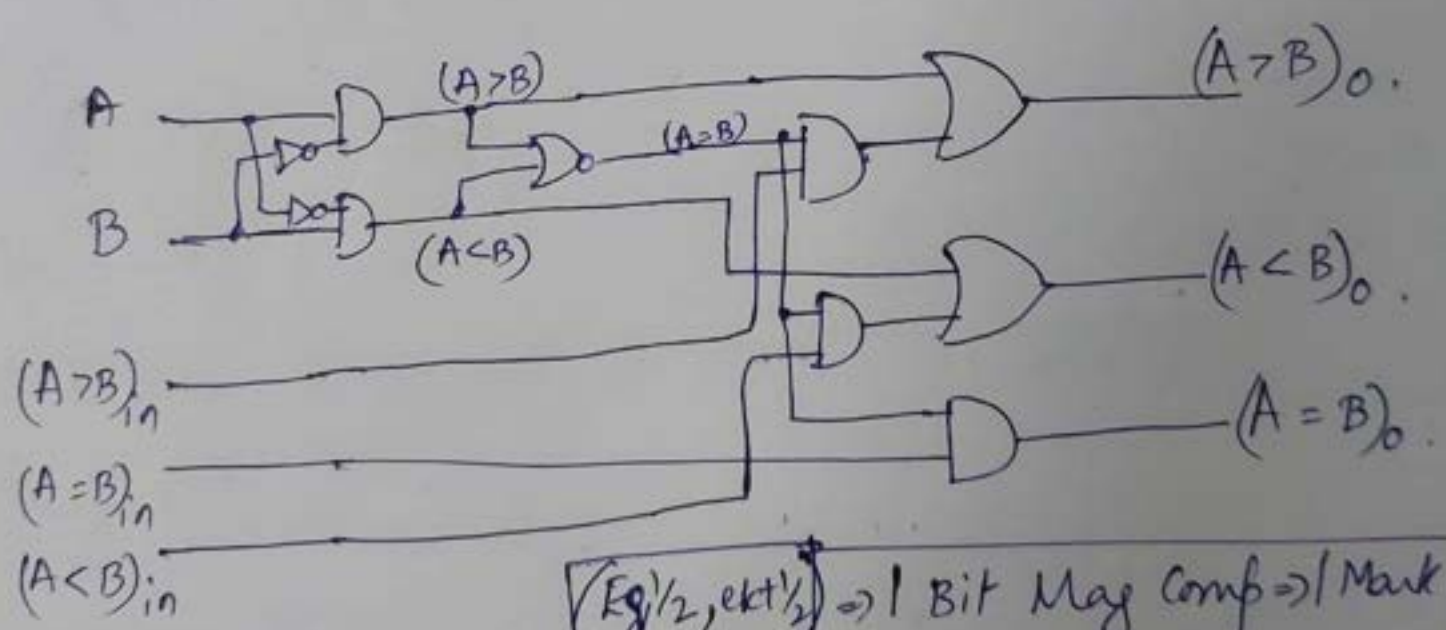
$$(A = B) = \overline{A \bar{B} + A B} = (\bar{A} B + A \bar{B})$$

Cascade Input to Comparator:-

$$(A > B)_0 = (A > B) + (A = B) (A > B)_{in}$$

$$(A < B)_0 = (A < B) + (A = B) (A < B)_{in}$$

$$(A = B)_0 = (A = B) (A = B)_{in}$$



(Eq 1/2, ckt 1/2)  $\Rightarrow$  1 Bit Mag Comp  $\Rightarrow$  1 Mark.  
 (Eq 1/2, ckt 1/2)  $\Rightarrow$  Cascade I/P  $\Rightarrow$  1 Mark.