Question Paper

Exam Date & Time: 27-Sep-2023 (08:00 AM - 10:00 AM)

MANIPAL ACADEMY OF HIGHER EDUCATION

III SEMESTER B.TECH (IT/CCE)
MID SEMESTER EXAMINATIONS, SEP 2023

DIGITAL SYSTEMS AND COMPUTER ORGANIZATION [ICT 2123]

Marks: 30 **Duration: 120 mins.**

A

Answer all the questions. Section Duration: 20 mins

1) Two 3x8 decoder can be combined to form a (0.5)

16x4 decoder | 2x16 decoder | 4x16 decoder | 2x16 decoder

Correct option is: 3

2) Which of the **following** is the output "A1, A0" for an encoder with 4 - bits "Y0, Y1, Y2, Y3" as "0001"? (0.5)

00 | 01 | 10 | 11

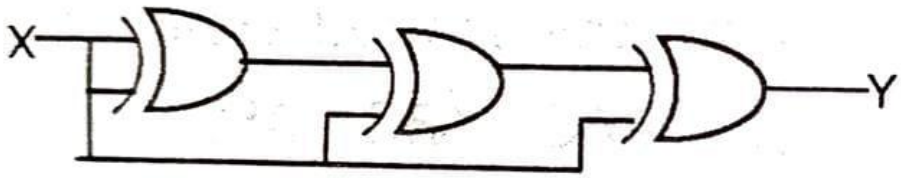
Correct option is: 4

3) A RS latch is (0.5)

Combinational circuit | Synchronous sequential circuit | 1-bit memory element | 1-clock delay element

Correct option is: 3

4) Find the output Y of the given circuit (0.5)



1 | 0 | X | X'

Correct option is: 2

5) If a multiplier is designed using **only** full adders, how many full adders are required to design 3 - bit X 2 - bit binary multiplier? (0.5)

3 | 5 | 7 | 9

Correct option is: 4

6) If a MUX is constructed using only 2x1 MUX, how many 2x1 MUXs are used to design 16x1 MUX? (0.5)

15 | 13 | 11 | 9

Correct option is: 1

7) Which of the following is not a self-complimenting code? (0.5)

8421 code | Excess 3 code | 84-2-1 code | 2421 code

Correct option is: 1

8) The equation for "equal to" in 1 - bit magnitude comparator with cascading input ((A>B)in, (A=B)in, (A< B)in) andA and B as input is: (0.5)

8) The equation for "equal to" in 4 - bit magnitude comparator with cascading input $(A>B)_{in}$, $(A=B)_{in}$, $(A<B)_{in}$ and A and B as input is: (0.5)

$(AB' + A'B)' (A=B)_{in}$ | $(AB' + A'B)(A=B)_{in}$ | $(AB + (AB)')(A=B)_{in}$ | $(A'B' + (AB)')(A=B)_{in}$

Correct option is: 1

9) A 4-bit Carry Look ahead Adder is --------times faster than 4-bit Ripple Carry Adder. (0.5)

2 | 3 | 5 | 8

Correct option is: 2

10) F(a,b) is realized using a 2:1 MUX by connecting 'b' to selection input. F = a, if the selection input is zero. Else F=1. Identify the function F. (0.5)

AND | OR | NAND | EXOR

Correct option is: 2

B

Answer all the questions.

11) Design single digit BCD adder using 4 - bit binary adders and minimum external gates. (3)

12) Design a code converter using NAND gates only to convert a decimal digit represented in 8 4 2 1 code to a decimal digit represented in 8 4 -2 -1 code. (3)

13) Design 5-to-32-line decoder using only 74138ICs. (3)

14) Implement a Boolean function using 4x1 multiplexer and external gates: (2)

F(A,B,C,D) = (0,3,5,12,14)
Connect the inputs AB to selection lines. The input requirements for the four data lines will be a function of variables C and D.

15) Design a logic circuit to evaluate the arithmetic expression (A^2-B^2) using Half Adders ONLY. Where A & B are 2-bit binary numbers. (4)

16) Design an arithmetic circuit using 7483ICs and minimum external NAND gates only to perform: (4)

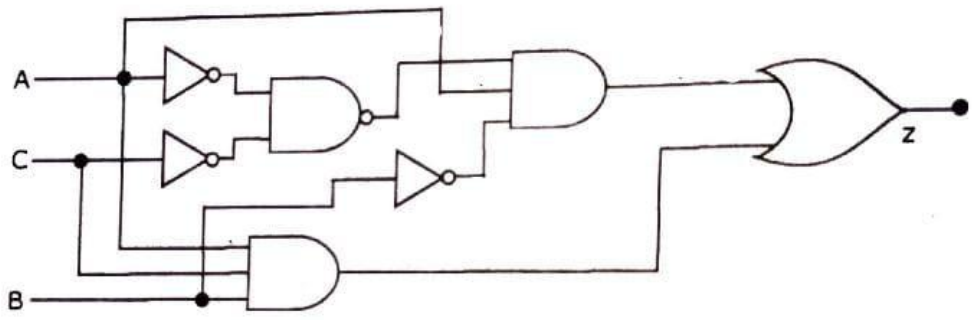
F=4Y when A< B and

F=3Y when A>=B.

Where A,B are 4 - bit binary numbers

Y is a 2 - bit binary number

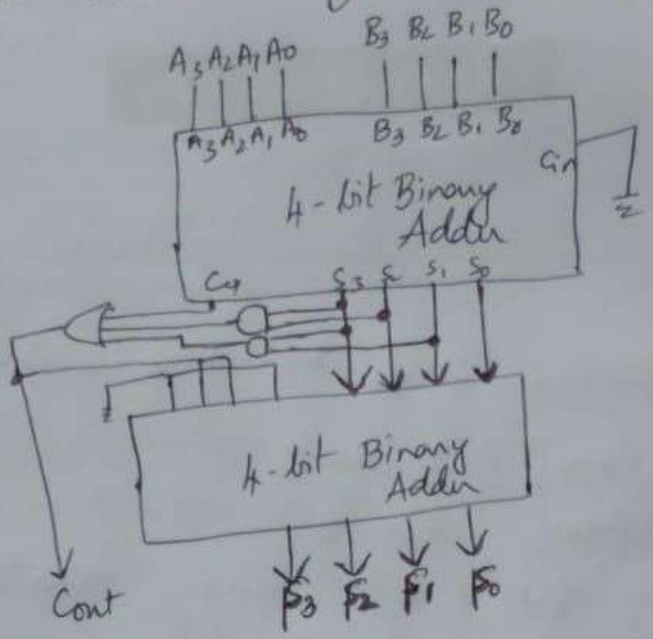
17) Write the function represented by the logic circuit given. Draw the simplified logic circuit of the logic diagram shown below with the minimum number of basic gates possible. (3)

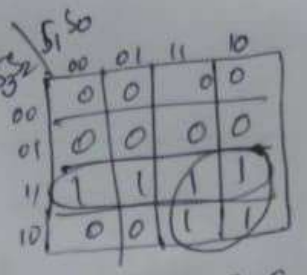


18) Construct a Full subtractor using 74153IC and minimum external gates. (3)

-----End-----

(11) Single digit BCD adder using 4-bit binary adders & minimum external gates.

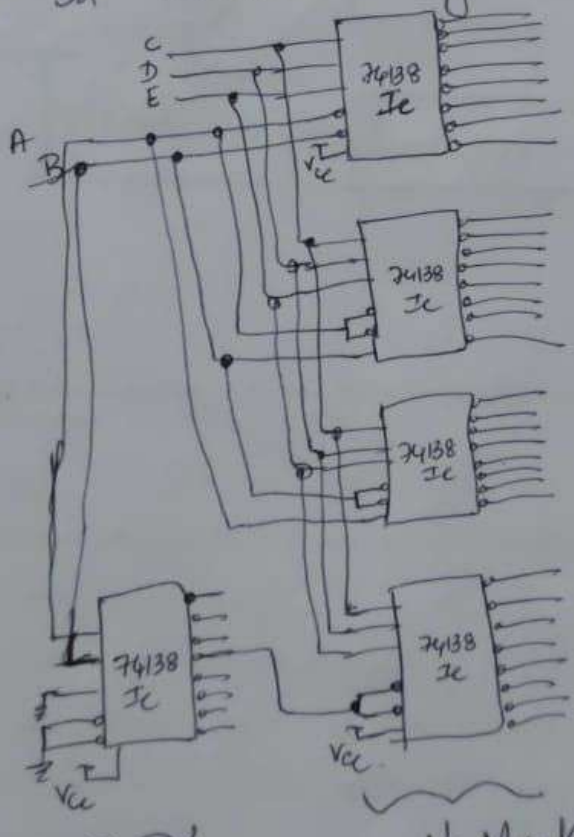




$S_3S_2 + S_3S_1$

First adder → 1 Mark
ADD 6 → 1 Mark
Carry out → ½ Mark
Second adder → ½ Mark

(13) 5 to 32 decoder using 74138 ICs only.



1½ Mark. 1½ Mark.

Question 14 Design a code converter using NAND gates only to convert a decimal digit represented in 8 4 2 1 code to a decimal digit represented in 8 4 -2 -1 code.

Answer 14

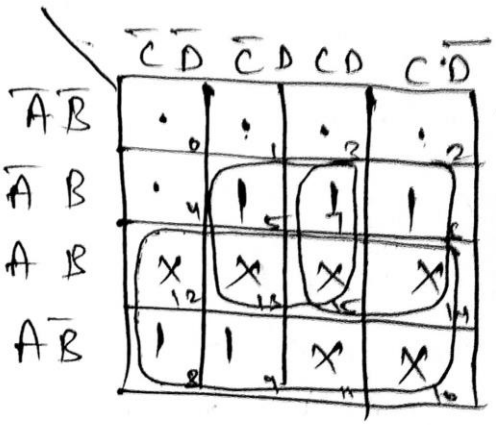
8421 to 8 4 -2 -1 Code Converter

Truth Table.

A B C D (8 4 2 1)	E F G H (8 4 -2 -1)
0 0 0 0	0 0 0 0
0 0 0 1	0 1 1 1
0 0 1 0	0 1 1 0
0 0 1 1	0 1 0 1
0 1 0 0	0 1 0 0
0 1 0 1	1 0 1 1
0 1 1 0	1 0 1 0
0 1 1 1	1 0 0 1
1 0 0 0	1 0 0 0
1 0 0 1	1 1 1 1
1 0 1 0	X X X X
1 0 1 1	X X X X
1 1 0 0	X X X X
1 1 0 1	X X X X
1 1 1 0	X X X X
1 1 1 1	X X X X

↳ 1 Mark

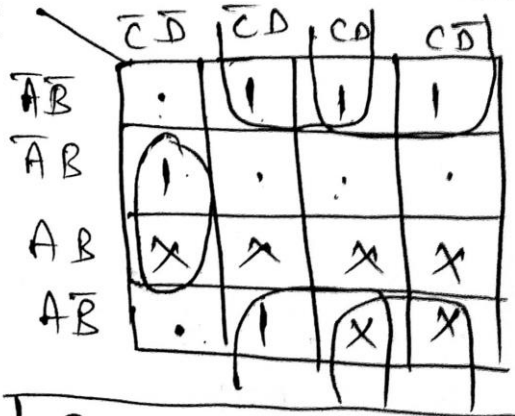
E



$E = A + BD + BC.$

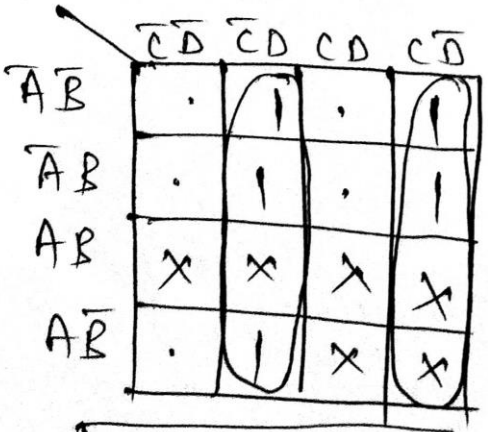
0.25 Mark.

F



$F = \bar{B}D + \bar{B}C + B\bar{C}\bar{D}$

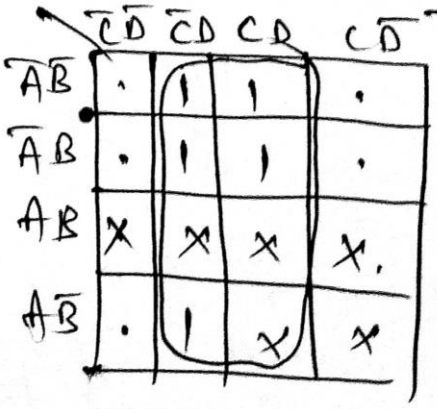
G



$G = \bar{C}D + C\bar{D}$

0.25 Mark

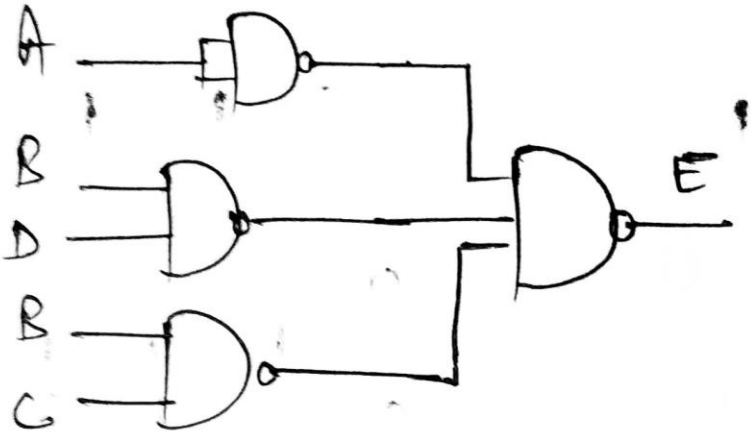
0.25 Mark



$H = D$

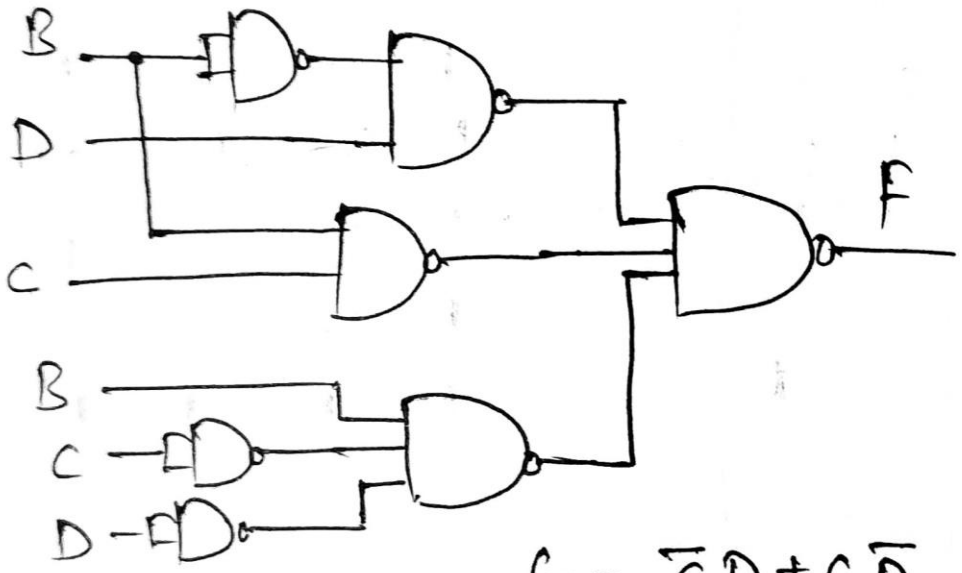
0.25 Mark

$$E = A + BD + BC = \overline{\overline{A}.\overline{BD}.\overline{BC}}$$



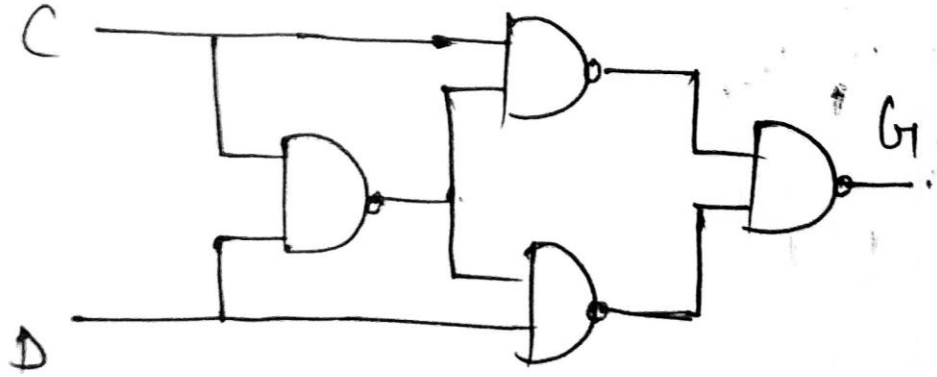
0.25 Marks

$$F = \overline{\overline{BD}.\overline{BC}.\overline{B\bar{C}\bar{D}}}$$

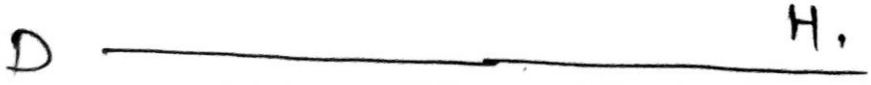


0.25 Marks

$$G_1 = \bar{C}D + C\bar{D}$$ 0.25 Marks



0.25 Marks

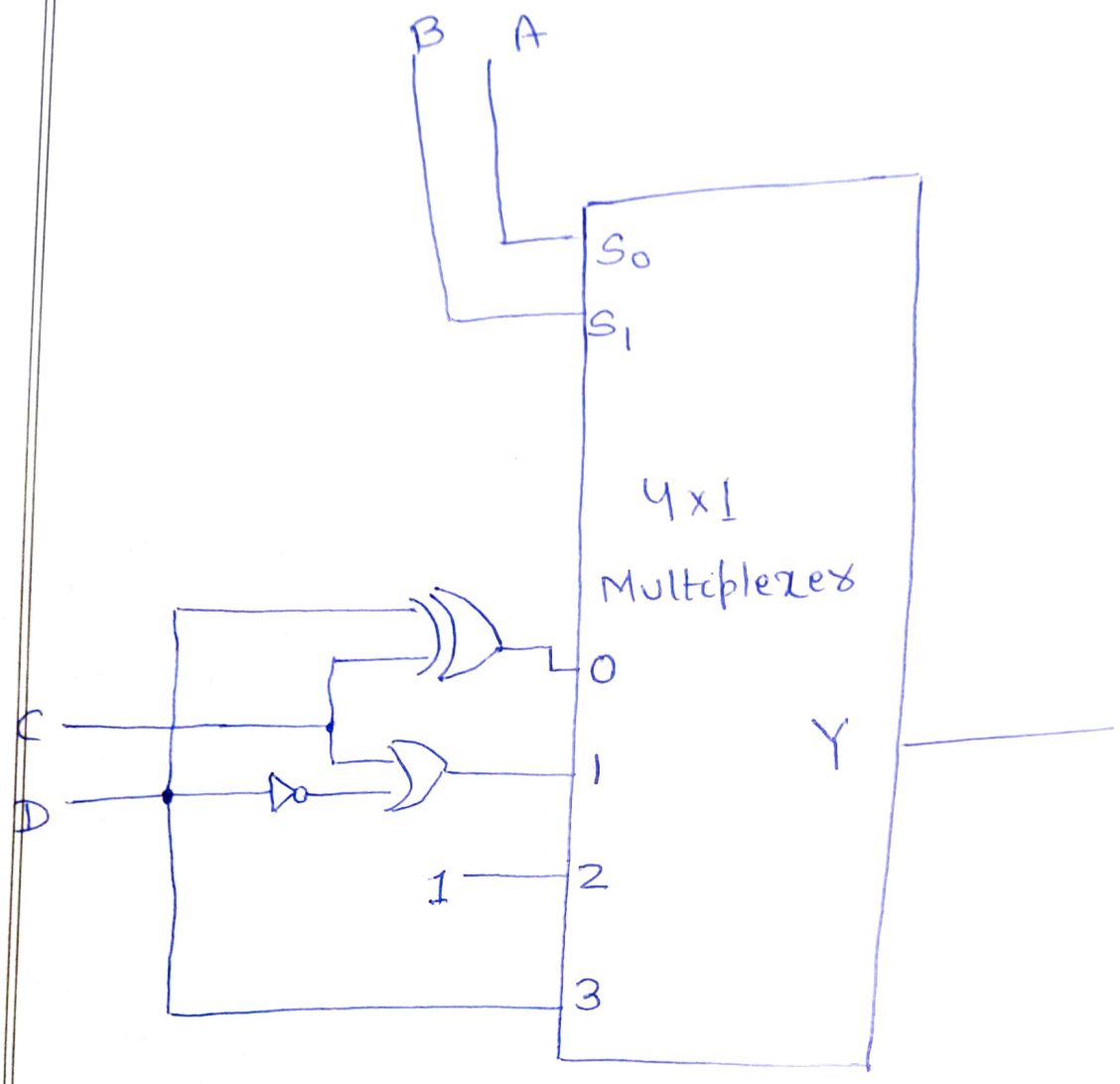


14)

$F(A, B, C, D) = \pi(0, 3, 5, 12, 14)$

$= \Sigma(1, 2, 4, 6, 7, 8, 9, 10, 11, 13, 15)$

Inputs				outputs	
A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	1	$AB = 00$
0	0	1	0	1	$F = C'D + CD'$
0	0	1	1	0	
0	1	0	0	1	$AB = 01$
0	1	0	1	0	$F = D' + CD$
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	$AB = 10$
1	0	1	0	1	$F = 1$
1	0	1	1	1	
1	1	0	0	0	
1	1	0	1	1	$AB = 11$
1	1	1	0	0	$F = D$
1	1	1	1	1	


B
A
S_0
S_1
4 x 1
Multiplexer
0
1
2
3
C
D
1
Y

$A = A_1 A_0$ $B = B_1 B_0$

$A^2 = A_1 A_0 \times A_1 A_0$

A_1 $(A_1 A_0)$ A_0

$(A_1 A_0)$

S_3 S_2 S_1 S_0

Similar to A^2

Obtain $B^2 - b_3 b_2 b_1 b_0$

HA

x, y → S, C

A^2, B^2 — 1 mark

AND, INV — 1 mark

$A^2 - B^2$ — 2 marks

$A^2 - B^2$

$a_3 a_2 a_1 a_0$ +

$\bar{b}_3 \bar{b}_2 \bar{b}_1 \bar{b}_0$

1

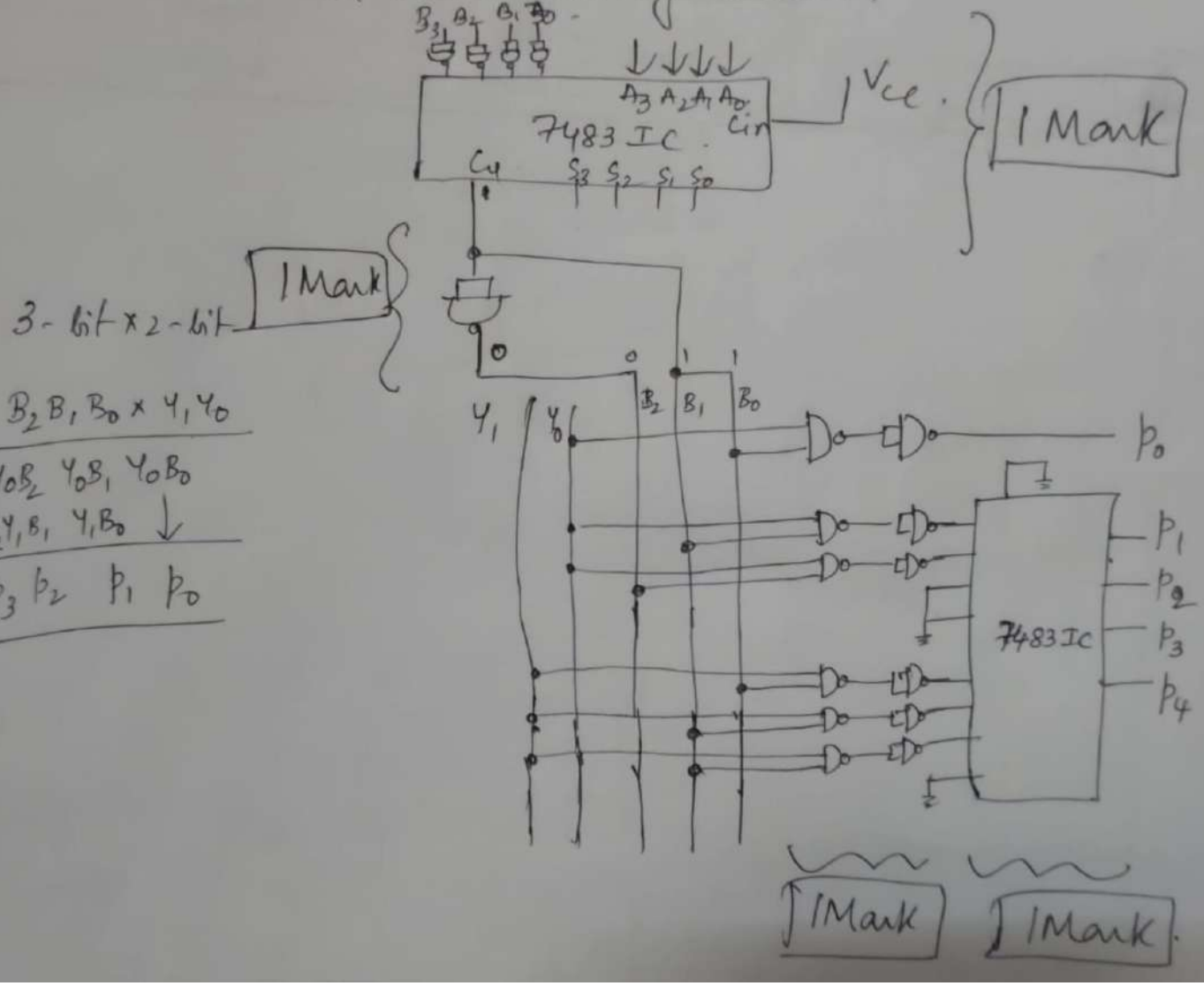
a_3 a_2 a_1 a_0

b_3 b_2 b_1 b_0

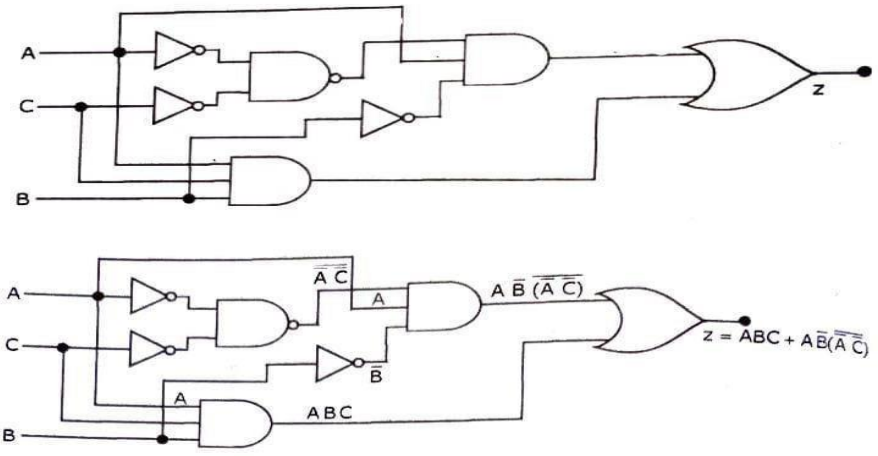
FA

c d_3 d_2 d_1 d_0

(16). Using 7483 Ics & minimum external NAND gates $F = 4Y$ When $A < B$ and $F = 3Y$ when $A >= B$.
where A, B are 4-bit binary numbers
Y is a 2-bit binary number.



17. Draw the simplified logic circuit of the logic diagram shown below with the minimum number of logic gates possible.



$$z = A\bar{B}C + A\bar{B}\cdot(\overline{\overline{A}\,\overline{C}})$$

Once the expression is determined, it is usually a good idea to break down all large inverter signs using DeMorgan's theorems and then multiply out all terms.

$$z = A\bar{B}C + A\bar{B}\left(\overline{\bar{A}} + \overline{\bar{C}}\right)$$

$$= A\bar{B}C + A\bar{B}(A + C) \quad \text{[cancel double inversions]}$$

$$= A\bar{B}C + A\bar{B}A + A\bar{B}C \quad \text{[multiply out]}$$

$$= A\bar{B}C + A\bar{B} + A\bar{B}C \quad [A \cdot A = A]$$

With the expression now in SOP form, we should look for common variables among the various terms with the intention of factoring. The first and third terms above have AC in common, which can be factored out:

$$z = AC\left(B + \bar{B}\right) + A\bar{B}$$

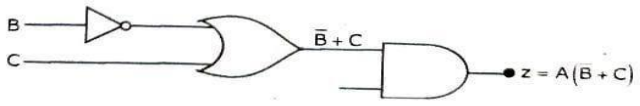
Since $B + \bar{B} = 1$, then

$$z = AC(1) + A\bar{B}$$

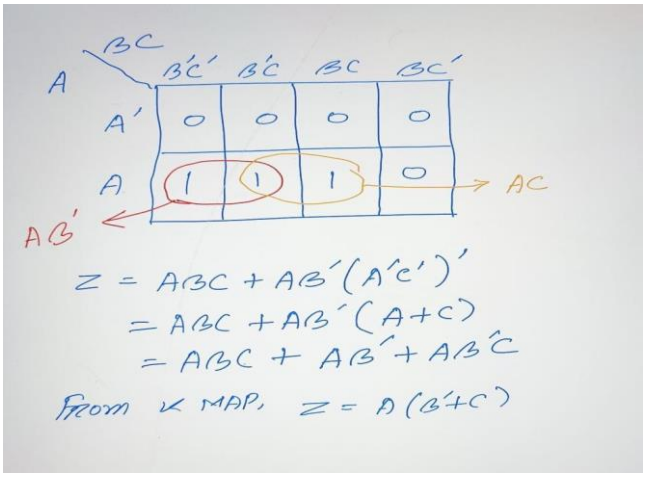
$$= AC + A\bar{B}$$

We can now factor out A, which results in

$$z = A\left(C + \bar{B}\right)$$



OR.. Students can use K MAP also to get the final expression, as shown below



(18). Full Subtractor using 74153 IC and minimum gates.

A	B	C_{in}	D	B_o	
0	0	0	0	0	C_{in}
0	0	1	1	1	
0	1	0	1	1	$\bar{C}_{in}$
0	1	1	0	1	
1	0	0	1	0	C_{in}
1	0	1	0	0	
1	1	0	0	0	C_{in}
1	1	1	1	1	

1 Mark