MANIPAL ACADEMY of HIGHER EDUCATION

Question Paper - Report

13-Oct-2023 10:34:45
PRATHAM SHETTY . .
Logout

Question Paper

Back

MANIPAL ACADEMY OF HIGHER EDUCATION

III Semester BTech Mid Term Examination - September 2023

DIGITAL SYSTEM DESIGN [CSE 2123]

Marks: 30 **Duration: 120 mins.**

Multiple Choice Questions

Answer all the questions. Section Duration: 20 mins

1) Suppose 16-bit adder blocks are used for constructing a hierarchical carry look ahead adder with second level carry generator to add two 64 bit numbers, then the total gate delay is _____. (0.5)

129 8 16 4

2) Choose the true expression(s) for generating c3 in a carry-lookahead adder.

i. c3=g3+p3c3

ii. c3=g2+p2g1+p2p1g0+p2p1p0c0

iii. c3=g2+p2c0

iv. c3=g2+p2c2

(0.5)

i, ii and iv only i and ii only ii and iv only ii only

3) Select the equivalent BCD representation for 83. (0.5)

10000011 100011 1000011 1010011

4) $(12)_{10}$ converted sequentially into it's equivalent a) binary followed by b) BCD followed by c)Excess-3. Determine the final representation. (0.5)

0100 0101 0000 1111 0100 0110 0101 0110

5) Select the minimum number of 2:1 multiplexers required to generate a 2 input XNOR gate without using any external gates. (0.5)

1 2 3 4

6) (0.5)

Identify the number of 3-to-8 decoders and AND gates required to design an 8:1 multiplexer.

2,8 8,1. 1,1. 1,8.

7) Identify the product term that represent essential prime implicant in the following K-map. (0.5)

RS \ PQ	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	1	1	1	0
10	1	0	0	1

PR'S Q'RS Q'S' P'Q'R

8) Suppose a single bit comparator compares two numbers P and Q and produce output Z1=1 when P=Q, Z2=1 when P>Q and Z3=1 when P< Q, then select the correct expression for Z1, Z2 and Z3. (0.5)

Z1= P⊙Q, Z2= PQ' , Z3= P'Q | Z1= P ⊕Q, Z2= P'Q , Z3= PQ' | Z1= P ⊕Q, Z2= P'Q , Z3= PQ | Z1= P⊙Q', Z2= P'Q , Z3= PQ'

9) Choose the simplified SOP expression for the function y (A,B,C) = ∑m (1,4,7) + D(2,5). (0.5)

y = B'C + AB' + AC | y = B'C' + A'B' + AC | y = BC + A'B' + AC' | y = BC + AB' + A'C

10) Identify the equivalent expression for the function f(X1, X2, X3, X4) = X3X4+X2'X4+X1X4. (0.5)

f = Σ(1,3,7,9,11,13,15) | f = Σ(1,2,5,9,10,13,15) | f = Σ(2,4,7,10,12,13,15) | f = Σ(2,5,7,10,11,13,15)

Descriptive Type Questions

Answer all the questions.

11) With examples show the two cases where correction has to be made during the addition of two BCD digits. Also show the result after correction. Using four bit binary adders, design the single digit BCD adder by deriving the expression for the above correction. (4)

12) Design a logic diagram that converts single digit BCD into its equivalent gray code. (4)

13) Identify whether the overflow is there or not after performing the 2's complement addition for the following numbers: (3)

a) +7 + (+2) b) +7 + (-2)

14) Design a full adder using basic logic gates starting from the truth table. Write the Verilog code for full adder. (3)

15) Simplify the function f (x1,..., x4) = x1'x3'x4' + x3x4 + x1'x2'x4 + x1x2x3'x4 using Karnaugh map to obtain the minimum-cost SOP expression assuming that there are also don't-cares defined as D = ∑m (9, 12, 14) (3)

16) Make use of functional decomposition to find the minimum-cost circuit for the function $f(x1, \ldots, x4) = \sum m(0, 4, 8, 13, 14, 15)$. Assume that the input variables are available in uncomplemented form only. (3)

17) Write the truth table for an 8 to 3 priority encoder. Provide an output 'Z' to indicate that at least one of the inputs is present. The input with the least subscript number has the highest priority. Develop the behavioural Verilog code for the same using for loop. (3)

18) Design and implement the function f(A,B,C,D)= ∑m(1,3,4,11,12,13,14,15) using 8:1 MUX and other necessary gates. Assume A, B and C as the select signals for 8:1 MUX. (2)

© 2023 All rights reserved. epm IP: 45.112.148.130 epCloud 1.5

LM Exam Suite
Paperless Digital Exams

^ Top