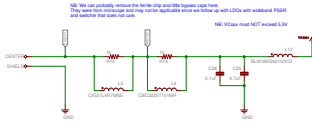
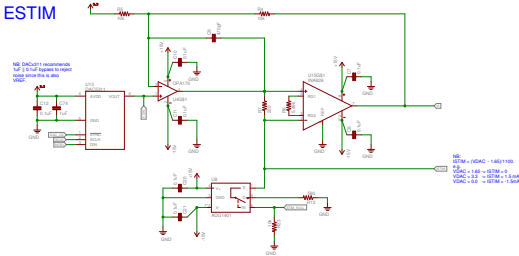


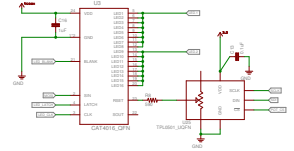
INPUT



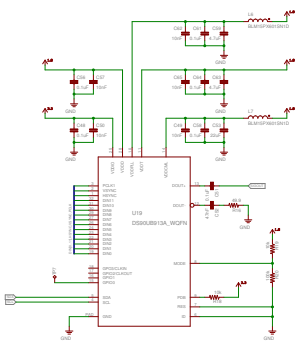
ESTIM



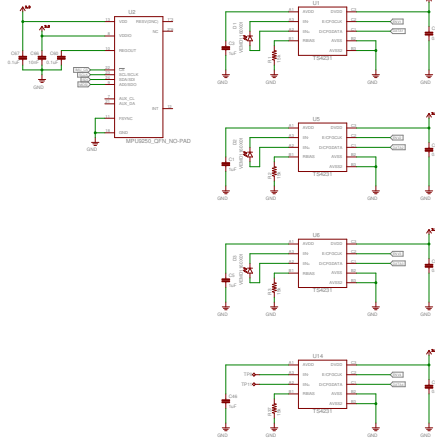
OPTOSTIM



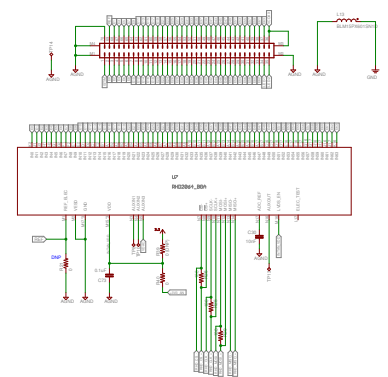
SERIALIZER



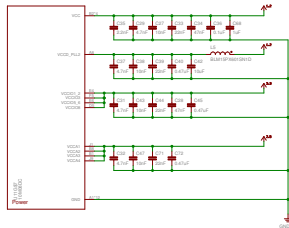
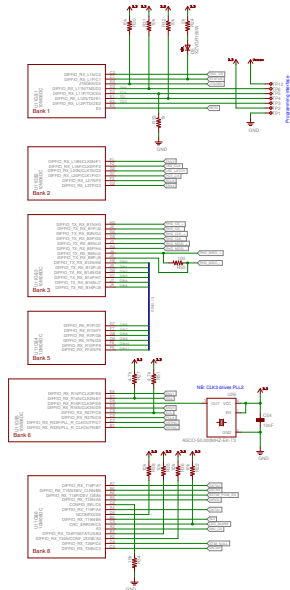
TRACKING



ADC

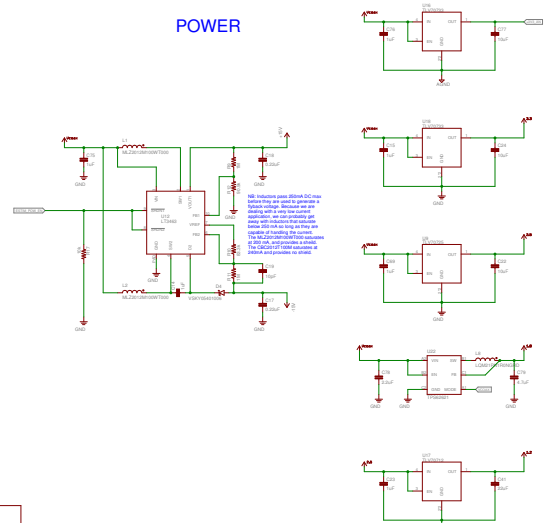


FPGA



NOTE: Because we are using a 0.9V VDDcore for bank 0, the internal calibration may be affected. The time at 0.9V and early boot of VDDcore is a result of using 0.9V supply to the bank and memory. The time at 0.9V and early boot of VDDcore is a result of using 0.9V supply to the bank and memory. The time at 0.9V and early boot of VDDcore is a result of using 0.9V supply to the bank and memory.

POWER



DESIGNED BY:
JON NEWMAN, JAKOB VOIGTS
TITLE: HEADSTAGE-64
LICENS: REL4
CERN_GH_v1.2 L4
Date: 5/7/18 12:46 PM Sheet: 1/1