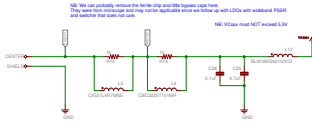
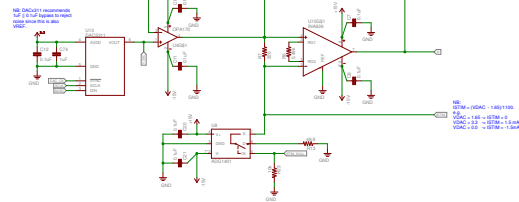


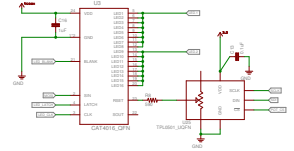
INPUT



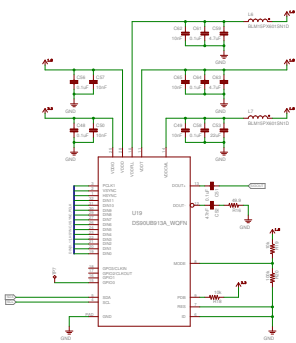
ESTIM



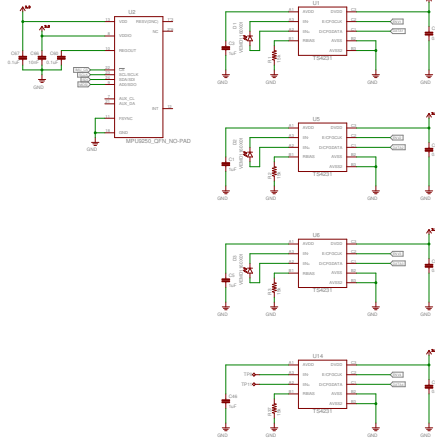
OPTOSTIM



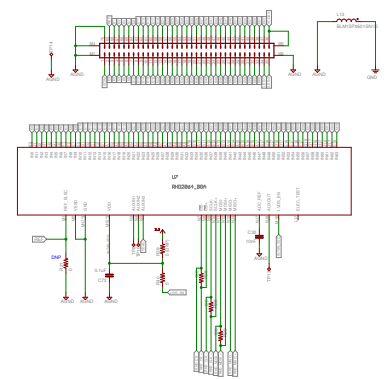
SERIALIZER



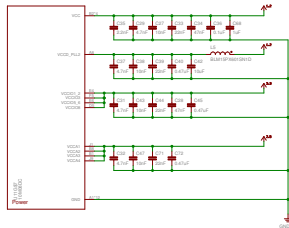
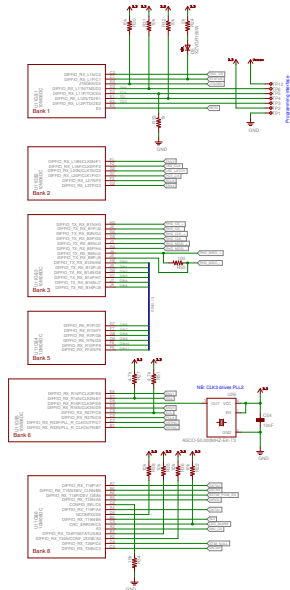
TRACKING



ADC

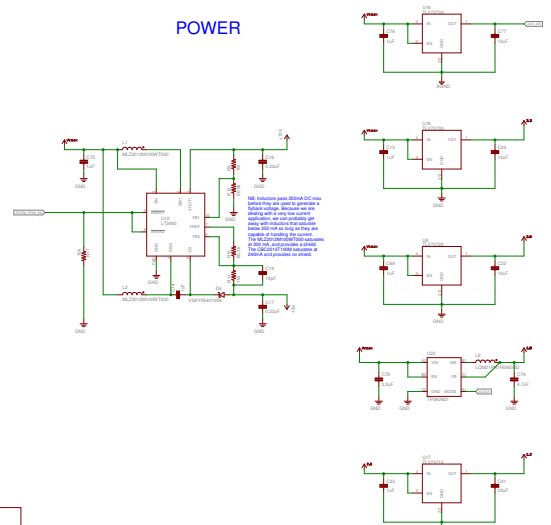


FPGA



NOTE: The input is a differential signal. The input is a differential signal. The input is a differential signal.

POWER



DESIGNED BY:
JON NEWMAN, JAKOB VOIGTS
TITLE: HEADSTAGE-64
LICENS: CC-BY-SA
Date: 4/14/18 6:48 PM

Sheet 1/1