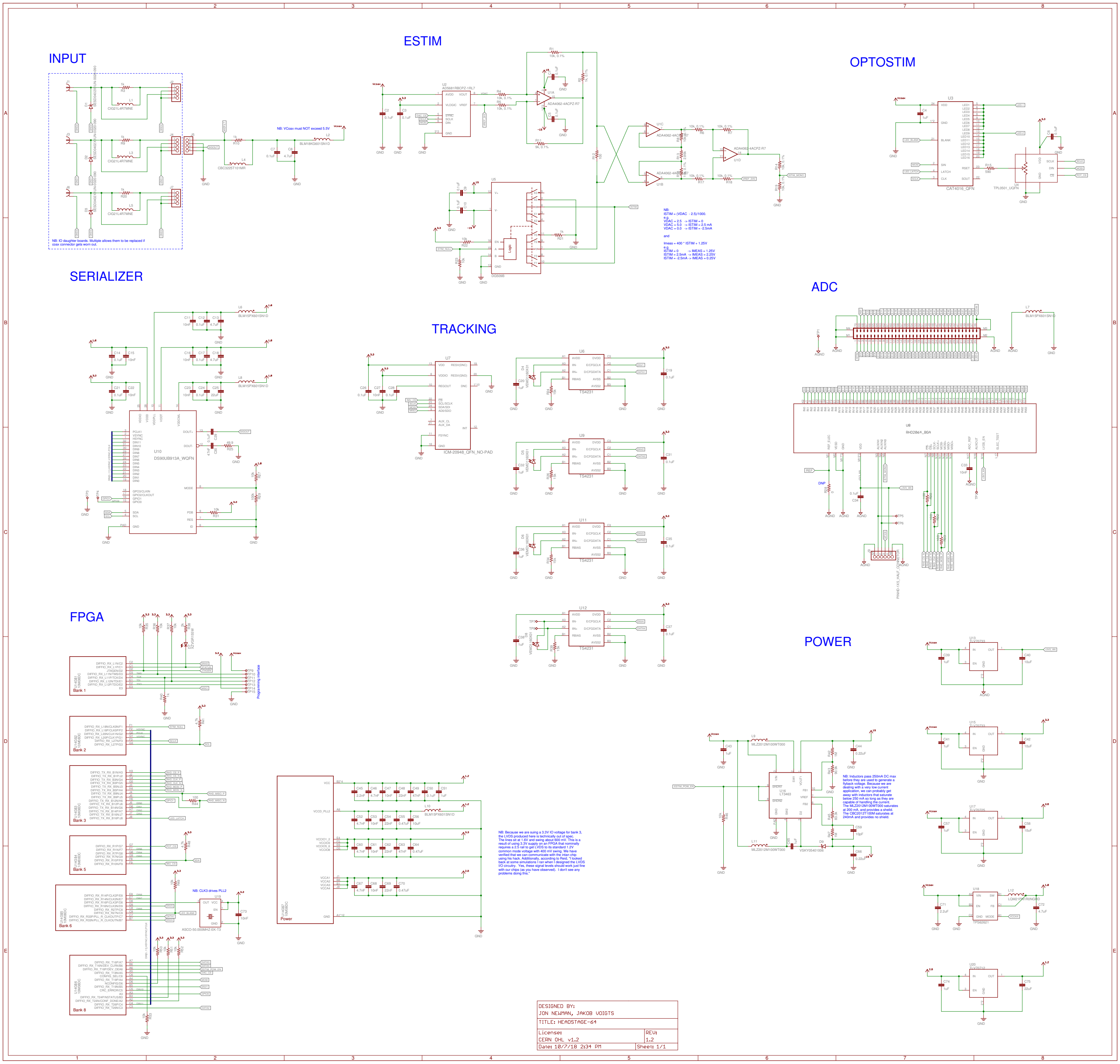
INPUT
NB: IO daughter boards. Multiple allows them to be replaced if coax connector gets worn out.
NB: VCoax must NOT exceed 5.5V
ESTIM
NB:
ISTIM = (VDAC - 2.5)/1000.
e.g.
VDAC = 2.5 -> ISTIM = 0
VDAC = 5.0 -> ISTIM = 2.5 mA
VDAC = 0.0 -> ISTIM = -2.5mA
and
Imeas = 400 * ISTIM + 1.25V
e.g.
ISTIM = 0 -> IMEAS = 1.25V
ISTIM = 2.5mA -> IMEAS = 2.25V
ISTIM = -2.5mA -> IMEAS = 0.25V
OPTOSTIM
SERIALIZER
ADC
TRACKING
FPGA
NB: CLK3 drives PLL2
NB: Because we are suing a 3.3V IO voltage for bank 3, the LVDS produced here is technically out of spec. The lines sit at 1.6V and swing about 600 mV. This is a result of using 3.3V supply on an FPGA that nominally requires a 2.5 rail to get LVDS to its standard 1.2V common mode voltage with 400 mV swing. We have verified that we can communicate with the intan chip using his hack. Additionally, according to Reid, "I looked back at some simulations I ran when I designed the LVDS I/O circuitry. Yes, these signal levels should work just fine with our chips (as you have observed). I don't see any problems doing this."
POWER
NB: Inductors pass 250mA DC max before they are used to generate a flyback voltage. Because we are dealing with a very low current application, we can probably get away with inductors that saturate below 250 mA so long as they are capable of handling the current. The MLZ2012M100WT000 saturates at 200 mA, and provides a sheild. The CBC2012T100M saturates at 240mA and provides no shield.
DESIGNED BY:
JON NEWMAN, JAKOB VOIGTS
TITLE: HEADSTAGE-64
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