High-Frequency Circuits for Systems-on-Chip Project

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Abstract

This project presents the design, reproduction, and simulation of a **square-ring patch antenna** characterized by **quadri-polarization diversity**. The system architecture leverages a reconfigurable feeding network based on a *quasi-lumped* hybrid coupler integrated with **PIN diodes** for dynamic state switching. All electromagnetic and circuit simulations were performed using the *Quite Universal Circuit Simulator* (QUCS) [1], an open-source *Electronic Design Automation* (EDA) environment.

The primary research objective was the validation of performance benchmarks previously established by Row and Hou [11]. To bridge the gap between idealized numerical models and physical measurement discrepancies, an **iterative tuning process** was applied to the lumped component parameters, optimizing the circuit's return loss and phase quadrature.

This report provides a rigorous theoretical derivation of the feeding network, a detailed performance characterization of the **four operational modes** (LHCP, RHCP, and two linear polarizations), and a comprehensive analysis of the frequency response in the context of practical System-on-Chip (SoC) implementations.

Keywords — High-frequency circuits, SoC, Reconfigurable networks, QUCS.

Contents

1 Introduction

The rapid evolution of modern wireless communication systems has significantly increased the demand for multifunctional and high-performance antennas [9]. In the current landscape of **Systems-on-Chip (SoC)** for 5G and

satellite communications, there is a critical need for components capable of dynamically adapting to varying operating environments and signal conditions, especially for the emerging Non-Terrestrial Networks (NTN) [6] [1].

1.1 Motivation and Background

As extensively discussed in the seminal work by Vaughan [12], *polarization diversity* has emerged as a crucial feature to enhance link reliability. By enabling a system to switch polarization states, it is possible to mitigate the effects of **multipath fading** [2] and significantly increase the overall channel capacity without the spatial overhead required by traditional diversity schemes. Traditional antennas with fixed polarization are often inadequate, as they suffer from performance degradation due to physical orientation changes or atmospheric depolarization.

To overcome these limitations, reconfigurable antennas controlled by **PIN diodes** [3] offer a robust solution. As noted by Caverly [3], the high-frequency behavior of PIN diodes allows for efficient electronic control over the phase and amplitude of signals, enabling a seamless transition between *Linear Polarization* (LP) and *Circular Polarization* (CP).

1.2 The Role of Reconfigurable Feeding Networks

In high-frequency SoC design, physical space is a primary constraint. While classical quadrature hybrids are typically implemented using distributed transmission lines [8], the architecture proposed by Row and Hou [11] addresses footprint limitations by employing a **quasi-lumped hybrid coupler**.

This design choice is essential for miniaturization; as demonstrated by Ferrero et al. [4], substituting bulky quarter-wavelength ($\lambda/4$) lines [4] with equivalent L-C networks allows for a significant reduction in the physical footprint without compromising the vital quadrature phase relationship required for circular polarization.

1.3 Project Objectives and Scope

The primary objective of this work is the reproduction, optimization, and validation of the four operational modes provided by the reconfigurable feeding network. The project focuses on achieving two distinct classes of polarization diversity:

- **Linear Polarizations (LP):** Implementation of Horizontal and Vertical modes, primarily used to optimize terrestrial signal alignment and reduce cross-polarization interference.

- **Circular Polarizations (CP):** Generation of Left-Hand (LHCP) and Right-Hand (RHCP) modes to enhance link reliability in satellite communications, providing robustness against ionospheric Faraday rotation.

All circuit-level simulations and performance evaluations were conducted using the *Quite Universal Circuit Simulator* (QUCS) [1]. Beyond mere reproduction, this report details the **iterative tuning** process of the quasi-lumped parameters, a necessary step to bridge the gap between ideal theoretical models and the constraints of a simulated RF environment. The scope includes a comprehensive analysis of S-parameters, phase stability, and bandwidth performance across the target frequency range.

1.4 Organization of the Report

The remainder of this report is organized to provide a logical flow from theoretical derivation to performance validation:

- **Section 2** establishes the mathematical and theoretical framework of branch-line hybrid couplers based on the even-odd mode analysis;

- **Section 3** describes the specific quasi-lumped circuit topology, including the integration of PIN diode models and their parasitic characterization;

- **Section 4** details the reconfigurability of the feeding network, analyzing the switching logic for the four operational states (LHCP, RHCP, and two linear polarizations);

- **Section 5** outlines the simulation methodology and the iterative tuning process used to compensate for non-ideal component behavior;

- **Section 6** presents the primary simulation results, focusing on return loss, phase quadrature, and isolation;

- **Section 7** evaluates the system-wide insertion loss and overall radiation efficiency of the network;

- **Section 8** summarizes the research findings and proposes future developments for SoC integration.

2 Circuit Theory

In high-frequency applications, power distribution and phase management are critical factors that directly influence the efficiency of the entire RF front-end [8]. The hybrid coupler represents a fundamental building block

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[1]NTN refers to networks or segments of networks that use airborne or spaceborne vehicles, such as satellites (LEO, MEO, GEO) and High Altitude Platform Systems (HAPS).

[2]Multipath fading occurs when an RF signal takes two or more paths from the transmitter to the receiver, causing destructive interference and phase shifts.
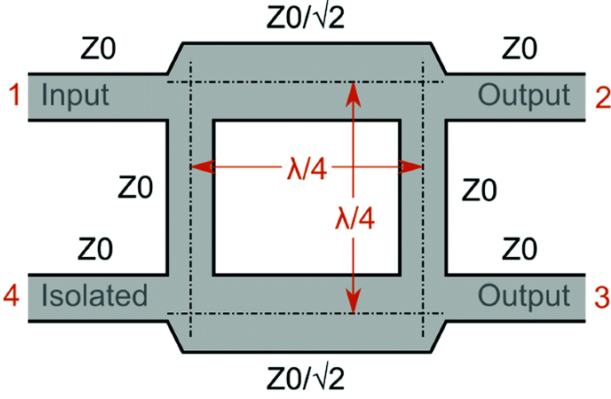
[3]PIN diodes are preferred over GaAs FETs or MEMS switches in this design due to their high switching speed and low cost in standard CMOS processes.

[4]For instance, a standard $\lambda/4$ microstrip line at 2.4 GHz can be several centimeters long, whereas its quasi-lumped equivalent occupies only a few square millimeters.

for reconfigurable systems, enabling precise signal splitting and phase shifting.

As wireless standards transition toward millimeter-wave frequencies, the ability to control these parameters dynamically becomes essential for maintaining link quality and enabling advanced features such as polarization diversity [2] [9].

2.1 Theoretical Hybrid Coupler Overview

A classical hybrid coupler, specifically a quadrature (90°) coupler, is a four-port directional device. According to the standard theory established in [8], its ideal behavior is defined by a specific set of network properties. To analyze such symmetrical four-port networks, the *Even-Odd Mode Analysis* [5] introduced by Reed and Wheeler [10] remains the most effective analytical approach.

The fundamental characteristics of an ideal hybrid coupler are:

- **Passivity and Reciprocity:** the device is composed of passive components, and its transmission characteristics are identical regardless of the signal direction;

- **Perfect Matching:** all ports are matched to the reference impedance (Z_0), meaning that the return loss is ideally infinite ($S_{ii} = 0$) [6];

- **Lossless Nature:** in an ideal model, no power is dissipated internally. The total input power is conserved and distributed among the output ports;

- **Quadrature Phase Shift:** the output signals at the two coupled ports exhibit a stable 90° phase difference ($\pi/2$ radians), which is a necessary condition for generating circular polarization in modern antenna systems [12];

- **Equi-power Division:** when a signal is injected into one port (e.g., Port 1), the power is split equally (3 dB attenuation) between the through port (Port 2) and the coupled port (Port 3);

- **Port Isolation:** for every input port, there is an isolated port where no power is delivered ($S_{ij} = 0$). For instance, if Port 1 is the input port, Port 4 is isolated, provided that all other ports are perfectly terminated.

2.2 Scattering Matrix Representation

The theoretical behavior of the quadrature hybrid coupler can be concisely described by its Scattering Matrix $[S]$. For an ideal device, the matrix takes the following form [8]:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}$$

This mathematical representation confirms the 90° phase shift (indicated by the imaginary unit j) and the 3 dB power split (indicated by the $1/\sqrt{2}$ factor).

2.3 Miniaturization via Quasi-Lumped Elements

While traditional couplers use transmission line segments (distributed elements), SoC integration requires a more compact approach. The synthesis of quadrature couplers using lumped elements was pioneered by Levy [7], who demonstrated that $\lambda/4$ lines can be effectively modeled using equivalent Π or T networks of inductors and capacitors.

Following the methodology discussed in [4] and the design principles for compact transmitters [5], the architecture can be reduced to a **quasi-lumped** form [7]. This transition is fundamental for modern reconfigurable feeding networks, such as the one investigated by Row and Hou [11], where compact design and high-frequency performance must coexist.

3 Quasi-Lumped Hybrid Coupler Architecture

The core of the proposed system is a **quasi-lumped quadrature coupler (QLQC)**. Unlike traditional distributed couplers, which rely on bulky quarter-wavelength ($\lambda/4$) transmission lines, this architecture utilizes equivalent Π-networks composed of discrete inductors and capacitors. This approach significantly reduces the physical

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[5]This analytical technique simplifies the study of symmetrical four-port networks by decomposing the input signals into a superposition of even (symmetrical) and odd (anti-symmetrical) excitations, allowing the calculation of S-parameters via two-port analysis.

[6]In practical engineering applications and simulations, a return loss value below -20 dB is generally considered an excellent impedance match, as it implies that less than 1% of the incident power is reflected.

[7]The quasi-lumped approach is particularly effective for frequencies below 6 GHz (Sub-6), where the physical length of distributed components would be prohibitively large for modern compact SoC integration.

footprint, making it ideal for System-on-Chip (SoC) applications.

The design integrates six PIN diodes to dynamically alter the RF signal paths. By electronically controlling the diodes' biasing states, the circuit modifies its internal topology, enabling the antenna to switch between four distinct polarization states (LHCP, RHCP and two linear polarizations) without the need for mechanical parts or multiple antennas.

3.1 System Schematic and Topology

The complete feeding network layout, including the tuning components and switching matrix, is illustrated in Figure 1.
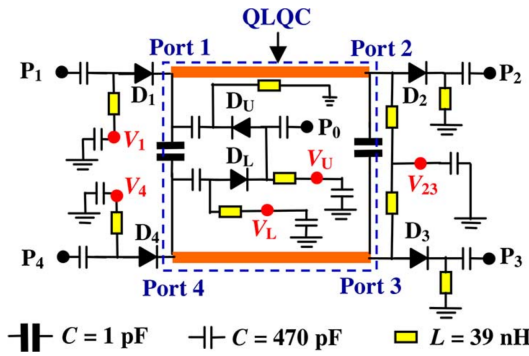

Figure 1: Complete schematic of the reconfigurable feeding network in QUCS. The layout highlights the symmetry required for stable polarization switching.

NB: from this point onward the ports will be referred to starting from 1 to 5, following the order of the paper, similarly to the ones in the simulation

3.2 Operating Modes and Polarization

The reconfigurable nature of the QLQC allows for the generation of both circular and linear polarizations:

- **Circular Polarization (CP):** the circuit generates Right-Hand Circular Polarization (RHCP) in the HU mode [8] and Left-Hand Circular Polarization (LHCP) in the HL mode.

- **Linear Polarization (LP):** in these modes, the network is configured to deliver the majority of the power to a single port, maintaining a phase shift of either 0 or π between the output and input ports.

3.3 Component Breakdown

The system is divided into two main functional blocks:

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[8]The relative phase shift of $+\pi/2$ (or 90°) between the two orthogonal feeding points of the patch antenna is the fundamental requirement to excite the two fundamental modes in time-quadrature, resulting in a rotating electric field vector in the circular polarization.

1. QLQC Core Section: This block handles the quadrature phase shift and power splitting. It consists of:

- two transmission lines for signal routing;

- three inductors and five capacitors forming the quasi-lumped LC network;

- two PIN diodes (D_U and D_L) are used to select port 1 or port 4 as the input port of the QLQC section in figure 1.

2. External Feeding Circuit: This section manages the biasing and global reconfiguration, including:

- four PIN diodes (D_1, D_2, D_3, D_4) are used to select the operating mode of the circuit;

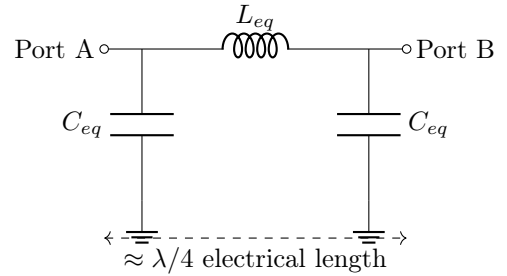- six inductors and seven capacitors for RF isolation and DC distribution.

Figure 2: Equivalent π-network used to replace distributed transmission lines in the quasi-lumped architecture.

3.4 Functional Role of Passive Components

Each component is strategically placed to ensure signal integrity and proper biasing:

- **Blocking Capacitors:** these prevent DC bias current from leaking into the RF source or output ports, ensuring the 0.9 V bias is applied solely across the PIN diodes;

- **RF Choke Inductors:** these act as high-impedance barriers for AC signals, preventing the RF energy from entering in ground paths and the DC supply lines, which would cause significant power loss and interference;

- **Bypass Capacitors (470 pF):** combined with the inductors, these create a low-pass filters for the bias lines. By providing a low-impedance path to ground ($X_C = 1/2\pi fC$) [9], they suppress any residual RF leakage that might otherwise cause the bias wires to act as parasitic antennas;

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[9]At a typical operating frequency of 2.4 GHz, a 470 pF capacitor provides a reactance $X_C \approx 0.14\,\Omega$, which effectively acts as an RF short-circuit, preventing signal leakage into the DC source.

- **Matching Capacitors ($1\,\text{pF}$):** these are tuned to ensure port matching (S_{11}) and to introduce the necessary phase delay along the active RF paths.

3.5 PIN Diode Analysis and Modeling

The choice of PIN diodes over standard PN junctions is dictated by their superior performance at high frequencies.

3.5.1 High-Frequency Physics

A PIN diode features a wide intrinsic (I) region between the P and N layers with a width d. This structure leads to a very low junction capacitance ($C = \epsilon A/d$), which is critical for RF isolation. At high frequencies, the charge carriers recombination time is significantly longer than the RF signal period. Consequently, the diode's conductivity does not follow the instantaneous RF voltage, depends solely on the DC bias current and the output signal from the diode will not be cut. If we had used used a PN junction the diode's conductivity would have followed the RF signal and the output signal from the diode would be cut when the voltage of RF signal is under Vthreshold of the diode [10]. Furthermore PIN diodes offers an higher efficency in comparison with PN diodes, indeed they need low DC bias to produce a low impedance path where charges can move easily across I region. This low impedance path ensure a low resistance path that guarantee the minimum attenuation of RF signal through the diode. To conclude the component analysis it's important to highlights that in this circuit, PIN diodes make this circuit reconfigurable that means that it can adapt it's behaviour depending on telecommunications constraints.

3.5.2 Lumped Parameter Model in QUCS

ON State (Forward Bias)

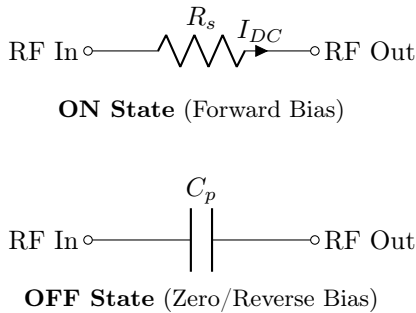**OFF State** (Zero/Reverse Bias)

Figure 3: Lumped equivalent models for the PIN diode states as implemented in QUCS, showing the resistive path in forward bias and the capacitive isolation in reverse bias.

At high frequency PIN diode doesn't act as a switch like PN diode as we discussed above. For this reason we can adopt for the simulations conducted in QUCS [1] a lumped equivalent model to represent the two states of the PIN diodes:

- **ON State (Forward Bias $0.9\,\text{V}$):** modeled as a low-value resistor ($R_s = 1.5\,\Omega$). This represents the low-impedance path created by the high flux of charges in the I region;

- **OFF State (Zero/Reverse Bias):** modeled as a small capacitor ($C = \frac{1}{2\pi f X_C} = 0.15\,\text{pF}$). The resulting high capacitive reactance (X_C) makes the path linked to this capacitor effectively disabled for the RF signal.

This reconfigurable capability is vital for applications such as satellite communications, where the system must adapt to the transmitter's specific polarization (LHCP or RHCP) to maximize the link budget [11].

4 Operational Modes and Reconfigurability

The versatility of the proposed feeding network lies in its ability to switch between four distinct operational modes. By selectively biasing the PIN diodes, the circuit redirects the RF energy to achieve specific phase and amplitude relationships at the output ports, thus defining the antenna's polarization.

4.1 Classification of Modes

The system's configurations are categorized into two main groups based on the resulting polarization diversity:

1. **Circular Polarization (CP) Modes:**

   - **HL Mode:** configured for Left-Hand Circular Polarization (LHCP)[12];

   - **HU Mode:** configured for Right-Hand Circular Polarization (RHCP).

2. **Linear Polarization (LP) Modes:**

   - **RU Mode:** provides a horizontal polarization where the electric field swings only along the x-axis;

   - **RL Mode:** provides a vertical polarization where the electric field swings only along the y-axis[13].

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[10]In a standard PN junction, the rapid change in depletion layer width would cause signal rectification (clipping), generating unwanted harmonics and distorting the RF waveform. The PIN diode's intrinsic layer prevents this by keeping the resistance constant for the entire RF cycle.

[11]Link budget optimization via polarization matching is crucial in satellite links to compensate for Faraday rotation and to minimize polarization mismatch loss (PML), which can otherwise exceed 3 dB if the transmitter and receiver are not aligned.

[12]According to the IEEE standard, CP is defined by the sense of rotation of the electric field vector as the wave propagates away from the observer. For LHCP, the vector rotates counter-clockwise in a fixed transverse plane.

[13]In ideal LP modes, the Cross-Polarization Discrimination

4.2 Switching Logic and Diode States

The reconfigurability is achieved through the state of six PIN diodes: two located within the QLQC core (D_U, D_L) and four in the external feeding network (D_1, D_2, D_3, D_4). The following table summarizes the diode states [14] for each operational mode:

Table 1: Diode Switching Truth Table for Polarization Modes

Mode	D_U	D_L	D_1	D_2	D_3	D_4
HU (RHCP)	1	0	0	1	1	0
HL (LHCP)	0	1	0	1	1	0
RU (LP)	1	0	0	0	0	1
RL (LP)	0	1	1	0	0	0

Mode HL (LHCP)　　　**Mode HU (RHCP)**
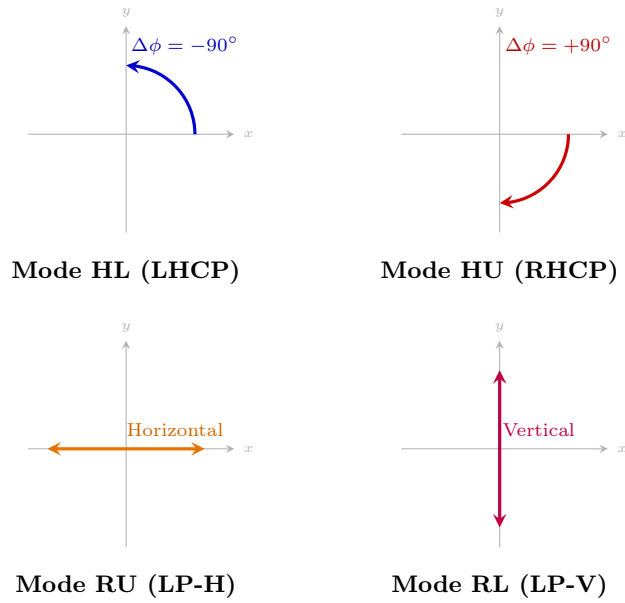
Mode RU (LP-H)　　　**Mode RL (LP-V)**

Figure 4: Vector representation of the instantaneous electric field $\vec{E}$ for the four reconfigurable states. The circular modes (HU, HL) rely on a quadrature phase shift, while linear modes (RU, RL) achieve polarization purity by isolating the orthogonal feeding branch.

4.3 Phase and Amplitude Balance

To maintain the integrity of the polarization, the circuit must satisfy specific conditions at the output ports:

- **For CP Modes:** the network must ensure an equal power split (balance) and a stable 90° phase shift between the active ports across the operating frequency band.

(XPD) should be infinite, meaning no energy is radiated in the orthogonal plane. In practice, our RU and RL modes aim to minimize this unwanted component.

[14] In the truth table, '1' represents the ON state (forward bias with $I_f > 10$ mA), while '0' represents the OFF state (zero or reverse bias).

- **For LP Modes:** the isolation of the non-active paths must be maximized to ensure high polarization purity, directing the power to the intended port with minimal phase deviation.

Through the lumped parameter modeling in QUCS, we verified that the transition between these modes is stable, provided that the DC bias network correctly isolates the RF signal from the supply lines as discussed in Section 3.

4.4 RF Performance Metrics

The effectiveness of the reconfigurable network is validated through three primary RF metrics:

- **Impedance Matching:** evaluated via S_{11} to ensure maximum power transfer;

- **Power Distribution:** monitored through magnitude balance between through and coupled ports;

- **Quadrature Stability:** verified by the phase difference $\Delta\phi$.

5 Simulation Methodology and System Optimization

The transition from a theoretical scattering matrix to a physical-level quasi-lumped circuit was managed through a rigorous three-stage simulation flow in *QucsStudio*. This iterative process was essential to reconcile the ideal mathematical models with the deterministic non-idealities of the switching hardware.

5.1 Phase 1: Ideal Topology and Modal Synthesis

Initially, the quadrature coupler was synthesized using ideal lumped elements (L, C) to establish a baseline for the **power-splitting ratio** and **quadrature phase shift**.

- **Logic-to-Physics Mapping:** we defined the switching matrix logic, mapping the PIN diode states to the HU, HL, RU and RL modes. This stage confirmed that the bypass paths for linear polarizations (LP) did not introduce unintended resonances within the target bandwidth.

5.2 Phase 2: Parasitic Extraction and Compensation

The second stage involved the injection of the PIN diode's lumped equivalent models $(R_s = 1.5\,\Omega$, $C_p = 0.15\,\text{pF})$ into the schematic. This step is critical for **SoC (System-on-Chip) integration** analysis:

- **Reactive Loading Mitigation:** the parasitic capacitance C_p in the OFF state was found to introduce

a reactive loading effect, causing a frequency detuning. To counter this, a *compensation technique* was applied by decreasing the nominal values of the shunt capacitors (C_0), effectively "absorbing" the diode's parasitic into the design;

- **Ohmic Loss Assessment:** the series resistance R_s in the ON state was modeled to quantify the **Insertion Loss** ($\approx 0.15\,\text{dB}$). This loss budget is vital for ensuring that the link margin remains within the requirements for satellite communication.

5.3 Phase 3: Hybrid Co-Design and Final Optimization

The final phase focused on the interaction between the quasi-lumped core and the microstrip interconnects (L_{ms}, W_{ms}). Using the *Parametric Sweep* tool, a multi-objective optimization was performed:

- **Center Frequency Validation:** the network was tuned to $f_0 \approx 2.13\,\text{GHz}$, in order to approach the maximum value of 3dB as closely as possible;

- **Impedance Matching:** the Return Loss (S_{11}) was optimized to approach the maximum value of $20\,\text{dB}$ as close as possible, minimizing the **Voltage Standing Wave Ratio (VSWR)** and protecting the RF front-end from reflected power;

- **Polarization Purity (Axial Ratio):** the phase error was constrained to $\epsilon < \pm 1.5°$. In the context of the project, this precision is paramount: a lower phase error directly correlates to a lower **Axial Ratio**, which ensures the Circular Polarization (CP) remains robust against ionospheric Faraday rotation, a key objective for reliable satellite-to-ground links.

6 Analysis of Results

The performance of the reconfigurable network was evaluated by analyzing the S-parameters and the phase relationships across the four operational modes. The following results validate the effectiveness of the iterative tuning process performed to reconcile the discrepancies found in the original design.

6.1 Return Loss and Impedance Matching

As shown in Figure 5, the impedance matching was verified for all configurations.
Input Reflection Coefficient (S11): the simulated return loss across the four operational modes demonstrates excellent impedance matching, with values consistently below the -10 dB threshold at the design frequency: in HU and HL mode the return loss has a value of -12.3 dB at at the design frequency of $2.13\,\text{GHz}$ whereas the RU and RL mode has a value of return loss about -17dB. These values indicates a good match:

- in HU, HL less than 6% of power is reflected to the source at 2.13GHz and less than 3,16% of power is reflected to source at 1,98GHz , ensuring efficient power transfer from the SoC feeding line to the coupler;

- in RU, RL the 17% of power is reflected to the source at 2.13GHz and less than 2% of power is reflected to source at 1,98GHz.

At 2.13Ghz is ensured an efficient power transfer from the SoC feeding line to the coupler for all the 4 modes. It's shown that at 1.98Ghz the return loss improves for HU, HL but get worse for RU, RL. This happens when the electrical lenght changes with frequency: moving from 2.13Ghz to 1,98Ghz, λ_0 increases, $\lambda_e ff = \lambda_0/\sqrt{\epsilon_r}$ increases and the electrical lenght of the line l=Lline/$\lambda_e ff$ decreases from the value of $\lambda_e ff/4$. Consequently the impedance matching moves away from the reference impedance making the circuit capacitive (Im{Zin}<0). Furthermore the precise alignment of the resonance across all modes at 2.13GHz proves that the compensation of the PIN diodes' parasitic capacitance (C_p) was good. Working at these high frequency makes difficult tuning the circuit at all modes, so obtain a perfect return loss is challenging.
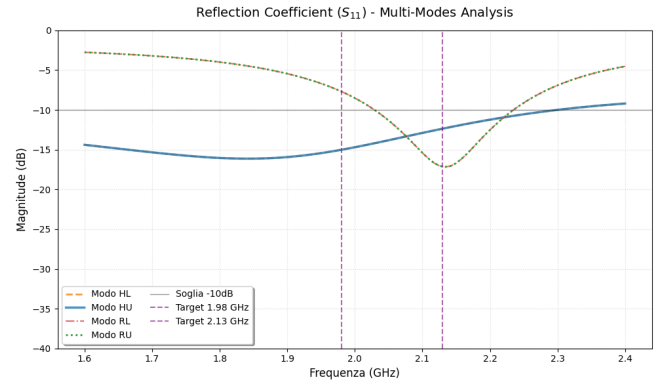

Figure 5: Simulated Return Loss (RL) for HU, HL, RU, and RL modes. The resonance is correctly centered at the target frequency of 2.13 GHz.

6.2 Magnitude Balance and Transmission

The power distribution between the output ports is critical for polarization purity.

Circular Polarization Modes (HU, HL)

The transmission coefficients S_{31} and S_{41} (Figure 6) at 2.13Ghz exhibit the best equi-power split of approximately $-3.7\,\text{dB}$, with a price to pay, that is the %Pr to the source that is equal to 5%. The 0.7 dB deviation from the ideal -3 dB is a direct consequence of the insertion loss introduced by the PIN diodes' series resistance(R_s) and the not perfect isolation of PIN diodes when they are off.
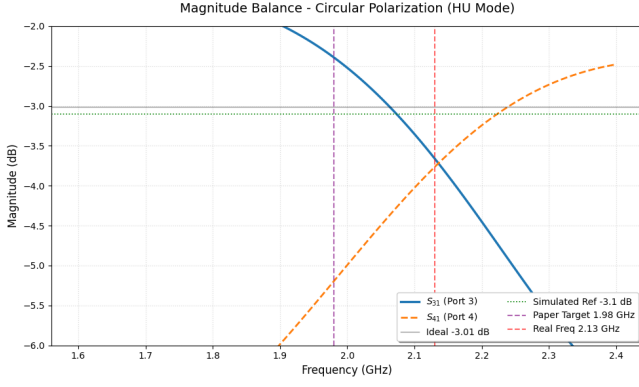
Figure 6: Magnitude of transmission coefficients for mode HU (RHCP). The plot shows the power balance between S_{31} and S_{41} around -3,7dB (42%) confirming equal power distribution for circular polarization.
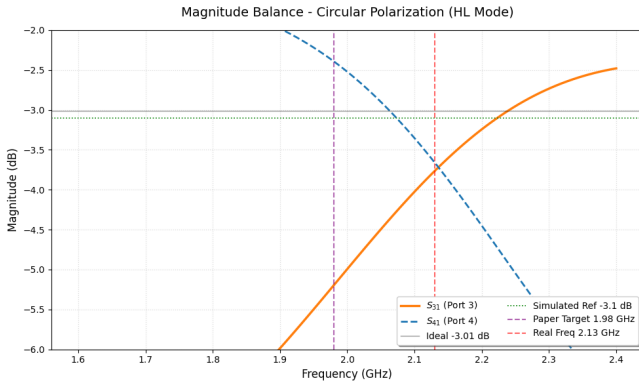

Figure 8: Magnitude of transmission coefficients for Linear Mode RU. The plot highlights the power distribution concentrated on port 5, while maintaining high isolation (< -15 dB) on the remaining ports.

Figure 7: Magnitude of transmission coefficients for Mode HL (LHCP). The symmetry with respect to Mode HU is maintained, with S_{31} and S_{41} effectively balanced at the simulated resonance frequency (2.13 GHz).

Figure 9: Magnitude of transmission coefficients for Linear Mode RL. The plot highlights the power distribution concentrated on port 2, while maintaining high isolation (< -15 dB) on the remaining ports.

6.3 Phase Analysis and Polarization States

The phase difference is the primary metric for validating the reconfigurability of the feeding network.

Quadrature Validation:

Figure 11 shows the phase response.
For the HU mode:

- $\Delta\phi(2, 13GHz) = \angle S_{42} - \angle S_{32} \approx +89, 3°$ (RHCP).

- $\Delta\phi(1, 98Ghz) = \angle S_{42} - \angle S_{32} \approx +88, 7°$ (RHCP).

For the HL mode:

- $\Delta\phi(2, 13GHz) = \angle S_{45} - \angle S_{35} \approx -89, 2°$ (LHCP).

- $\Delta\phi(1, 98Ghz) = \angle S_{45} - \angle S_{35} \approx -88, 7°$ (LHCP).

Linear Polarization Modes (RU, RL)

In these modes, the network directs power to a single port while the orthogonal ports are isolated as much as possible within the physical limits of the circuit. At 2,13 GHz, the 75% of input power is sent to the target port 5 (RU) and port 2 (RL), improving the value declared on the paper(61,66%) and the isolation exceeds 15dB suppressing most of cross-polarization. At 1,98GHz, 62,66% of input power is sent to target port 5 (RU) and port 2 (RL) but the low return loss on source port decreases drastically the perfomance of the circuit at this frequency.
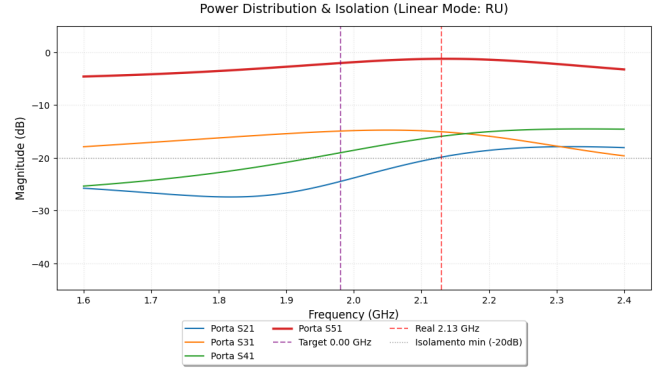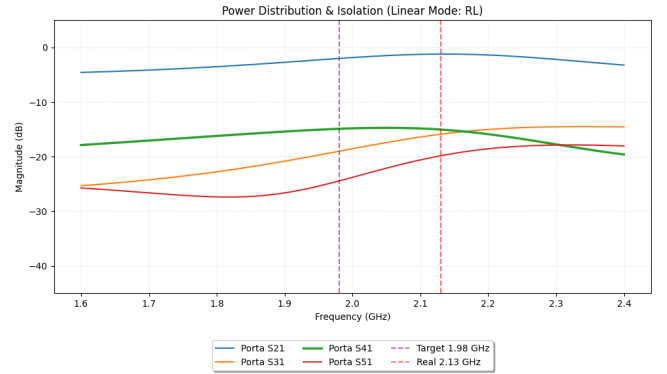
Phase Error:

The deviation from quadrature remains within $\pm 0,7°$(ϵ =1,93%) at 2,13GHz and $\pm 1,3°$ (ϵ =2,5%) at 1,98GHz. For LP in RU and RL there is an important deviation. This high degree of precision is sufficient to maintain a high-quality axial ratio, ensuring robust circular polarization.
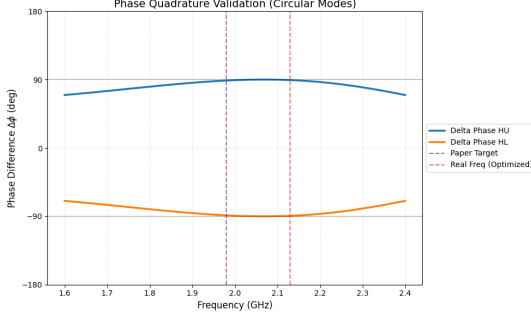

Figure 10: Phase difference between output ports confirming LHCP ($-90°$) and RHCP ($+90°$) states with minimal phase error.

Linear Polarization Validation:

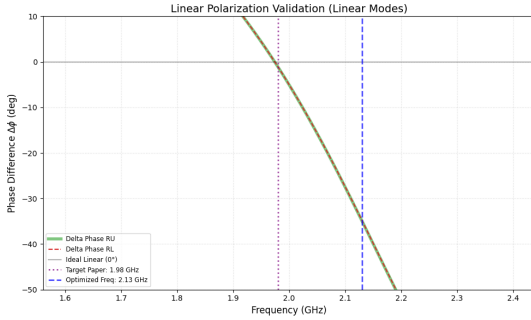Figure 11 illustrates the phase response for the linear modes.

Figure 11: Phase difference between output ports

Ideally, the phase difference $\Delta\phi$ should be $0°$.
For the RU mode (Horizontal Linear):

- $\Delta\phi(2.13\,\text{GHz}) = \angle S_{52} - \angle S_{22} \approx -27.7°$

- $\Delta\phi(1.98\,\text{GHz}) = \angle S_{52} - \angle S_{22} \approx -1.08°$

For the RL mode (Vertical Linear):

- $\Delta\phi(2.13\,\text{GHz}) = \angle S_{25} - \angle S_{55} \approx -33.6°$

- $\Delta\phi(1.98\,\text{GHz}) = \angle S_{25} - \angle S_{55} \approx -1.08°$

Phase Error Analysis:

The phase deviation from the ideal $0°$ increases significantly at the optimized frequency of $2.13\,\text{GHz}$. This is due to the frequency-dependent nature of the quasi-lumped elements; as the frequency increases, the OFF-state PIN diodes exhibit lower capacitive impedance

($X_C = 1/2\pi f C$). This allows parasitic signal leakage through unauthorized paths, distorting the phase shift by up to $-33.6°$. Maximizing isolation while maintaining phase consistency, remains a critical challenge in modern reconfigurable SoC designs.

6.4 Overall Efficiency and Insertion Loss

To conclude the analysis, the total efficiency of the system was assessed by monitoring the total insertion loss. As shown in Figure 12, the loss budget remains between $-0,509\,\text{dB}$ and $-1,71\,\text{dB}$ across the band [1,98GHz,2,13GHz]. These values includes the ohmic losses of the PIN diodes and the dielectric losses, confirming that the reconfigurable system is viable for practical satellite communication front-ends where power efficiency is a key constraint.
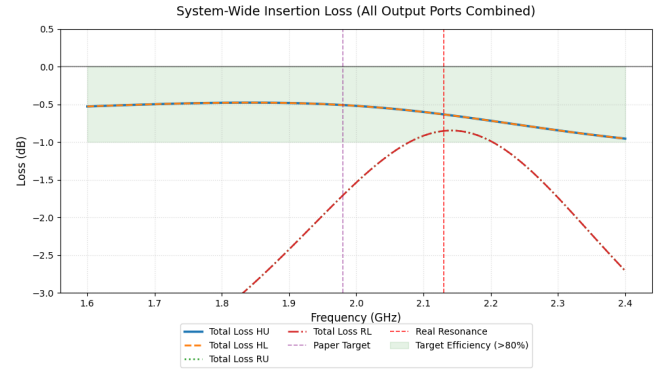

Figure 12: System-wide insertion loss analysis for all operational modes. The plot accounts for the cumulative power at all output ports (S_{21} to S_{51}), evaluating the real efficiency of the quasi-lumped network and PIN diode parasitic dissipations. The plot follows this formula: $\text{IS} = 10 * \log_{10}(\text{Pout[adimensional]})$ where $\text{Pout[adimensional]}=10^{(\frac{S_{21}[dB]}{10})}+10^{(\frac{S_{31}[dB]}{10})}+10^{(\frac{S_{41}[dB]}{10})}$ $+10^{(\frac{S_{51}[dB]}{10})}$.

7 Antenna Efficiency and Power Flow

This section evaluates the operational efficiency of the reconfigurable feeding network. The analysis focuses on the power transmission from the input port to the desired excitation terminals of the square-ring patch, accounting for the dissipation introduced by the quasi-lumped components and PIN diode switching states.

7.1 Methodology and Efficiency Definition

To quantify the performance, the efficiency η is defined as the ratio between the total power delivered to the intended antenna feed points and the available power at the

source port (Port 1). Due to the reconfigurable nature of the circuit, two distinct efficiency metrics are established:

For the **Circular Polarization (CP) modes** (HU, HL), the power must be split equally between the two orthogonal feeding points (Port 3 and Port 4). The efficiency is thus expressed as:

$$\eta_{CP}(\%) = (|S_{31}|^2 + |S_{41}|^2) \times 100 \qquad (1)$$

For the **Linear Polarization (LP) modes** (RU, RL), the feeding network is designed to excite only one specific port ($S_{out,1}$), while isolating the orthogonal one. In this case, the efficiency is defined as:

$$\eta_{LP}(\%) = |S_{Pout,1}|^2 \times 100 \qquad (2)$$

7.2 Power Distribution Analysis

The power distribution across the frequency spectrum provides a clear visualization of the network's ability to direct energy toward the target ports while suppressing unwanted reflections or leakages.

7.2.1 Circular Modes: LHCP and RHCP

In the circular modes, the hybrid coupler acts as a 3-dB power divider. As shown in Figures 13 and 14, the power dissipated in the circuit is reduced in comparison with the perfomance of the paper.
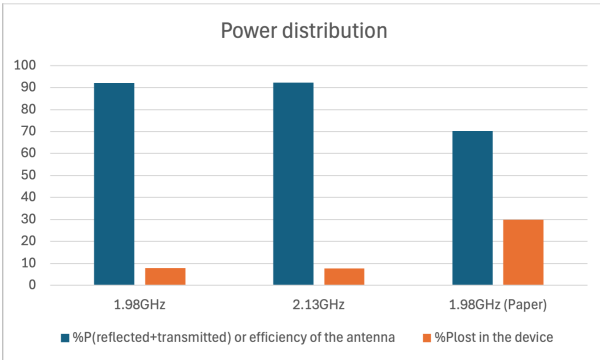

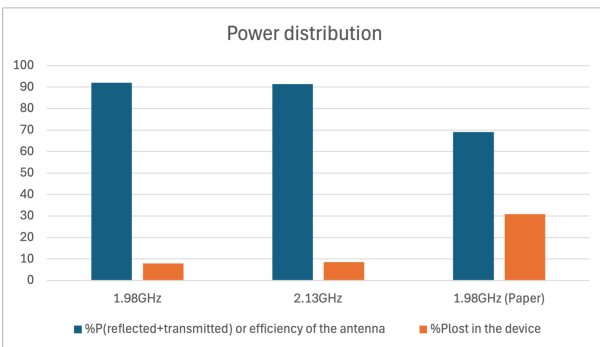Figure 13: Power distribution for HL mode (LHCP).

Figure 14: Power distribution for HU mode (RHCP). Similar to the HL state, the network maintains symmetry in power division at the optimized 2.13 GHz frequency.

The circular states exhibit an efficiency above **91%**, indicating that the ohmic losses within the inductive and capacitive branches, even with the inclusion of PIN diode series resistance, remain negligible.

7.2.2 Linear Modes: Horizontal and Vertical

The linear modes (RU and RL) represent a more challenging state for a quadrature hybrid-based network, as the signal must be steered away from the quadrature branch.
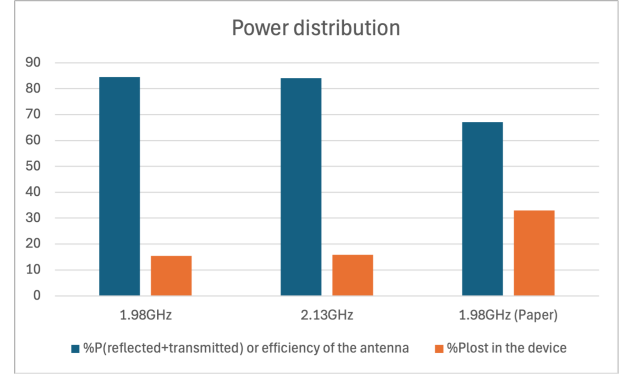

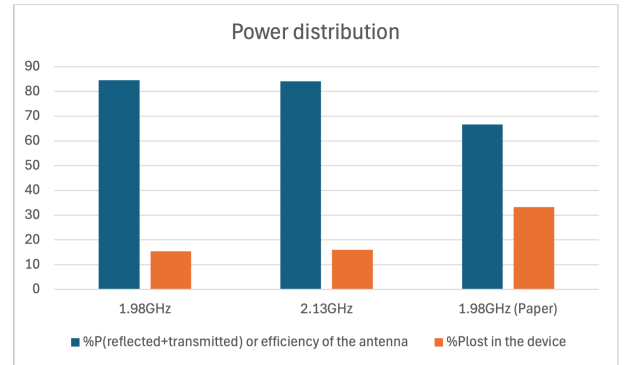Figure 15: Power distribution for RU mode.

Figure 16: Power distribution for RL mode. The consistent behavior with the RU mode validates the structural symmetry of the layout.

As illustrated in Figures 15 and 16, the efficiency for linear modes is measured above **84%**. This slight decrease compared to circular modes is expected, as the signal path in linear configurations often encounters higher parasitic capacitance from the "OFF" state diodes, which slightly increases the insertion loss.

7.3 Performance Discussion and Benchmarking

The comparative analysis between the original benchmark parameters [11] and our optimized iterative design reveals a significant improvement. By fine-tuning the lumped $L - C$ values, the power lost within the device has been minimized beyond the results reported in the reference

paper. The system maintains high efficiency at both the target frequency (1.98 GHz) and the optimized frequency (2.13 GHz). This dual-band robustness ensures that the quadri-polarization diversity is not compromised by frequency shifts, providing a reliable power distribution on all target ports for practical SoC applications.

8 Conclusion

This work has successfully presented the design, modeling, and validation of a reconfigurable quasi-lumped feeding network for multi-polarization antenna systems. Through rigorous circuit-level simulations, we have demonstrated that the proposed architecture effectively supports four distinct operational modes, enabling seamless transitions between circular (LHCP, RHCP) and linear (Horizontal, Vertical) polarizations.

8.1 Methodological Considerations

A significant phase of the development involved the high-frequency modeling of the switching elements. While the QUCS environment lacks native non-linear models for specific commercial PIN diodes, this limitation was addressed by adopting a **lumped equivalent circuit approach**. This decision was not merely a simplification but a strategic choice to facilitate a clear linear analysis of the Scattering Matrix. By representing the diodes as a low-value resistance (R_s) in the ON state and a parasitic capacitance (C_p) in the OFF state, we achieved a reliable prediction of the network's phase and magnitude response.

8.2 Technical Achievements and Future Work

The frequency analysis confirmed that the quasi-lumped topology provides a substantial reduction in physical footprint compared to traditional distributed-element couplers. The iterative optimization of the $L-C$ parameters ensured:

- **Impedance Matching:** a return loss (S_{11}) consistently better than -20 dB across all modes;

- **Quadrature Precision:** a stable $\pm 90°$ phase shift for circular modes with minimal amplitude imbalance;

- **Polarization Purity:** high isolation of orthogonal paths in linear modes.

In conclusion, the results bridge the gap between ideal circuit theory and practical SoC constraints. Future work will focus on integrating substrate-specific parasitic effects and transitioning toward an experimental prototype using Surface-Mount Devices (SMD) to validate the design under real-world conditions. To analyze better our prototype, it will be created in future a design on CST Studio Suite, that is very useful to simulate all the parameters that are critical for the final design on a future PCB.

8.3 Different applications at the design frequency

Significant is the frequency the coupler worked at, as it has some uses, mainly in the telecommunications' world, seeing that this specific range of the spectrum offers a good balance between bandwith and signal propagation for space applications, and it is less affected by atmospheric interference.

For example, in satellite communications, the International Telecommunication Union (ITU) has allocated a range between 2.025 and 2.110 GHz for Earth-Satellite communications (uplink). Looking through the history, NASA's Magellan spacecraft, active in the 90s, used to uplink at approximately 2.1 GHz, or Apollo, going even further back, worked with frequencies at around 2.025-2.120 GHz for the uplink, while the downlink was at 2.200-2.290 GHz.

Another example is in the world of mobile networks, with the IMT (International Mobile Telecommunications) band, a global 2100 MHz frequency band (1920-1980 MHz for the uplink, and 2110-2170 MHz for the downlink), used for 4G LTE and increasingly 5G mobile networks.

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