Taisir Hassan

\$\cup 647-667-3006 \sqrt{\sqrt{\sqrt{aisir.hassan@uwaterloo.ca}}} \sqrt{\sqrt{\sqrt{\sqrt{n}} linkedin.com/in/taisir-hassan}} \sqrt{\sqrt{\sqrt{\sqrt{\sqrt{aisir.hassan@uwaterloo.ca}}}} \sqrt{\sin\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\sqrt{\synt{\sqrt{\sq}}}}}}}}}}}\signt{\sqrt{\sqnt{\sq}}}}}}}}}}}}} \end{\sqit{\sqrt{\sqrt{\sqrt{

Technical Skills

Languages: C/C++, Java, Python, C#, Go, VHDL, Verilog, SystemVerilog, Rust, MATLAB, SQL, JavaScript/ Typescript, HTML/CSS CAD/Engineering Software: KiCAD, AutoCAD, Simulink, Multisim, LTspice, Vivado, Quartus Prime, SolidWorks, PSpice

Communication Protocols: I2C, SPI, UART, CAN

Frameworks/ Libraries: UVM, FreeRTOS, pandas, NumPy, Matplotlib, OpenCV, ROS, React, PyTorch, TensorFlow, React Native Developer Tools: Git, CMake, Bash, Linux, Docker, Kubernetes,, GDB, GCC, Google Cloud Platform, VSCode, Visual Studio, CLion, Eclipse, CI/CD, Agile, Jira, Github, Gitlab, AWS (S3, Cloudfront, Terraform, X-Ray)

Incoming: Onboard Payload Embedded Software Engineering Co-op

Jan 2025 – Apr 2025

Ottawa, ON

Will develop software for satellite User Terminal systems using C++ and Python
Will implement networking solutions and software tools on Linux systems using Git and GCC
Will perform testing and troubleshooting of software features to ensure robust system communication

Electrical Team Member

May 2024 - Present

Developed PWM and ADC drivers with low-pass filter logic for the PIC18F26K83, validated using oscilloscopes and wave

generators
Designing Software Defined Radio (SDR) with APRS receiver using RTL in Verilog for real-time telemetry data transmission
Leading schematic design for USB debug board PCB featuring 12V boost converter and CAN-USB communication with

Harwin connectors

Autonomous Vehicle Research Assistant

September 2024 – Present

Controls, Learning and Logic Research Group, University of Waterloo
• Verify CAN bus messages and implement OBD-II data logging to monitor vehicle control systems (throttle, brake, steering, shifting) using **Dataspeed DBW** drivers, debugging hardware firmware faults for system reliability

• Develop a **ROS2** node in **C++** for drive-by-wire control integration with **Dataspeed** modules, implementing both autonomous and

joystick teleop control modes Create and manage launch files using Python to facilitate deployment and testing of ROS2 nodes, including parameter

configuration for different control modes

Autonomous Vehicle Embedded Systems Developer

December 2023 – Present

Watonomous Design Team Waterloo, ON Engineered and debugged ROS2 nodes for camera and LiDAR functionality in autonomous vehicles using C++ and Python Optimized Docker containers for simultaneous operation of FLIR camera and LiDAR, resolving networking and ROS DDS

compatibility issues

• Implemented X11 forwarding for real-time visualization of sensor data within containers, enhancing development and debugging

capabilities **Data Quality Specialist**

May 2023 – Sept 2023, May 2024 - Aug 2024

Cohere.ai

Toronto, ON

Collaborated in the quality assurance of a state-of-the-art Large Language Model.
Achieved an average task completion rate of 98%, ensuring timely and accurate completion of text and code-based tasks.
Decreased data discrepancies and inconsistencies by 25% through meticulous data quality control measures

Junior Fullstack Developer

Jan 2022 - Apr 2022Toronto, ON

Playfair Technologies Spearheaded the launch of a React Native mobile application, leading to a remarkable 50% increase in user engagement. This

initiative involved a strategic transition from existing Swift (iOS) and Flutter (Android) applications, ensuring timely and accurate completion of text-based tasks Significantly improved application performance and response time by 30%, achieved through meticulous optimization of back-end

functionalities utilizing Scala.
Enhanced the application's deployment process by integrating Docker containers, leading to a 40% reduction in deployment time.

This advancement contributed to quicker and more efficient software releases.

Projects

*O URA Research Project: Digital Circuit State Verification via De Bruijn Sequences | Scala, Verilog, SystemVerilog
 *Developing a Verilog parser and synthesis engine to extract gate-level circuit descriptions and state transitions from hardware designs
 *Implementing De Bruijn sequence generation algorithms to create optimal test sequences that guarantee complete state coverage

through Hamiltonian cycle analysis

Creating a verification framework that automatically generates test vectors to traverse all possible state combinations in digital circuit designs

32-bit RISC-V Softcore Processor | Verilog, GTKWave, Icarus Verilog
 Designed and implemented RV32I base instruction set in Verilog, featuring 5-stage pipeline with hazard detection/forwarding logic
 Created test bench and assembly programs to validate instruction functionality, pipeline hazards, and branching logic
 Utilized GTKWave for waveform analysis and debugging of pipeline stages, ensuring correct instruction execution and timing

 \bigcirc Firefighting Robot | C++, Arduino• Developed an autonomous firefighting robot with a sophisticated navigation system capable of precise maneuvering through intricate

physical environments utilizing servo motors Engineered and integrated specialized sensors for detecting heat and flames, coupled with an effective fire extinguishing system to address fire hazards.

 Traffic Light Controller | VHDL, Quartus Prime
 Designed a Traffic Light Controller using VHDL to model sequential logic and state machines, integrating pedestrian crossing requests with traffic light sequences for an FPGA implementation.
Employed both **Moore** and **Mealy** finite state machine models to design a synchronized traffic control system, ensuring safe and

efficient pedestrian and vehicular movement.
Utilized **Quartus Prime** for VHDL code compilation, simulation, and FPGA programming, demonstrating proficiency in digital design tools and methodologies. $\ensuremath{\mathsf{EDUCATION}}$

University of Waterloo

Waterloo, ON

Candidate for BAsc in Honours Computer Engineering, Minor in Comb & Optimization Expected Graduation: May 2028
• Cumulative GPA: 3.3
• Relevant Courses: Data Structures & Algorithms (C++), Digital Circuits (VHDL), Digital Computers (RISC-V ASM), Electronic Circuits, Linear Algebra, Numerical Methods (MATLAB)