Question 1
Correct
Mark 1.00 out of 1.00
Flag question

The digital multiplexer is basically a combination logic circuit to perform the operation

a. AND-AND
b. OR-OR
c. OR-AND
d. AND-OR ✔

Your answer is correct.
The correct answer is:
AND-OR

Question 2
Correct
Mark 1.00 out of 1.00
Flag question

How many $4:1$ MUXes are required to create a $16:1$ MUX, without any additional gates?

a. 2
b. 5 ✔
c. 4
d. 3

Your answer is correct.
The correct answer is:
5

Question 3
Correct
Mark 1.00 out of 1.00
Flag question

A JK flip flop with $K = \bar{J}$ CAN function as a:

a. SR Latch
b. D flip flop ✔
c. T flip flop
d. Both (a) and (b)

Your answer is correct.
The correct answer is:
D flip flop

Question 4
Correct
Mark 1.00 out of 1.00
Flag question

A combinational circuit is to be designed which takes a single 4-bit BCD digit as input and outputs 1 if the digit ≥ 4 and ≤ 8, and 0 otherwise. Using only basic gates, what is the minimum number of gates required?

a. 6
b. 3
c. 2 ✔
d. 4

Your answer is correct.
The correct answers are:
2,
3

Question 5
Correct
Mark 1.00 out of 1.00
Flag question

Two 4-bit binary numbers (1011 and 1101) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?

a. S = 1001, C = 1 ✔
b. S = 1011, C = 0
c. S = 1101, C = 1
d. S = 1101, C = 1

Your answer is correct.
The correct answer is:
S = 1001, C = 1

Question 6
Correct
Mark 1.00 out of 1.00
Flag question

Which of the following expression is not equivalent to X'?

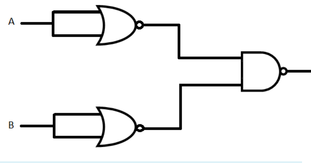
a. X NAND X
b. X NAND 1
c. X NOR X
d. X NOR 1 ✔

Your answer is correct.
The correct answer is:

X NOR 1

Question 7
Correct
Mark 1.00 out of 1.00
Flag question

In the circuit shown below, which logic function does this circuit generate?



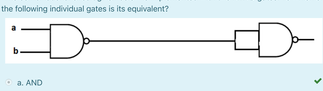
a. OR ✔
b. AND
c. NAND
d. NOR

Your answer is correct.
The correct answer is:

OR

Question 8
Correct
Mark 1.00 out of 1.00
Flag question

The combinational circuit given below is implemented with two NAND gates. To which of the following individual gates is its equivalent?



a. AND ✔
b. OR
c. XOR
d. NOT

Your answer is correct.
The correct answer is:
AND

Question 9
Correct
Mark 1.00 out of 1.00
Flag question

An OR gate can be imagined as

a. Switches connected in parallel ✔
b. MOS transistors connected in series
c. None of these
d. Switches connected in series

Your answer is correct.
The correct answer is:

Switches connected in parallel

Question 10
Correct
Mark 1.00 out of 1.00
Flag question

The simplified expression of full adder sum for inputs x, y and z is

a. s=x'y'z+x'yz'+xy'z'+xyz ✔
b. s=x'yz+xy'z+xyz'+xyz
c. s=x'y'z+x'yz'+xy'z'+x'y'z'
d. s=xy+xz+yz

Your answer is correct.
The correct answer is:
s=x'y'z+x'yz'+xy'z'+xyz