# 专家一

The evaluated manuscript deals with the hardware implementation of the RFLMR algorithm with the MSD binary system for the performance of a high-speed multi-bit adder and multiplier. This is important because it determines the speed and therefore the efficiency of digital processing. The issue is not new, but in recent years its importance has been increasing due to the possibility of a simpler implementation of the algorithm in quantum computers. The authors of the paper have shown that it is possible to implement this algorithm in modern, classical digital systems effectively too. At the same time, attention was paid to the possibility of implementation not in sequential processors but in concurrent systems of the SoC FPGA type. The new algorithm has been successfully realized and verified, as evidenced by the results in Chapter 4. Thus, the new algorithm implementation using Zynq 7000 is the authors' own contribution to the development of the field. Hence, I believe that the presented work can publish after making minor corrections. These changes, in my opinion, will not require re-review.

The work is correctly written in understandable English. The analysis of the state of the art in the field was correctly carried out. The analytical part and the description of the new solution were correctly presented. The system was implemented and run on ALINX AC7020 platform containing SoC FPGA type Zynq 7000.

The weaker side of the work is the insufficient confirmation of the thesis contained in the Abstract. The essence of this thesis is the assumption that the presented implementation allows fast multiplication operations and exceeds expectations in terms of performance, that is, indirectly, the speed of computation. The speed of computation is easiest to prove by comparing the values of delays carried by the new solution in relation to others, such as described in the literature. The effectiveness of the implementation in the SoC of a new solution does not proving the speed of its working. The speed of the work is decided by the numerically expressed results of time simulation or laboratory tests. These should be the values expressed in physical units of the delay between the change of the input signal and the stable appearance of the result at the output, that is, the values of the delay in us, ns, ps, etc. Such measured figures are not included in the work.

Therefore, I recommend supplementing the work in the following.  
1. Correct description of the project position and confirmation of the synthesis process.  
Please describe what design systems and software languages were used to sysnthesis the system in the FPGA part and ARM Cortex-A9 processors of the Zynq 7000 internal structure. To confirm the implementation, please include screen shots of the compilation results and a view of the top-level file structure of the application.

2. Please add the numerical values of the delays brought by the developed combiner/multiplier. These can be either the results of simulations, e.g. Model Sim or the results of measurements with a multi-channel oscilloscope.

3. Please improve the readability of Figures 9 and 10.

4 Conclusions should detail the strengths and weaknesses of the developed method. In particular, it should be a comparison with existing/described implementations of this type available in the literature and technology - in terms of speed, performance and size of hardware resources required. Please also evaluate what the processing speed of the implemented system can be with similar installations of MSD combiners by optical processing methods. Some of this data can be found in the literature available or cited in the paper.

评审的稿件涉及使用MSD二进制系统进行RFLMR算法的硬件实现，以提升高速多位加法器和乘法器的性能。这一点很重要，因为它决定了数字处理的速度和效率。虽然这个问题并不新鲜，但近年来其重要性在增加，因为该算法在量子计算机中的实现变得更加简单。论文的作者们表明，该算法也可以有效地在现代经典数字系统中实现。同时，他们关注到该算法在SoC FPGA类型的并发系统（而非顺序处理器）中的实现可能性。新算法已成功实现并验证，其结果体现在第4章。因此，使用Zynq 7000实现新算法是作者对该领域发展的独特贡献。因此，我认为在进行一些小的修正后，所提交的工作可以发表。依我看，这些更改不需要重新评审。

论文写作正确，英语表达通顺。该领域的现有研究分析正确。分析部分和新方案的描述也得当。系统在包含SoC FPGA类型Zynq 7000的ALINX AC7020平台上实现并运行。

论文的弱点在于对摘要中所包含的论点确认不足。该论点的核心是所述实现能够快速执行乘法操作，并在性能方面超出预期，即间接证明计算速度。最简单的方法是通过与文献中描述的其他解决方案的延迟值进行比较来证明计算速度。新方案在SoC中的有效实现并不能证明其运行速度。工作的速度由时间模拟或实验室测试的数值结果决定。这些结果应该是输入信号变化与输出结果稳定出现之间延迟的物理单位表达值，例如us、ns、ps等。然而，工作中未包含这样的测量数据。

因此，我建议补充以下内容：

1. 纠正项目位置的描述并确认综合过程。请描述在FPGA部分和Zynq 7000内部结构的ARM Cortex-A9处理器中，使用了哪些设计系统和编程语言进行系统综合。为确认实现情况，请包括编译结果的截图和应用程序顶层文件结构的视图。
2. 请补充所开发的组合器/乘法器的延迟数值。这些可以是模拟结果，例如Model Sim的结果，或使用多通道示波器进行测量的结果。
3. 请改善图9和图10的可读性。
4. 结论部分应详细说明所开发方法的优点和缺点。特别是，应该与现有的或文献中描述的同类实现进行比较——比较速度、性能和所需硬件资源的大小。请评估在类似安装MSD组合器的情况下，所实现系统的处理速度能否通过光学处理方法得到提高。这些数据的一部分可以在文献中找到或在文章中引用。

# 专家二

Overall, the paper is well-written, the methodology is coherent, and both the developed method and the results seem meaningful.

The references are relevant to the content and are appropriately cited throughout the text. The title and abstract accurately reflect the contents of the paper.

Aside from a few typos, missing articles, and similar errors, the quality of the English language is very good.

I would suggest a few points for further improvement of the text:

- On page 3/17, lines 111-112, the sentence is not sufficiently clear: "The symbol set for this system is u, 0, 1, where you represent the value -1." Should "you" be replaced by "u"?

- In subsection 4.1.1 (Experimental Equipment, page 10/17), some of the qualifiers ("perfect blend of HW and SW," "wealthy external interfaces," "unlimited expansion possibilities") used in the text sound subjective. Consider using more objective language.

- In subsection 4.2.2, where Software Environment Preparation steps are listed, I would suggest removing "ensuring the installation process is completed smoothly," since it is presupposed that the tool should be correctly installed.

- In the next step, the "COM8" port is specified, but this is device-specific, as on other PCs, it may not be the same COM port (depending on the number and kind of other active COM ports).

总体而言，论文写得很好，方法一致，所开发的方法和结果都具有意义。

参考文献与内容相关，并在全文中得到了适当引用。标题和摘要准确反映了论文的内容。

除了一些拼写错误、漏用冠词以及类似的错误外，英语语言的质量非常好。

我建议以下几点，以进一步改进文本：

* 在第3页（共17页），第111-112行，句子不够清晰：“The symbol set for this system is u, 0, 1, where you represent the value -1.” 应该将“you”替换为“u”吗？
* 在第4.1.1节（实验设备，第10页，共17页）中，文中使用的一些修饰语（“硬件和软件的完美结合”，“丰富的外部接口”，“无限的扩展可能性”）听起来主观。建议使用更为客观的语言。
* 在第4.2.2节中，列出了软件环境准备步骤，我建议删除“ensuring the installation process is completed smoothly”，因为工具的正确安装是前提条件。
* 在下一个步骤中，指定了“COM8”端口，但这是特定于设备的，因为在其他PC上，可能不是相同的COM端口（取决于其他活动COM端口的数量和种类）

# 专家三

Thank you for your interesting paper. Please find below some general and specific comments.

General:

- In the abstract you claim that the RFLMR provides a Better efficiency and performance than RFLEP. However, there is no such comparison in the theory or experimental sections. I would suggest comparing them both at theoretical and experimental levels.

- Please add in section 4 how much resources the RFLMR uses and latency values.

- Please check the size of the Figures, and even the colours. E.g. it is very difficult to read figures 9 and 10.

Specific comments:

- Please add a space before brackets (e.g. in line 23) "processor (RFLEP), and after points.

-MSD is used in section 1 but not defined until section 2

-L112 "you" -> u

- please, change all variables to italic e.g. L112 -> u,0,1 or L213 -> "a and b". it will improve the readability.

-L131 "aandb"->a and b

- Caption Figure 2 RMLEP-> RFLEP

- reduce the size of table 3

- caption table 3 ERLMR -> RFLMR

* 在摘要中，您声称RFLMR比RFLEP提供更好的效率和性能。然而，理论或实验部分没有进行这样的比较。我建议在理论和实验层面进行比较。
* 请在第4节中添加RFLMR使用的资源量和延迟值。
* 请检查图表的大小，甚至颜色。例如，图9和图10非常难以阅读。

**具体建议**：

* 请在括号前后添加空格（例如，第23行）"processor (RFLEP)"，并在句号后面添加空格。
* MSD在第1节中使用，但直到第2节才定义。
* 第112行 "you" -> u
* 请将所有变量更改为斜体，例如第112行 -> u, 0, 1 或第213行 -> "a and b"。这将提高可读性。
* 第131行 "aandb" -> a and b
* 图2标题中的 RMLEP -> RFLEP
* 缩小表3的大小
* 表3标题中的 ERLMR -> RFLMR