CMPEN 331 – Computer Organization and Design,
Lab 1
Due Thursday September 27, 2016 at 11:59 pm (Drop box on Canvas)

In this lab, the students will obtain experience with sequential logic design, and study digital design using the Xilinx design package for FPGAs. It is assumed that students are familiar with the operation of the Xilinx design package for Field Programmable Gate Arrays (FPGAs) through the Xilinix tutorial available in the class website.

1. A sequential circuit has one input (X), a clock input (CLK), and two outputs (S and V). X, S and V are all one-bit signals. X represents a 4-bit binary number N, which is input least significant bit first. S represents a 4-bit binary number equal to N + 3, which is output least significant bit first. At the time the fourth input occurs, V = 1 if N + 3 is too large to be represented by 4 bits; otherwise, V = 0. The value of S should be the proper value, not a don't care, in both cases. The circuit always resets after the fourth bit of X is received. For simplicity, assume the sequential circuit is implemented with the following state table. The outputs are (S,V). All state changes occur on the falling edge of the clock pulse. **For simplicity, you can just follow the following table for your code.**

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
S0	S1	S2	1,0	0,0
S1	S3	S4	1,0	0,0
S2	S4	S4	0,0	1,0
S3	S5	S5	0,0	1,0
S4	S5	S6	1,0	0,0
S5	S0	S0	0,0	1,0
S6	S0	S0	1,0	0,1

2. Write a Verilog Description using the state table shown above. Compile and simulate your code using the following test sequence

X = 1011 1100 1101

The first input bit is at the far right. This is the LSB of the first 4-bit value. Therefore, you will be adding 3 to 13, then to 12, and then to 11. While simulating, keep the period of the CLK to be 10ns. Change X, 1/4 clock period after the rising edge of the clock. S0 = 000, S1 = 010, S2 = 001, S3 = 101, S4 = 011, S5 = 100, S6=111

3. Write a report that contains the following:
   a. The corresponding state diagram.
   b. Your Verilog® design code. Use:
      i. Device Family: Zynq-7000
      ii. Device: XC7Z010- -1CLG400C
   c. Your Verilog® Test Bench design code. Add "`timescale 1ns/1ps" as the first line of your test bench file.
   d. The waveforms resulting from the verification of your design with ModelSim.
   e. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints. Use a clock period of 1 µS as the timing constraint.

f. Snapshot of the routed design.
g. Snapshot of the I/O Planning and
h. Snapshot of the floor planning

4. REPORT FORMAT: Free form, but it must be:
   a. One report per student.
   b. Have a cover sheet with identification: Title, Class, Your Name, etc.
   c. Using Microsoft word and it should be uploaded in word format not PDF. If you know LaTex, you should upload the Tex file in addition to the PDF file.
   d. Double spaced

5. You have to upload the whole project design file zipped with the word file.

6. The following code should be **helpful guide** to your lab (You need to make modifications, this code is for illustration purpose only):

```
module controller1(x,clk,rstn,y,z);
    input x;
    input clk; input rstn;
    output y;
    output z;
  parameter S0 = 3'h0, S1 = 3'h1, S2 = 3'h2, S3 = 3'h3, S4 = 3'h4;

  reg [2:0] PRState, NXState;
  reg y;
  assign z = ~y;

  always @ (PRState) begin
    if (PRState == S4) y = 1'b1;
    else y = 1'b0;
  end

  always @ (posedge clk or negedge rstn) begin
    if (rstn == 1'b0) PRState = S0;
    else PRState = NXState;
    end

  always @ (PRState or x) begin
    case (PRState)
      S0 : if (x == 1'b0) NXState = S1;
         else NXState = S0;
      S1 : if (x == 1'b0) NXState = S2;
         else NXState = S1;
      S2 : if (x == 1'b1) NXState = S3;
         else NXState = S2;
      S3 : if (x == 1'b0) NXState = S4;
         else NXState = S3;
      S4 : NXState = S4;
    endcase
  end
endmodule
```