Name:_____ Student No.: _____

1.1 What is the largest 32-bit binary number that can be represented with
(a) unsigned numbers?
(b) two's complement numbers?
(c) sign/magnitude numbers?
(Hint: The answers can be written in the format of 2's powers.)

1.2 What is the smallest (most negative) 32-bit binary number that can be represented with
(a) unsigned numbers?
(b) two's complement numbers?
(c) sign/magnitude numbers?
(Hint: The answers can be written in the format of 2's powers.)

1.3 Convert the following unsigned binary numbers to decimal. Show your work. (Hint: The answer to Question (b) can omit the final value calculation, but requires to show the calculation process.)
(a) 100100_2
(b) 0111010101001002

1.4 Convert the following hexadecimal numbers to decimal. Show your work. (Hint: The answer to Question (b) can omit the final value calculation, but requires to show the calculation process.)
(a) $4E_{16}$
(b) $403FB001_{16}$

1.5 Convert the following two's complement binary numbers to decimal.
(a) 1110_2
(b) 100011_2

1.6 Convert the following decimal numbers to 8-bit two's complement numbers or indicate that the decimal number would overflow the range.
(a) 24_{10}
(b) -150_{10}

1.7 Convert the following 4-bit two's complement numbers to 8-bit two's complement numbers.
(a) 0111_2
(b) 1001_2

1.8 Perform the following additions of unsigned binary numbers. Indicate whether or not the sum overflows a 4-bit result.
(a) $1001_2 + 0100_2$
(b) $1101_2 + 1011_2$

1.° Convert the following decimal numbers to 6-bit two's complement binary numbers and add them. Indicate whether or not the sum overflows a 6-bit result.

(a) $16_{10} + 9_{10}$

(b) $-27_{10} + -31_{10}$

1.10 Draw the symbols, Boolean equations, and truth tables for the following logic gates:

(a) a four-input OR gate

(b) a three-input XNOR gate

(c) a five-input NAND gate

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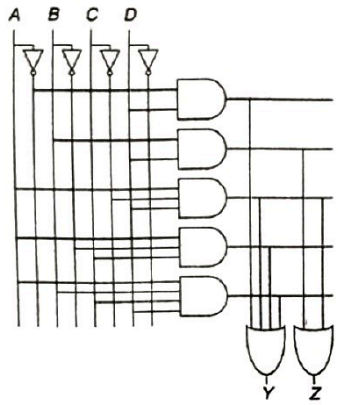
2.1 (10 pints) Write a Boolean equation in **sum-of-products canonical form** for each of the following truth tables.

2.2 (10 pints) **Minimize** each of the Boolean equations in 2.1.

2.3 (10 pints) Sketch a reasonably **simple combinational circuit** implementing each of the functions in 2.2.

2.4 (10 pints) Write **Boolean equations** for the following circuit. You **need not minimize** the equations.



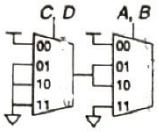
2.5 (10 pints) Find a **minimal Boolean equation** for the function in the following figure. Remember to take advantage of the **don't care** entries.

A	B	C	D	Y
0	0	0	0	X
0	0	0	1	X
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	X
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

2.6 (10 pints) A circuit has four inputs and two outputs. The inputs $A_{3:0}$ represent a number from 0 to 15. Output P should be TRUE if the number is prime (0 and 1 are not prime, but 2, 3, 5, and so on, are prime). Output D should be TRUE if the number is divisible by 3. (Note: 0 is divisible by any non-zero integer.) Give the **truth tables** and **simplified Boolean**

equations for each output.

2.7 (10 pints) Write the **truth table** and the **minimized Boolean equation** for the function performed by the circuit in the following figure.



2.8 (20 pints) **Implement** the function (**sketch a circuit**) from the following truth table using

(a) (6 pints) an 8:1 multiplexer

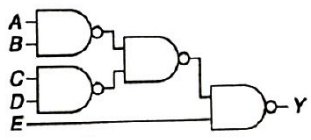
(b) (7 pints) a 4:1 multiplexer and one inverter

(c) (7 pints) a 2:1 multiplexer and two other logic gates

	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

2.9 (10 pints) Determine the **propagation delay** and **contamination delay** of the circuit in following figure. Use the gate delays given in the following table.

Gate	t_{pd} (ps)	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40



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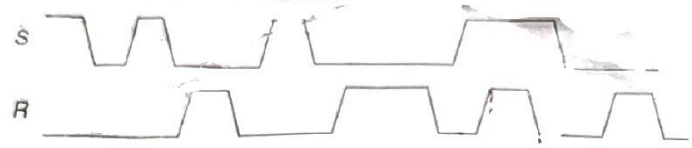
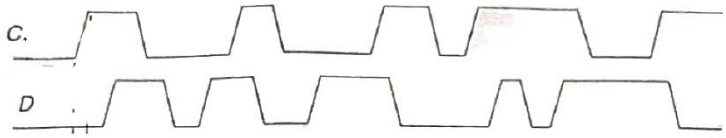
3.1 (20 points) Given the input waveforms shown in the following figure, sketch the **output Q** of an SR latch. (Hint: You had better draw a truth table

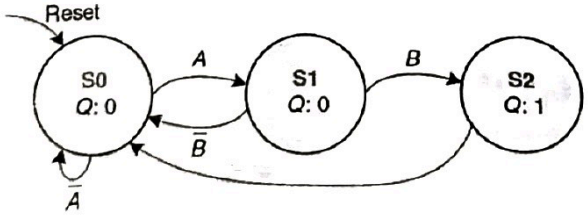


3.2 (20 points) Given the input waveforms shown in the following figure, sketch the **output Q** of a D latch. (Hint: You had better draw a truth table first.)



3.3 (20 points) You are designing an FSM to keep track of the mood of four students working in the digital design lab. Each student's mood is either HAPPY (the circuit works), SAD (the circuit blew up), BUSY (working on the circuit), CLUELESS (confused about the circuit), or ASLEEP (face down on the circuit board). **How many states** does the FSM have? What is **the minimum number of bits necessary to represent these states**? (Hint: For the second question, think about state encoding methods.)

3.4 (40 points) Describe in words **what the state machine** in the following figure does. Using **binary state encodings,** complete a **state transition table** and **output table** for the FSM. Write **Boolean equations** for the next state and output logic, and **sketch a schematic** of the FSM. (Hint: Recall the FSM design methodology.)



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4.1 Write a Boolean equation in **sum-of-products canonical form** for each of the truth tables in the following figure.

(a)

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(b)

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

4.2 **Minimize** each of the Boolean equations from 4.1.

4.3 Sketch a reasonably **simple combinational circuit** implementing each of the functions from 4.2.

4.4 Is the circuit in the following figure combinational logic or sequential logic? Explain in a simple fashion what the **relationship is between the inputs and outputs**. What would you call this circuit? (Hints: You had better draw a truth table first. Recall the names of circuits you learned in Chapter 3 and make some modification to the name.)

4.5 Convert the following two's complement binary fixed-point numbers to base 10. The implied binary point is explicitly shown to aid in your interpretation.

(a) 0101.1000

(b) 1111.1111

(c) 1000.0000

4.6 Implement the following functions using a single 16 × 3 ROM. Use dot notation to indicate the ROM contents.

(a) $X = \overline{AB} + B\overline{C}D + AB$

(b) Y = AB+BD

(c) Z = A+B+C+D

(Hint: Write the truth table first.)