Computer Organization & Architecture

7-5 Direct Memory Access

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Contents of this lecture

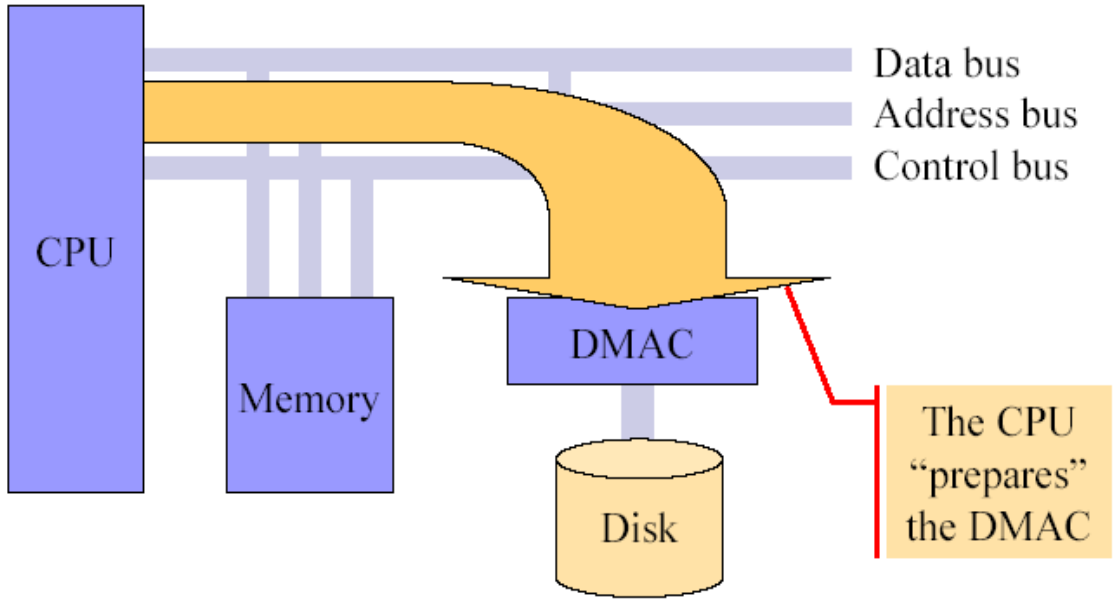
- Communication Methods with CPU
  - Program-controlled I/O (Polling)
  - Interrupt-driven I/O
  - Direct Memory Access (DMA)

Direct Memory Access

- Interrupt driven and programmed I/O require active CPU intervention.
  - Transfer rate is limited
  - CPU is tied up in managing an I/O transfer
- Solution: Direct Memory Access (DMA)
  - Used for high-speed block transfers directly between an external device and the main memory
  - A DMA controller is provided to take over control of the system from CPU
  - During the transfer, the CPU is not involved

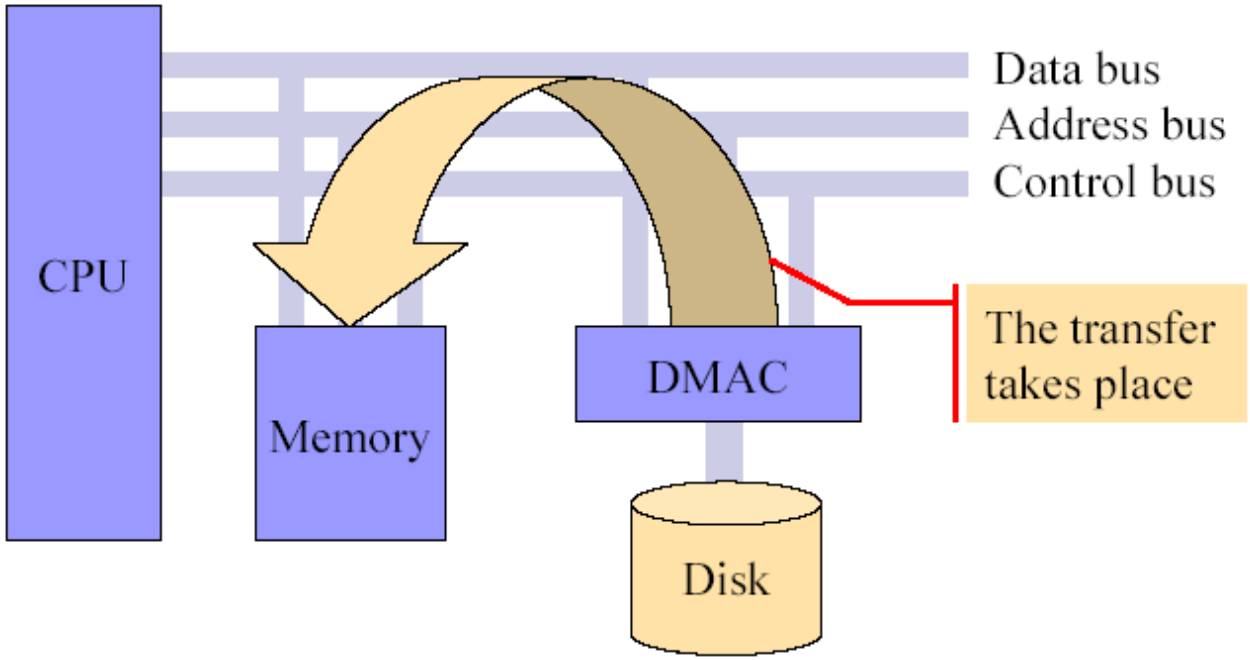
DMA Operation (1)

- Program-Controlled I/O in DMA
  - The CPU “prepares” the DMA operation by transferring information to a DMA controller(DMAC).
    - Location of the data on the device
    - Location of the data in memory
    - Size of the block to transfer
    - Direction of the transfer
    - Mode of transfer (burst, cycle steal)



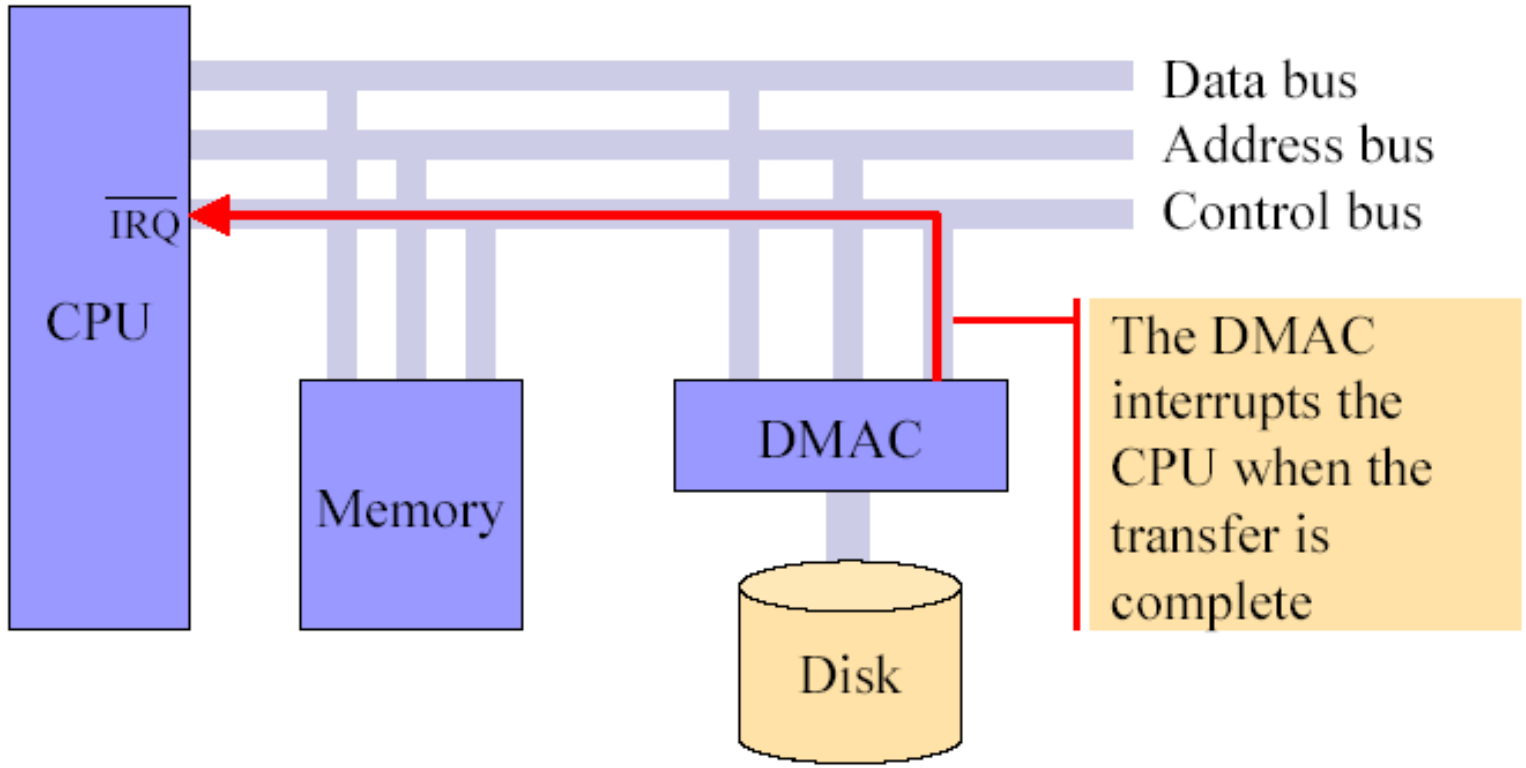
DMA Operation (2)

- DMAC controls data transfer
  - When the device is ready to transfer data, the DMAC takes control of the system buses (DMAC deals with transfer), and CPU carries on with other work.



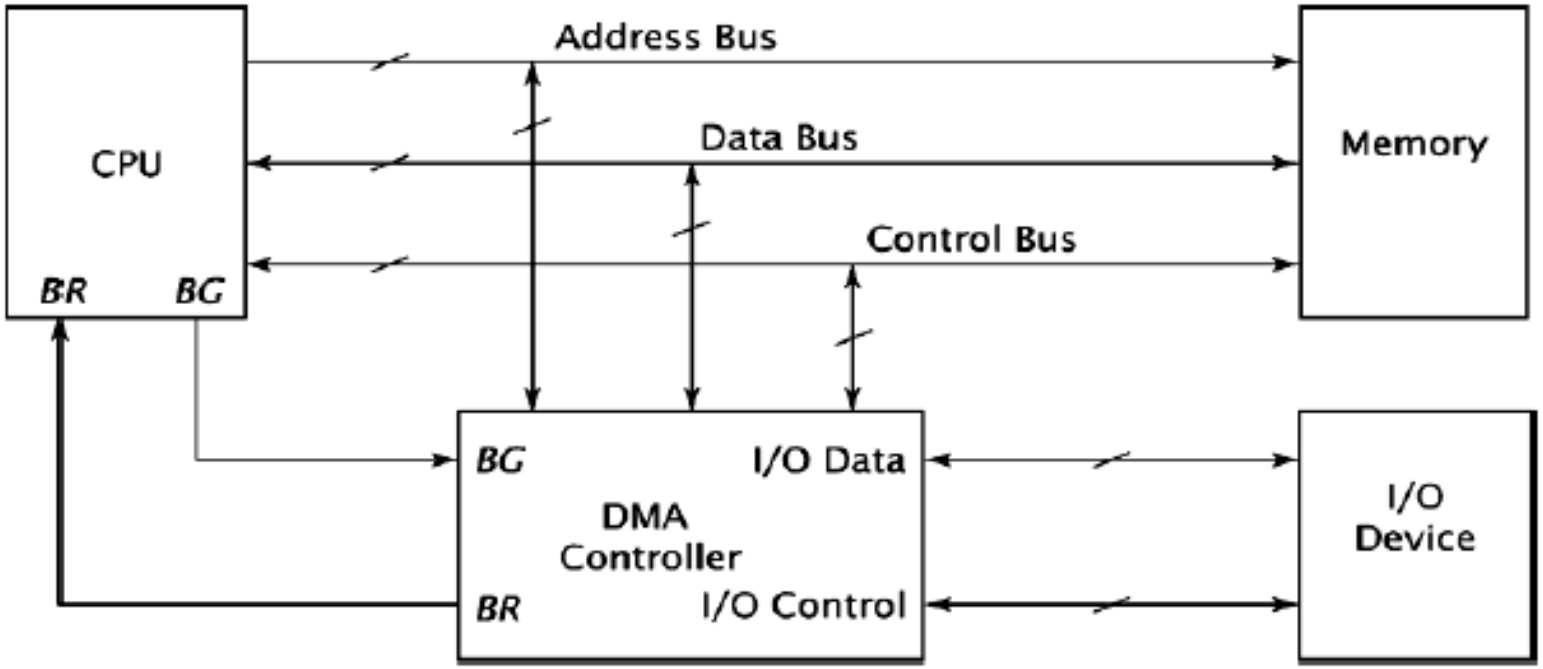
DMA Operation (3)

- I/O Interrupt in DMA
  - DMAC sends interrupt when finished.



DMA Controller (1)

- A computer system with DMA controller



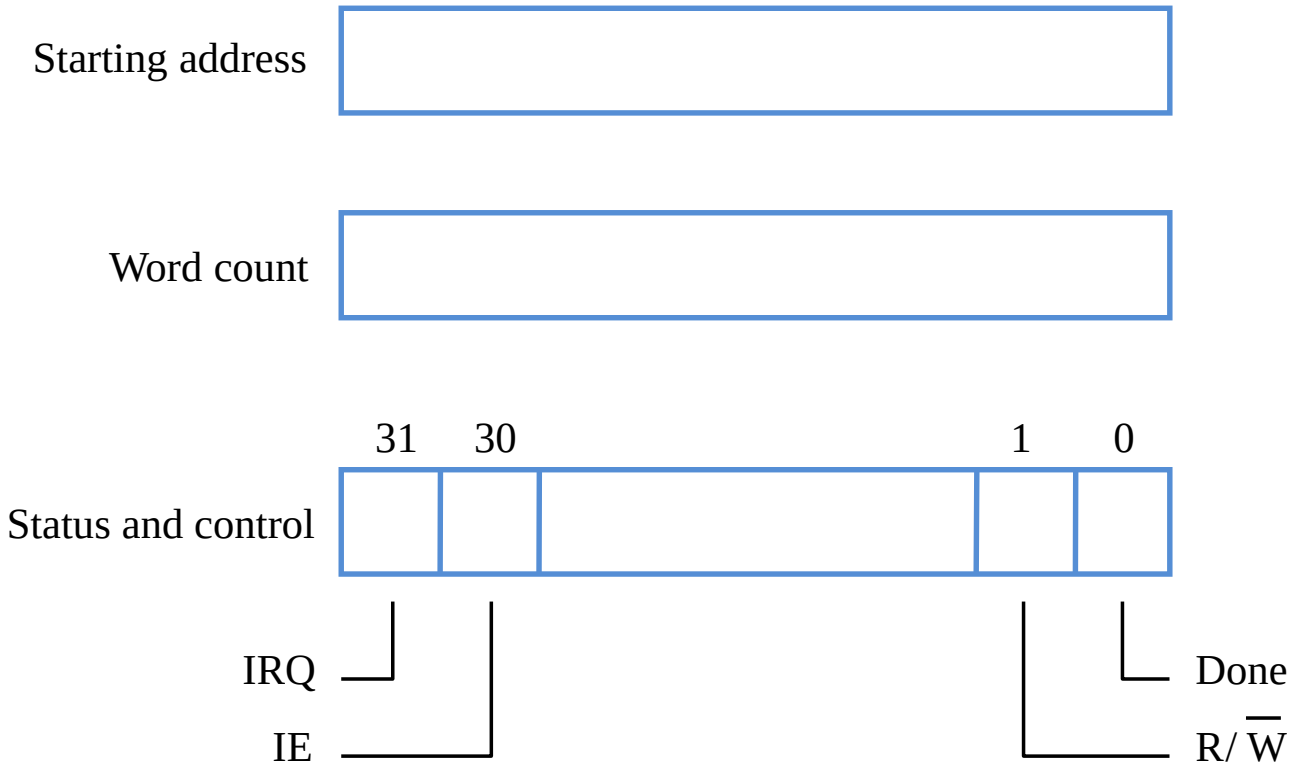
- BR: Bus Request BG: Bus Grant

DMA Controller (2)

- Function of DMA Controller
  - Take over control of the data transfer between the memory and I/O devices.
  - For words transferred, the DMA controller
    - Provides the memory address
    - Provides all the bus signal that control data transfer
    - Increases the memory address for successive words
    - Keeps track of the number of transfers

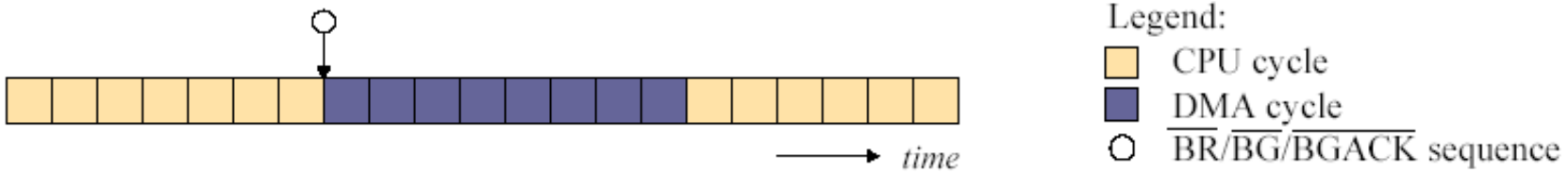
DMA Controller (3)

- Registers in a DMA interface



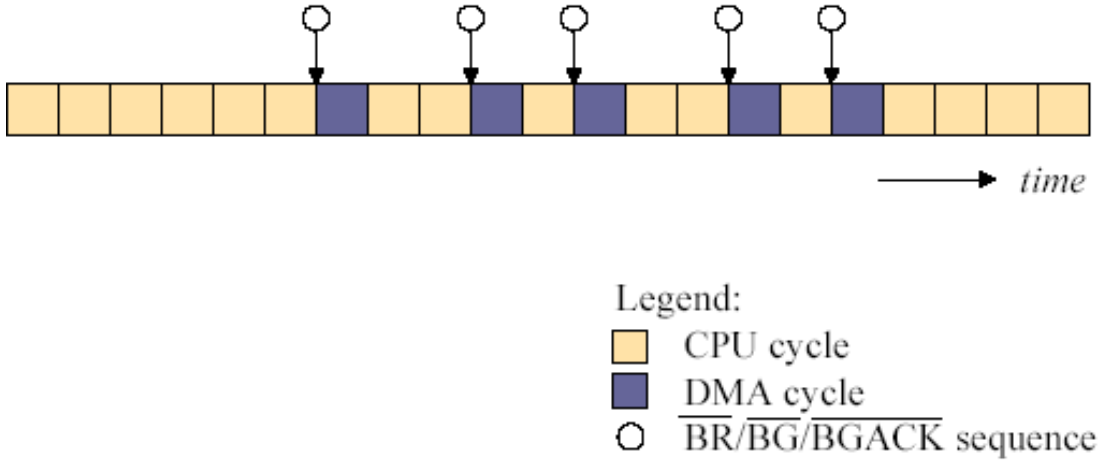
DMA Transfer Mode (1)

- Burst Mode (Block Mode)
  - Once the DMA controller is granted access to the system bus by the processor, it transfers all bytes of data in the data block before relinquishing control of the system bus back to the processor.
  - Usage: It is useful for loading programs or data files into memory.
  - Disadvantage
    - Render the processor inactive for relatively long periods of time
    - Low CPU efficiency



DMA Transfer Mode (2)

- Cycle Stealing Mode
  - Once the DMA controller obtains access to the system bus, it transfers one byte of data and then returns the control of system bus to the processor.
  - It continually issues requests, transferring one byte of data per request, until it has transferred its entire block of data.

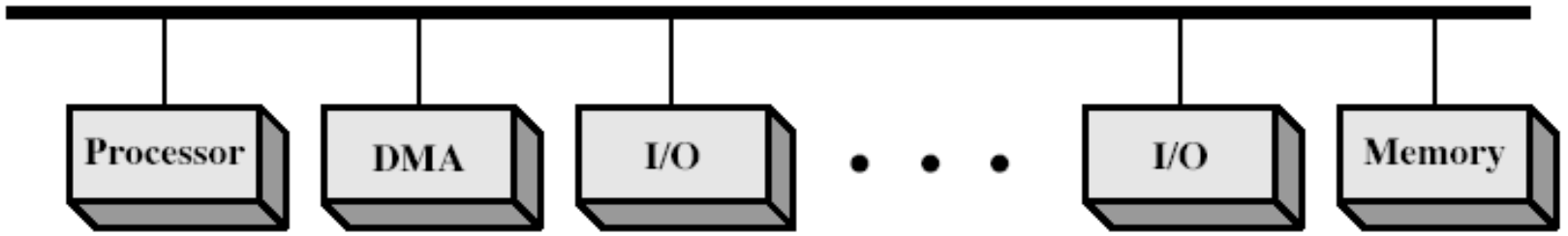


DMA Transfer Mode (3)

- Transparent Mode
  - The DMA controller only transfers data when the CPU is performing operations that do not use the system bus.
  - Note: The DMA controller does not need to request the control of the system bus.
  - Advantage
    - Processor never stops executing its program.
  - Disadvantage
    - The hardware needed to determine when the processor is not using the system bus can be quite complex and relatively expensive.

DMA Configurations (1)

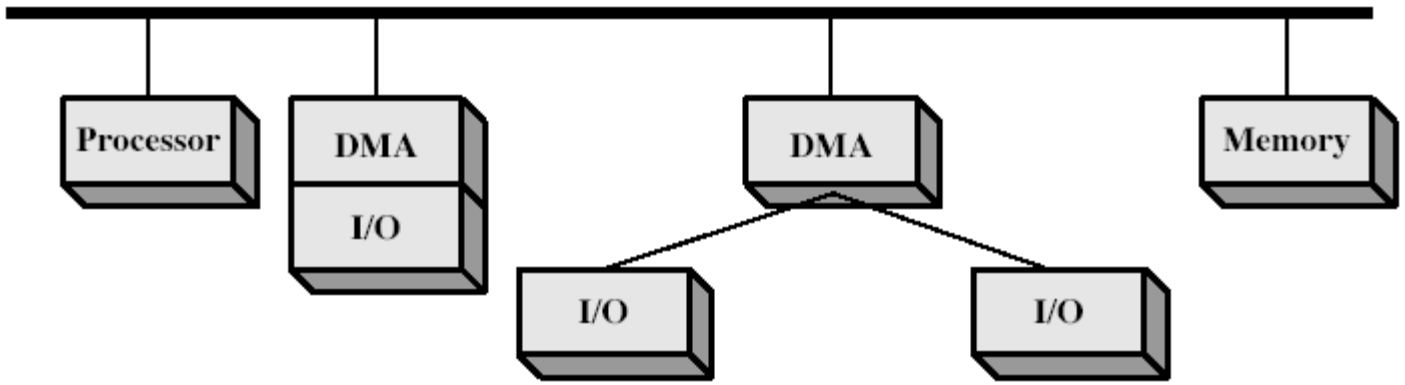
- Single-bus, Detached DMA Controller
  - Each transfer uses bus twice
    - I/O to DMA then DMA to memory
  - CPU is suspended twice



(a) Single-bus, detached DMA

DMA Configurations (2)

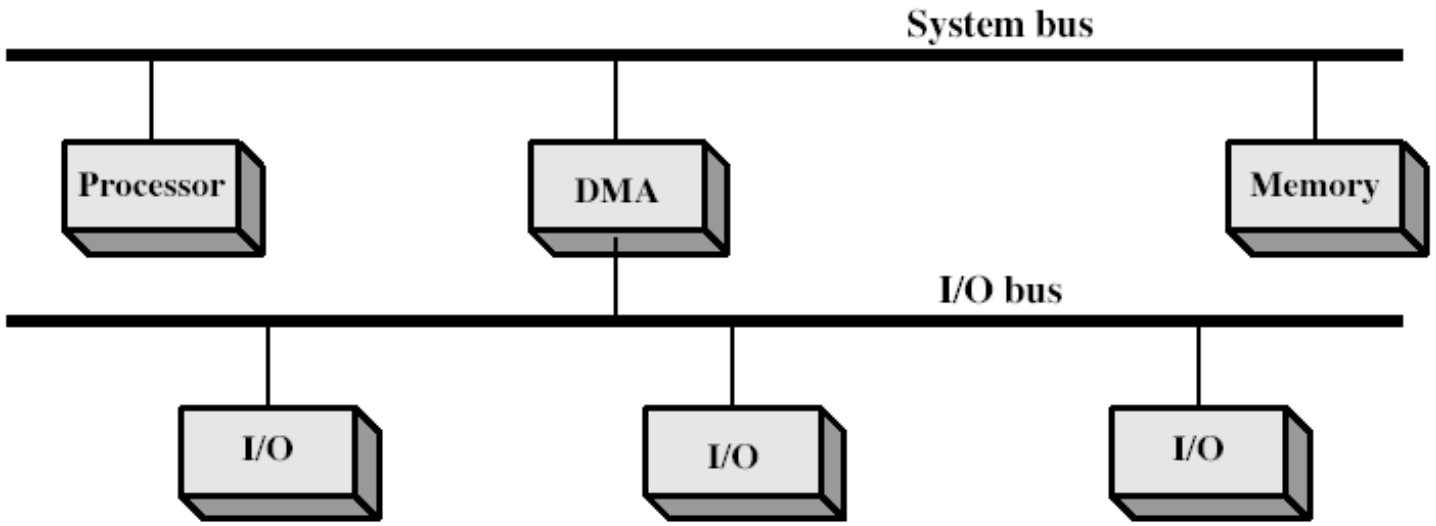
- Single-bus, Integrated DMA Controller
  - Controller may support more than one device
  - Each transfer uses bus once
    - DMA to memory
  - CPU is suspended once



(b) Single-bus, Integrated DMA-I/O

DMA Configurations (3)

- Separate I/O bus
  - Bus supports all DMA enabled devices
  - Each transfer uses bus once
    - DMA to memory
  - CPU is suspended once



(c) I/O bus

Quiz (1)

1. Which method bypasses the CPU for certain types of data transfer?

   A. Software interrupts
   B. Polled I/O
   C. Interrupted-driven I/O
   D. Direct Memory Access (DMA)

2. _____ is used for high-speed block transfers directly between an external device and the main memory.

   A. Program-controlled I/O
   B. Interrupt-driven I/O
   C. DMA approach
   D. Event-driven

Quiz (2)

3.Once the DMA controller obtains access to the system bus, it transfers one byte of data and then returns the control of system bus to the processor. This is _____.

A. burst mode

B. block mode

C. cycle stealing mode

D. transparent mode

Homework

- 3.1
- 3.3