Computer Organization & Architecture

2-4 Design of Fast Adders

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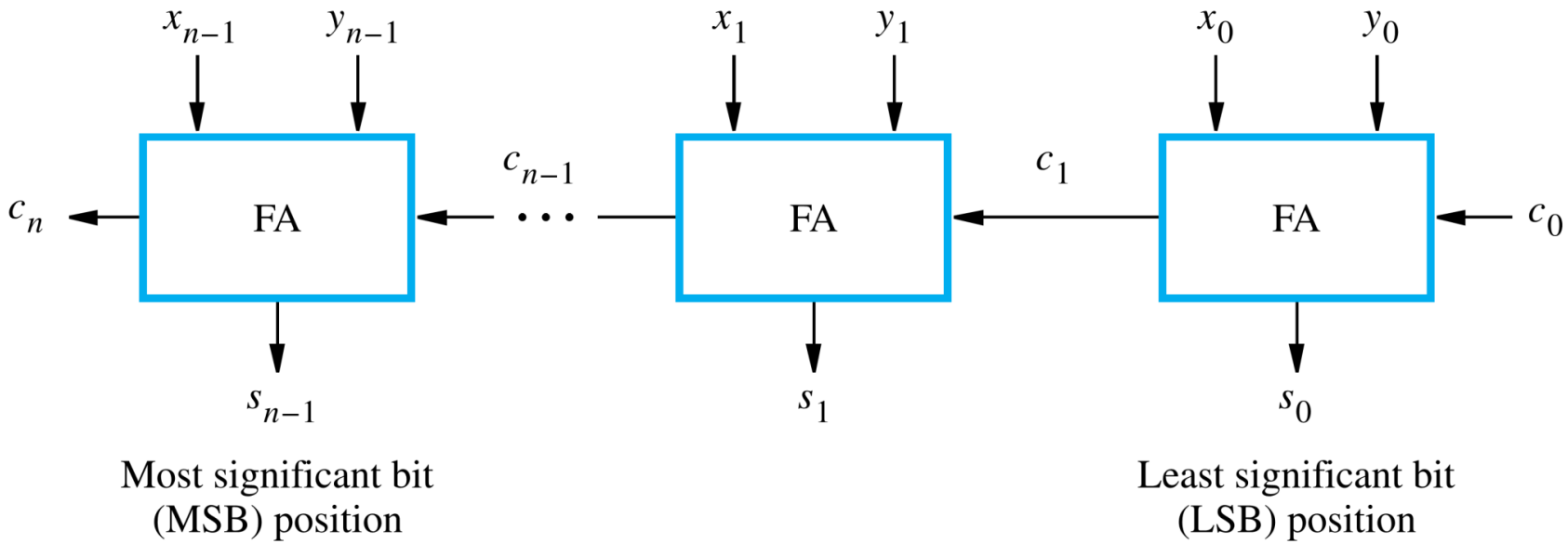
- n-bit Ripple Carry Adder Delay Analysis



S_{n-1} $2(n-1)T+T=(2n-1)T$

c_n $2(n-1)T+2T=(2n)T$

Drawback of n-bit Ripple-Carry Adder

- Drawback
  - It may have too much delay in developing its outputs, s_0 through s_{n-1} and c_n.
    - s_{n-1} $(2n-1)T$
    - c_n $(2n)T$
- Solutions
  - Use the fastest possible electronic technology in implementing the ripple-carry logic design or variations of it.
  - Use an augmented logic gate network structure

Carry-Lookahead Addition (1)

- Generate Function and Propagate Function

$$s_i = x_i \oplus y_i \oplus c_i$$

$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$

$$= x_i y_i + (x_i + y_i) c_i$$

$G_i = x_i y_i$ (generate function for stage i)

$P_i = x_i + y_i$ (propagate function for stage i)

$$c_{i+1} = G_i + P_i c_i$$

Carry-Lookahead Addition (2)

- A Simpler Circuit of Bit Stage

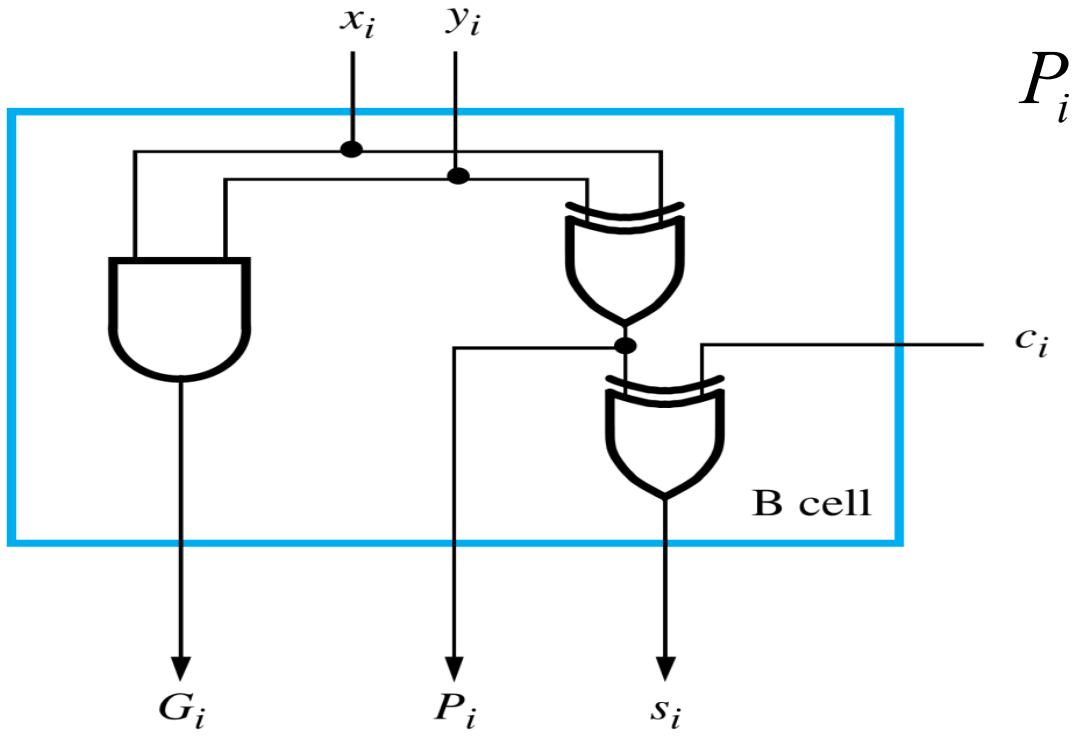


Figure 9.4 (a) Bit-stage cell

$$P_i = x_i + y_i \longrightarrow P_i = x_i \oplus y_i$$

x_i	y_i	x_i+y_i	$x_i \oplus y_i$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

if $x_i = 1$ and $y_i = 1$

$$c_{i+1} = G_i + P_i c_i = 1 + P_i c_i = 1$$

Carry-Lookahead Addition (3)

- Logic Functions Extension

$$s_i = x_i \oplus y_i \oplus c_i$$

$$c_{i+1} = G_i + P_i c_i$$

$$= G_i + P_i(G_{i-1} + P_{i-1}c_{i-1})$$

$$= G_i + P_i G_{i-1} + P_i P_{i-1} c_{i-1}$$

$$\cdots$$

$$= G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + \ldots + P_i P_{i-1} \ldots P_1 G_0 + P_i P_{i-1} \ldots P_0 c_0$$

Carry-Lookahead Addition (4)

- Delays of n-bit CLA
  - All carries can be obtained 3 gate delays after the input signal X, Y and c_0 are applied.
  - All sum bits are available 4 gate delays after the input signal X, Y and c_0 are applied.

4-bit Carry-Lookahead Adder (1)

- Logic Functions of 4-bit Carry-Lookahead Adder

$$s_i = x_i \oplus y_i \oplus c_i \qquad i = 0,1,2,3$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 G_0 + P_1 P_0 c_0$$

$$c_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0$$

$$c_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0$$

4-bit Carry-Lookahead Adder (2)

- Figure of 4−bit Carry-Lookahead Adder

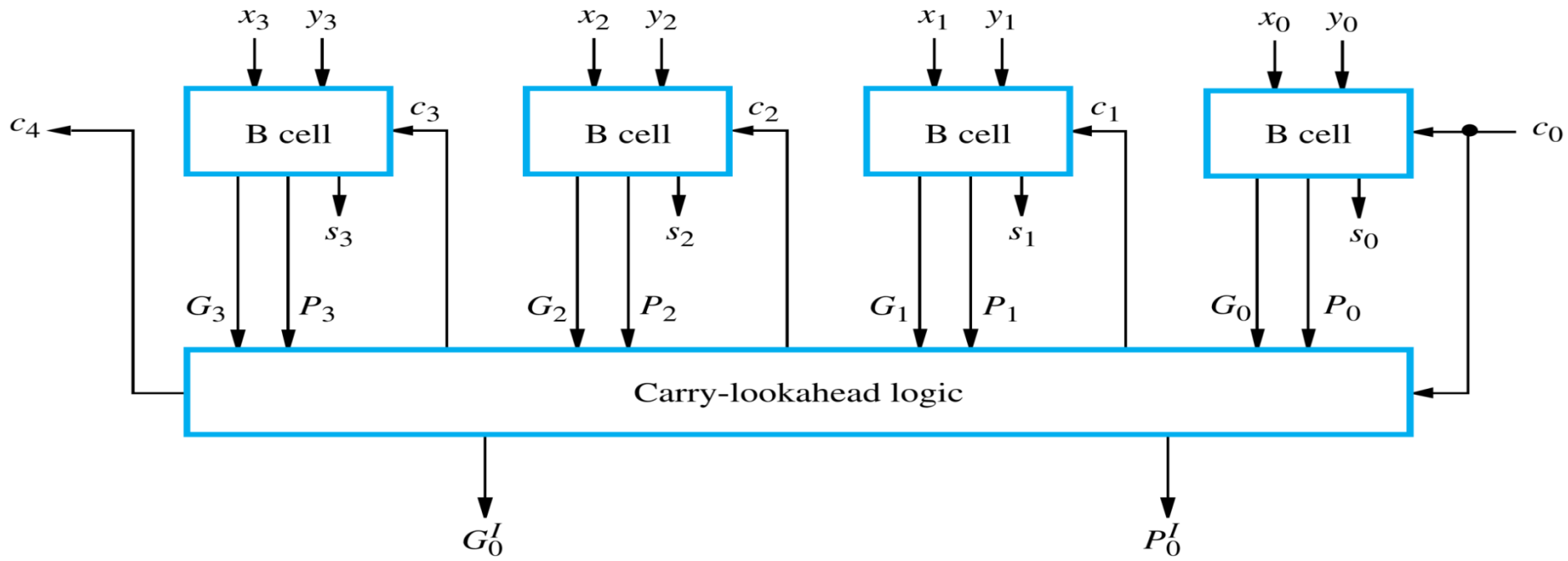


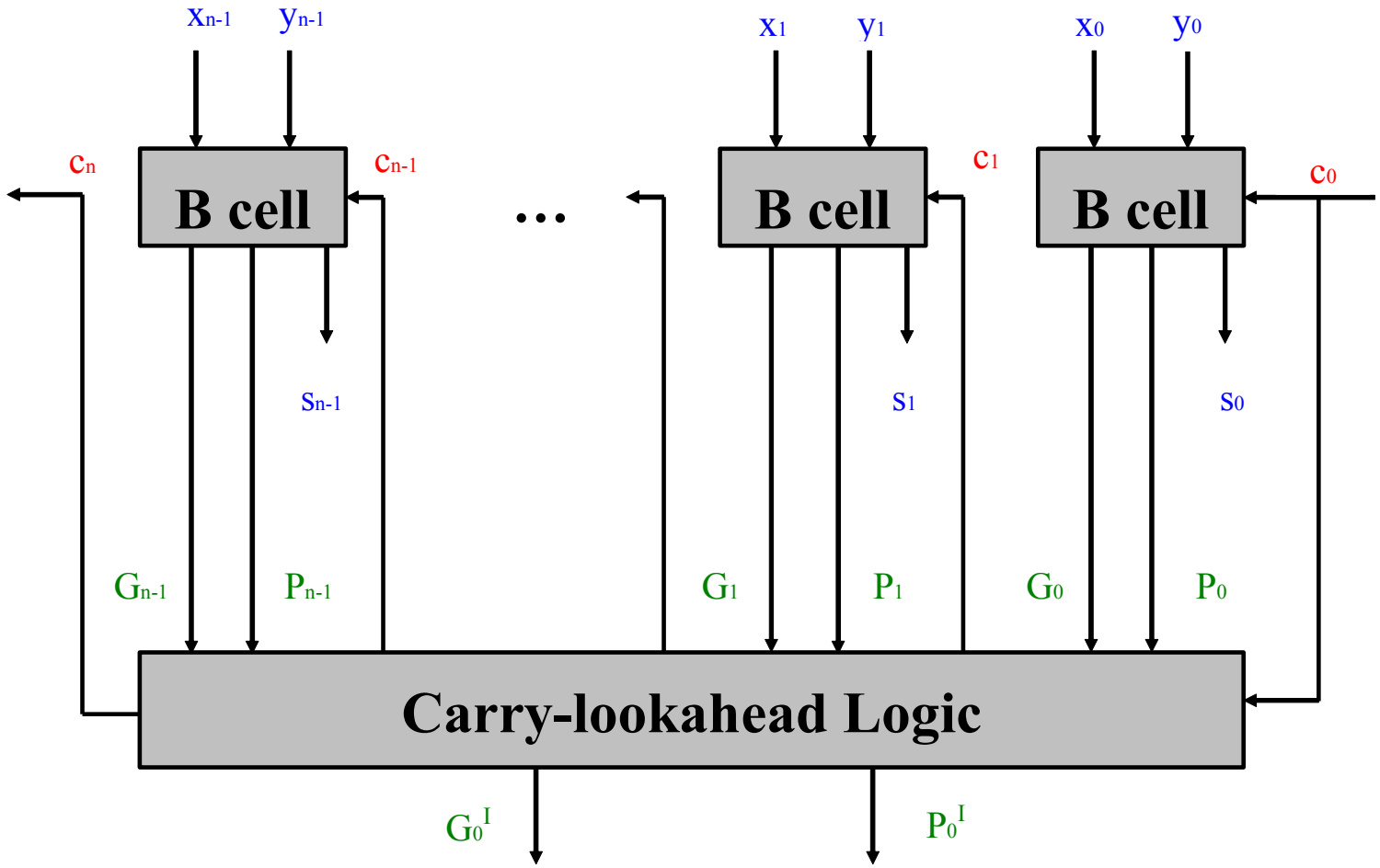
Figure 9.4 (b) 4-bit carry-lookahead adder

4-bit Carry-Lookahead Adder (3)

- Delay Comparison
  - 4-bit Carry-Lookahead Adder
    - $c_1 \quad c_2 \quad c_3 \quad c_4$ 3T
    - $s_0 \quad s_1 \quad s_2 \quad s_3$ 4T
  - 4-bit Ripple-Carry Adder
    - c_4 8T
    - s_3 7T

Build Longer Carry-Lookahead Adder (1)

- The 4-bit carry-lookahead adder design cannot be directly extended to longer operand sizes.



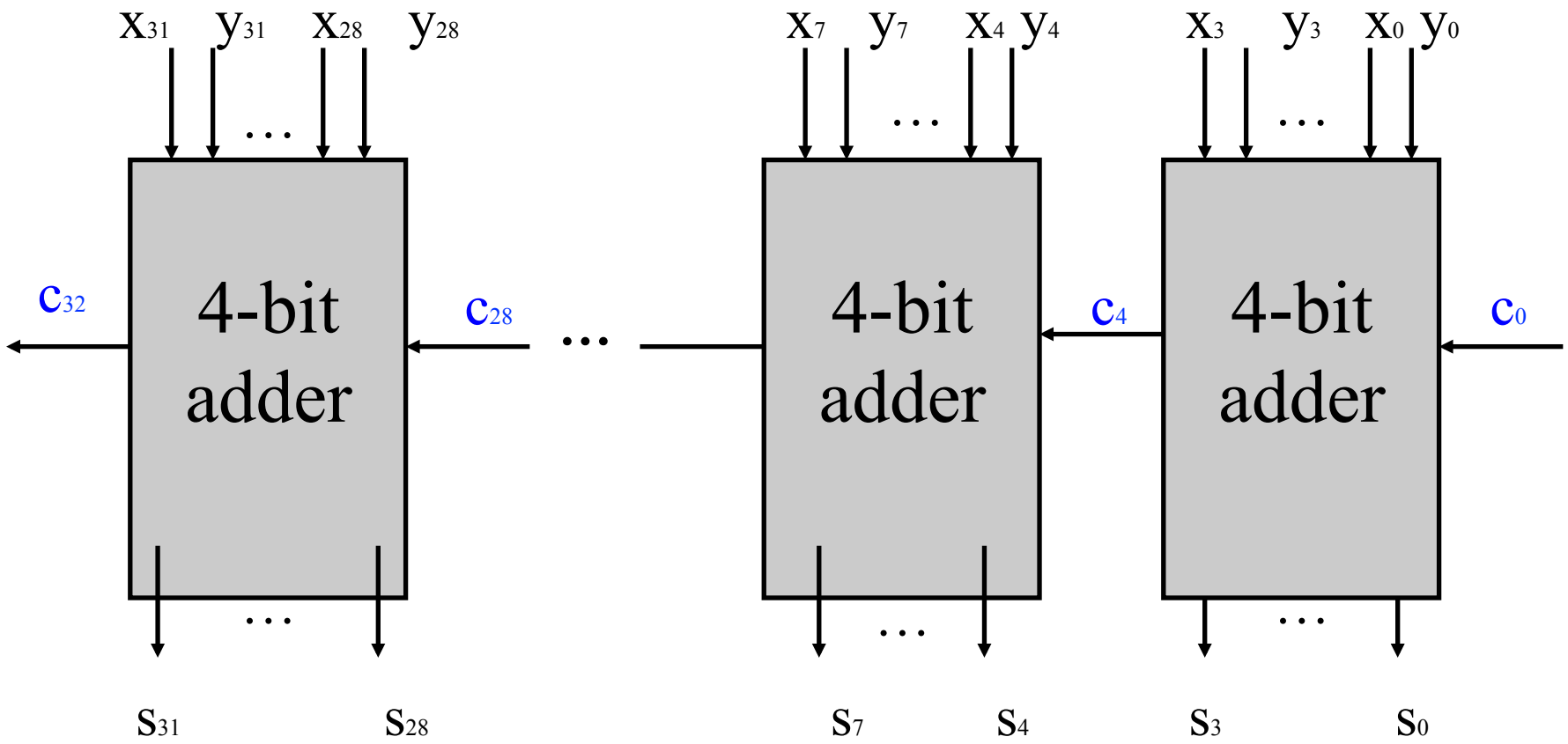
Build Longer Carry-Lookahead Adder (2)

- Fan-In Constraints
  - Fan-in: The number of inputs to a logic gate is called its fan-in.
  - Fan-out: The number of gate inputs that the output of a logic gate drives is called its fan-out.
  - Practical circuits do not allow large fan-in and fan-out because they both have an adverse effect on the propagation delay and hence the speed of the circuit.
  - Example: Fan-in of the last AND gate and the OR gate is i+2 in generating c_{i+1}.

$$c_{i+1} = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + \ldots + P_i P_{i-1} \ldots P_1 G_0 + P_i P_{i-1} \ldots P_0 c_0$$

Build Longer Carry-Lookahead Adder (3)

- Build 32-bit Adders with 4-bit Adders
  - Cascade of 8 4-bit Carry-Lookahead Adders



Build Longer Carry-Lookahead Adder (4)

- Build 32-bit Adders with 4-bit Adders (ctd.)
  - Calculate the delays in generating sum bits s_{28}, s_{29}, s_{30},s_{31}, and c_{32} in the high-order 4-bit adder.

c_4 3T c_8 3T+2T=5T

c_{12} 5T+2T …

c_{28} (6×2)T+3T=15T

c_{29} c_{30} c_{31} c_{32} 15T+2T=17T

s_{28} s_{29} s_{30} s_{31} 17T+T=18T

Ripple carry adders:

$S_{31} = (2n-1)T$

$= 2(2\times32-1)T = 63T$

$C_{32} = 2nT$

$= 2\times32T = 64T$

Quiz (1)

- A 16-bit ripple-carry adder is used to add two numbers X(x15x14…x1x0) and Y(y15y14…y1y0) to generate a 16-bit sum S(s15s14…s1s0). How many gate delays are required to compute s13 after all the inputs have been applied?

  A. 8 B. 25 C. 27 D. 31

- The advantage of carry-lookahead adder is_____.

  A. Optimize the structure of the adder

  B. Save hardware parts

  C. Augment the structure of the adder

  D. Accelerate the generation of the carries

Quiz (2)

- In carry-lookahead adder, which expression is called the propagate function Pi for stage i?

  A. x_i+y_i B. $x_i \oplus y_i$ C. x_iy_i D. $x_i \oplus y_i \oplus c_i$

- In carry-lookahead adder, which expression is called the generate function Gi for stage i?

  A. xi+yi B. xi ⊕ yi C. xiyi D. xi ⊕ yi ⊕ ci

- Ture or False? In a 4-bit carry-lookahead adder, all carries can be obtained 3 gate delays after the input signal X, Y and c0 are applied.