Computer Organization & Architecture

2-2 Addition and Subtraction of Signed Numbers

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- Subtraction of *n*-bit Signed Numbers

Addition of 1-bit Positive Numbers

- Addition of 1-bit Positive Numbers

$$\begin{array}{r} 0 \\ +\,0 \\ \hline 0 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 1 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

Carry-out

Addition of n-bit Signed Numbers (1)

- Addition Rule of n-bit Signed Numbers (In Signed 2's Complement Form)
  - To add two numbers, add their n-bit representations, treating the sign bit as the most significant bit (MSB), ignoring the carry-out signal from the MSB position.
  - The sum will be algebraically correct value in the two's-complement representation as long as the answer is in the range -2^{n-1} through $+2^{n-1}-1$.

Addition of n-bit Signed Numbers (2)

- Examples of 4-bit Signed Numbers Addition
  - Textbook P14 Figure 1.6 (a)-(d)

(a)	0 0 1 0	(+2)	(b)	0 1 0 0	(+4)
	+ 0 0 1 1	(+3)		+ 1 0 1 0	(–6)
	0 1 0 1	(+5)		1 1 1 0	(–2)
(c)	1 0 1 1	(–5)	(d)	0 1 1 1	(+7)
	+ 1 1 1 0	(–2)		+ 1 1 0 1	(–3)
	1 0 0 1	(–7)		0 1 0 0	(+4)

Addition of n-bit Signed Numbers (3)

- Examples of 4-bit Signed Numbers Addition (ctd.)
  - Overflow Examples
    - (+5) + (+4) = (+9)

$$\begin{array}{r} 0\ 1\ 0\ 1 \\ +0\ 1\ 0\ 0 \\ \hline 1\ 0\ 0\ 1 = (-7) \end{array} \longleftarrow \textbf{overflow}$$

    - (-6) + (-7) = (- 13)

$$\begin{array}{r} 1\ 0\ 1\ 0 \\ +1\ 0\ 0\ 1 \\ \hline \underline{1}\ 0\ 0\ 1\ 1 = (+3) \end{array} \longleftarrow \textbf{overflow}$$

Addition of n-bit Signed Numbers (4)

- Arithmetic Overflow
  - The result of an arithmetic operation is outside the representable range.
  - Sufficient and Necessary Condition
    - If two numbers are added, and they have the same sign, then overflow occurs if and only if the result has the opposite sign to both summands.
  - Note: The carry-out signal from the sign-bit position is not a sufficient indicator of overflow when adding signed numbers. Overflow can occur whether or not there is a carry-out.

Subtraction of n-bit Signed Numbers (1)

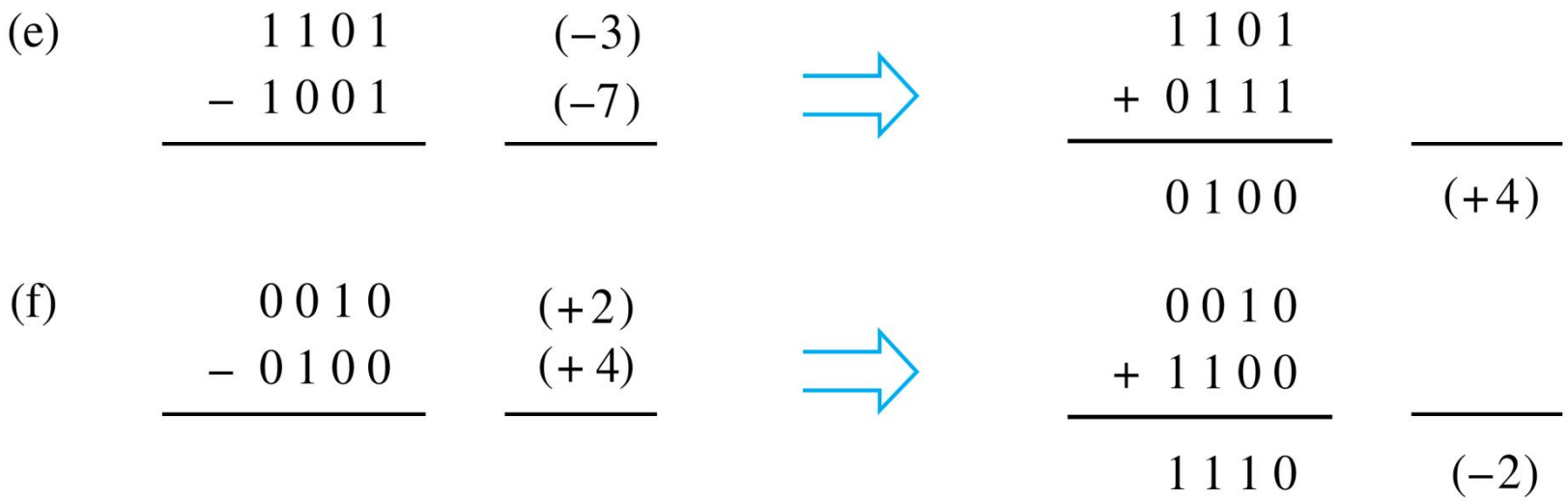
- Subtraction Rule of n-bit Signed Numbers (In Signed 2's Complement Form)
  - To subtract two numbers X and Y, that is, to perform X—Y, form the 2's-complement of Y and then add it to X, as in Addition Rule.
  - The result will be the algebraically correct value in the 2's-complement representation system if the answer is in the range -2^{n-1} through $+2^{n-1}-1$.
  - Essence of Subtraction Rule
    - X—Y= X + (—Y)

Subtraction of n-bit Signed Numbers (2)

- 2's Complement Operation (Negation Operation)
  - Take the Boolean complement of each bit of the integer (*including the sign bit*). That is ,set each 1 to 0 and each 0 to 1.
  - Treating the result as an unsigned binary integer, add 1.
  - Example
    - Y=6 and it can be represented by 0110 using signed 2's complement form. What is the signed 2's complement form of –Y?
    - Solution:
      - Because Y=0110, after negation 1001
      - So (–Y) =1001+0001=1010

Subtraction of n-bit Signed Numbers (3)

- Examples of 4-bit Signed Numbers Subtraction
  - Textbook P14 Figure 1.6 (e)-(f)



Subtraction of n-bit Signed Numbers (4)

- Examples of 4-bit Signed Numbers Subtraction (ctd.)
  - Overflow Example
    - X = 6, Y = -7 , X – Y = ?

      X = 6 = 0110, Y = -7 = 1001, (- Y) = 0111

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   0 1 1 0
 + 0 1 1 1
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   1 1 0 1 = (-3)   <-------- overflow
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Subtraction of n-bit Signed Numbers (5)

- Conclusions
  - The examples in Figure 1.6 (P14) show that two, n-bit, signed numbers can be added using n-bit binary addition, treating the sign bit the same as the other bit.
  - In other words, a logic circuit that is designed to add unsigned binary numbers can also be used to add signed numbers in 2's-complement.

Quiz

- Assume that X and Y are two 8-bit signed two's complement numbers 01011110 and 11001010. What is the result of X+Y?

  A. 00101000 B. 10010100 C. 01000100 D. 00011100

- Assume that X and Y are two 8-bit signed two's complement numbers 01011110 and 11001010. What is the result of X-Y?

  A. 00101000 B. 10010100 C. 01000100 D. overflow

- True or False? Subtracting a negative integer from another negative integer in 2’s-complement binary arithmetic can cause an overflow.