Computer Organization & Architecture

3-4 Structure of Larger Memories

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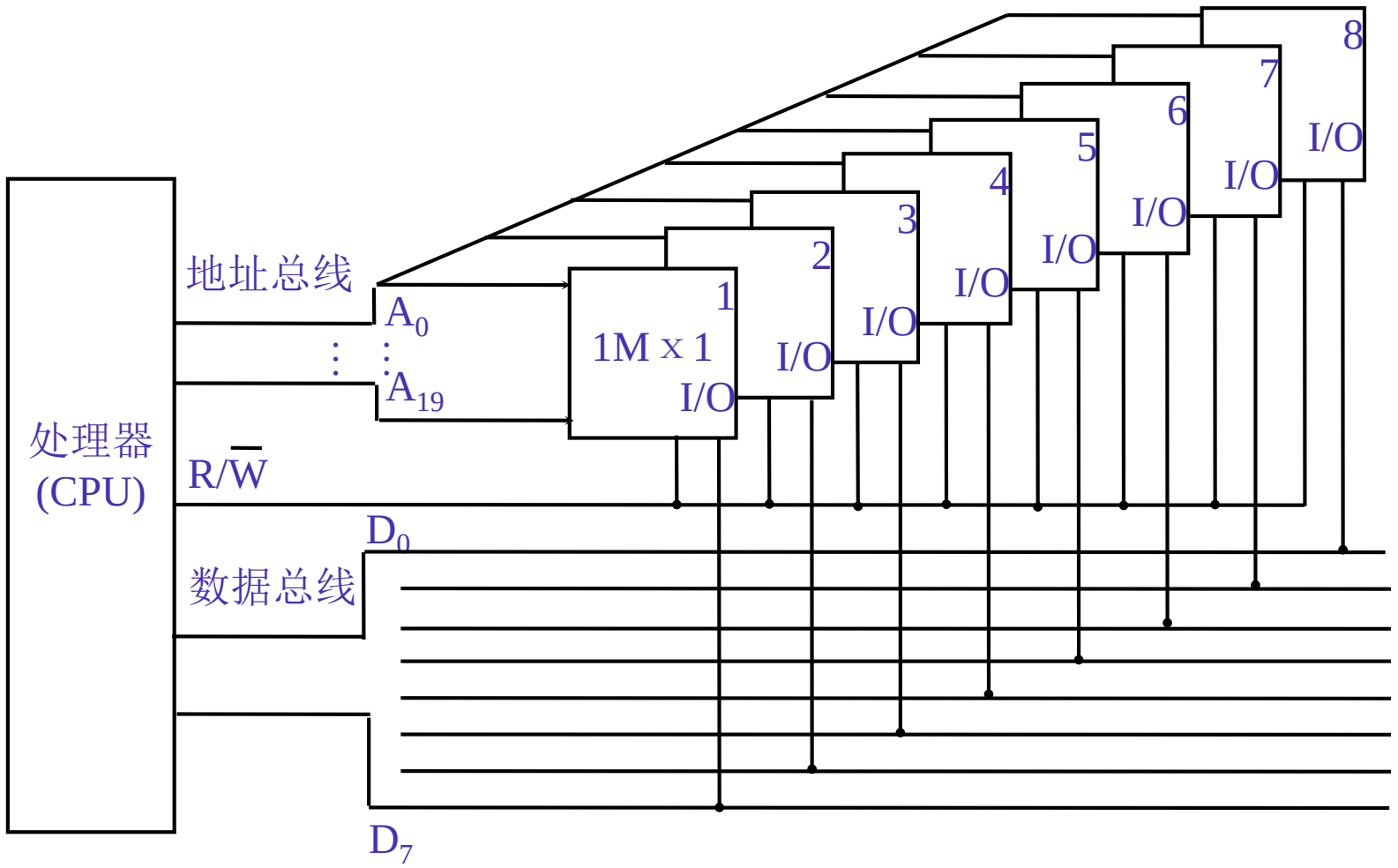
Contents of this lecture

- Static Memory Systems
  - How to connect a number of static memory chips to form a much larger memory?
- Dynamic Memory Systems
  - How to connect a number of dynamic memory chips to form a much larger memory?

Static Memory System (1)

- 位扩展法
  - 芯片每个存储单元的位数小于存储器字长，需进行位扩展
  - 例：用1M×1位存储芯片组成1M×8位 (1MB)的存储器
    - 共需8片1M×1位的芯片，每片存储同一位权的一位数据(片的I/O端接D_i)
    - 访问芯片需20位地址码A_{19}~A_0
    - 读写控制信号R/$\overline{W}$

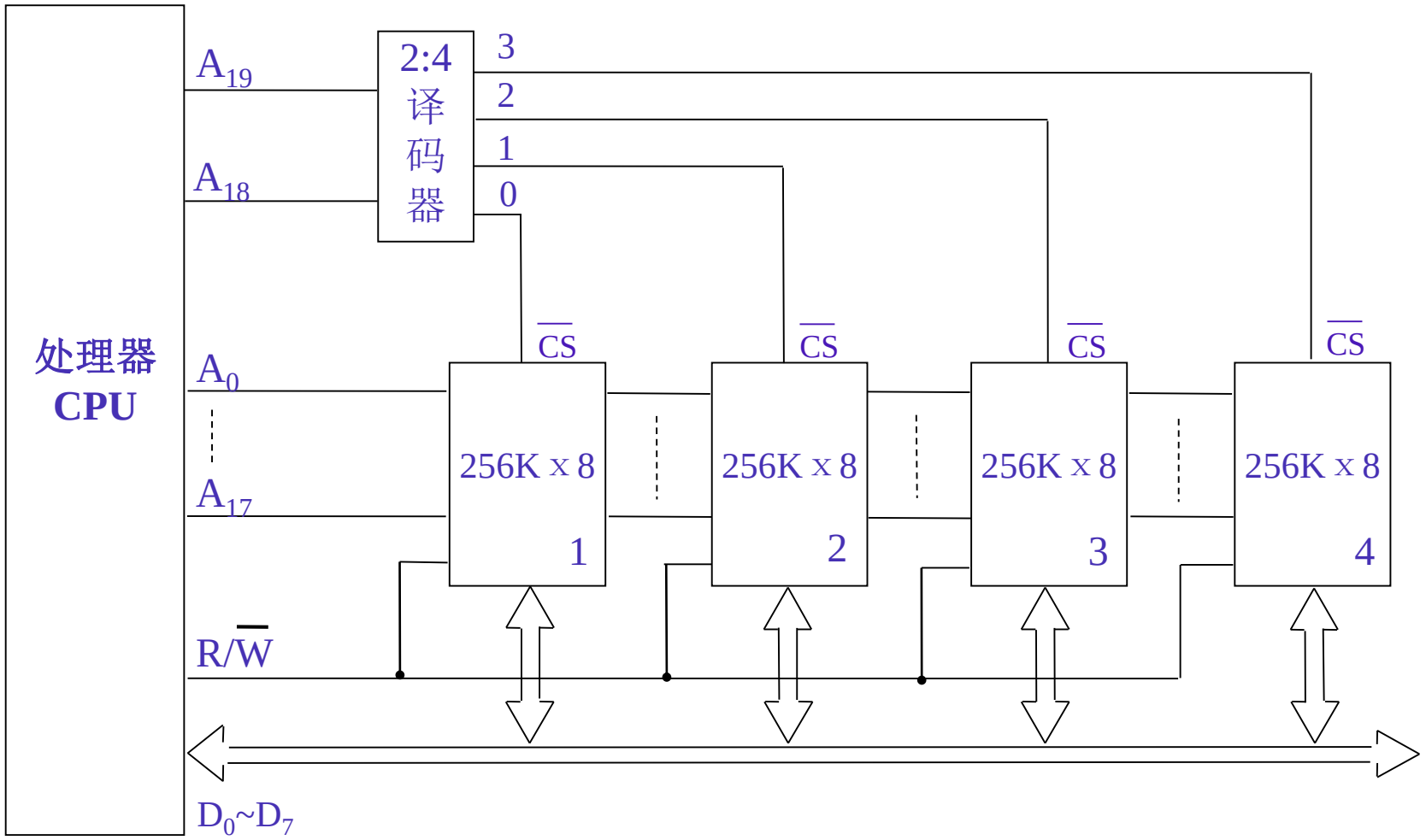
Static Memory System (2)



Static Memory System (3)

- 字扩展法
  - 芯片每个存储单元的位数等于存储器字长，但容量(字数)不够，需进行字扩展
  - 例：用256K×8位芯片组成1M×8的存储器
    - 共需1M/256K=4片256K×8位的芯片
    - 1MB容量需20位地址码(A_{19}~A_0)，而256KB芯片需18位片内地址码(A_{17}~A_0)
    - 用高二位地址$A_{19}A_{18}$经2:4译码器选择芯片读/写
    - 每片8条I/O线分别接D_7~D_0

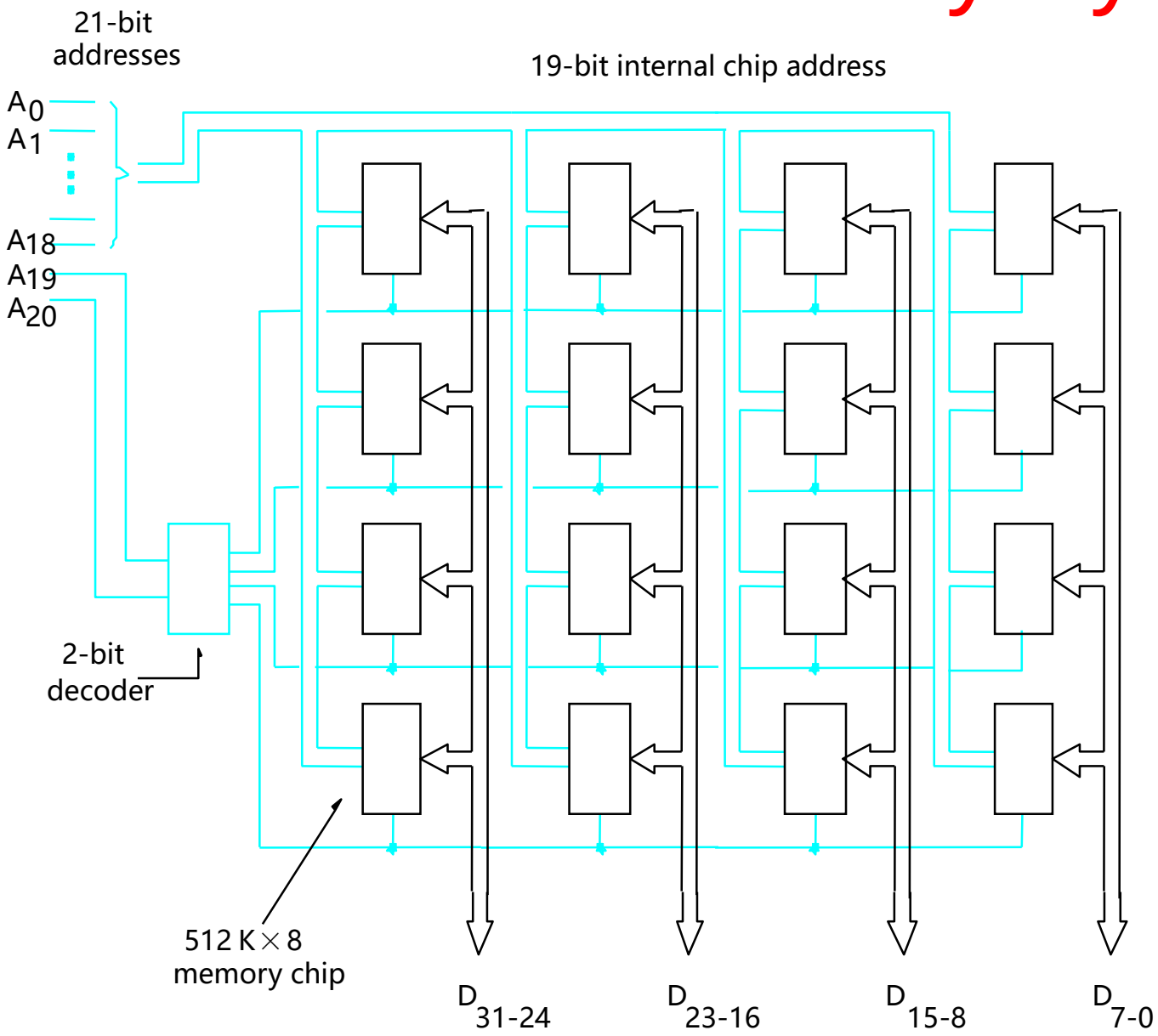
Static Memory System (4)

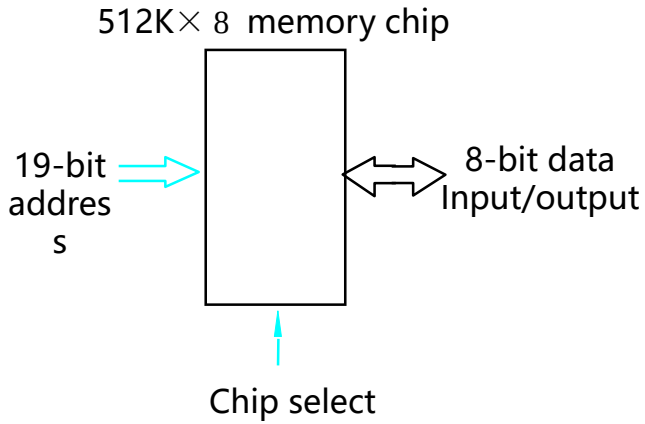


Static Memory System (5)

- 字位同时扩展法
  - 单片芯片的字数和位数均小于主存的容量要求，需进行字、位的扩展
  - 例：用512K×8位的存储器芯片组成2M×32位的存储器
    - 共需 $\frac{2\times1024}{512}\times\frac{32}{8}=4\times4$=16片512K×8位的芯片，组成4×4的阵列
    - 2M×32容量需21位地址码(A_{20}~A_0)，而512KB芯片需19位片内地址码(A_{18}~A_0)
    - 用高二位地址$A_{20}A_{19}$经2:4译码器选择一行芯片读/写
    - 每片8条I/O线分别接D_7~D_0

Static Memory System (6)





Static Memory System (7)

- Conclusion
  - Assume that the capacity of a memory unit is M × N bit, if constituted of using l × k bit chips, the number of total chips needed is (M/l) × (N/k).

Dynamic Memory System (1)

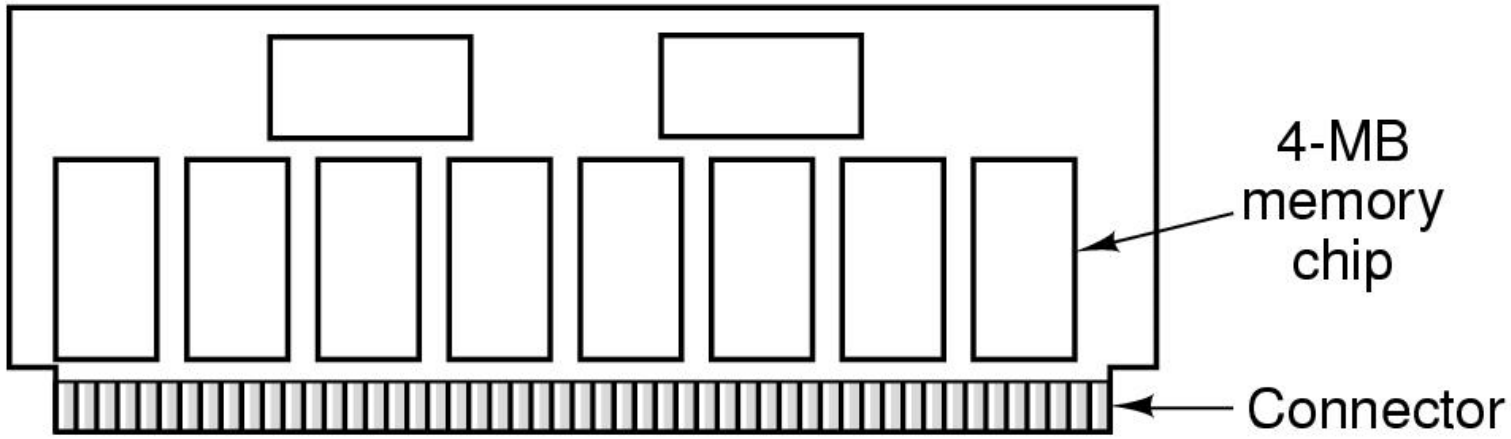
- The organization of large dynamic memory systems is essentially the same as the above static memory system
- Packaging: Memory Modules
  - Memory module: Assembly memory chips on a small board that plugs into a socket on the computer's motherboard
    - SIMM (Single In-line Memory Modules)
    - DIMM (Dual In-line Memory Modules)

Dynamic Memory System (2)

- SIMM
  - A SIMM is a basic DRAM packaging type that fits most older systems.
  - A SIMM can be either single-sided (with RAM chips on one side only) or double-sided (with RAM chips on both sides).
    - 30-pin SIMM: 1-16MB; 8 bits; plus 1bit for parity; single-sided
    - 72-pin SIMM: 1MB, 4MB, 16MB (single-sided); 2MB, 8MB, 32MB (double-sided); 32 bits, plus 4 bits for parity/ECC

Dynamic Memory System (3)

- SIMM Example
  - A single inline memory module (SIMM) holding 32MB. Two of the chips control the SIMM



Dynamic Memory System (4)

- DIMM
  - At present, DIMMs are the standard way for memory to be packaged.
  - A DIMM is capable of delivering 64 data bits at once.
  - Most common types of DIMMs
    - 72-pin, 144-pin, 200-pin DIMMs: used for SO-DIMM (Small Outline DIMM)
    - 168-pin DIMMs, used for FPM (Fast Page Mode) DRAM, EDO (Extended Data Out) DRAM, and SDRAM
    - 184-pin DIMMs, used for DDR SDRAM
    - 240-pin DIMMs, used for DDR2 and DDR3 SDRAM
    - 284-pin DIMMs, used for DDR4 SDRAM
    - 288-pin DIMMs, used for DDR5 SDRAM

Dynamic Memory System (5)

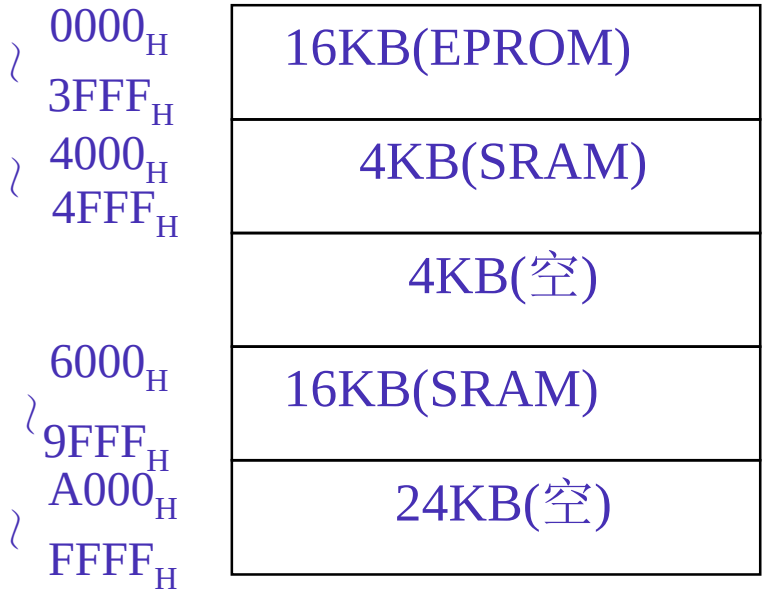
- DIMM Example
  - Two types of DIMMs: a 168-pin SDRAM module (top) and a 184-pin DDR SDRAM module (bottom)

Example

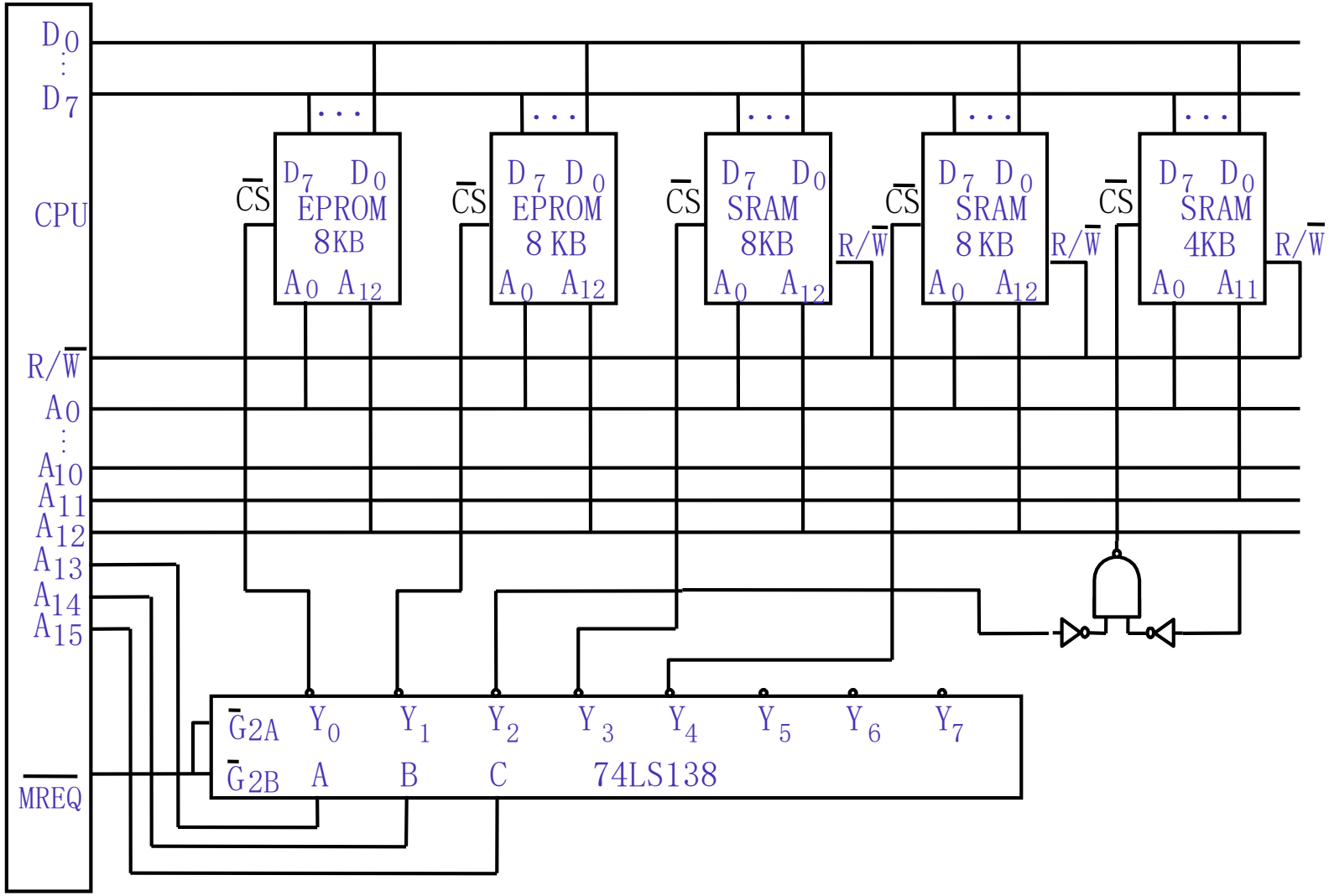
- CPU的地址总线16根 (A15~A0，A0为低位)，双向数据总线8根 (D7 ~ D0)，控制总线中与主存有关的信号有$\overline{\text{MREQ}}$ (允许访存，低电平有效)，R/$\overline{\text{W}}$ (高电平为读命令，低电平为写命令)
- 主存地址空间分配如下：0000_H～$3FFF_H$为系统程序区，由只读存储芯片组成；4000_H～$4FFF_H$为系统程序工作区，由SRAM组成；6000_H～$9FFF_H$为用户程序区，也由SRAM组成。按字节编址。现有如下存储器芯片:
  - EPROM：8K×8位 (控制端仅有 CS)
  - SRAM：16K×1位，2K×8位，4K×8位，8K×8位
- 请从上述芯片中选择适当芯片设计该计算机主存储器，画出主存储器逻辑框图，注意画出选片逻辑（可选用门电路及3:8译码器74LS138）与CPU的连接，说明选哪些存储器芯片及选多少片。

Example (ctd.)

- 主存地址空间分布：



Example (ctd.)


D0
D7
CPU
R/W
A0
A10
A11
A12
A13
A14
A15
MREQ
CS
D7 D0
EPROM
8KB
A0 A12
EPROM
8 KB
SRAM
8KB
SRAM
8 KB
SRAM
4KB
A0 A11
R/W
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
A
B
C
74LS138

Quiz (1)

1. Consider a 16M×128 memory built by using 512K×16 memory chips. How many rows of memory chips are needed?

   A. 8　　B. 16　　C. 32　　D. 64

   16M/512K=32

2. Consider a 64M×16 memory built by using 512K×8 memory chips. How many memory chips are needed?

   A. 32　　B. 64　　C. 128　　D. 256

   (64M*16)/(512K*8)=256

Quiz (2)

3. Consider a memory can be accessed with 20-bit address. Its word length is 64-bit and it is word-addressable. Assume that we use 256K×8bit SRAM chip to constitute this memory.

   – How many bytes can this memory store?

     2^{20} * 64 / 8 B = 1M * 8 B = 8 MB

   – How many SRAM chips do we need?

     8MB / (256K * 8 / 8 B) = 8MB / 256KB = 32片

   – How many address pins do we need for chip select? Why?

     因为每片芯片内部有18位地址 (对应于256K个存储单元)，所以，20位的地址中，低18位地址直接接芯片的18位地址端，高2位地址通过2:4译码器作芯片选择。

   – Draw a figure to show how this memory can be implemented using 256K×8bit SRAM chip.

Quiz (3)

4. Assume that there are two types of static memory chips: 128K×8 bit (total 4 chips) and 512K×4 bit (total 2 chips). Please use these memory chips to implement a 512K×16 bit memory. Draw the figure of the memory organization.

Solution

512K×16的存储器需要2片512K×4 和4片128K×8的芯片按下图组成。