Computer Organization & Architecture

3-2 Semiconductor Static RAM

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Contents of this lecture

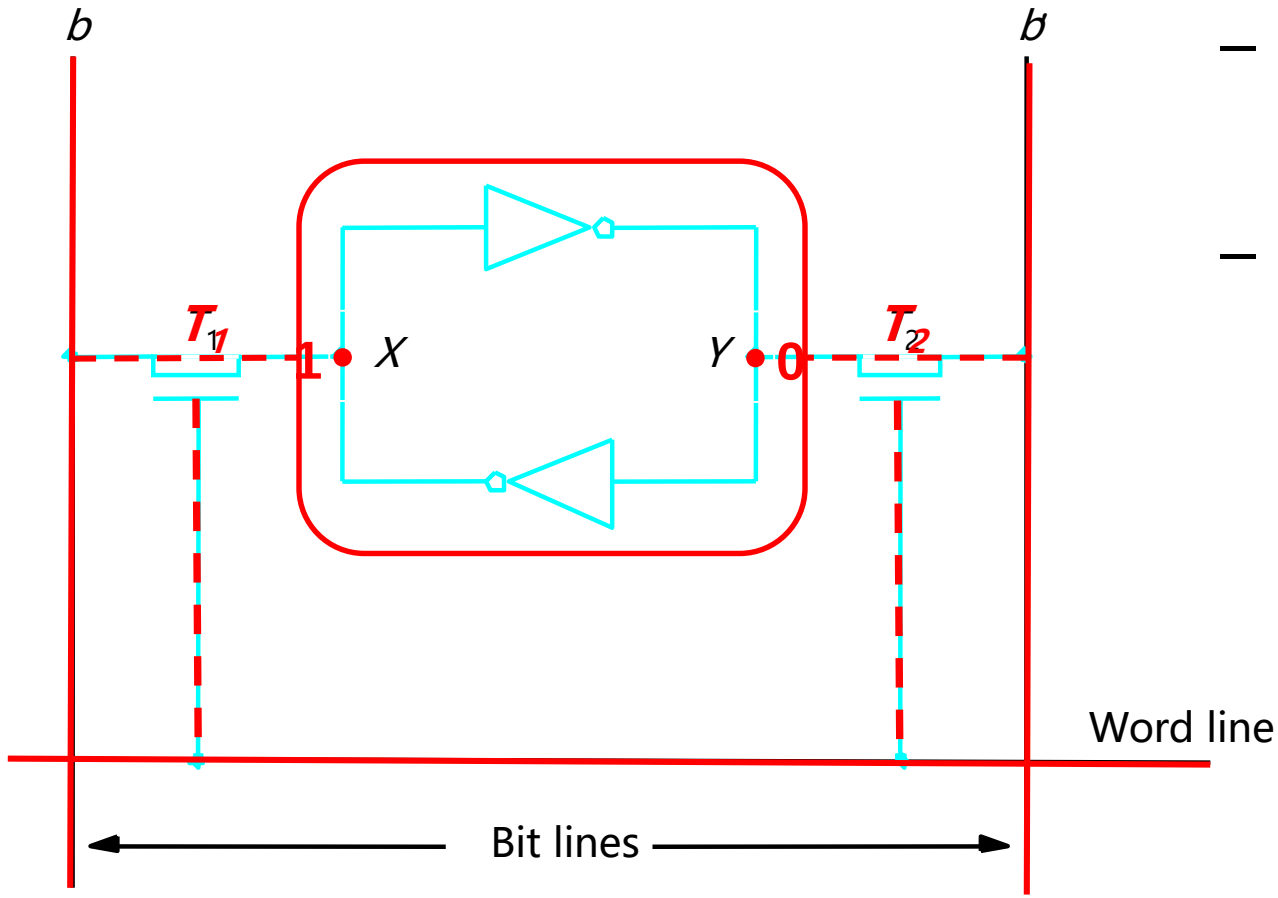
- Static RAM Cell
- Organization of Static RAM Chips

RAM Technology

- Static Technology
  - In a static RAM, binary values are stored using traditional flip-flop logic-gate configurations.
- Dynamic Technology
  - A dynamic RAM is made with cells that store data as charge on capacitors. The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0.

Static RAM (SRAM) Cell (1)

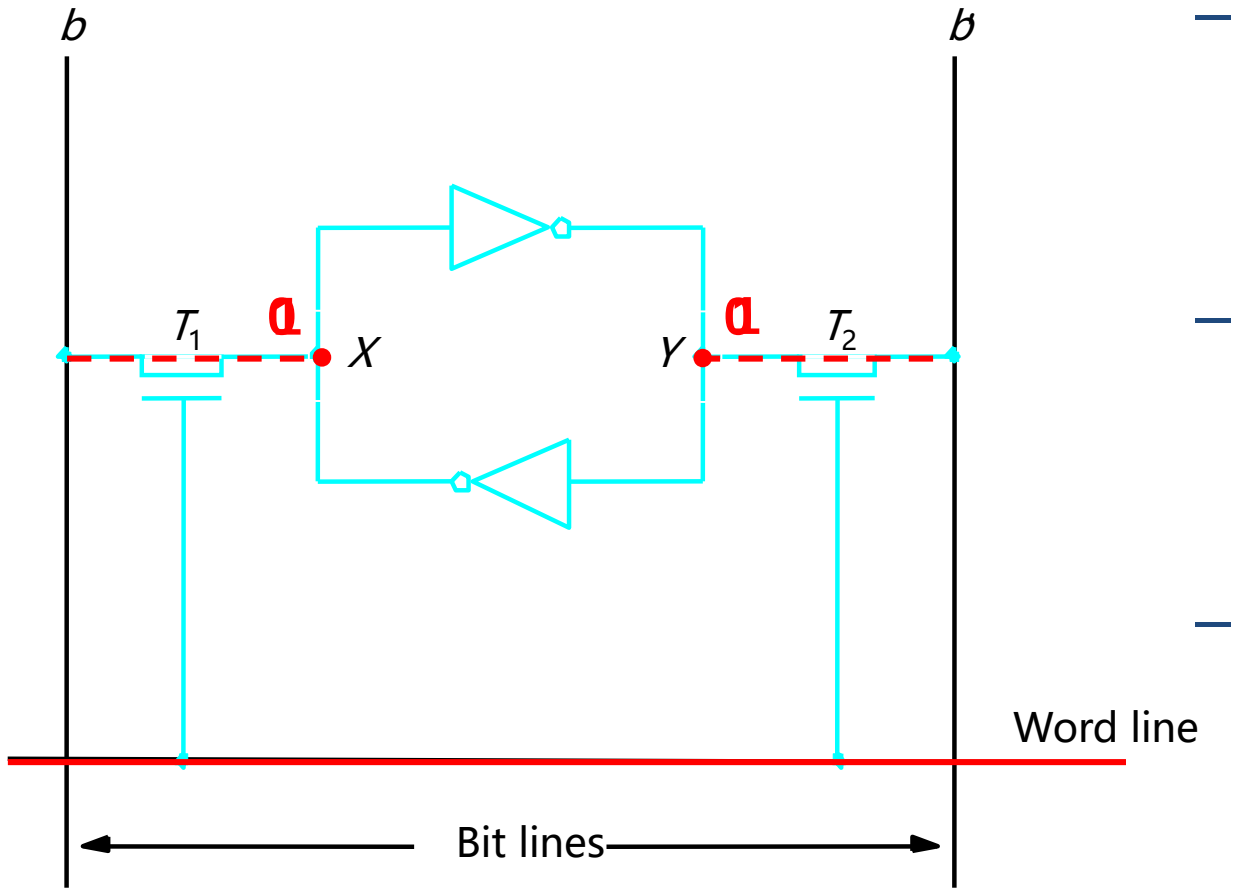
- Implementation of a SRAM cell



- Maintain State
  - The word line is at low level
- Assume that the cell is in state 1 if the logic value at point X is 1 and at point Y is 0.

SRAM Cell (2)

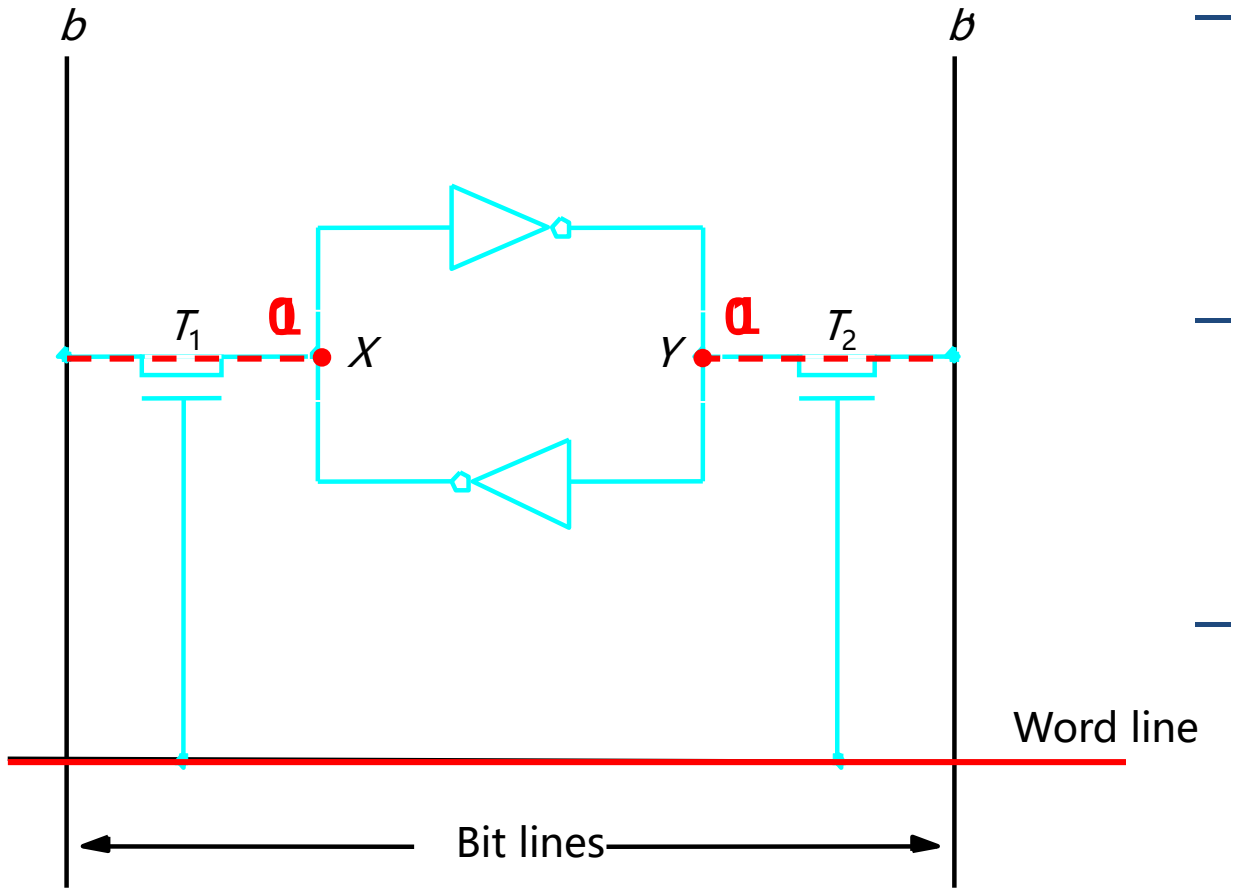
- Read Operation



  - The word line is at high level.
  - Read "1": The signal on the bit line *b* is high and the signal on the bit line *b'* is low.
  - Read "0": The signal on the bit line *b* is low and the signal on the bit line *b'* is high.
  - Note: *Sense/write circuits* at the end of the bit lines monitor the state of *b* and *b'* and set the output accordingly.

SRAM Cell (3)

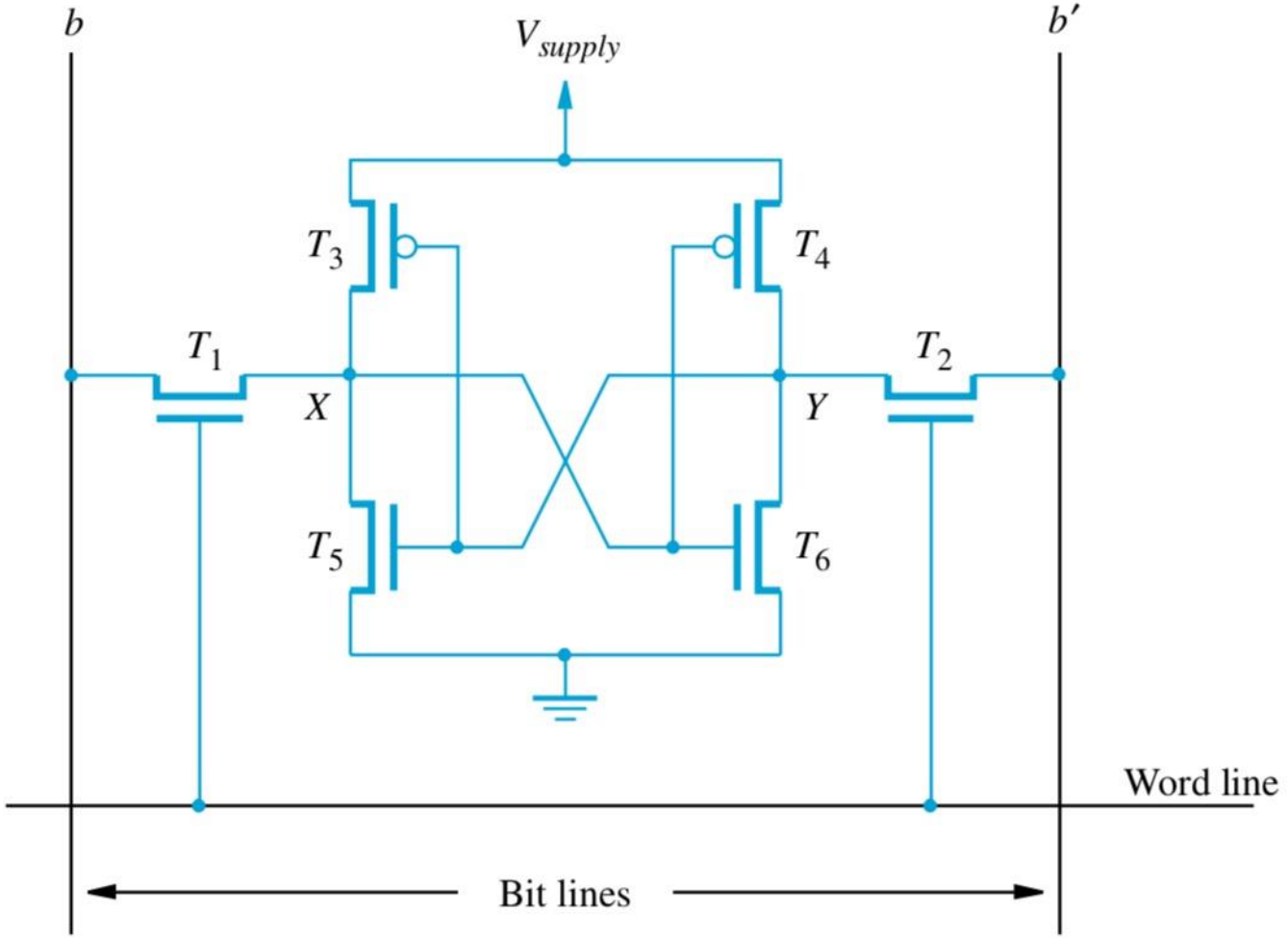
- Write Operation

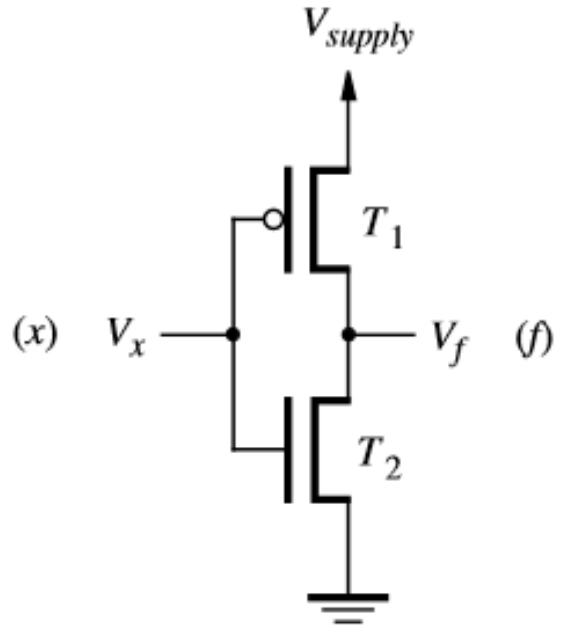


  - The word line is at high level.
  - Write “1” : Place high level signal on bit line *b* and place low level signal on bit line *b’*.
  - Write “0” : Place low level signal on bit line *b* and place high level signal on bit line *b’.*
  - Note: The required signals on the bit lines are generated by the Sense/Write circuit.

SRAM Cell (4)

- CMOS Realization of a SRAM cell





x	V_x	T_1	T_2	V_f	f
0	low	on	off	high	1
1	high	off	on	low	0

SRAM Cell (5)

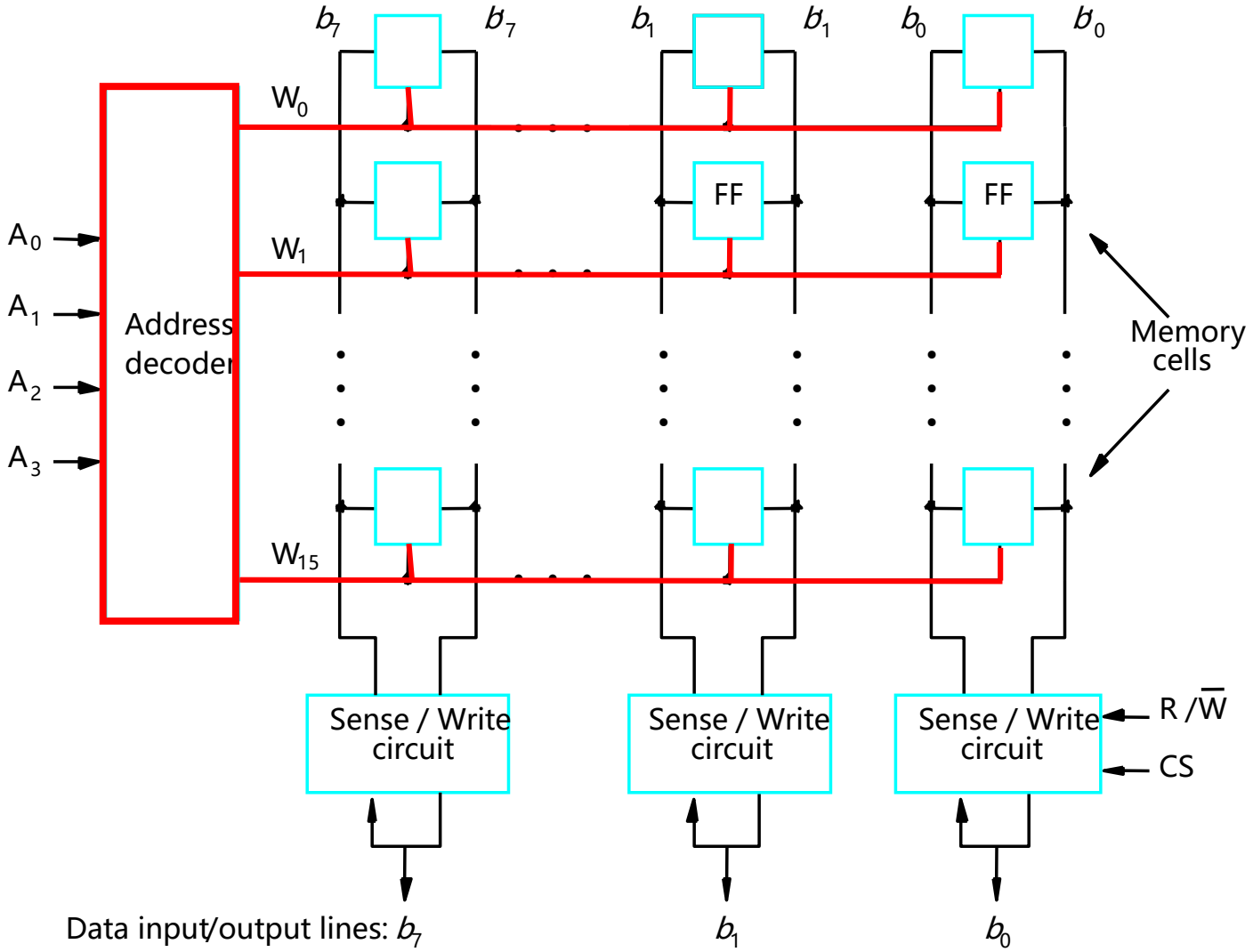
- CMOS Realization of a SRAM cell
  - The power supply voltage is 5V in older CMOS SRAMs or 3.3V in new low-voltage versions.
  - If power is interrupted and then it is restored, the latch will settle into a stable state, but it will not necessarily be the same state the cell was in before the interruption.
  - CMOS SRAMs' power consumption is very low.

SRAM Cell (6)

- Advantage and Disadvantage of SRAM
  - Advantage: Fast
  - Disadvantage: Low density, High cost

Organization of SRAM Chips (1)

- Organization of 128 Bit Cells (16 × 8)

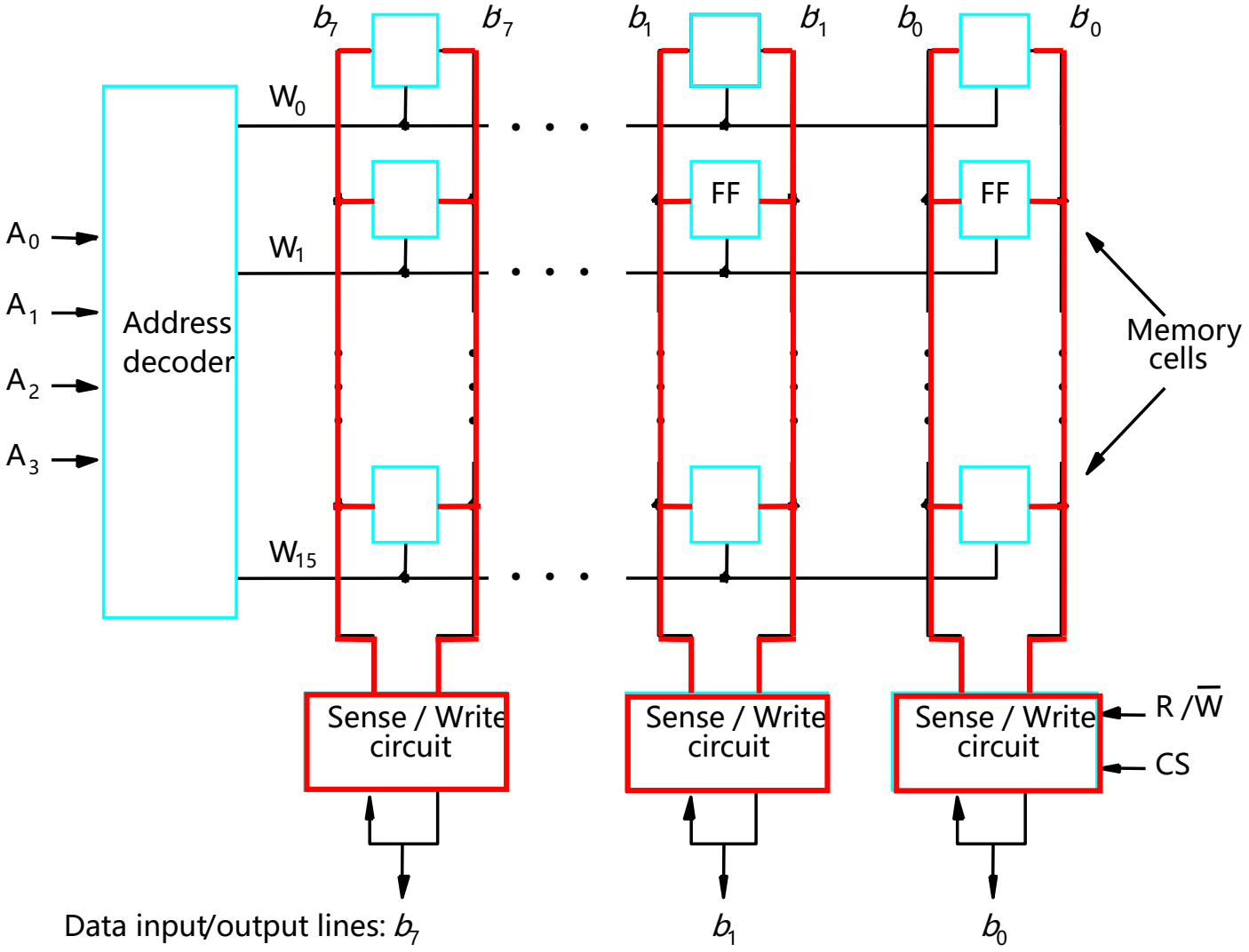


– Internal Organization

- Word line: All cells of a row are connected to the word line. It is driven by the address decoder.

Organization of SRAM Chips (2)

- Organization of 128 Bit Cells (16 × 8)

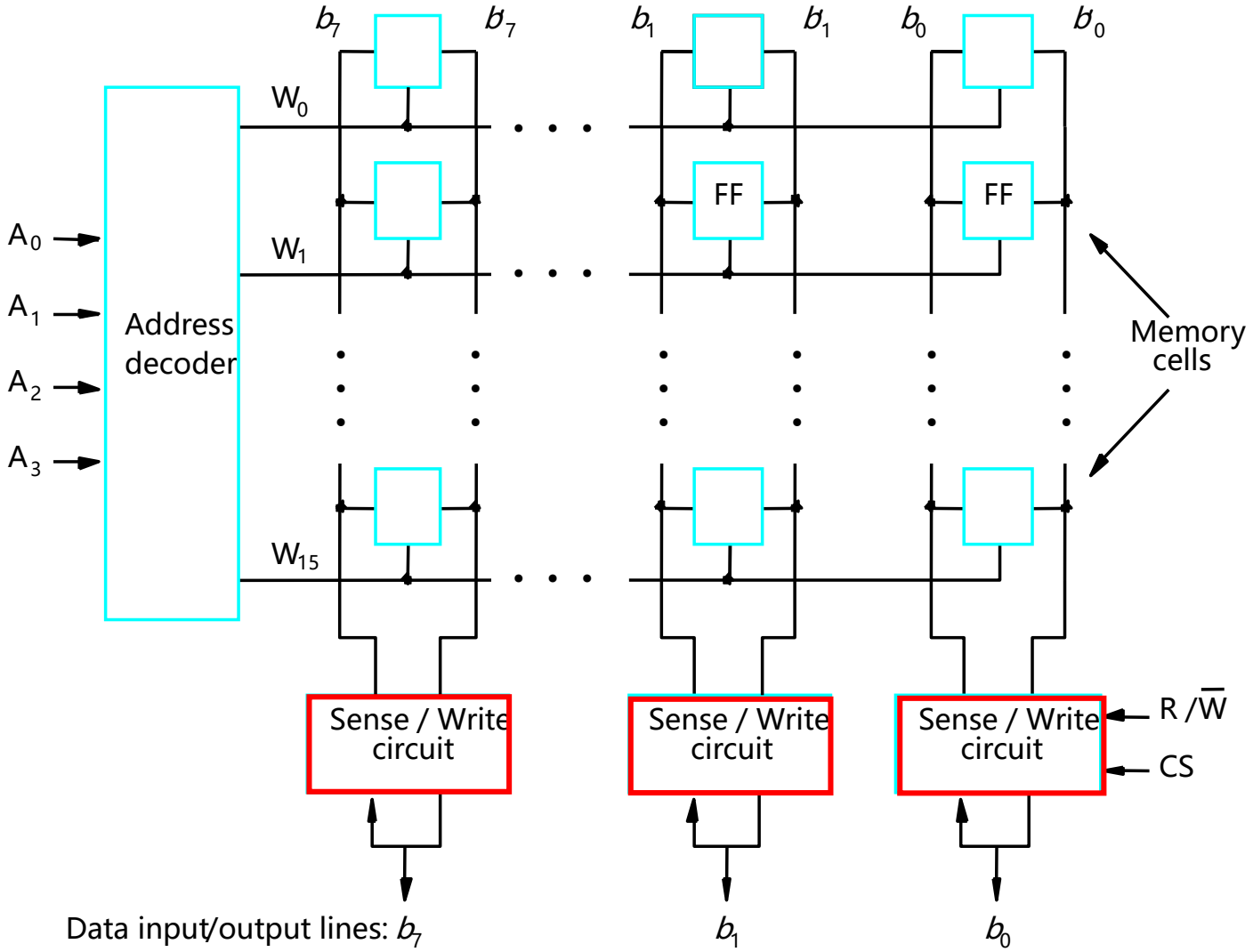


– Internal Organization

- Bit lines: The cells in each column are connected to a Sense/Write circuit by two bit lines.

Organization of SRAM Chips (3)

- Organization of 128 Bit Cells (16 × 8)

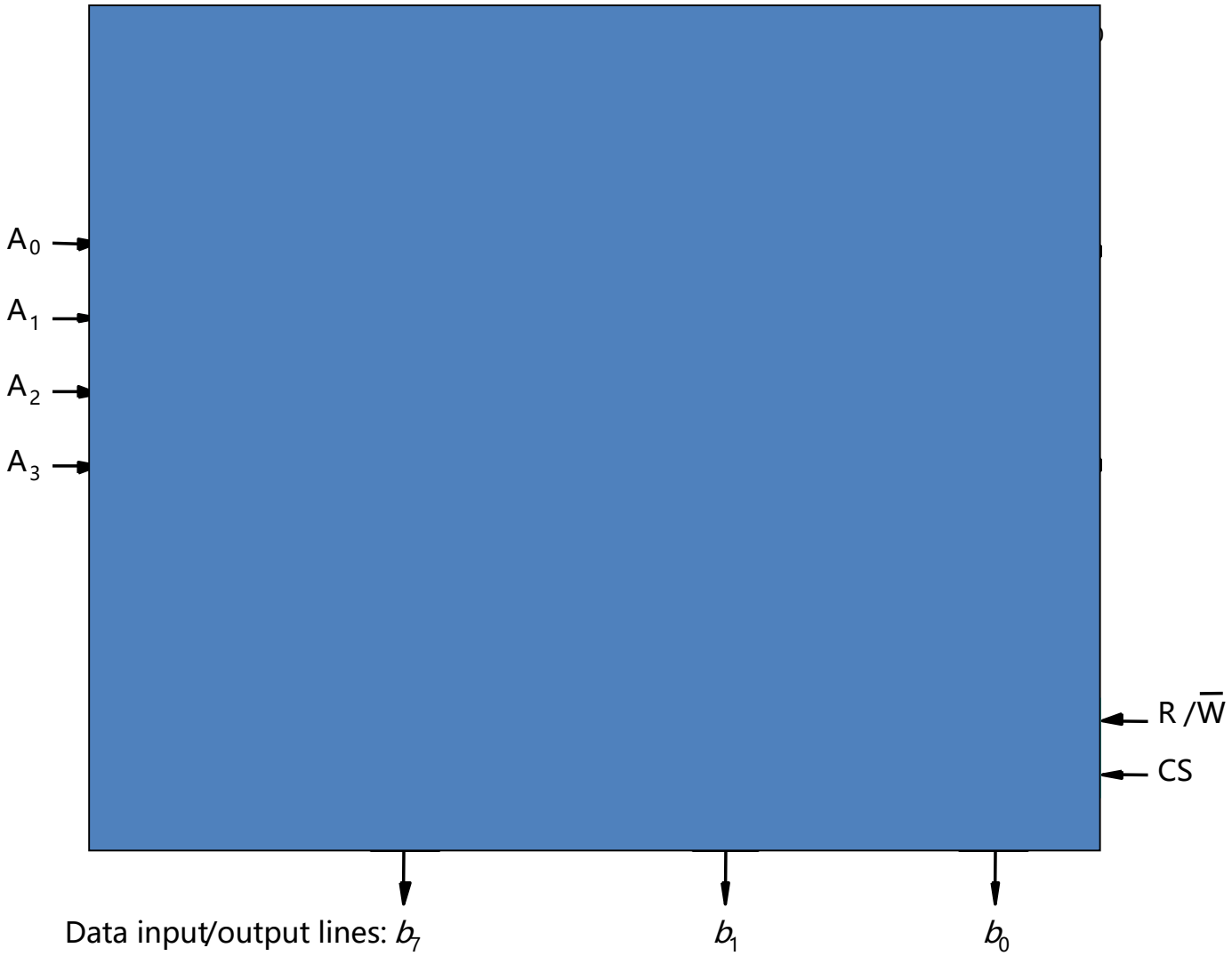


– Internal Organization

- Sense/Write circuits
  - Read: They sense the information stored in the cells selected by a word line and transmit this information to the output data lines.
  - Write: They receive input information and store it in the cells of the selected word

Organization of SRAM Chips (4)

- Organization of 128 Bit Cells (16 × 8)



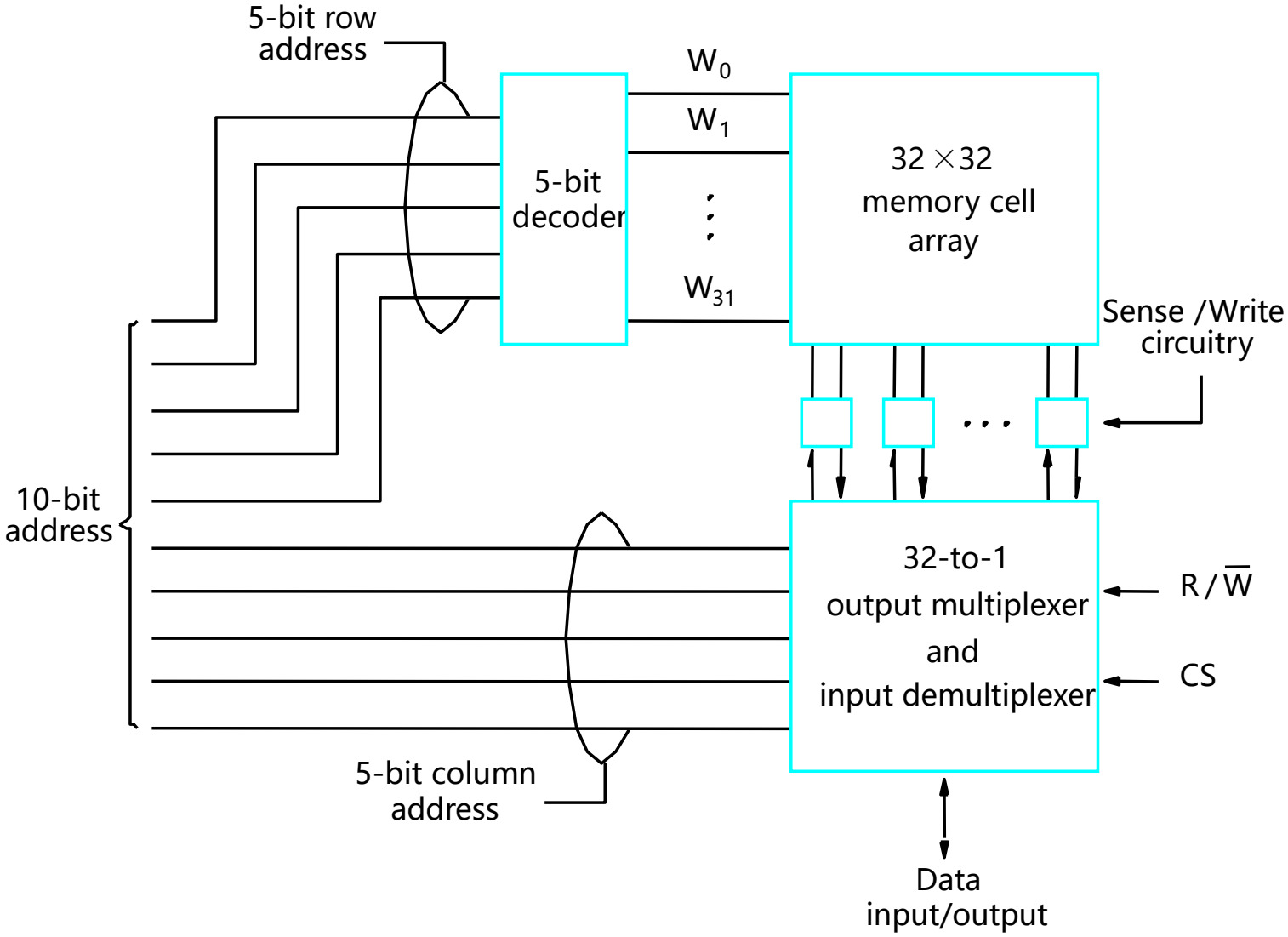
– External Organization

- Address lines (Input): $A_0 – A_3$
- Data lines (Input/Output): $b_0 – b_7$
- Control lines(Input)
  - R/W (Read/Write): Specify the required Read or Write operation.
  - CS (Chip Select): Select a given chip in a multi-chip memory system.
- Power Supply line
- Ground line
- Total Connections = 4 + 8 + 2 + 1 + 1

  = 16

Organization of SRAM Chips (5)

- Organization of 1024 Bit Cells (1K × 1)



Organization of SRAM Chips (6)

- Organization of 1024 Bit Cells (1K × 1)
  - External Organization
    - Address lines (Input): $A_0 – A_9$
    - Data lines (Input/Output): b_0
    - Control lines(Input): R/W, CS
    - Power Supply line
    - Ground line
    - Total Connections = 10 + 1 + 2 + 1 + 1 = 15

Quiz (1)

1. Assume that the capacity of a kind of SRAM chip is 8K×16, so the address lines and data lines of this chip are ____ respectively.

   A. 8,16 B. 13,16 C. 13,4 D. 8,4

2. Assume that the capacity of a kind of SRAM chip is 32K×32, so the sum of address lines and data lines of this chip is ____.

   A. 47 B. 64 C. 46 D. 74

Quiz (2)

3. What are the advantage and disadvantage of SRAM?

Advantage: Fast

Disadvantage: Low density, High cost