Solution for Chapter 5

5.4 Register contents are read in step 2 and loaded into the inter-stage registers at the end of that clock period.

Step	RA	RB	RZ	RY	R6
3	1000	2500	*	*	7500
4	1000	2500	−1500	*	7500
5	1000	2500	−1500	−1500	7500
1	1000	2500	−1500	−1500	−1500

* These values are determined by the previous instruction.

5.9 If register addresses are not in the same bit positions for all instructions, the processor needs to decode the instruction, at least partially, before being able to read its source registers. The source registers would then have to be read in step 3, adding a step to the execution sequence.
In order to maintain a five-cycle execution sequence, **the clock cycle may be extended to enable the processor to read the source registers at the end of step 2**, after the instruction has been sufficiently decoded to determine where the register addresses are in the IR. With this adjustment, a 5-step execution sequence can be used.
An alternative is to **delay reading the source registers until step 3, and to send their contents directly to the ALU**. Registers RA and RB would not be needed in this case. The clock cycle must be sufficiently long to accommodate a register access plus an ALU operation. Note that register access may start sometime towards the end of cycle 2, as soon as instruction decoding identifies the location of the register addresses in the IR.
Which of these two alternatives is preferable depends on design details and the associated delays.

5.15 The autoincrement addressing mode means that the contents of register R5 are incremented by 4 after being used to read the memory operand. **Both the updated value of register R5 and the operand read from the memory need to be written into the register file.** This is not possible in the hardware organization in Figure 5.8.

5.23 MuxPC selects RA in step 3 (T3) of a Call register instruction. It selects the adder output at all other times. MuxINC selects the immediate value in step 3, to be used in branch instructions.

$$\begin{aligned} \text{PC\_select} &= \overline{\text{T3} \cdot \text{Call\_Register}} \\ \text{INC\_select} &= \text{T3} \end{aligned}$$

1. Give the sequence of actions for a Return-from-subroutine instruction in a RISC processor. Assume that the address LINK of the general-purpose register in which the subroutine return address is stored is given in the instruction field connected to address A of the register file (IR_{31-27}).

   Solution: Whenever an instruction is loaded into the IR, the contents of the general-purpose register whose address is given in bits IR_{31-27} are read and placed into register RA (see Figure 5.18). Hence, a Return-from-subroutine instruction will cause the contents of register LINK to be read and placed in register RA. Execution proceeds as follows:

   1. Memory address←[PC], Read memory, Wait for MFC, IR←Memory data, PC←[PC] + 4
   2. Decode instruction, RA←[LINK]
   3. PC←[RA]
   4. No action
   5. No action

2. What are the advantages and disadvantages of hardwired and microprogrammed control?

   Solution: The main advantage of hardwired control is fast operation. The disadvantages include: higher cost, inflexibility when changes or additions are to be made, and longer time required to design and implement such units.
   Microprogrammed control is characterized by low cost and high flexibility. Lower speed of operation becomes a problem in high-performance computers.