Computer Organization & Architecture

Review

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Chapter 1 Basic Structure of Computers

1. Computer types

   Embedded Computers, Personal Computers, Server & Enterprise systems, Supercomputers & Grid Computers

2. Five basic functional units of computers
   - Input unit
   - Output unit
   - Memory
   - Arithmetic and logic unit
   - Control unit

3. Program Execution

4. Computer generations

Chapter 9 Arithmetic

1. Integer Representation

- Signed integer: The sign part is a 1-bit value that is 0 for positive numbers, and 1 for negative numbers.

  ① signed-magnitude

  ② 1's-complement

  ③ 2's-complement

2. Rules of Addition and subtraction of signed numbers (2 ’s-complement form)

① Addition

Add their n-bit representations, treating the sign bit as the most significant bit (MSB), ignoring the carry-out signal from the MSB position.

② Subtraction

to perform X－Y, form the 2’s-complement of Y and then add it to X, as in rule ①.

3. Arithmetic overflow (2 's-complement form)

If two numbers are added, and they have the same sign, then overflow occurs if and only if the result has the opposite sign to both summands.

4. Adder

① 1-bit Full-adder

$$S_i = \bar{x}_i \bar{y}_i c_i + \bar{x}_i y_i \bar{c}_i + x_i \bar{y}_i \bar{c}_i + x_i y_i c_i$$
$$= x_i \oplus y_i \oplus c_i$$
$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$

② n-bit ripple-carry Adder

Overflow = $x_{n-1} y_{n-1} \bar{s}_{n-1} + \bar{x}_{n-1} \bar{y}_{n-1} s_{n-1}$

Overflow = $c_n \oplus c_{n-1}$

4. Adder

③ Carry-lookahead addition

$$s_i = x_i \oplus y_i \oplus c_i$$

$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$

$$= x_i y_i + (x_i + y_i) c_i$$

$G_i = x_i y_i$ (generate function for stage i)

$P_i = x_i + y_i$ (propagate function for stage i)

5. Sequential multiplication (Positive Multiplication)
6. Booth algorithm (Signed-operand Multiplication)
7. Non-restoring division
8. Floating-point numbers
   ① IEEE 754 standard: Single-precision format, Double-precision format
   ② Arithmetic Operations On Floating-point Numbers
      - Addition and Subtraction
      - Multiplication and Division

Chapter 8 The Memory System

1. Basic Concepts

① Word: Each group of fixed size of bits is referred to as a word

② word length: The number of bits in each word is referred to as word length.

③ memory address: Addresses are numbers that identify memory locations.

④ big-endian: the lower byte addresses are used for the more significant bytes (the leftmost bytes) of the word.

⑤ little-endian: the lower byte addresses are used for the less significant bytes (the rightmost bytes) of the word.

⑥ accessing method: Sequential Access, Direct Access, Random Access

⑦ volatile/nonvolatile, erasable/nonerasable

2. Internal organization of static RAM chips (16 × 8, 1K × 1)
3. Internal Organization of an Asynchronous DRAM Chip (2M × 8)
4. Memory Latency, Memory Bandwidth
5. Use small memory chips to constitute large memory (draw the figure)
6. Memory hierarchy
7. Principle of cache

   Locality of reference: Temporal Locality, Spatial Locality
8. Mapping functions of cache
   - ① Direct mapping
   - ② Fully associative mapping
   - ③ Set-associative mapping
9. Replacement Algorithm
10. Write policy: Write back, Write through

12. Principle of virtual memory
13. Paging (Virtual Address to Physical address)
14. Magnetic Hard Disk
    - Sector, track, cylinder
    - Disk capacity

Chapter 2 Machine Instructions

1. Instruction and Instruction Sequencing
   - Register Transfer & Assembly-Language Notation
   - RISC Instruction Sets
   - Instruction Strait-line Sequencing & Branching
2. Instruction Formats
   - Instruction Representation
   - Common Instruction Address Field Formats: Zero-address Instruction, One-address instruction, Two-address instruction, Three-address instruction
   - Opcode format (expanding opcode)

3. Addressing Modes
   - ① Immediate mode
   - ② Absolute mode
   - ③ Register mode
   - ④ Register Indirect mode
   - ⑤ Indirect mode
   - ⑥ Indexed mode
4. Stacks
5. Subroutines
6. CISC Instruction Sets (Addressing modes; Conditional Codes)
7. RISC vs. CISC styles

Chapter 5 Basic Processing Unit

1. Instruction Execution: five steps
2. Hardware Components: five stages
3. Instruction Fetch and Execution Steps
4. Control Signals
5. Generation of Control Signals
   - ① Hardwired Control (RISC processor)
   - ② Microprogramming (CISC processor)
     - Microinstruction (control word)
     - Microprogram (microroutine)
     - Control Store
   - ③ Hardwired Control vs. Microprogramming

Chapter 6 Pipelining

1. Basic Concepts

   ① Pipelining: Multiple instructions overlapped in execution

   ② Rate: one instruction per cycle

2. Pipeline Organization

   - Five stages: Fetch, Decode, Compute, Memory, Write
   - Inter-stage buffers

3. Pipeline issues (hazards)

   ① Data dependencies: pipeline stalling & operand forwarding

   ② Memory delays

   ③ Resource limitations

   ④ Branch delays

Chapter 3 Basic Input/Output

1. Addressing Modes of I/O Devices: memory-mapped I/O, Isolated I/O
2. Principle of program-controlled I/O
3. Interrupt
   - ① Interrupt, Interrupt Request, Interrupt Acknowledge, Interrupt Service Routine
   - ② Difference between subroutine and interrupt-service routine
   - ③ Means to Enable and Disable Interrupt
   - ④ Handling multiple devices interrupt
     - Device identification: Software polling, vectored interrupt
     - Interrupt nesting
     - Handle simultaneous interrupt request
4. Principle of DMA
5. DMA Transfer Modes: Burst Mode, Cycle Stealing Mode, Transparent Mode

1. 按每一章的课件内容进行复习 (课件上没有的内容不会考)
2. 考试题型 (英文):
   ① 单项选择题 (20)
   ② 简答题 (20)
   ③ 综合题 (60)
3. 考试时间：18周周五下午14:00-16:00（2024.12.27）