Computer Organization & Architecture

3-3 Semiconductor Dynamic RAM

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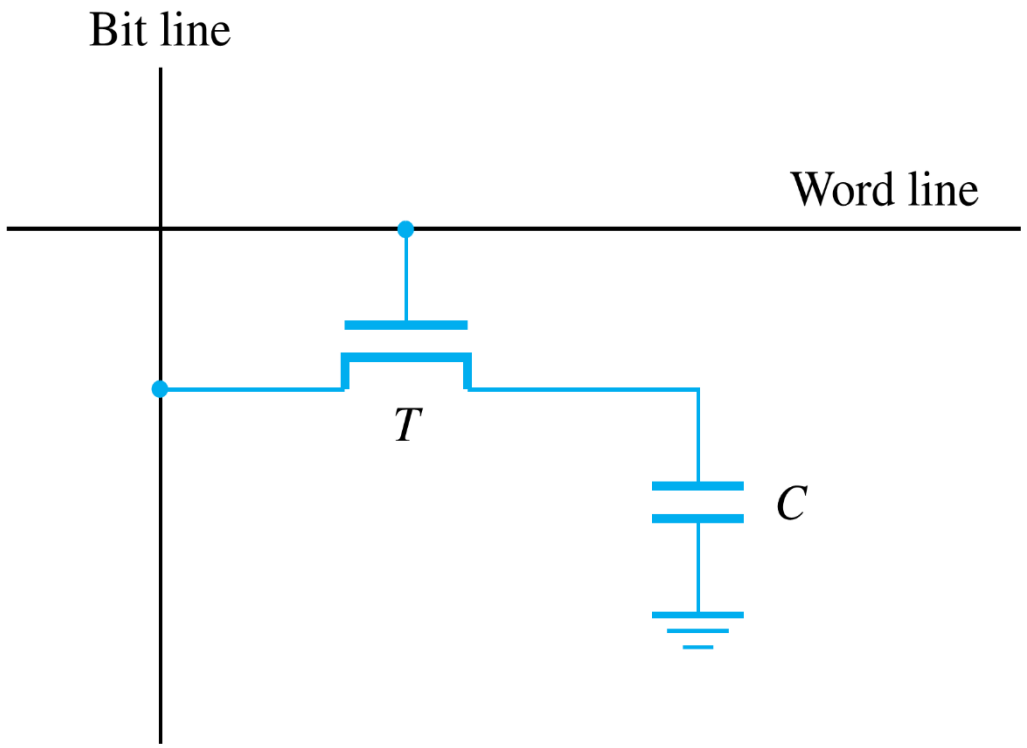
Contents of this lecture

- Dynamic RAM Cell
- Organization of Dynamic RAM Chips
- Synchronous DRAM

Dynamic RAM (DRAM) Cell (1)

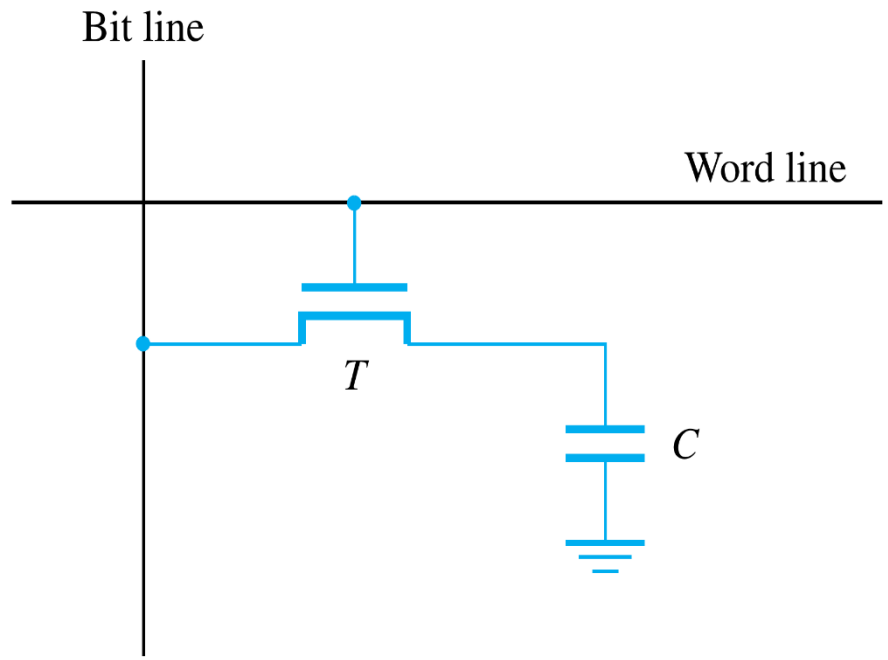
- Implementation of a DRAM cell



  - Information is stored in the form of a charge on the capacitor C.

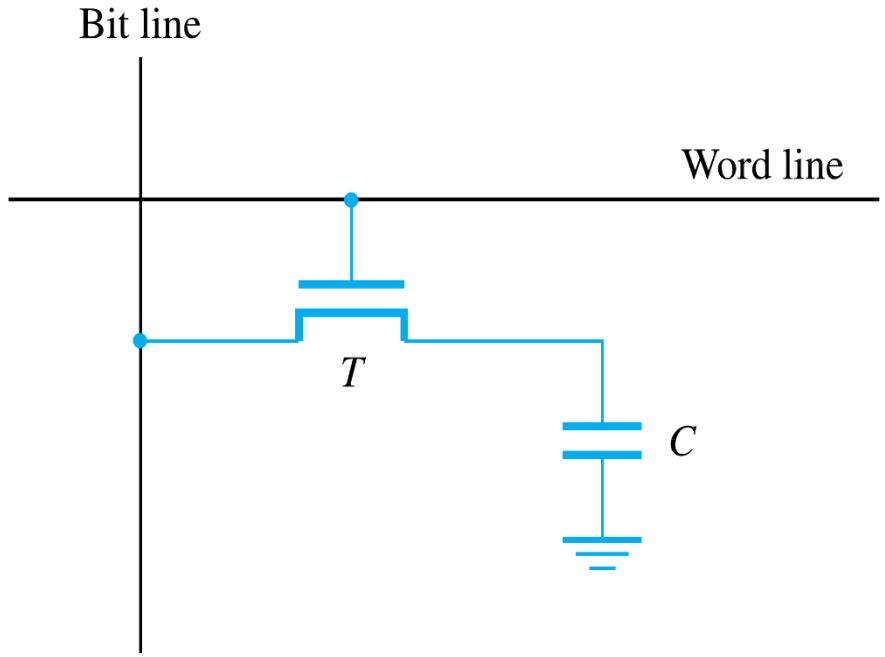
DRAM Cell (2)

- Read Operation
  - The word line is high.
  - Read “1”: If the charge stored on the capacitor is above the threshold value, the sense amplifier drives the bit line to a full voltage that represents “1”. This voltage recharges the capacitor to the full charge that corresponds to “1”.
  - Read “0”: If the charge stored on the capacitor is below the threshold value, the sense amplifier pulls the bit line to ground level, which ensures that the capacitor will have no charge, representing “0”.



DRAM Cell (3)

- Write Operation
  - The word line is high.
  - Write “1”: The bit line is applied high voltage.
  - Write “0”: The bit line is applied low voltage.
- Maintain State
  - The word line is low.
- Refresh
  - Leaky storage
  - Refresh periodically

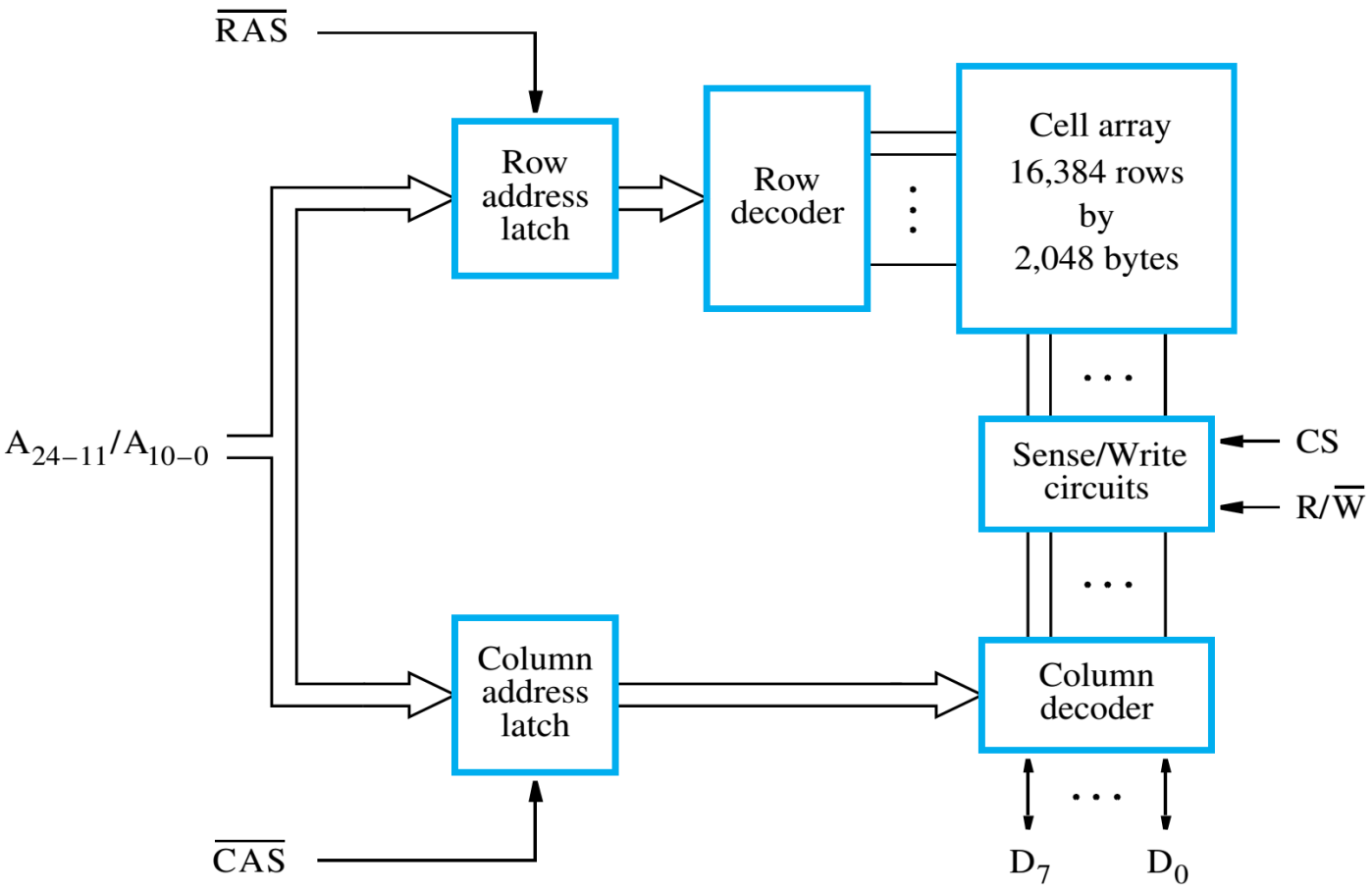


DRAM Cell (4)

- Advantages
  - High density, low cost
- Disadvantage
  - Longer access times
  - Leaky, needs to be refreshed

Organization of DRAM Chips (1)

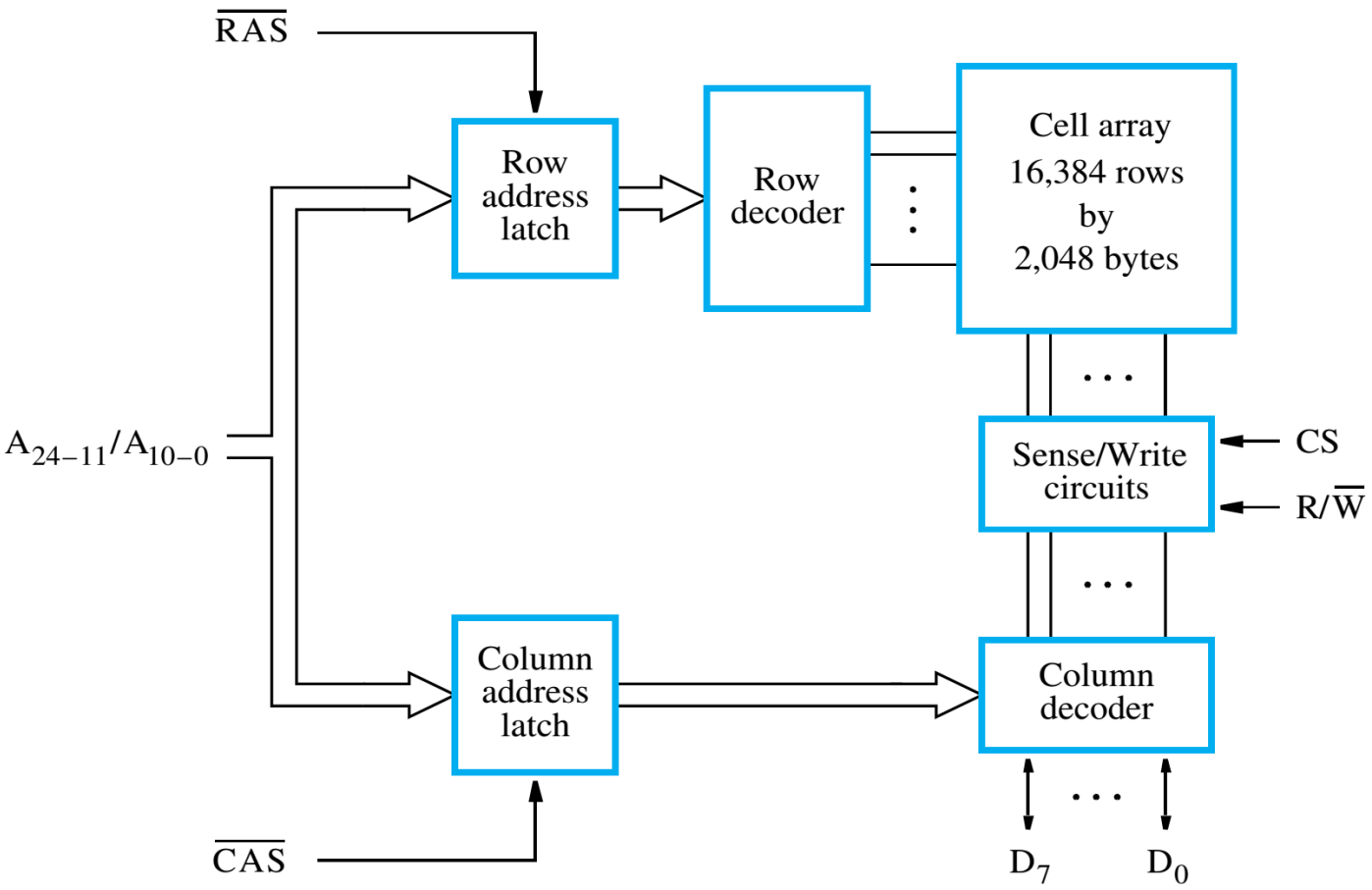
- Organization of 256M Bit Cells (32M × 8)



- 14 bit address bits are needed to select a row.
- Another 11 bits are needed to specify a group of 8 bits in the selected row.
- Total: 25-bit address

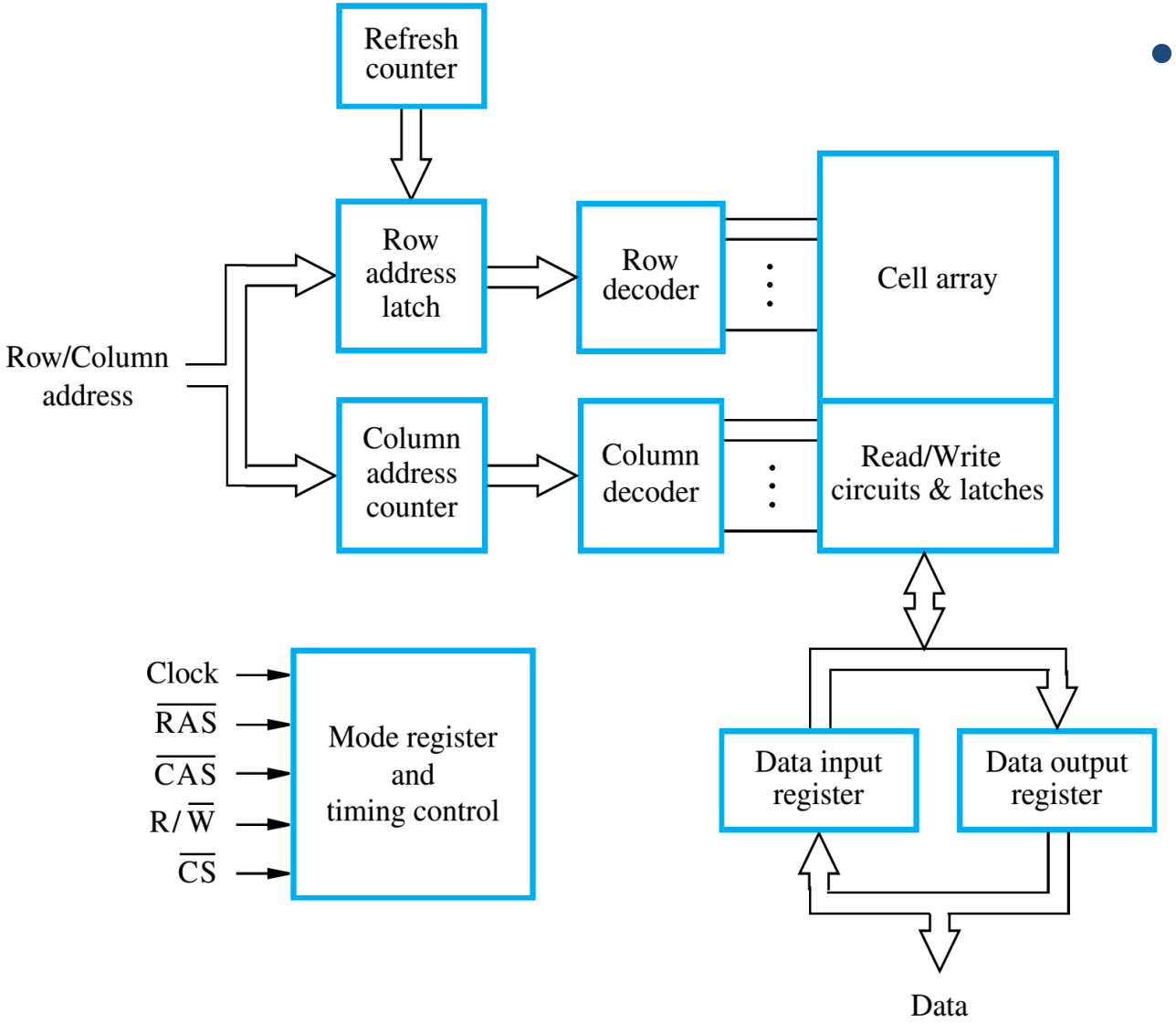
Organization of DRAM Chips (2)

- Organization of 256M Bit Cells (32M × 8)



- To reduce the number of pins needed for external connections, the row and column addresses are multiplexed on 14 pins.
- Row Address Strobe ($\overline{RAS}$)
- Column Address Strobe ($\overline{CAS}$)

Synchronous DRAM (1)



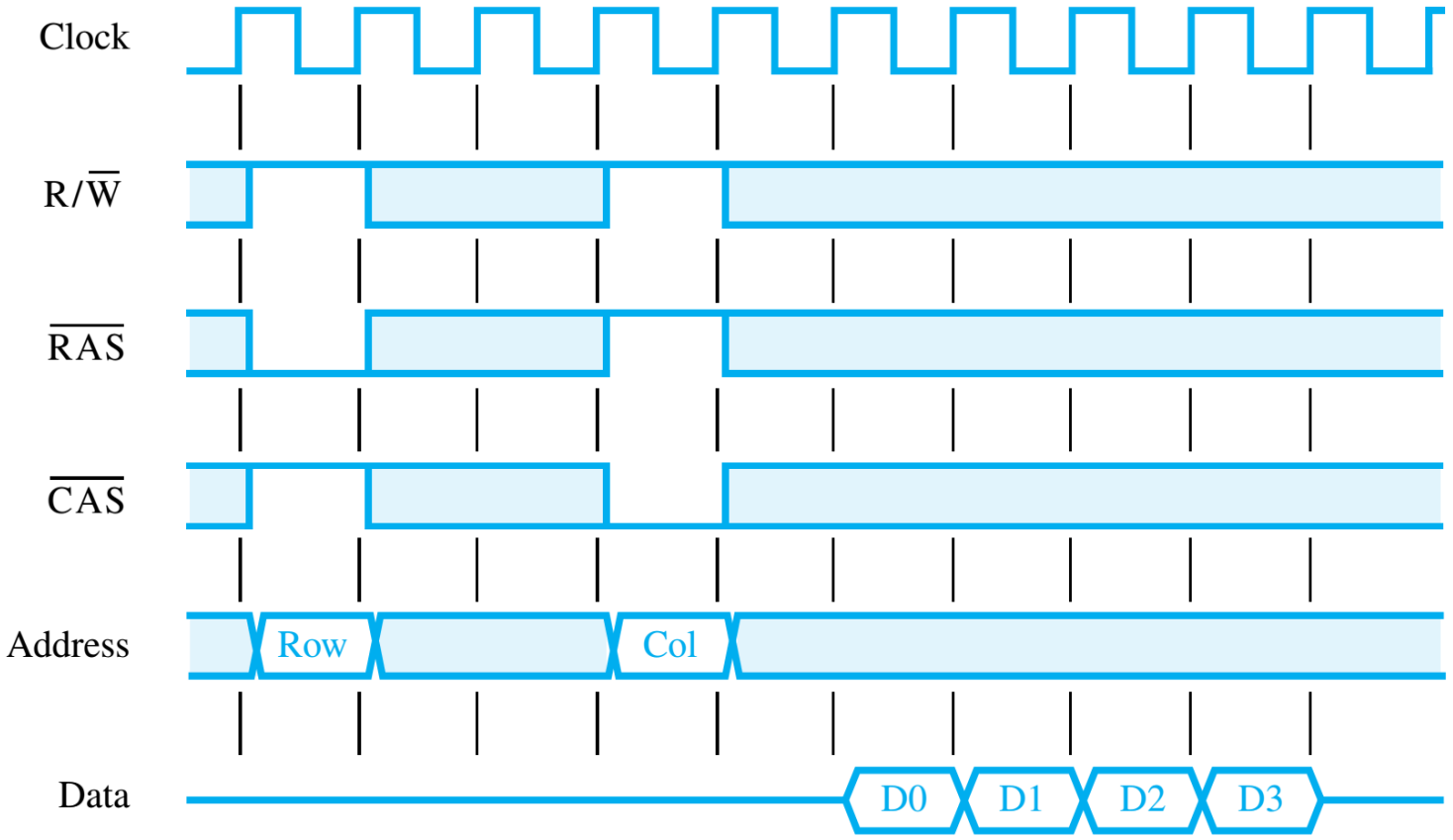
- SDRAM
  - Their operation is directly synchronized with a clock signal.
  - Structure of a SDRAM Chip

Synchronous DRAM (2)

- Burst Operation
  - SDRAMs have several different modes of operation, which can be selected by writing control information into a *mode register*.
  - The burst operations use the block transfer capability.
  - The mode register holds a 12-bit value that the SDRAM looks at in order to determine how many columns it should BURST and in what order it should BURST them.

Synchronous DRAM (3)

- Example: Burst read of length 4 in an SDRAM

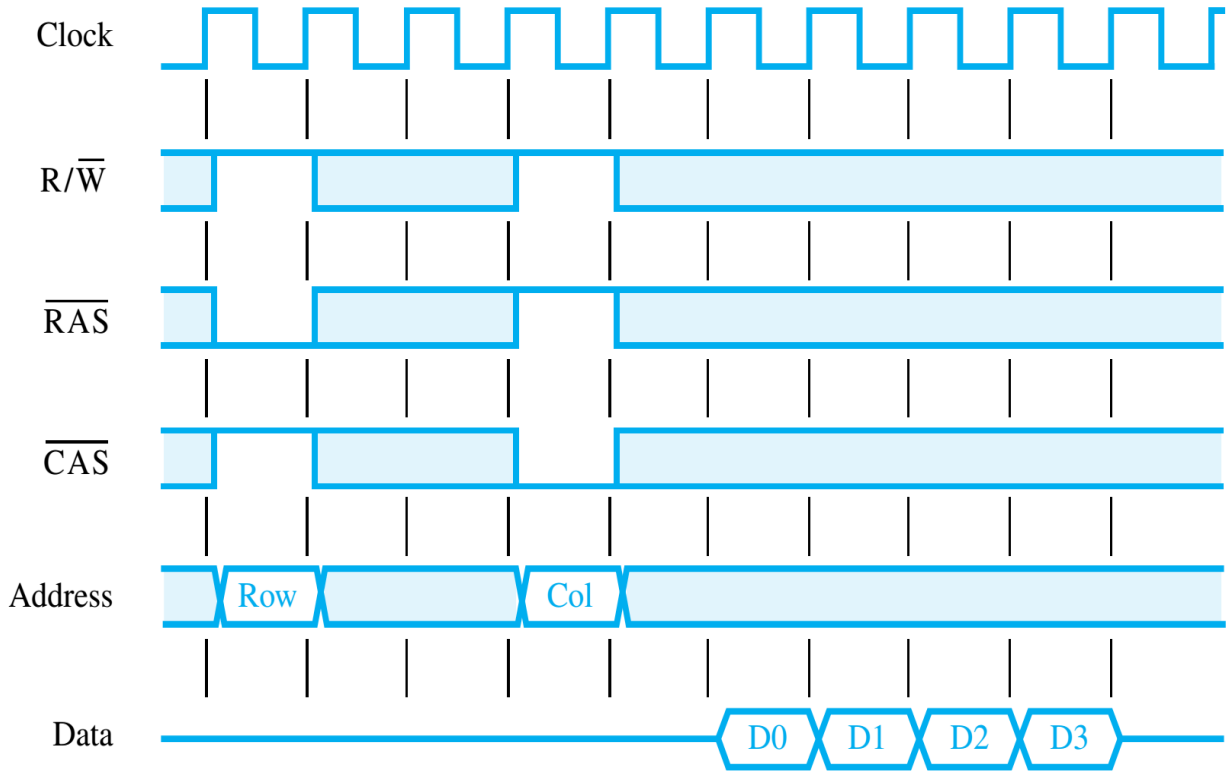


Synchronous DRAM (4)

- Latency and Bandwidth
  - Latency and Bandwidth are two parameters indicating the performance of a memory system.
  - Latency: Refers to the amount of time it takes to transfer a word of data to or from the memory.
  - Note: In block transfers, latency is used to denote the time before it takes to transfer the first word of data.

Synchronous DRAM (5)

- Example
  - The first word of data is transferred 5 clock cycles later. The latency is 5 clock cycles.



Synchronous DRAM (6)

- Bandwidth
  - The number of bits or bytes that can be transferred in one second is referred to as *bandwidth*.
  - Unit: bit per second or byte per second.
  - The bandwidth of a memory unit depends on the speed of access to the stored data and on the number of bits that can be accessed in parallel.
  - The effective bandwidth also depends on the transfer capability of the links that connect the memory and the processor.
  - Effective Bandwidth = Bus Speed $\times$ Bus Width

Synchronous DRAM (7)

- Double-Data-Rate SDRAM (DDR SDRAM)
  - It accesses the cell array in the same way with SDRAM, but transfer data on both edges of the clock.
  - The latency of these devices is the same as for standard SDRAMs, and their bandwidth is essentially doubled for long burst transfers.

Name	Clock Freq.	Data Rate
DDR200	100 MHZ	200 MHZ
DDR266	133 MHZ	266 MHZ
DDR333	167 MHZ	333 MHZ
DDR400	200 MHZ	400 MHZ

Synchronous DRAM (8)

- Versions of DDR
  - DDR (2.5V, 200~400MHz, 1GB)
  - DDR2 (1.8V, 400~800MHz, 4GB)
  - DDR3 (1.5V, 800~2400MHz, 8GB)
  - DDR4 (1.2V, 1600~3200MHz, 32GB)
  - DDR5 (1.1V, 4800~6400MHz, 128GB)

Quiz (1)

1. Comparing to SRAM, the main advantage of DRAM is ____.

   A. high speed B. non-volatile stored data

   C. high density D. easily controlled

2. What are advantages and disadvantages of DRAM?

   Advantages: High density, low cost

   Disadvantages: Longer memory access time;

   Leaky, needs to be refreshed.

Quiz (2)

3. 某一动态RAM芯片，容量为64K×1，除电源线、接地线和刷新线外，该芯片的最少引脚数目应为多少？

64K=2^{16}，由于地址线引脚只引出一半，因此地址线引脚数为8。数据线引脚数为1 (有的芯片数据输入线与数据输出线是分开的，则数据线引脚数就为2)。它有R/W信号，而没有CS信号。它有行地址选通信号RAS和列地址选通信号CAS。综上所述，除电源线、接地线和刷新线外，该芯片的最少引脚数目应为12。