Computer Organization & Architecture

2-3 Ripple-Carry Adder & Addition/Subtraction Logic Unit

Guohua Wang

School of Software Engineering

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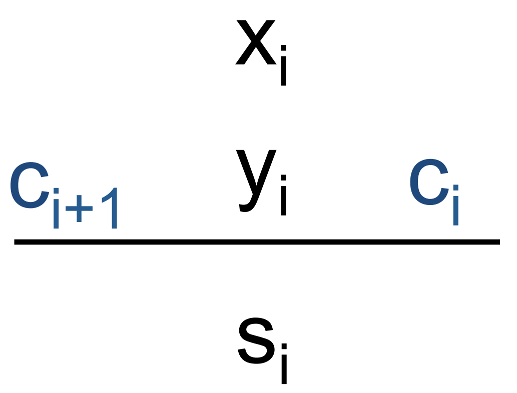
1-bit Full Adder (1)

- Full Adder
  - A full adder circuit takes three bits of input, and produces a two-bit output consisting of a sum and a carry out.



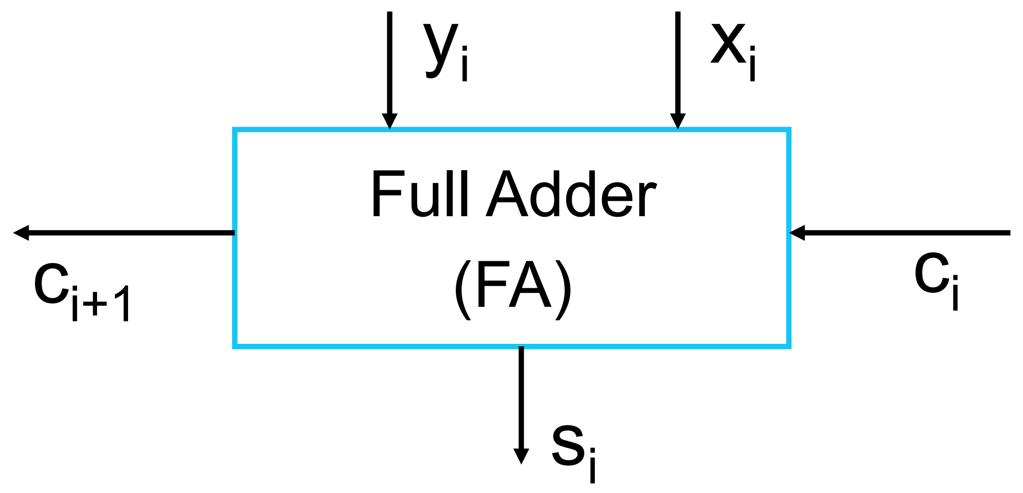


Figure 9.2 (a) Logic for a single stage

1-bit Full Adder (2)

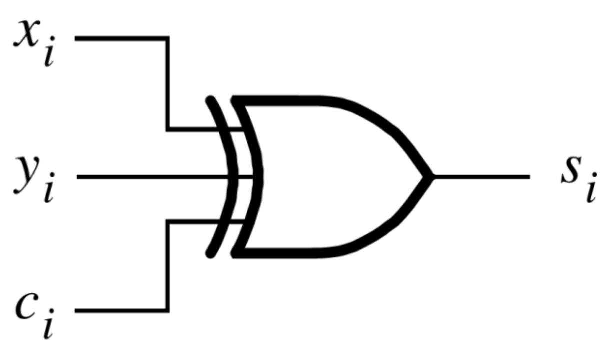
- Logic Truth Table

x_i	y_i	c_i	s_i	c_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1-bit Full Adder (3)

- Logic Expressions and Logic Figures
  - s_i

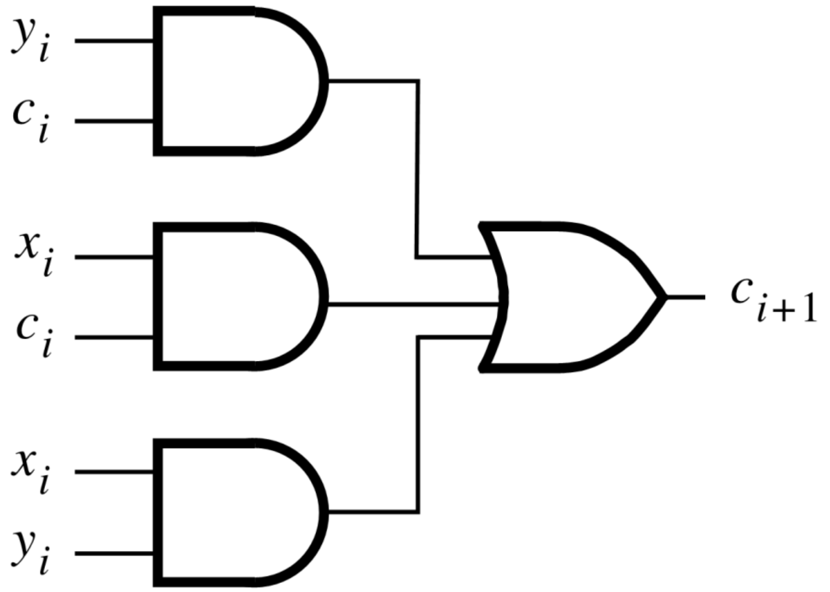
$$s_i = \bar{x}_i \bar{y}_i c_i + \bar{x}_i y_i \bar{c}_i + x_i \bar{y}_i \bar{c}_i + x_i y_i c_i$$
$$= x_i \oplus y_i \oplus c_i$$



1-bit Full Adder (4)

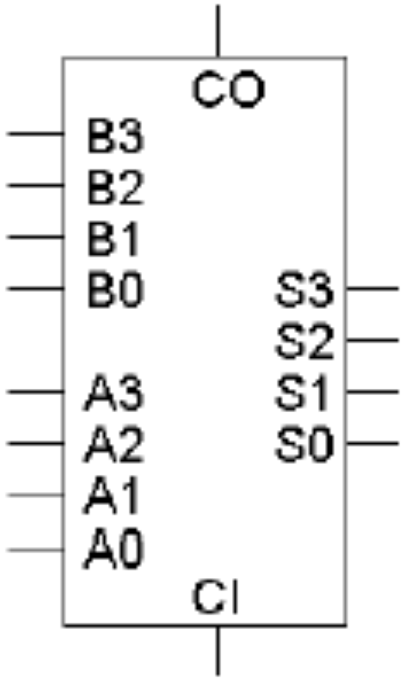
- Logic Expressions and Logic Figures (ctd.)
  - c_{i+1}

$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$



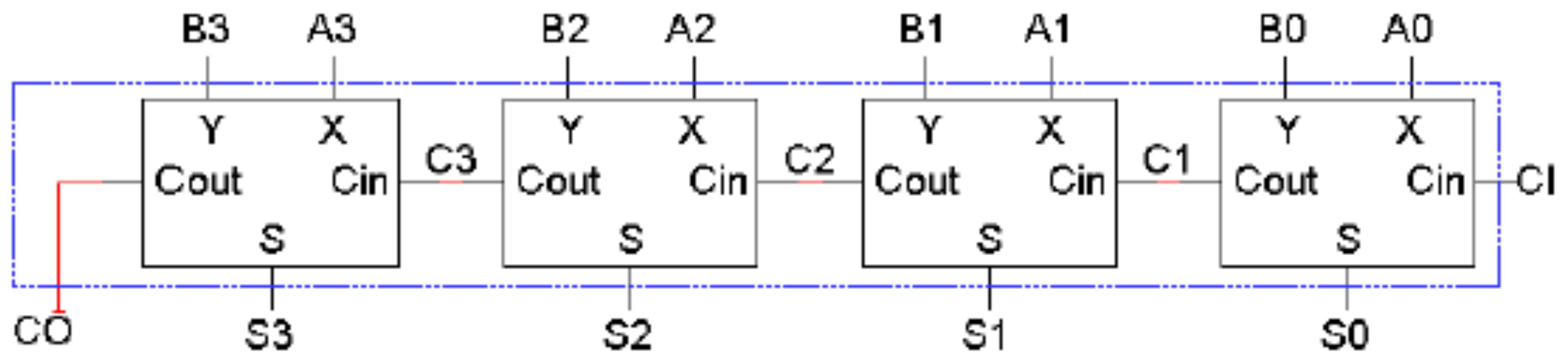
n-bit Ripple-Carry Adder (1)

- A 4-bit Adder
  - Four full adders together make a 4-bit adder.
  - There are nine total inputs:
    - Two 4-bit numbers, A3 A2 A1 A0 and B3 B2 B1 B0
    - An initial carry in, CI
  - The five outputs are:
    - A 4-bit sum, S3 S2 S1 S0
    - A carry out, CO



n-bit Ripple-Carry Adder (2)

- A 4-bit Adder



n-bit Ripple-Carry Adder (3)

- Organization of *n*-bit Ripple-Carry Adder

Input: $X=x_{n-1}\ldots x_1x_0$
$Y=y_{n-1}\ldots y_1y_0$
c_0

Output: $S=s_{n-1}\ldots s_1s_0$
c_n

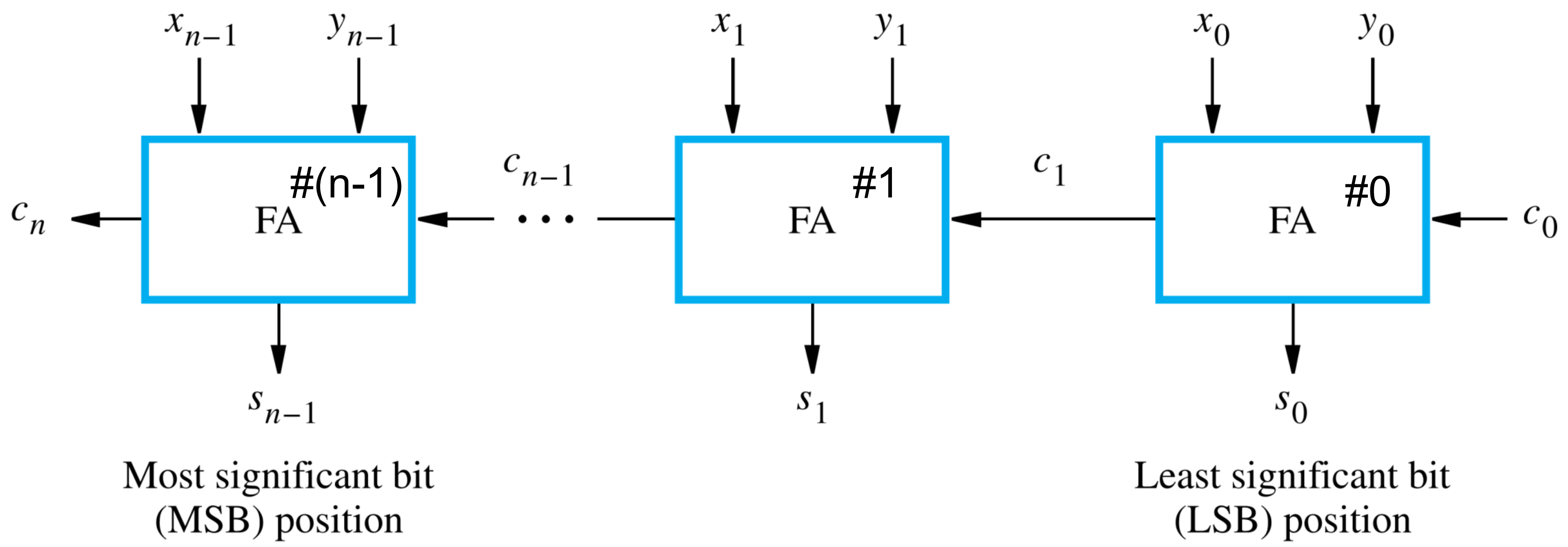


Figure 9.2 (b) An n-bit ripple-carry adder

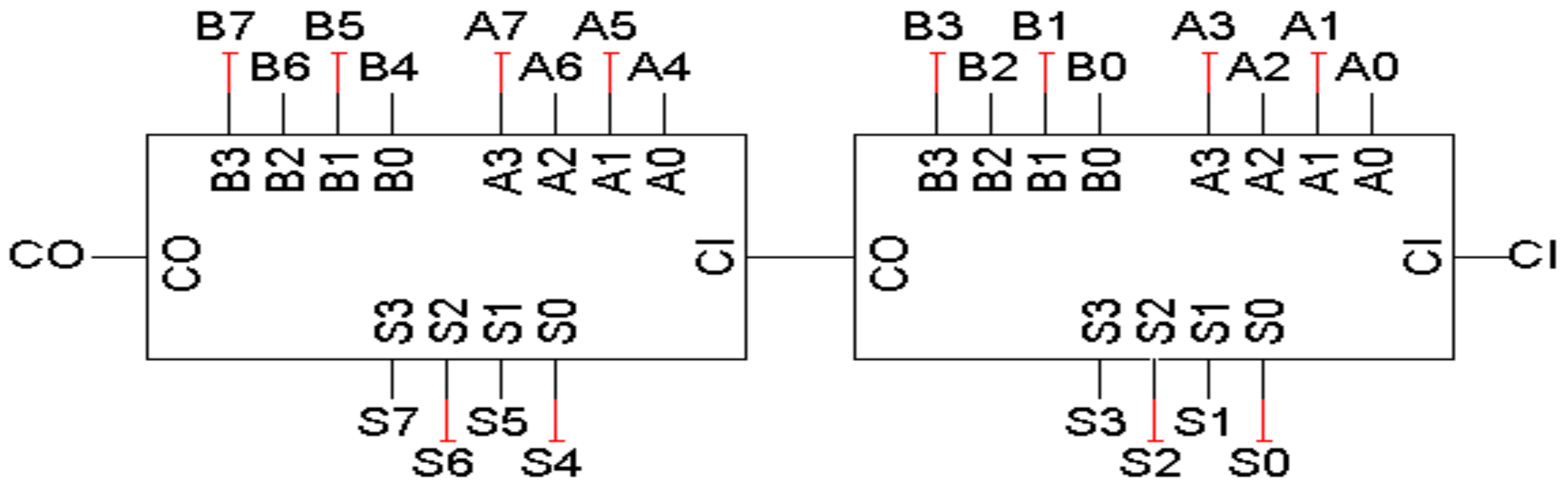
n-bit Ripple-Carry Adder (4)

- Overflow Detect
  - Overflow = $x_{n-1} y_{n-1} \bar{s}_{n-1} + \bar{x}_{n-1} \bar{y}_{n-1} s_{n-1}$
  - Or Overflow = $c_n \oplus c_{n-1}$

x_{n-1}	y_{n-1}	s_{n-1}	Overflow
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Hierarchical Adder (1)

- Using 4-bit adders to design an 8-bit adder
  - Example Figure



A3A2A1A0:	input pins of summand
B3B2B1B0:	input pins of summand
CI:	input pin of carry-in
S3S2S1S0:	output pin of sum
CO:	output pin of carry-out

Hierarchical Adder (2)

- Using *n*-bit adders to design a *kn*-bit adder
  - Example Figure

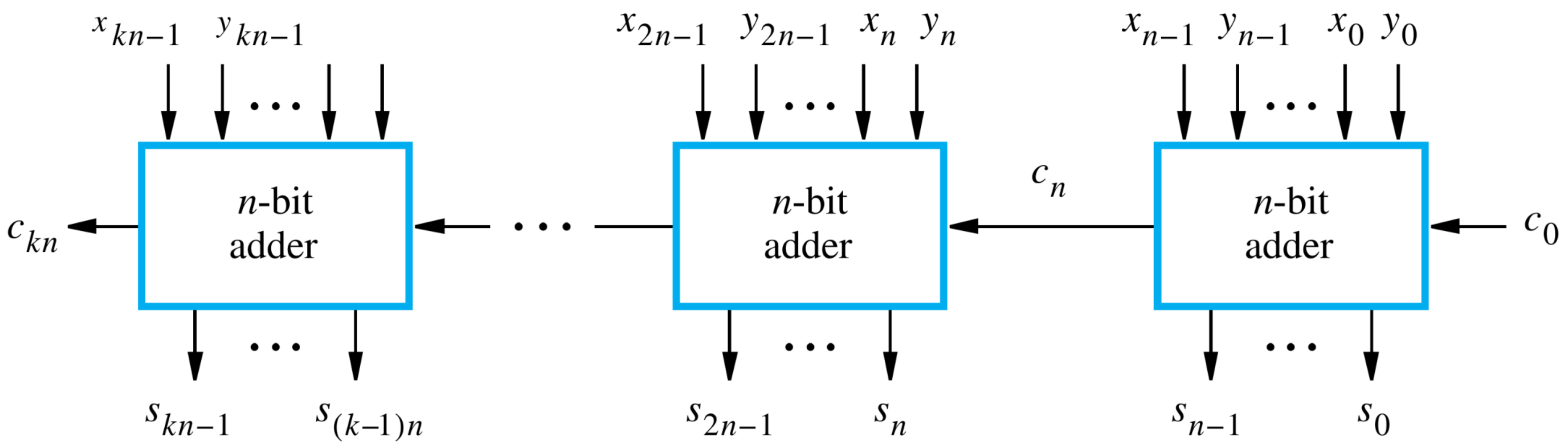


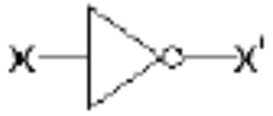
Figure 9.2 (c) Cascade of k n-bit adders

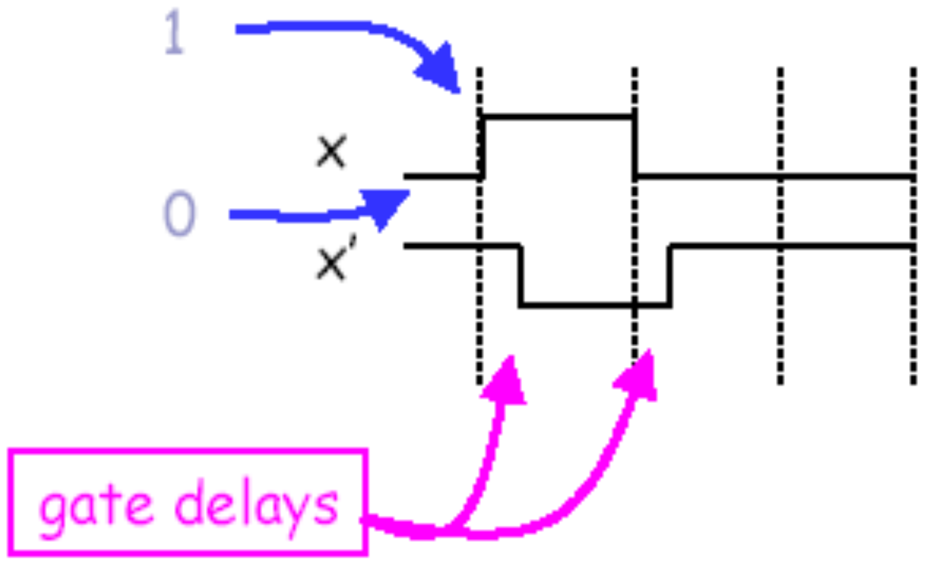
Gate Delays (1)

- Every gate takes some small fraction of a second between the time inputs are presented and the time the correct answer appears on the outputs. This little fraction of a second is called a gate delay.
- There are actually detailed ways of calculating gate delays that can get quite complicated, but for this class, let’s just assume that there’s some small constant delay that’s the same for all gates.

Gate Delays (2)

- We can use a timing diagram to show gate delays graphically.



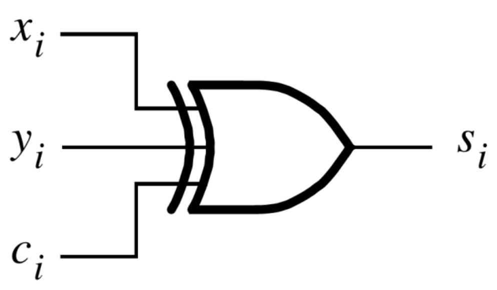


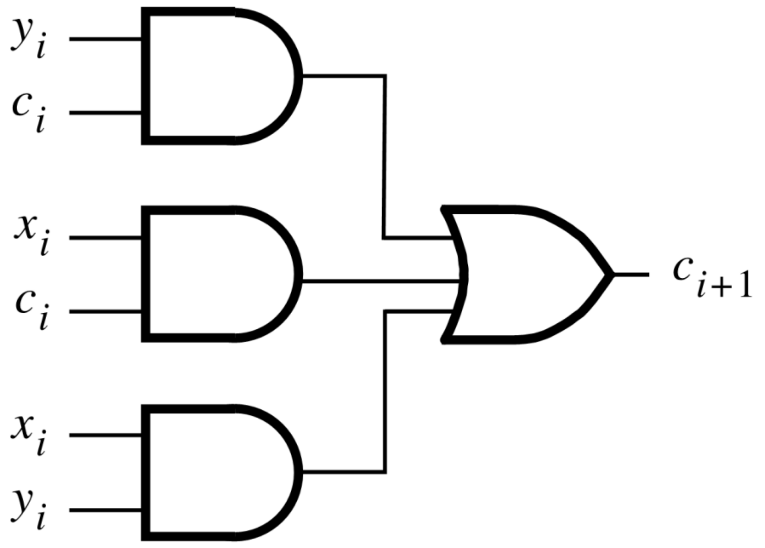
Propagation Delays in the Ripple Carry Adder (1)

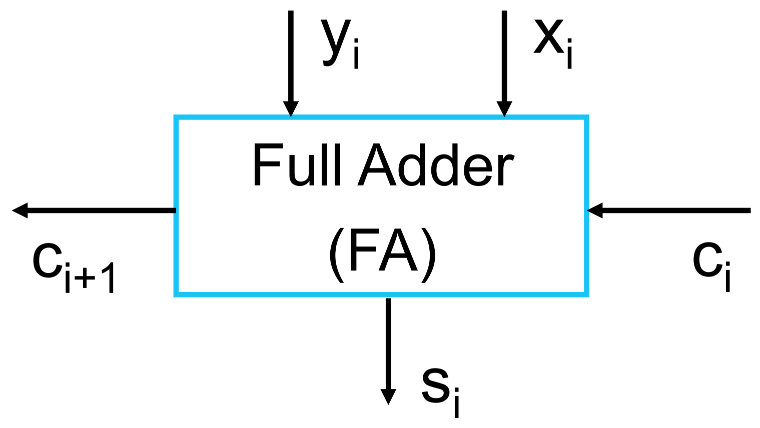
- The delay through a network of logic gates depends on the *integrated circuit electronic technology* used in fabricating the network and on *the number of gates* in the paths from inputs to outputs.
- The delay through any combinational logic network constructed from gates in a particular technology is determined by *adding up the number of logic-gate delays along the longest signal propagation path* through the network.
- In the case of the *n*-bit ripple-carry adder, the longest path is from inputs x_0,y_0 and c_0 at the LSB position to outputs c_n and s_{n-1} at the MSB position.

Propagation Delays in the Ripple Carry Adder (2)

- Assume that the gate delay of an AND gate or an OR gate or a XOR gate is T.

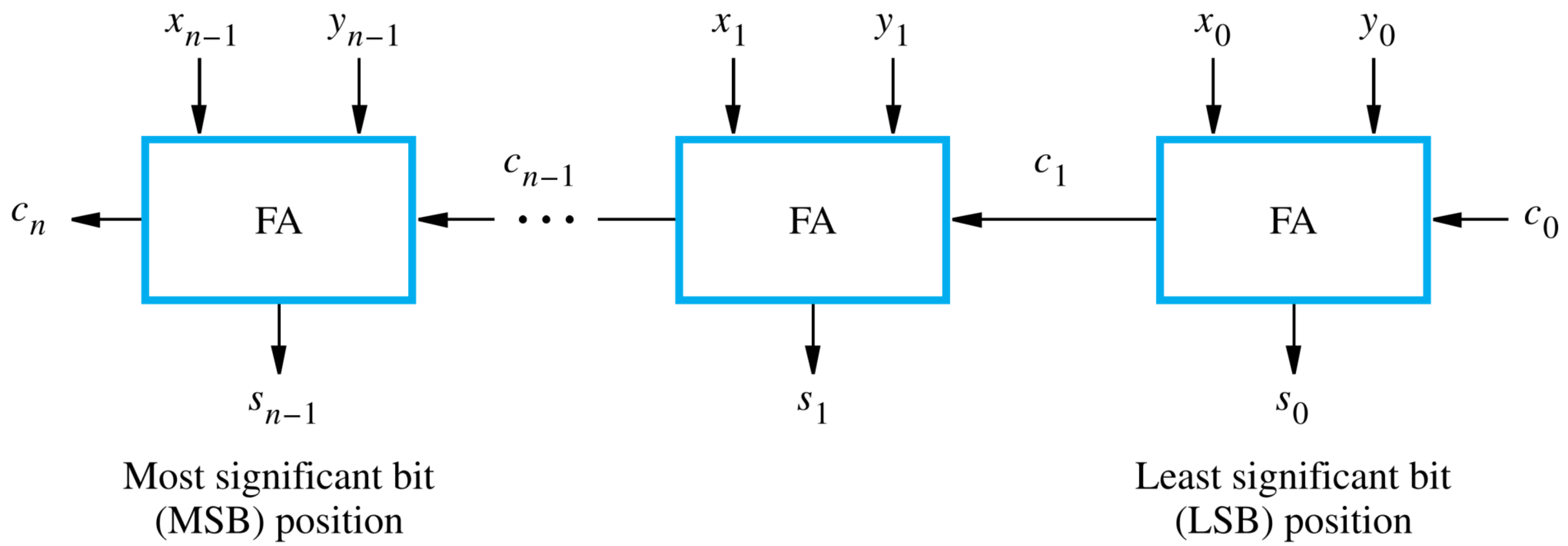






s_i	T
c_{i+1}	2T

Propagation Delays in the Ripple Carry Adder (3)



c_{n-1}	$2(n-1)T$
s_{n-1}	$2(n-1)T+T = (2n-1)T$
c_n	$2(n-1)T + 2T = (2n)T$

Addition/Subtraction Logic Unit (1)

- Organization of the Addition/Subtraction Logic Unit

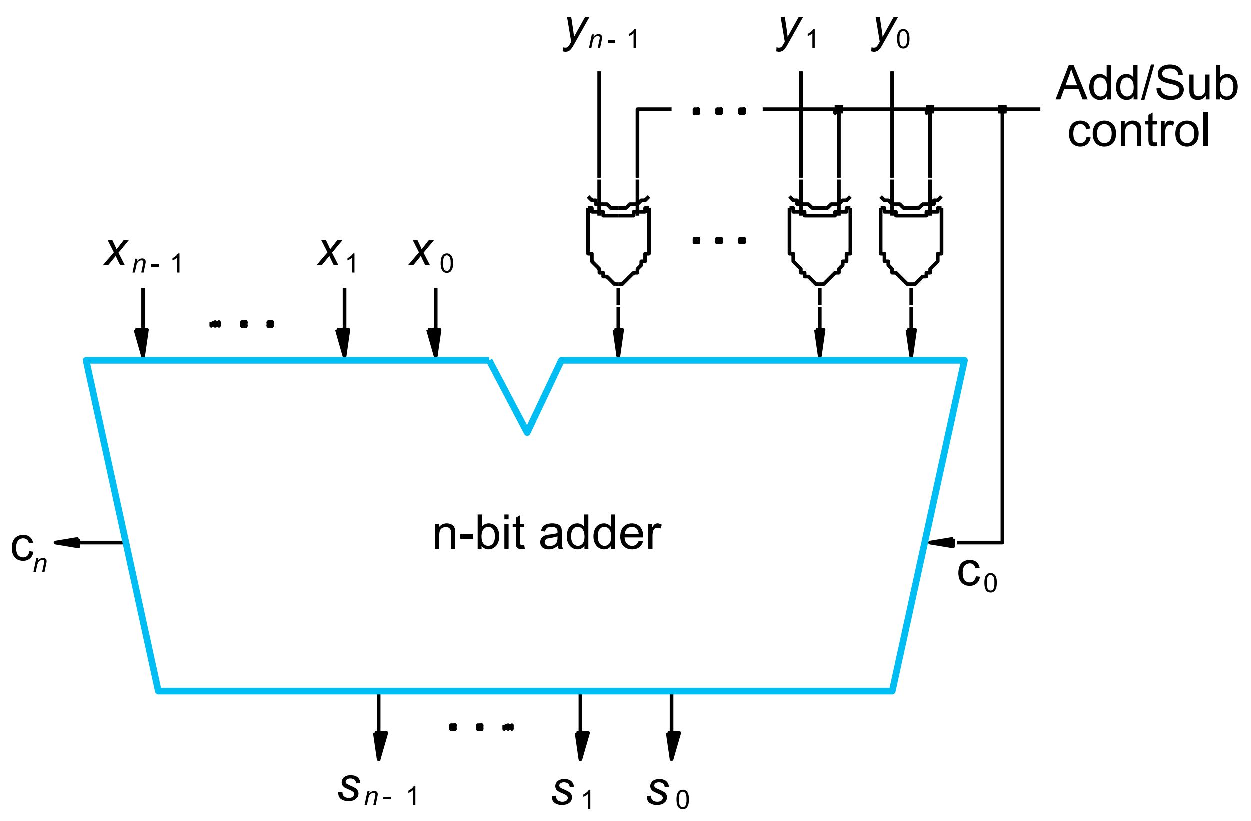


Figure 9.3. Binary addition-subtraction logic network

$$0 \oplus Y = Y$$

$$1 \oplus Y = \overline{Y}$$

Add/Sub Control=0 $c_0=0$

Perform Addition

Add/Sub Control=1 $c_0=1$

Perform Subtraction

Addition/Subtraction Logic Unit (2)

- An XOR gate can be added to detect the overflow.
- All sum bits are available in *2n* gate delays, including the delay through the XOR gate on the Y input.

Quiz

- In a 1-bit full adder, which expression is s_i?

  A. x_i+y_i B. $x_i \oplus y_i$ C. x_iy_i D. $x_i \oplus y_i \oplus c_i$

- In a 1-bit full adder, which expression is c_{i+1}?

  A. $x_i+y_i+c_i$ B. $x_iy_ic_i$ C. $x_iy_i+x_ic_i+y_ic_i$ D. $x_i \oplus y_i \oplus c_i$

- If we want to construct a 64-bit adder, how many adders do we need if we have some 4-bit ripple carry adders?

  A. 32 B. 16 C. 8 D. 4