1. Which type of memory will need refresh circuitry.

A. DRAM B. Flash C. ROM D. Blu-ray

2. The advantage of carry-lookahead adder is.

A. decrease cost of the adder. B. save hardware parts.

C. augment CPU clock frequency. D. accelerate the generation of the carries.

3. In the direct addressing mode.

A. The operand is inside the instruction.

B. The address of the operand is inside the instruction.

C. The register containing the address of the operand is specified inside the instruction.

D. The location of the operand is implicit.

4. In a microprogram-control computer, the microinstructions are stored in a memory called the.

A. direct memory B. physical memory C. virtual memory D. control store

5. Consider a four bit ALU which does four bit arithmetic. When computing 1101 + 1011, what is the status of NZCV flags.

6. The pipelining technique typically improves the performance of a computer by.

A. decreasing the execution time of an instruction B. improving CPU block frequency

C. improving the throughput D. decreasing the cache miss rate

7. The required control signals in a hardwired control unit are determined by the following information except.

A. contents of the control step counter B. contents of the MAR (memory address register)

C. contents of the IR (instruction register) D. contents of the condition code flags

8. The processor informs the IO devices that it is ready to acknowledge interrupts by.

A. enabling the interrupt request line B. activating the interrupt acknowledge line

C. activating the interrupt completion line D. enabling the interrupt starting line

9. The starting address sent by the device in the vectored interrupt is called as.

A. interrupt vector B. location ID C. service location D. service ID

10. If the bytes 0x12, followed by 0x34, followed by 0x56, followed by 0x78 are interpreted as a 4-byte little endian integer, what value will they have.

1. Explain the process of DMA.

2. Imagine a system with the following parameters. Virtual addresses 20 bits, physical addresses 18 bits, page size 1 KB. Please give the format of virtual address and physical address. Explain your answer.

3. The two numbers given below are multiplied using the Booth's algorithm. Multiplicand: 0101101011101110. Multiplier: 0111011110111101. How many additions/subtractions are required for the multiplication of the above two numbers.

4. In a computer, can we build a memory system with one type of memory to get a large, fast and cheap memory.

1. Suppose we have a 7-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 3 exponent bits, and 3 fraction bits. The exponent part uses an excess-3 representation. The remaining 3-bit mantissa is normalized with an implied 1 to the left of the binary point. Rounding is employed as the truncation methal.

(1) Write the largest positive normalized floating-point number. And write the smallest positive normalized floating-point number.

(2) Write the result and computation process of A+B. Give the result in normalized form. A = 1.001, B= 0.010111.

2. Is it possible to design an expanding opcode to allow the following to be encoded in a 12-bit instruction. Justify your answer. Assume a register operand requires 3 bits and this instruction set does not allow memory addresses to be directly used in an instruction.

(1) 6 instructions with 3 registers (2) 14 instructions with 2 registers (3) 15 instructions with 1 register (4) 8 instructions with 0 register

3. Part of a RISC-style processor's datapath is shown as the following figure. Instruction execution can be divided into 5-stages. Now we want to execute Mutiply R7, R8, R9 on this datapath. Before this instruction, [R7]=20, [R8]=10, [R9]=30. Write the values of registers at the end of instruction stage 2, stage 3, stage 4. 2.[RA],[RB]. 3.[RZ]. 4.[RY].

4. The following sequence of RISC instructions are executed on a 5-stage pipeline. We can indicate the 5 stages of the pipeline using: F, D, C, M and W. Add R2, R1, R3. Sub R4, R2, R1 And R5, R1, R2 Sub R6, R2, R4

(1) Write all the data dependencies in the four instructions above.

(2) Draw a figure to illustrate the execution of the four instructions on the pipeline. Assume that the pipeline has operand forwarding paths. Pay attention to mark the forwarding paths.

5. An integrated circuit RAM chip can hold 2048 words os 8 bits each (2k\*8).

(1) How many addresses and the data lines are there in the chips.

(2) How many chips are needed to construct a 32k\*16 RAM.

(3) How many addresses and the data lines are there in a 32k\*16 RAM.

(4) What size of the decoder is needed to construct 32k\*16 memory from the 2k\*8 chips. What are the inputs to the decoder and where are its outputs connected.

6. A computer system uses 16-bit memory addresses. It has a 2k-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

(1) Calculate the number of bits in each of the tag, block and word fields of the memory address.

(2) When a program is executed, the processor reads data sequentially from the following word addresses: 0080H, 0090H, 0880H, 0884H, 0080H, 0880H. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

1. \_\_\_\_\_ is not a kind of random access memory.

A. DRAM B. SRAM C. Floppy disk D. Cache

2. \_\_\_\_\_ is not the basic functional unit of a computer.

A. Input unit B. Network interface card C. Memory D. Control unit

3. \_\_\_\_\_ addressing mode only exists in CISC-style processors.

A. Indirect B. Immediate C. Index D. Register indirect

4. \_\_\_\_\_ is not a kind of cache mapping scheme.

A. Fully associative mapping B. set associative mapping

C. Segmentation with paging D. Direct mapping

5. In program-controlled IO, the processor always polls \_\_\_\_\_\_\_ register in the IO interface to see if the IO device is ready.

A. status B. data C. control D. none of above

6. The functions of the IO interface do not include \_\_\_\_\_.

A. device communication B. instruction decoding

C. error detection D. control and signaling

7. Which of the following statements is true for memory-mapped IO?

A. IO devices and memory use separate address spaces.

B. Input/Output operations of the devices look different from memory read/write.

C. The instructions which can access memory can not be used to access IO devices.

D. The address space for the memory is reduced.

8. \_\_\_\_\_ is a kind of DMA transfer mode.

A. Direct mode B. Burst mode C. Indirect mode D. Relative mode

9. Which of the following statements is true in a CISC-style processor.

A. Each instruction fits in a single word.

B. It has a small set of instructions.

C. A load/store architecture is used.

D. Autoincrement addressing mode can be used.

10. A microprogram is stored in \_\_\_\_\_.

A. control store B. microinstructions C. control word D. micro memory

1. Assuming that register R3 contains a number 200, register R5 contains a number 100, and the memory is byte-addressable, what is the effective address in each of the following cases.

(1) -(R5) (2) (R3)+ (3) 20(R3,R5)

2. In a 16-bit floating-point number format, the most significant bit is the sign bit, the following 6 bits are for excess -31 exponent, and the remaining 9 bits are for normalized mantissa with an implied 1 to the left of the binary point.

(1) What is the 16-bit floating-point representation of -36.

(2) What is the decimal equivalent of the floating-point number 0 100010 010100000.

3. Describe the differences between interrupt-service routine and subroutine call.

4. How many types of pipeline hazards. What are they. Which hazard is caused by data dependencies. And which hazard is caused by resource limitation.

1. Design a 32Kx32 memory using 4Kx8 memory chips.

(1) How many rows and columns are the memory chips organized.

(2) How many bits are required for the memory chip select.

(3) Draw the implementation figure of the 32Kx32 memory.

2. Assume that a computer's instruction length is 15 bits, and the length of operand address is 4 bits. Design four types of instructions: three-address instructions, two-address instructions, one-address instructions, and zero-address instruction. Please describe the design of the instruction format and specify the number of each type of instructions.

3. Show A➗B on the 5-bit unsigned numbers A=11010 and B=01001 using non-restoring division.

4. Consider the following instructions at given hexadecimal addresses in the memory.

0x0010 Add R5,R1,R2

0x0014 Subtract R6,R5,#8

0x0018 Add R7,R5,#12

0x001C Subtract R8,R1,R2

Registers R1,R2 and R5 contain decimals 30, 400 and 50 respectively. The instructions are executed in a computer with a five-stage pipeline. The first instruction is fetched in clock cycle 1, and the remaining instructions are fetched in successive cycles.

(1) Draw a diagram showing the flow of the instructions through the pipeline, assuming that the pipeline provides no forwarding paths.

(2) Draw a diagram showing the flow of the instructions through the pipeline, assuming that the pipeline provides forwarding paths to the ALU from registers RY and RZ.

(3) Write down the contents of registers IR, PC, RA, RB, RZ and RY in the pipeline with operand forwarding during cycles 2 to 8.

5. In a 2-way set associative mapped cache consisting of eight words, each cache line can hold two 32-bit words. The memory is byte-addressable. The processor reads data sequentially from the following memory addresses which are represented by hexadecimal numbers: 18, 14, 1C, 20, 2C, 48.

Assume that the cache is initially empty. Show the contents of the cache (denoted by the memory addresses) at the end of each data read. LRU replacement algorithm is used.