Chapter5 Parallel Processor and Multiprocessor

Parallelism

At the same time or at the same interval, multiple same or different tasks are processed.

- **Simultaneity**
- **Concurrency**

Chapter5 Parallel Processor and Multiprocessor

Granularity

Applications exhibit parallelism at various levels.

- **Fine grain:**
  Parallelism inherent in a single instruction stream and usually does not involve the OS but done at compilation stage.
- **Medium grain:**
  Potential parallelism of an application can be implemented by multiple threads in a single process. Usually programmer specifies the parallelism in the design.
- **Coarse grain:**
  Multiprocessing of concurrent processes can be implemented in a multiprogramming environment.

Chapter5 Parallel Processor and Multiprocessor

Technical ways to improve the parallelism of the computer system:

- **Time Interleaving**
- **Resource Replication**
- **Resource Sharing**

Chapter5 Parallel Processor and Multiprocessor

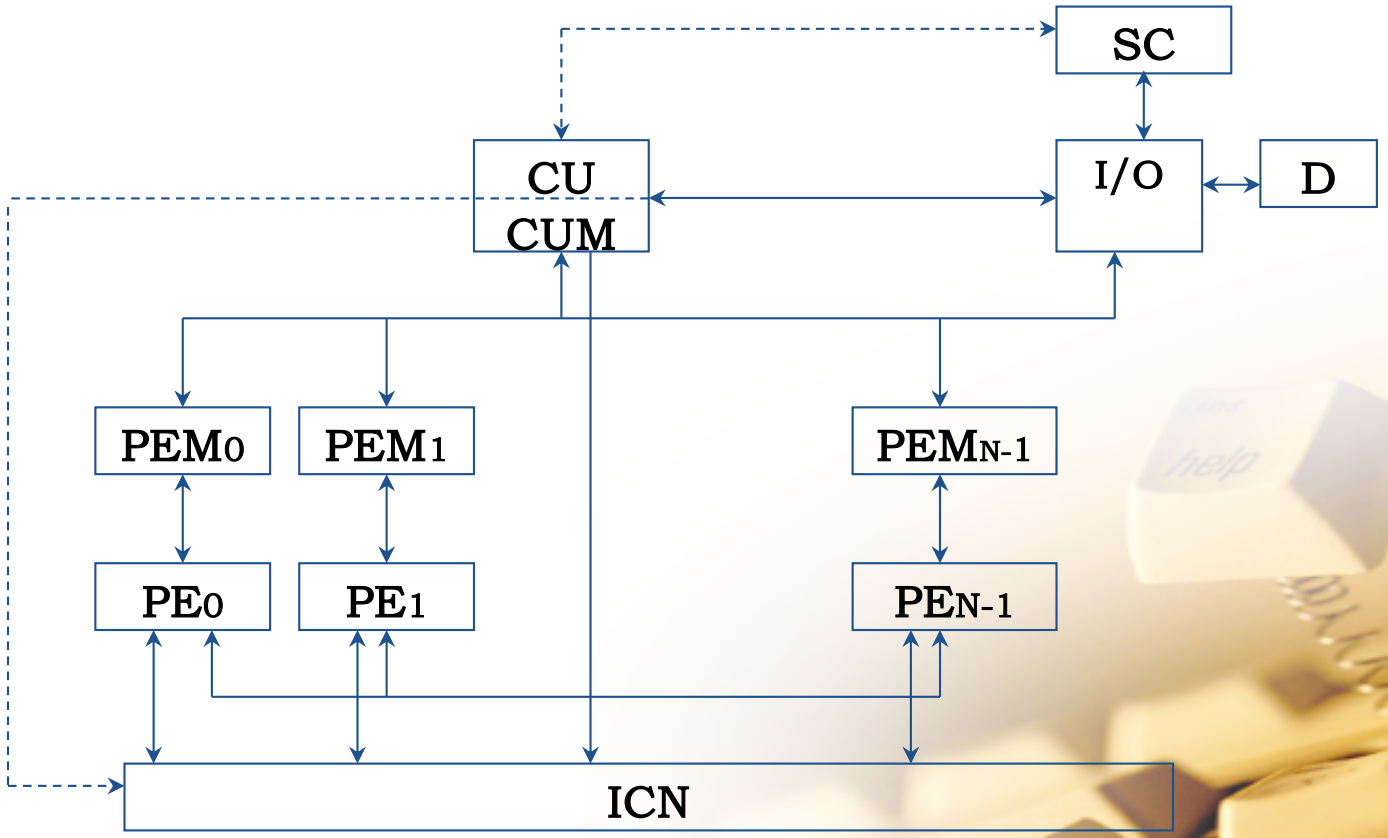
Principle of Array Processor

In an array processor , we set up multiple same processing units (PE), and put them in a certain way of interconnection. Under a common control unit(CU), multiple different data can be completed in parallel according to the same instruction operation. It depends on the operation level parallel processing to improve the speed of the computer system.

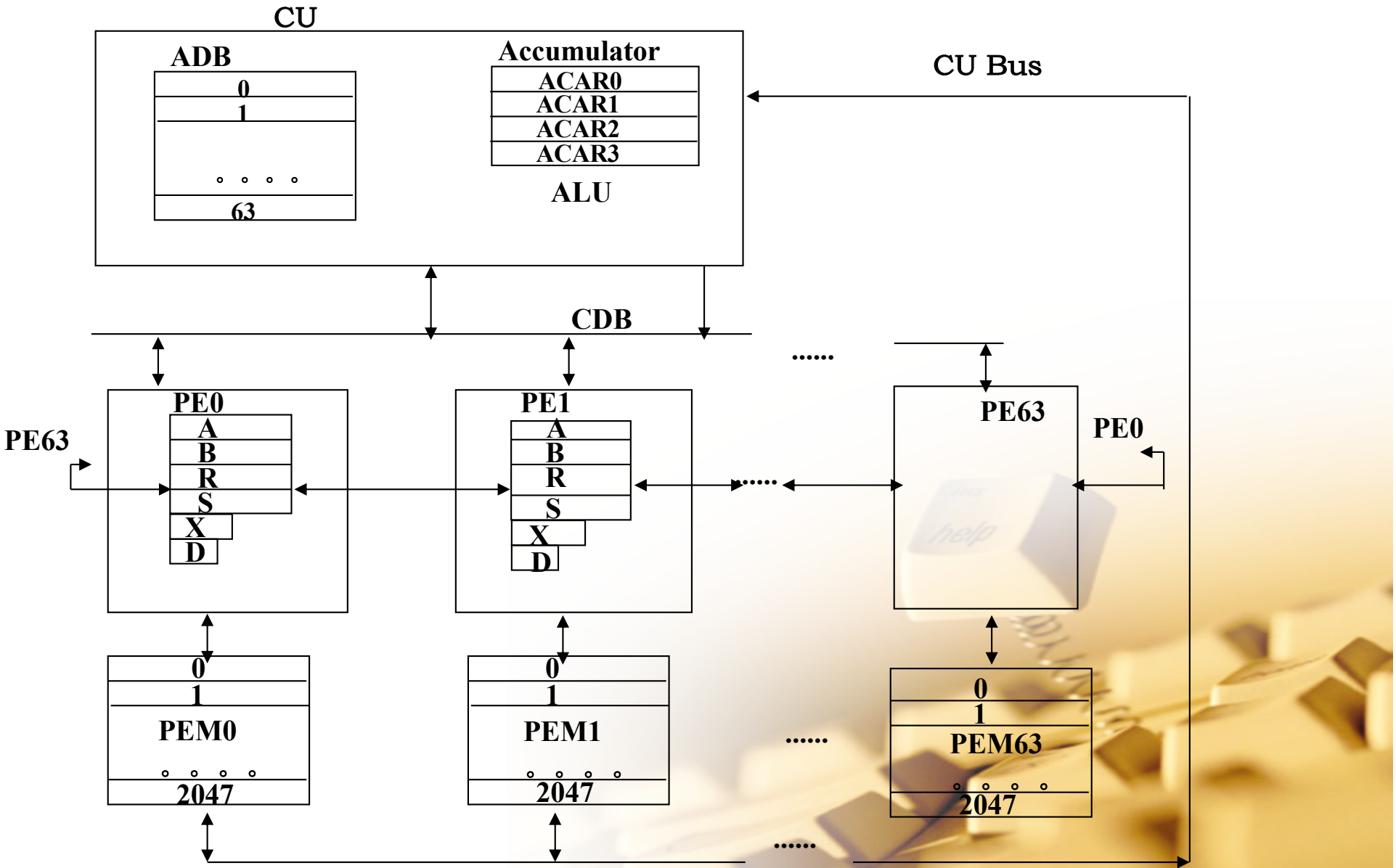
Chapter5 Parallel Processor and Multiprocessor

Classification of Array Processor

1. Distributed Memory Processor

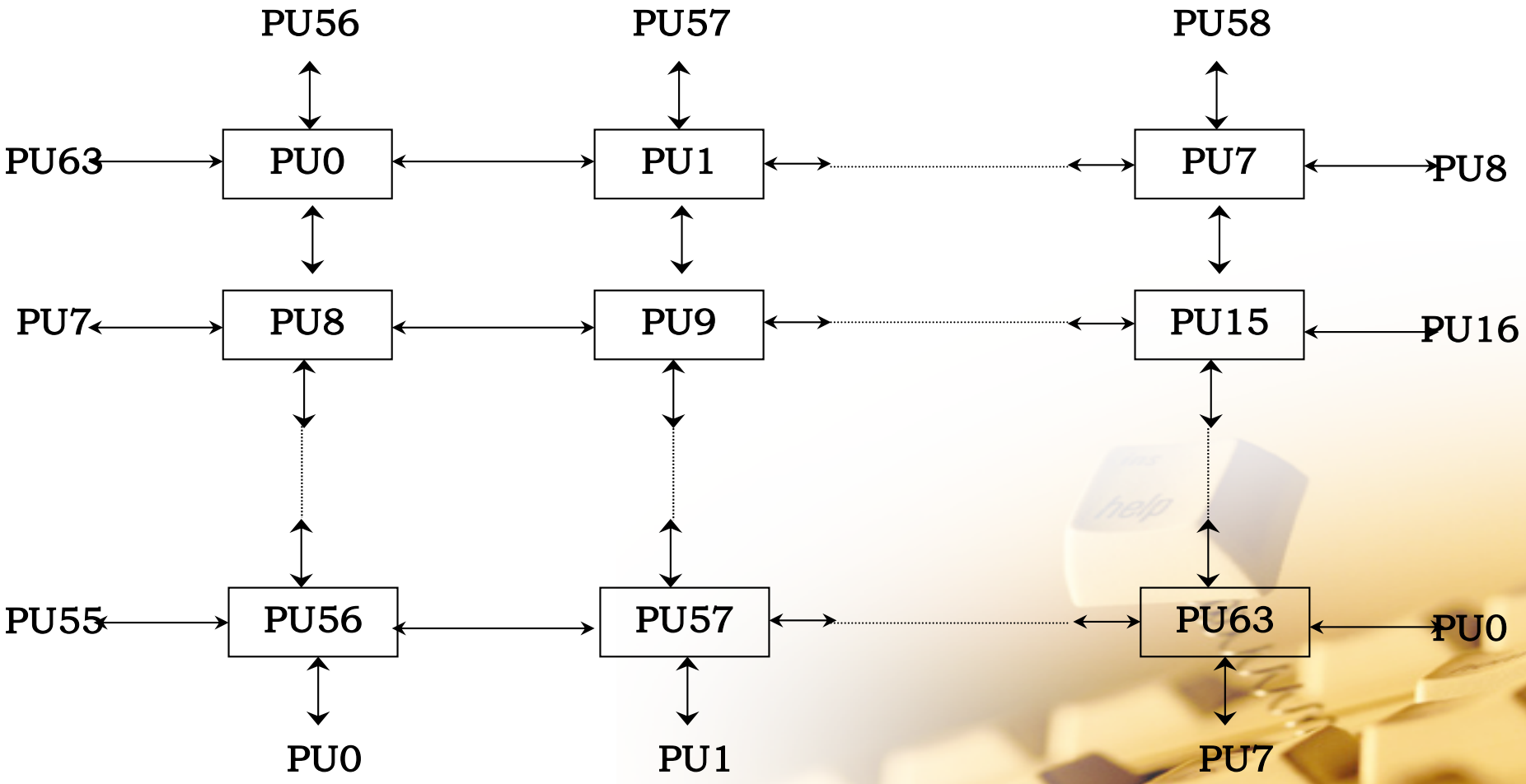


Chapter5 Parallel Processor and Multiprocessor



ILLIAC-IV Principle Diagram

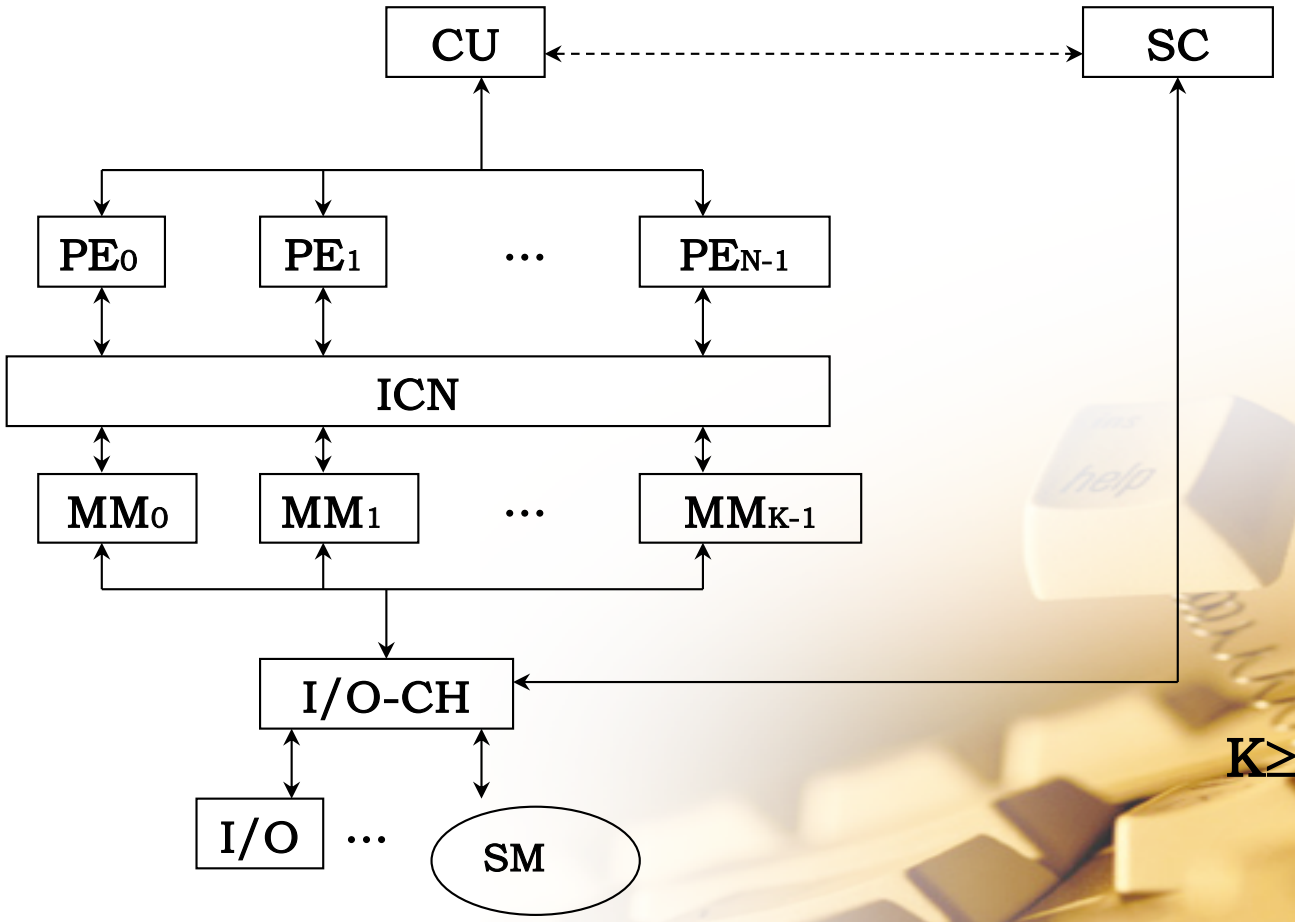
Chapter5 Parallel Processor and Multiprocessor



Example: PU63→PU7→PU8→PU9→PU10

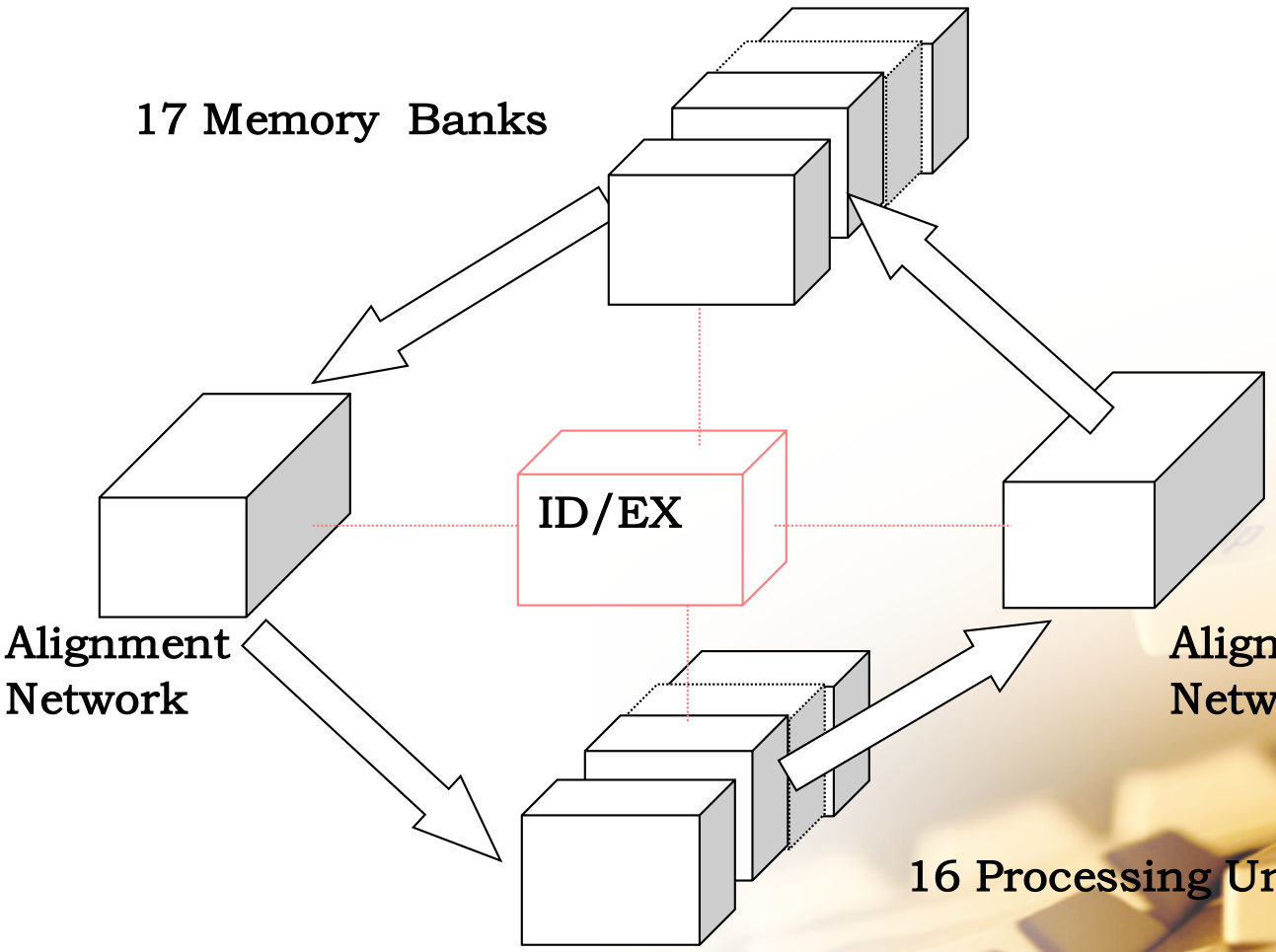
Chapter5 Parallel Processor and Multiprocessor

2. Shared Memory Processor



Chapter5 Parallel Processor and Multiprocessor

BSP Processor

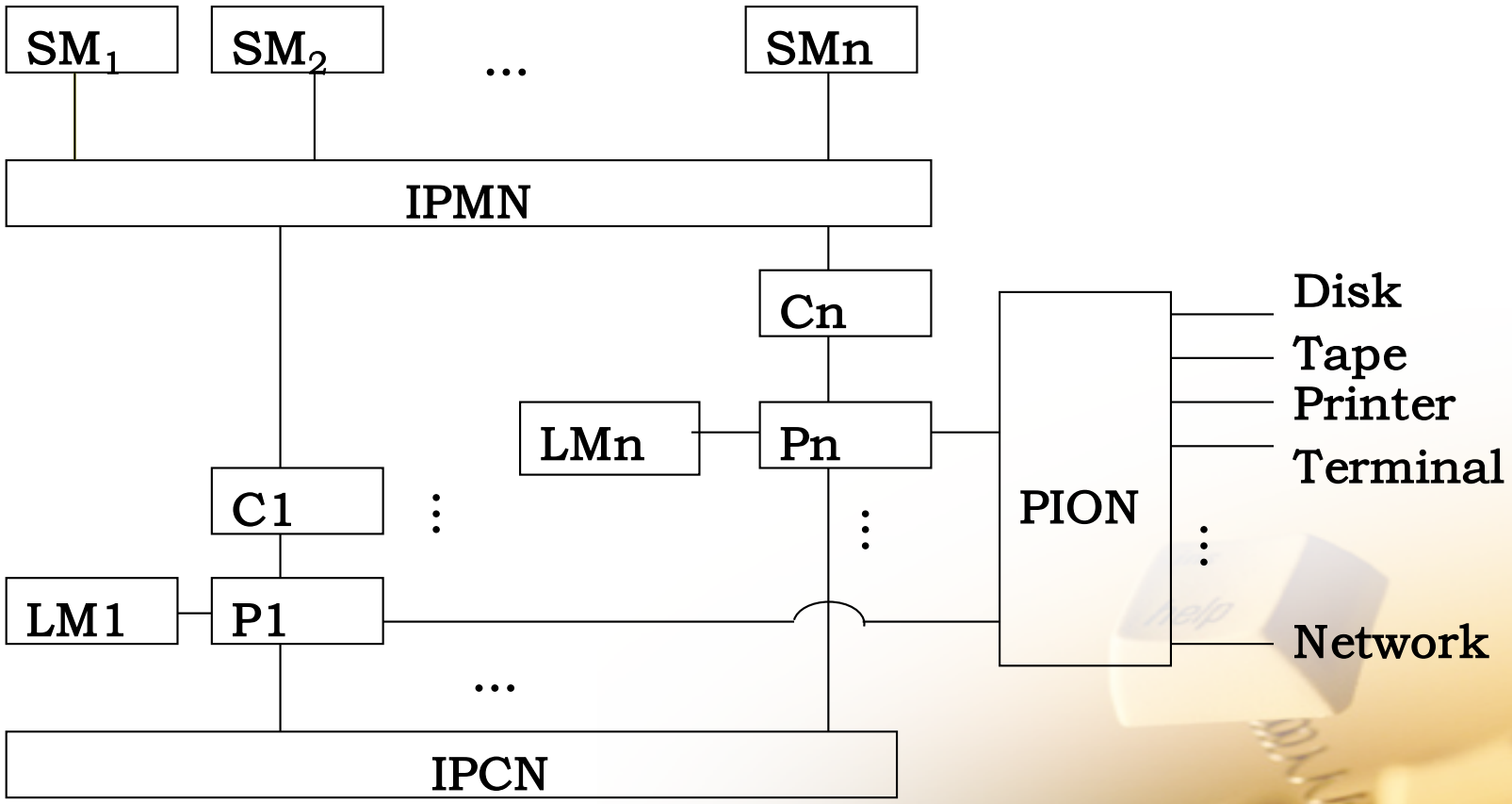


Chapter5 Parallel Processor and Multiprocessor

Interconnect Network

It is composed of the switching elements, according to a certain topological structure and control mode, used for connecting multiple components of a computer system or multiple processors.

Chapter5 Parallel Processor and Multiprocessor



Chapter5 Parallel Processor and Multiprocessor

Interconnect Function

- I/O Mapping Representation
- Cyclic Representation
- Function Representation

Chapter5 Parallel Processor and Multiprocessor

- **I/O Mapping Representation**

  0---f(0),1---f(1),・・・,N-1---f(N-1)

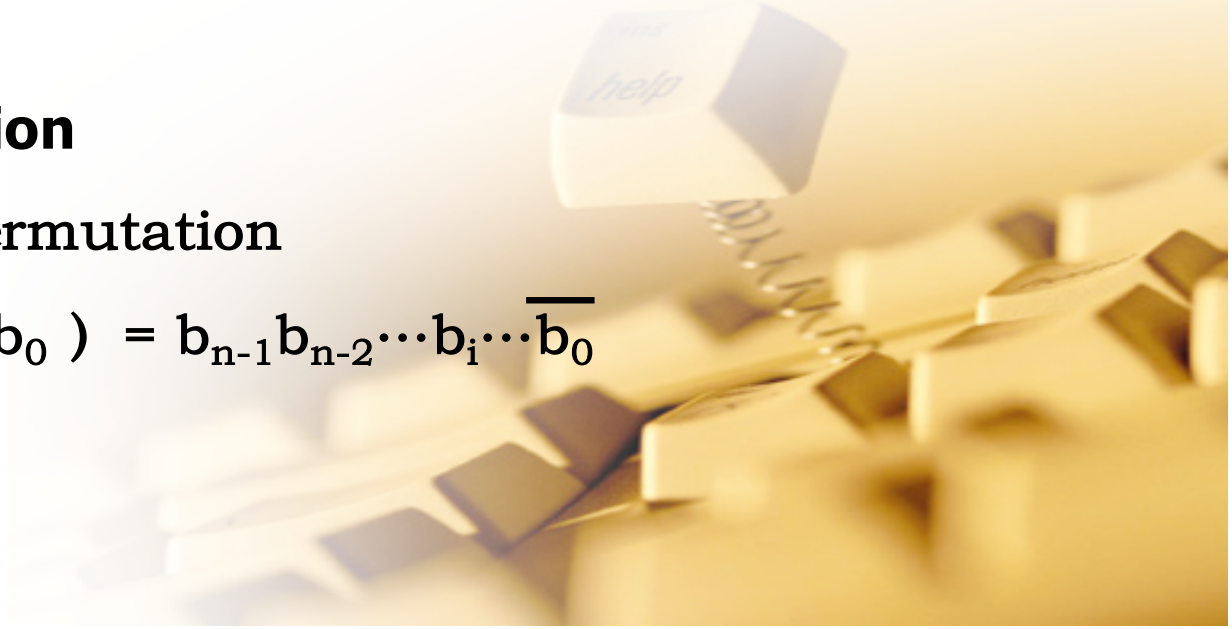
- **Cyclic Representation**

  $f\ (X_0) = X_1,\ f\ (X_1) = X_2,\ \cdots\cdots,\ f\ (X_j) = X_j+1,\ \cdots\cdots,\ f\ (X_{k-1}) = X_0$

- **Function Representation**

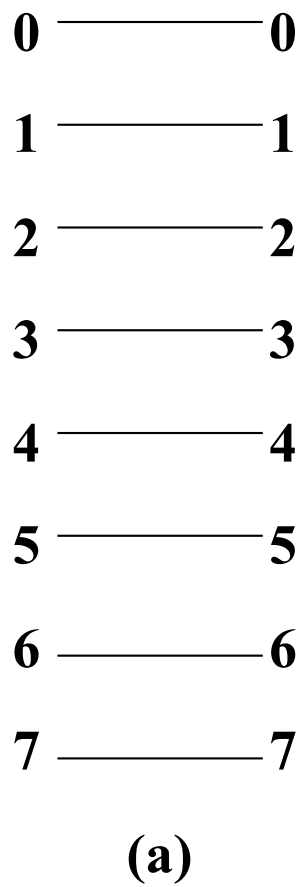
  Example: Exchange Permutation

  $$E\ (\ b_{n-1}b_{n-2}\cdots b_i\cdots b_0\ ) = b_{n-1}b_{n-2}\cdots b_i\cdots \overline{b_0}$$

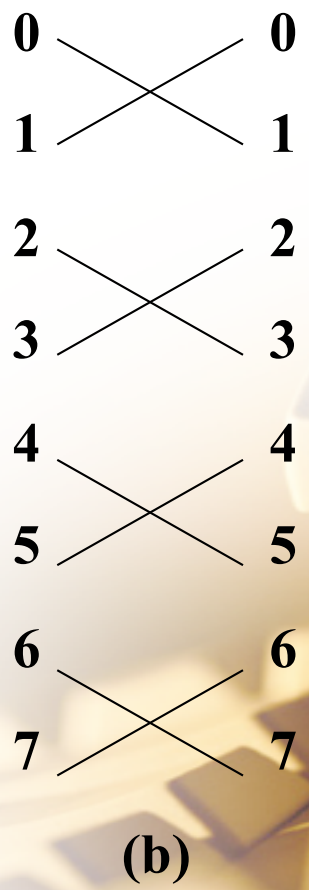


Chapter5 Parallel Processor and Multiprocessor

- **Identity Permutation (a)**
- **Exchange Permutation (b)**



(a)



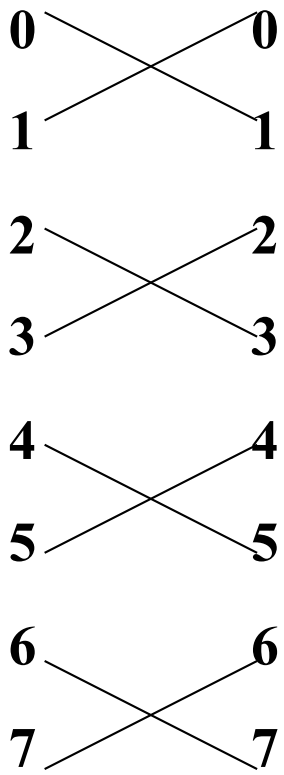
(b)

Chapter5 Parallel Processor and Multiprocessor

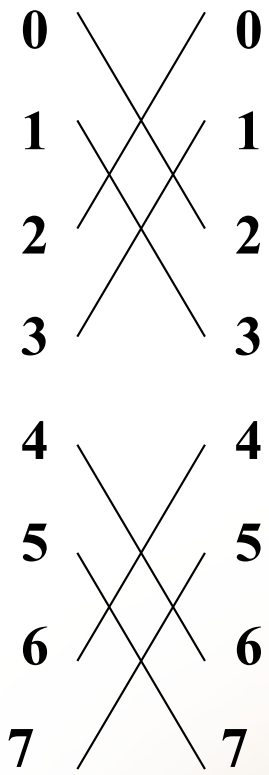
Single-stage Cube Permutation

$$\mathrm{Cube}_k(X_{n-1}X_{n-2}\cdots X_{k+1}X_kX_{k-1}\cdots X_1X_0)$$
$$= X_{n-1}X_{n-2}\cdots X_{k+1}\overline{X_k}X_{k-1}\cdots X_1X_0$$

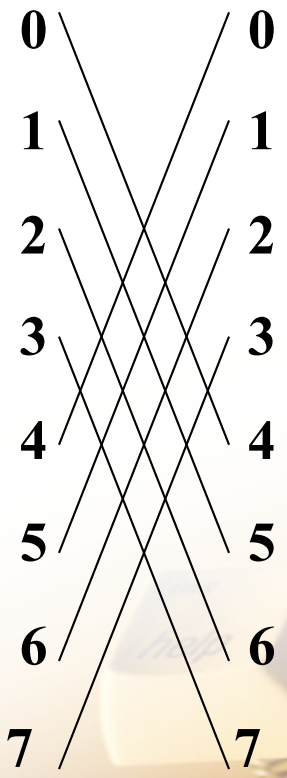
Chapter5 Parallel Processor and Multiprocessor



(a) C_0



(b) C_1



(c) C_2

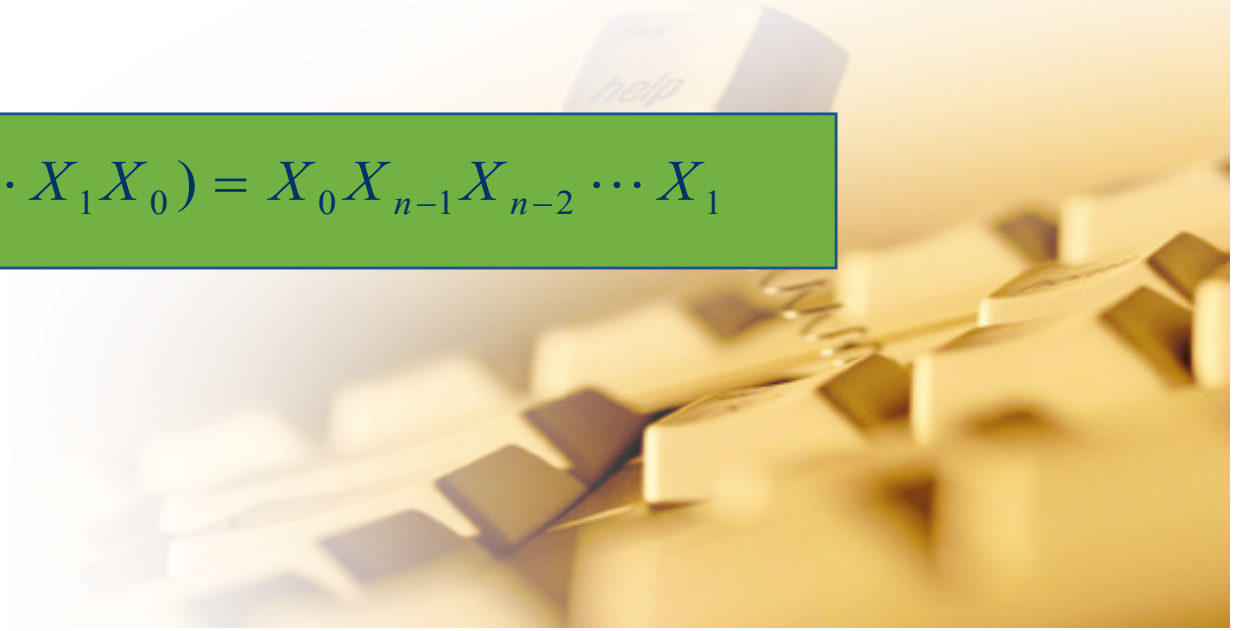
Chapter5 Parallel Processor and Multiprocessor

Perfect Shuffle Permutation

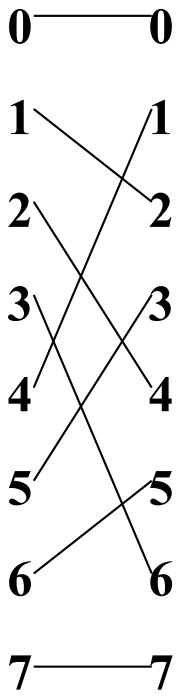
$$\sigma(X_{n-1}X_{n-2}\cdots X_1X_0) = X_{n-2}\cdots X_1X_0X_{n-1}$$

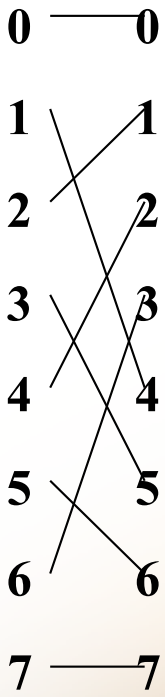
Inverse Perfect Shuffle Permutation

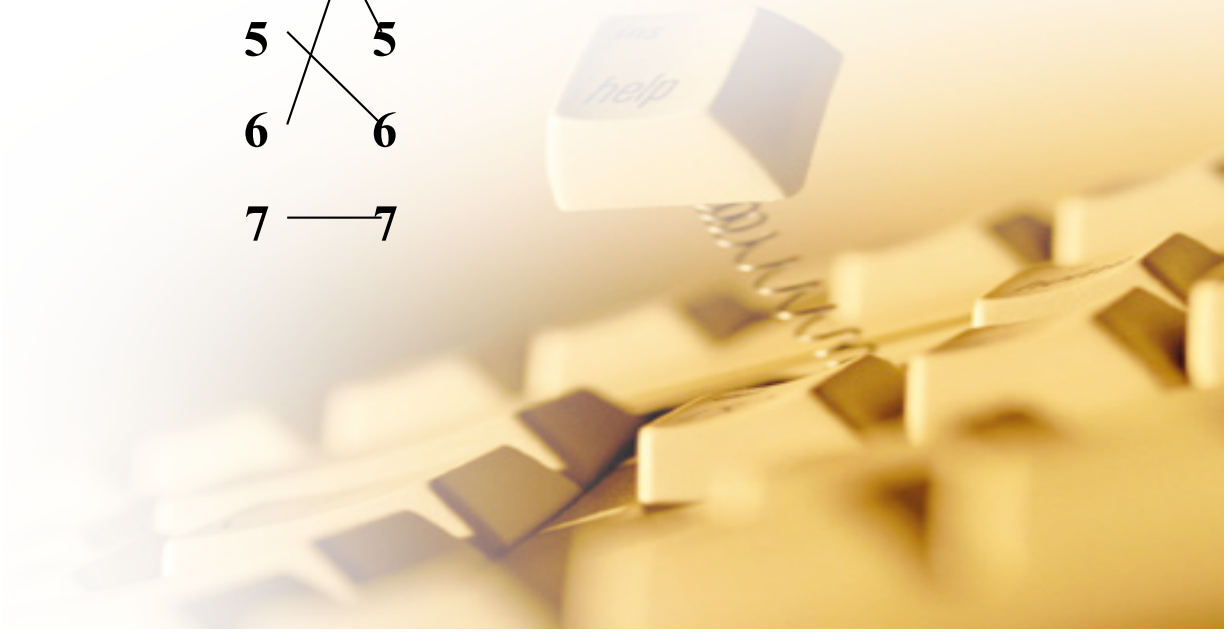
$$\sigma^{-1} = (X_{n-1}X_{n-2}\cdots X_1X_0) = X_0X_{n-1}X_{n-2}\cdots X_1$$



Chapter5 Parallel Processor and Multiprocessor







Chapter5 Parallel Processor and Multiprocessor

Butterfly Permutation

$$\beta\ (X_{n-1}X_{n-2}\cdots X_1X_0) = X_0X_{n-2}\cdots X_1\ X_{n-1}$$

Subbutterfly Permutation

$$\beta_{(K)}(X_{n-1}X_{n-2}\ \cdots X_{k+1}X_kX_{k-1}\cdots X_1X_0)$$

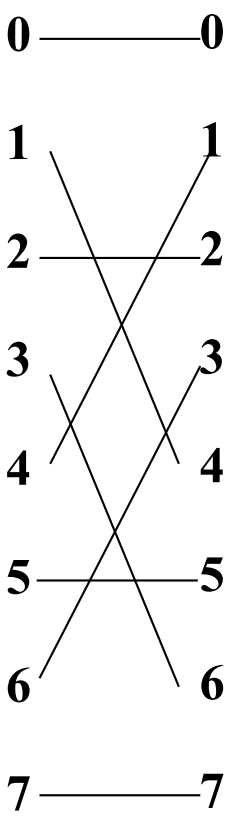
$$= X_{n-1}X_{n-2}\ \cdots X_{k+1}X_0X_{k-1}\cdots X_1X_k$$

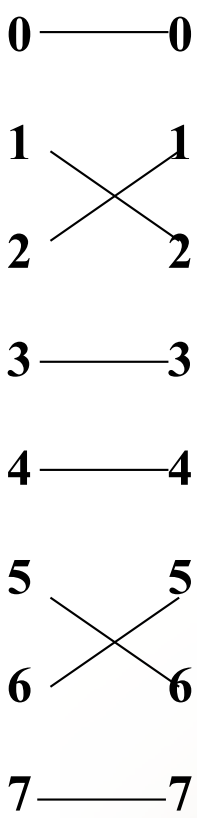
Superbutterfly Permutation

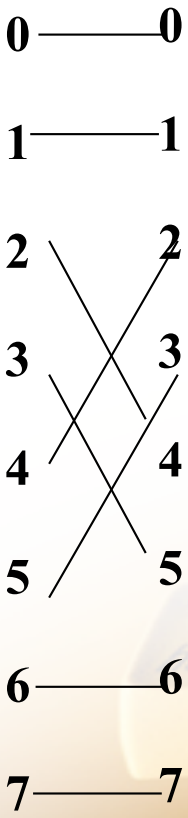
$$\beta^{(k)}\ (X_{n-1}X_{n-2}\ \cdots X_{n-k}X_{n-k-1}\cdots X_1X_0)$$

$$= X_{\ n-k-1}X_{n-2}\cdots X_{n-k}X_{n-1}X_{n-k-2}\ \cdots X_1\ X_0$$

Chapter5 Parallel Processor and Multiprocessor



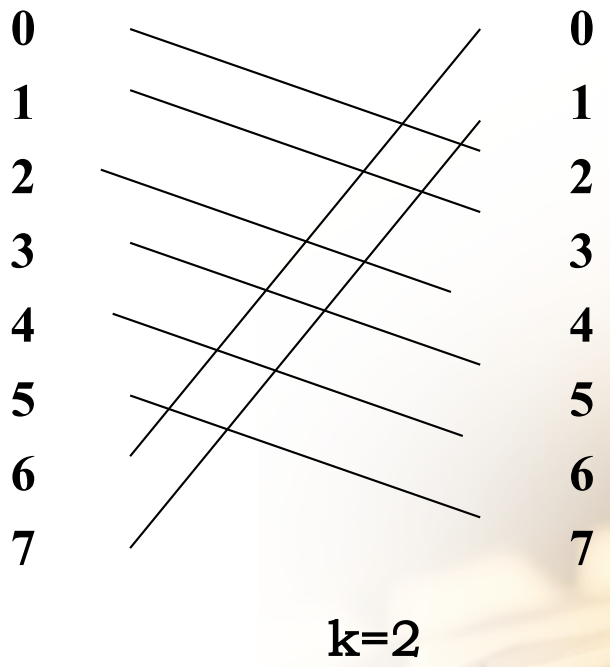




Chapter5 Parallel Processor and Multiprocessor

Shift Permutation

$$a(X)=(X+k) \bmod N, \quad 0 \le X \le N$$



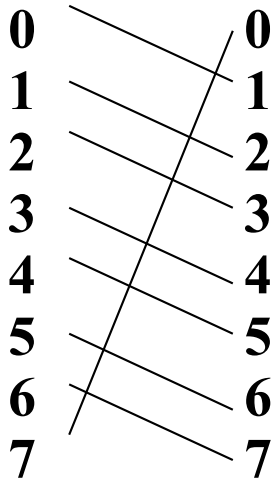
Chapter5 Parallel Processor and Multiprocessor

Plus-Minus 2^i Permutation

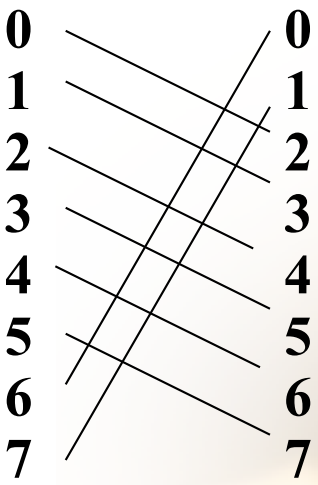
$$PM2_{+i}(j) = j + 2^i \pmod N$$

$$PM2_{-i}(j) = j - 2^i \pmod N$$

$(0 \leqslant j \leqslant N-1,\ 0 \leqslant i \leqslant n-1,\ n=\log_2 N)$



(a)i=0

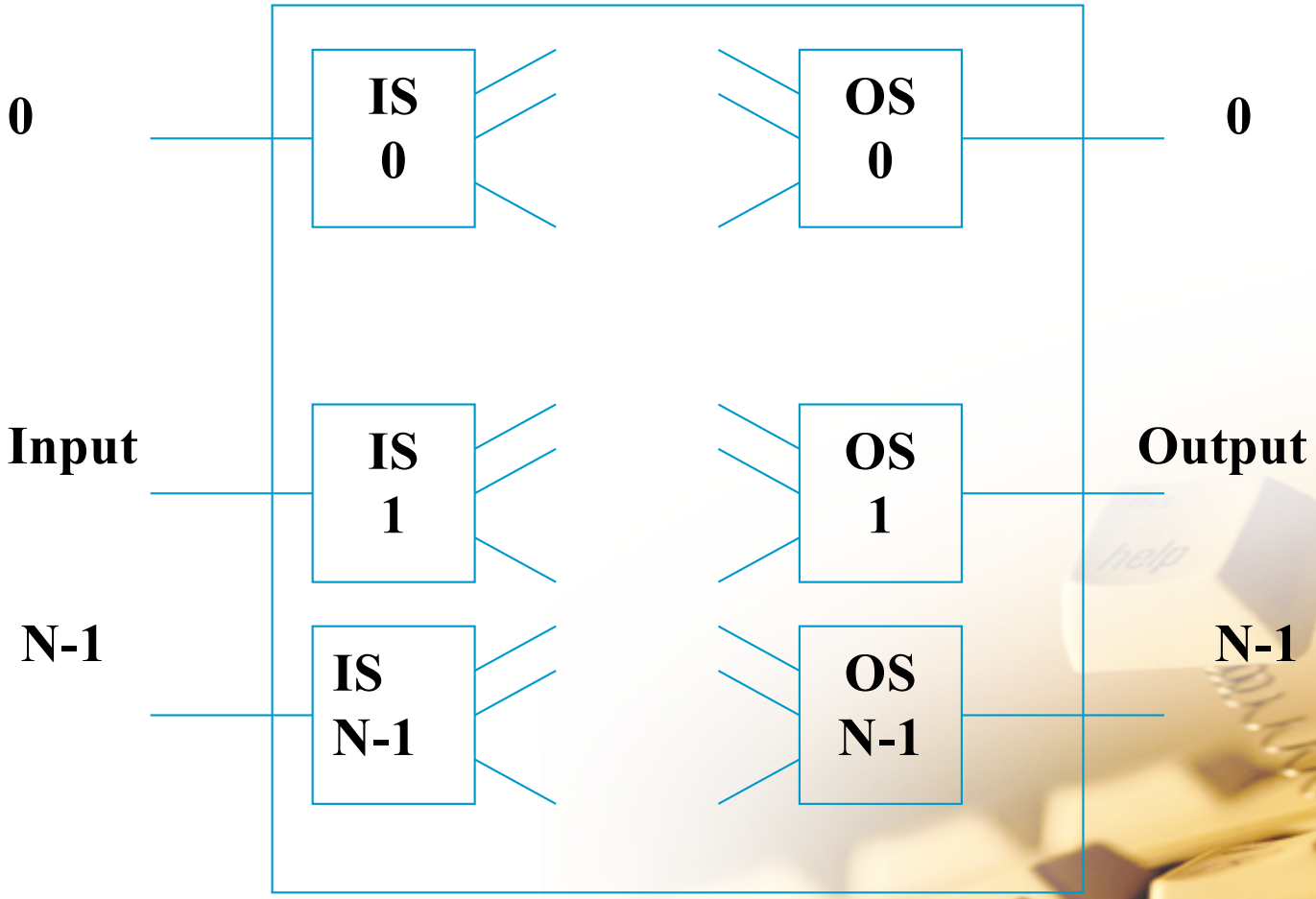


(b) i=+1

(c) i=+2

Chapter5 Parallel Processor and Multiprocessor

Interconnect Network Structure



Single-level Interconnect Network

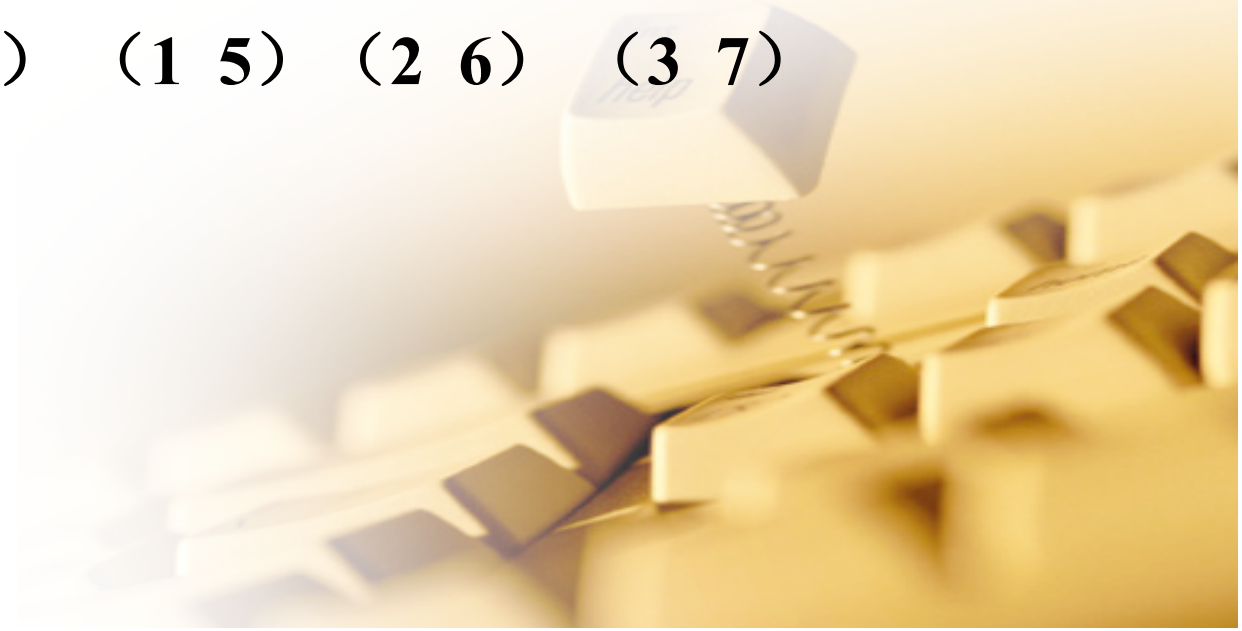
Chapter5 Parallel Processor and Multiprocessor

- **Three kinds of Single-level Interconnect Network (Assume N=8)**
  - **The Cube Network**

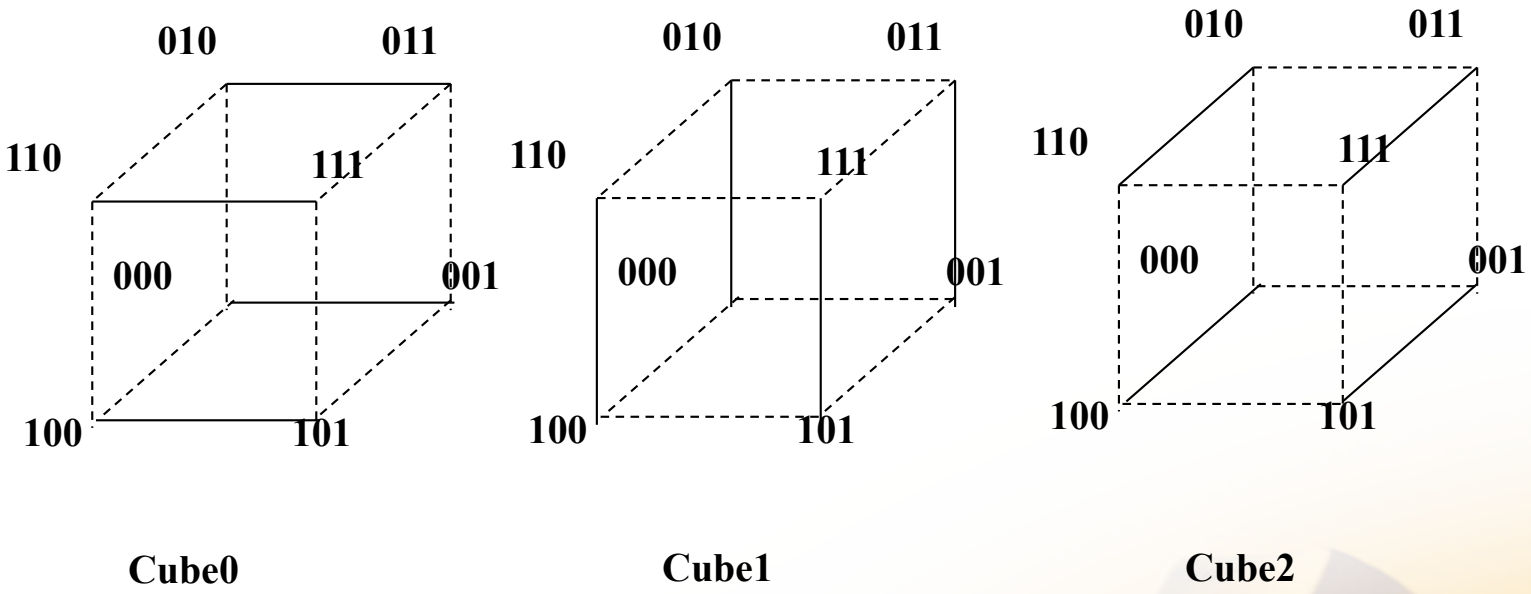
Cube0：（0 1）（2 3）（4 5）（6 7）

Cube1：（0 2）（1 3）（4 6）（5 7）

Cube2：（0 4）（1 5）（2 6）（3 7）



Chapter5 Parallel Processor and Multiprocessor



Chapter5 Parallel Processor and Multiprocessor

- **The PM2I Network**

$PM2_{+0}$: （0 1 2 3 4 5 6 7）

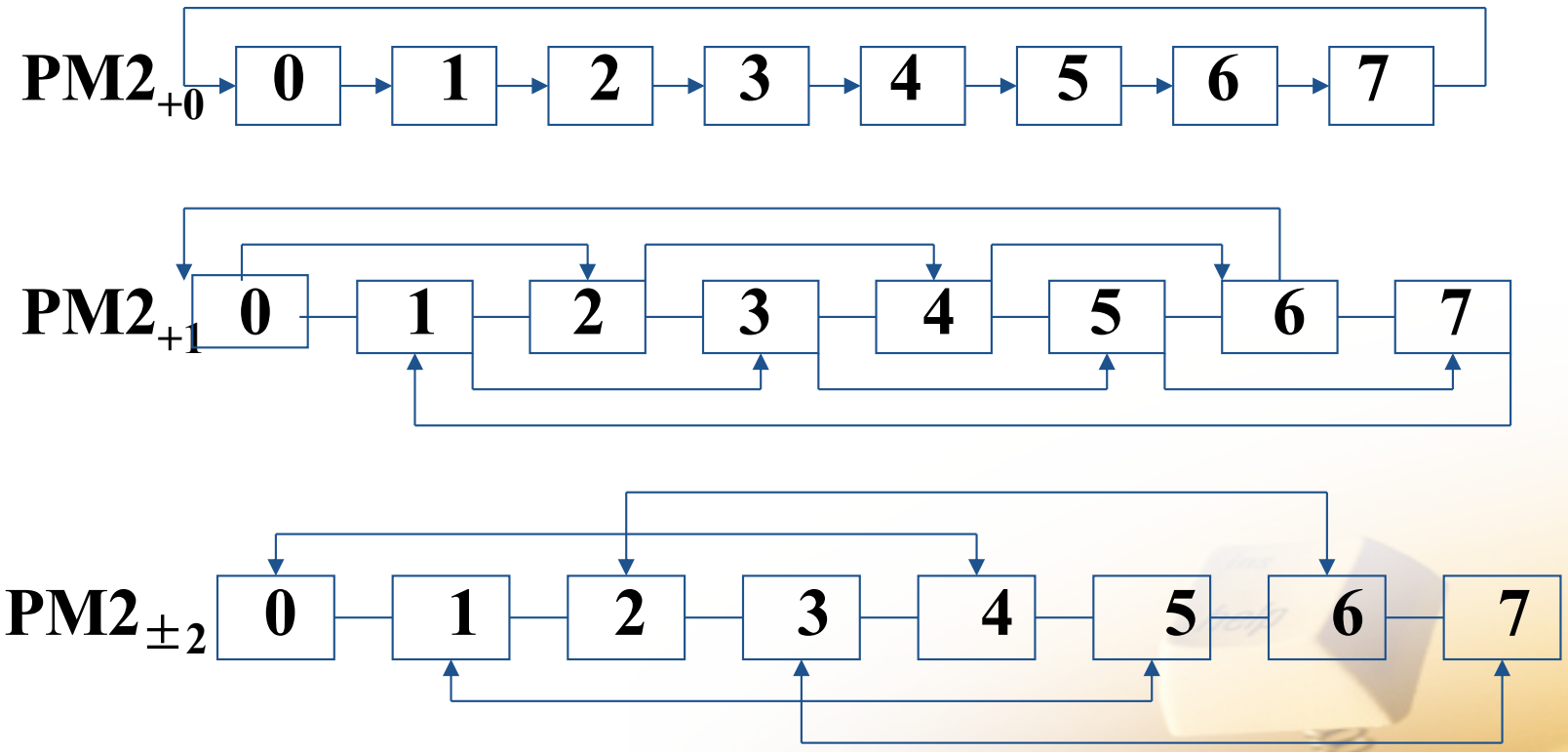
$PM2_{-0}$: （7 6 5 4 3 2 1 0）

$PM2_{+1}$: （0 2 4 6）（1 3 5 7）

$PM2_{-1}$: （6 4 2 0）（7 5 3 1）

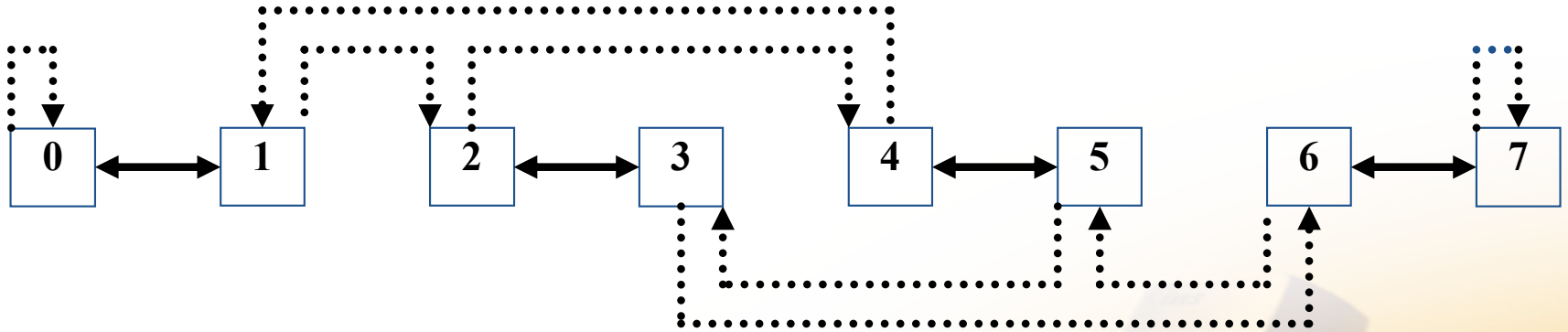
$PM2_{\pm 2}$: （0 4）（1 5）（2 6）（3 7）

Chapter5 Parallel Processor and Multiprocessor



Chapter5 Parallel Processor and Multiprocessor

- **The Perfect Shuffle and Exchange Network**



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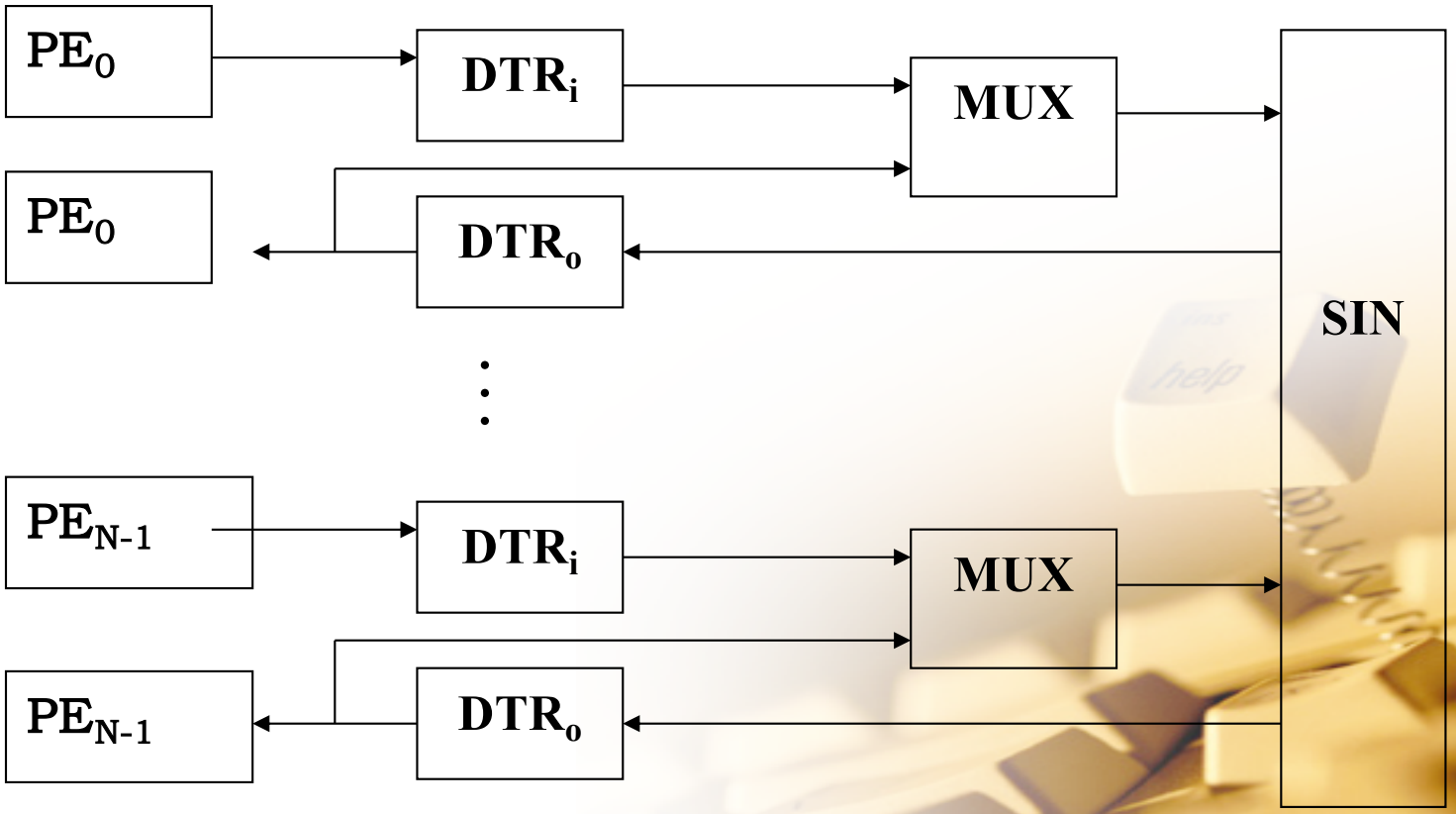
Cyclic Interconnect Network



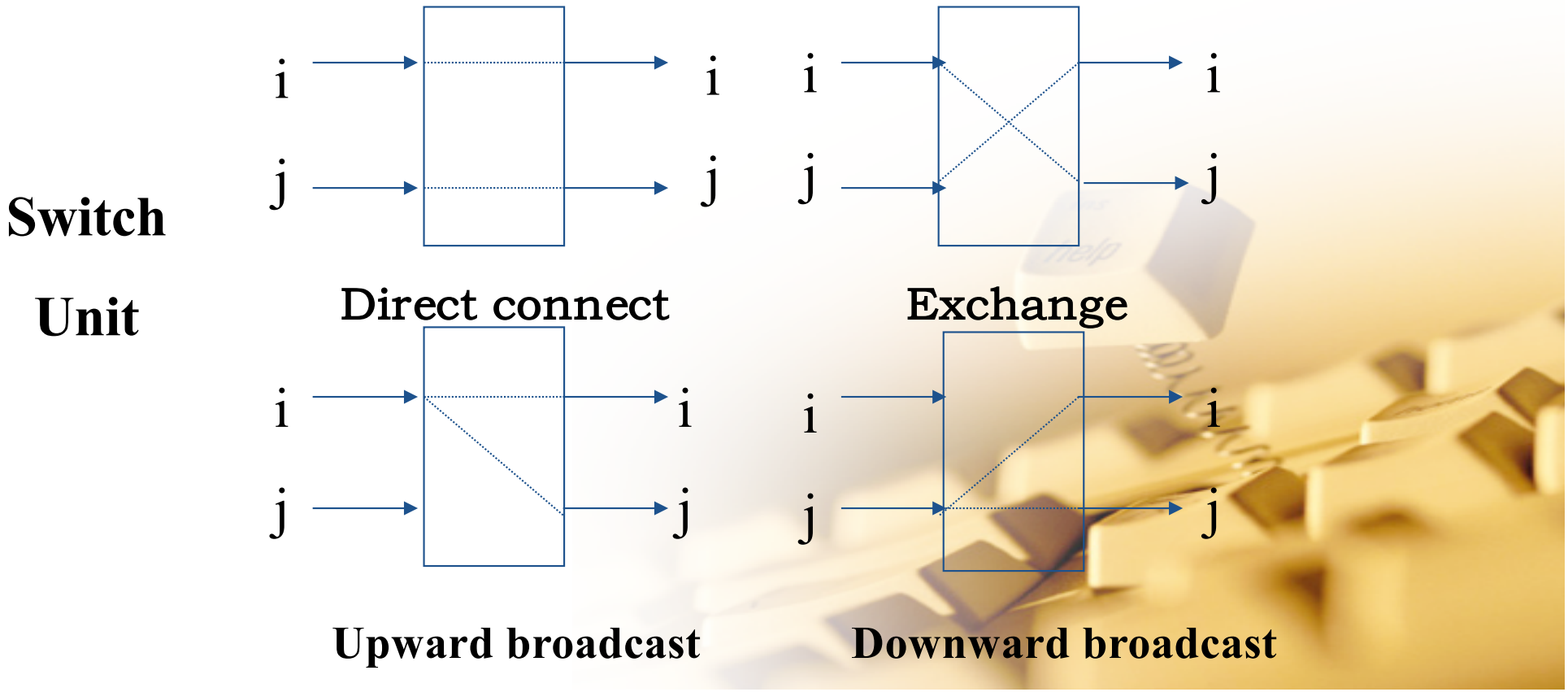
Chapter5 Parallel Processor and Multiprocessor

Multiple-level Interconnect Network

Multiple-level Cube Interconnect Network

Multiple-level Perfect Shuffle and Exchange Interconnect Network

Multiple-level PM2I Interconnect Network



Chapter5 Parallel Processor and Multiprocessor

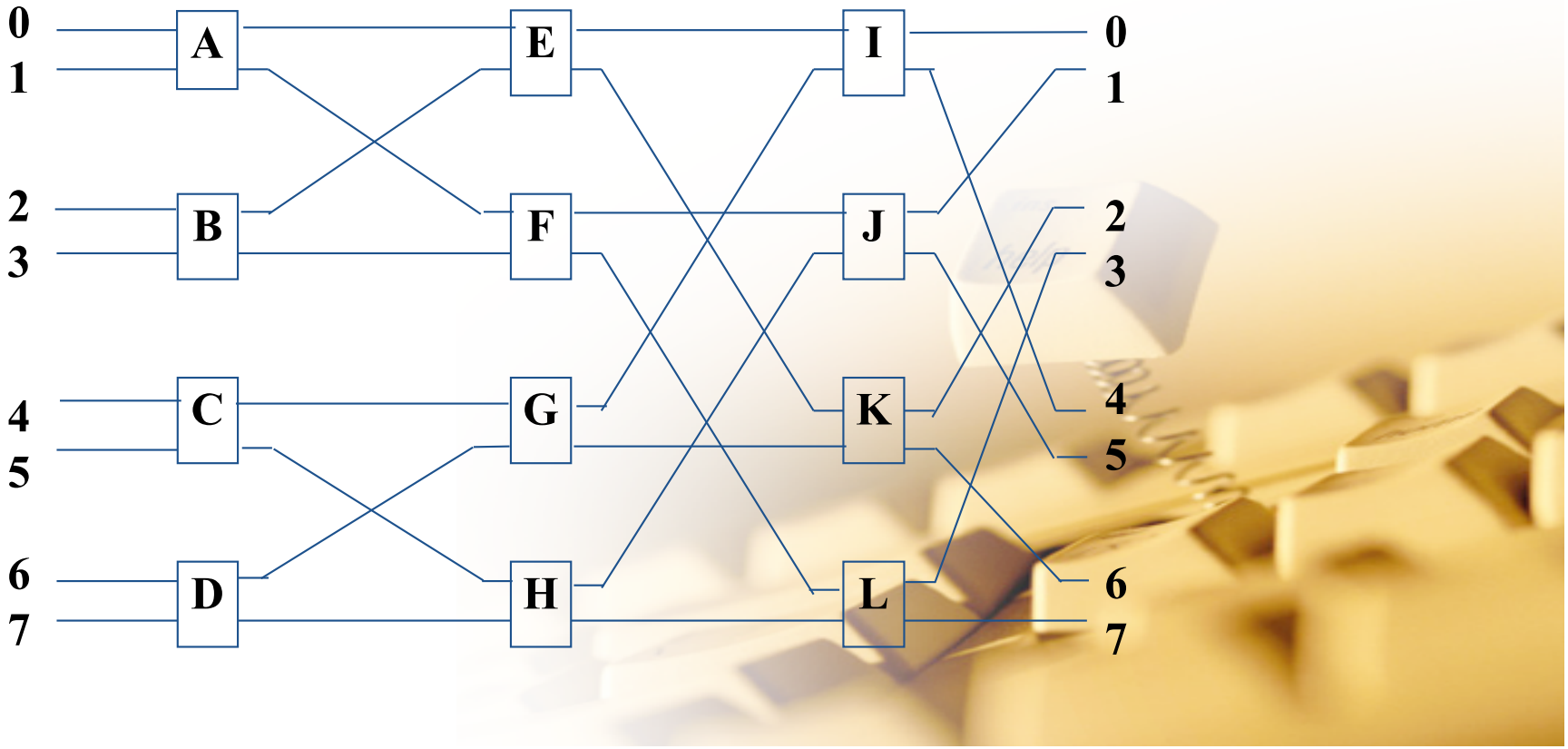
Switch Control Mode

- ✓**Level Control Mode**
- ✓**Unit Control Mode**
- ✓**Partial Level Control Mode: i Level -------i+1 Control Signals**

Chapter5 Parallel Processor and Multiprocessor

Multiple-level Cube Interconnect Network

i Level : If the control signal is '1', then the switch is in the exchange state and realize the cube $_i$ interconnect function; otherwise the switch is in the direct connect state.



Chapter5 Parallel Processor and Multiprocessor

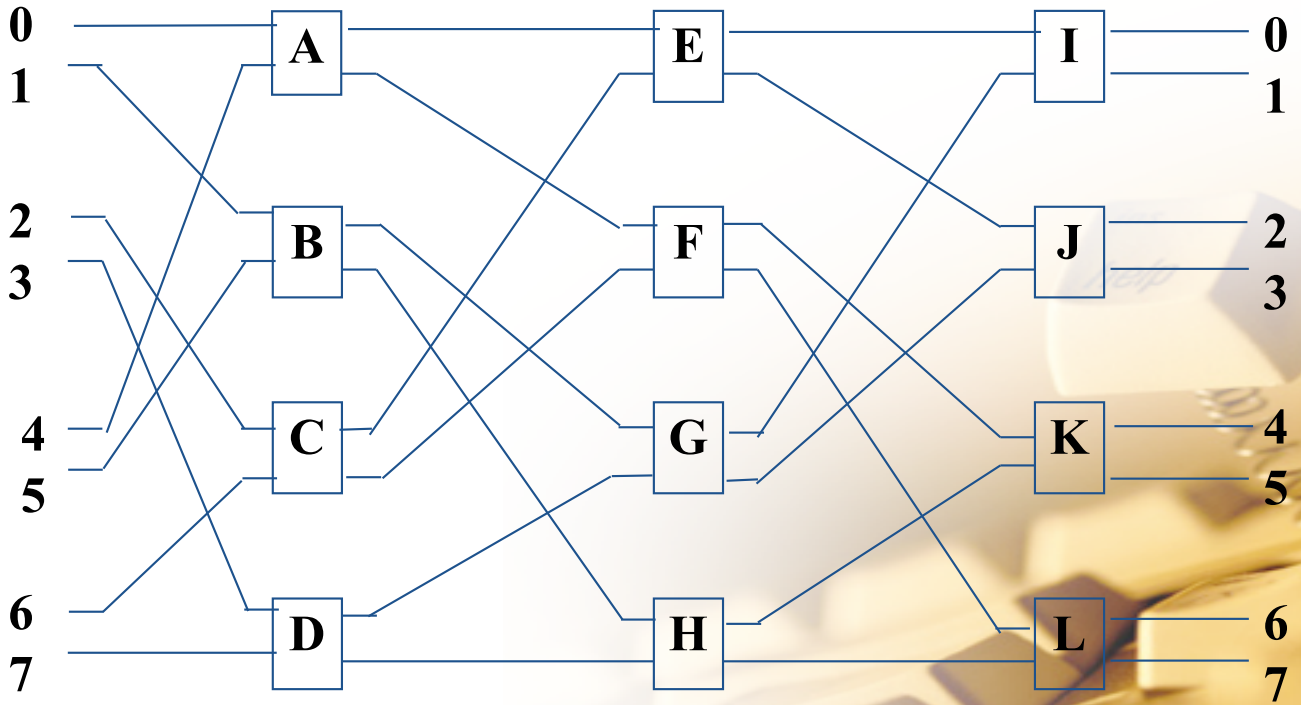
Three-Level STARAN Network

	Level Control Signal							
	000	001	010	011	100	101	110	111
0	0	1	2	3	4	5	6	7
1	1	0	3	2	5	4	7	6
2	2	3	0	1	6	7	4	5
3	3	2	1	0	7	6	5	4
4	4	5	6	7	0	1	2	3
5	5	4	7	6	1	0	3	2
6	6	7	4	5	2	3	0	1
7	7	6	5	4	3	2	1	0

Chapter5 Parallel Processor and Multiprocessor

Multiple-level Perfect Shuffle and Exchange Interconnect Network

Also named as Omega network, consists of the n-level same network, each level contains a perfect shuffle and then a list of 2^{n-1} four function switch unit, using unit control mode.



Chapter5 Parallel Processor and Multiprocessor

Four Characteristics of Interconnect Network

1. Communication Mode

   Synchronous and Asynchronous

2. Control Strategy

   Centralized and Decentralized

3. Switching Mode

   Circuit switching and packet switching

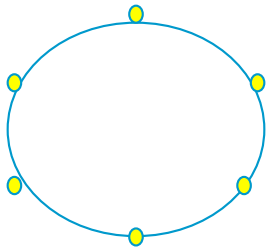
4. Network topology

   Static and Dynamic

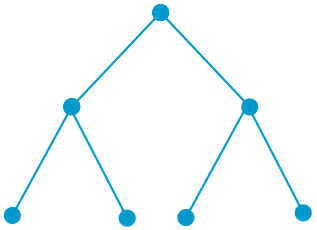
Chapter5 Parallel Processor and Multiprocessor

Static Interconnect Network Topology

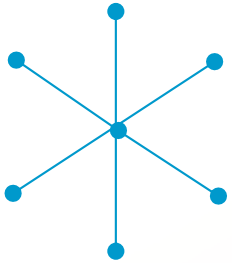
One-dimensional



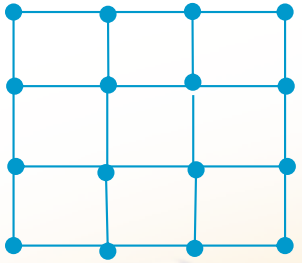
Ring



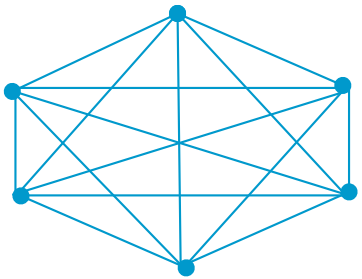
Tree



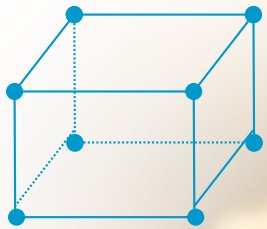
Star



Grid



Fully Meshed Network



Cube

Chapter5 Parallel Processor and Multiprocessor

Topology	Connections	Max Connectivity	Network Diameter
One-dimensional	N－1	2	N－1
Ring	N	2	N/2
Grid （N*N)	2N（N－1）	4	2（N－1）
Star	N-1	N-1	2
Cube （N＝2^K）	kN/2	Log_2N	Log_2N
FMN	N（N－1）/2	N－1	1
Tree	N－1	3	$2[Log_2(N+1)-1]$

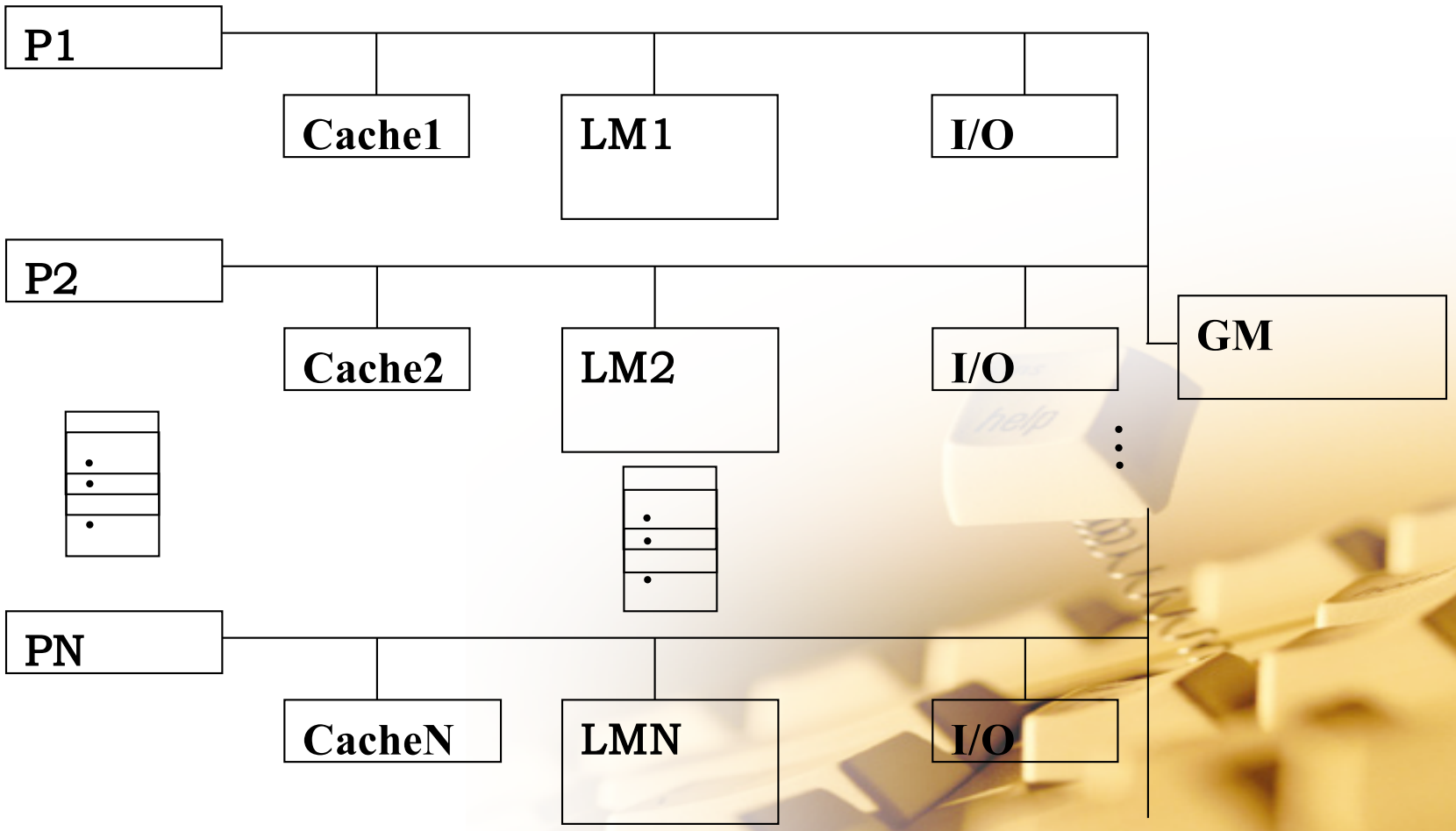
Chapter5 Parallel Processor and Multiprocessor

Dynamic Interconnect Network Topology

1. Bus-Structured Network
2. Crossbar Network
3. Multi-Port Memory Network
4. Multi-Level Dynamic Network

Chapter5 Parallel Processor and Multiprocessor

Bus-Structured Network



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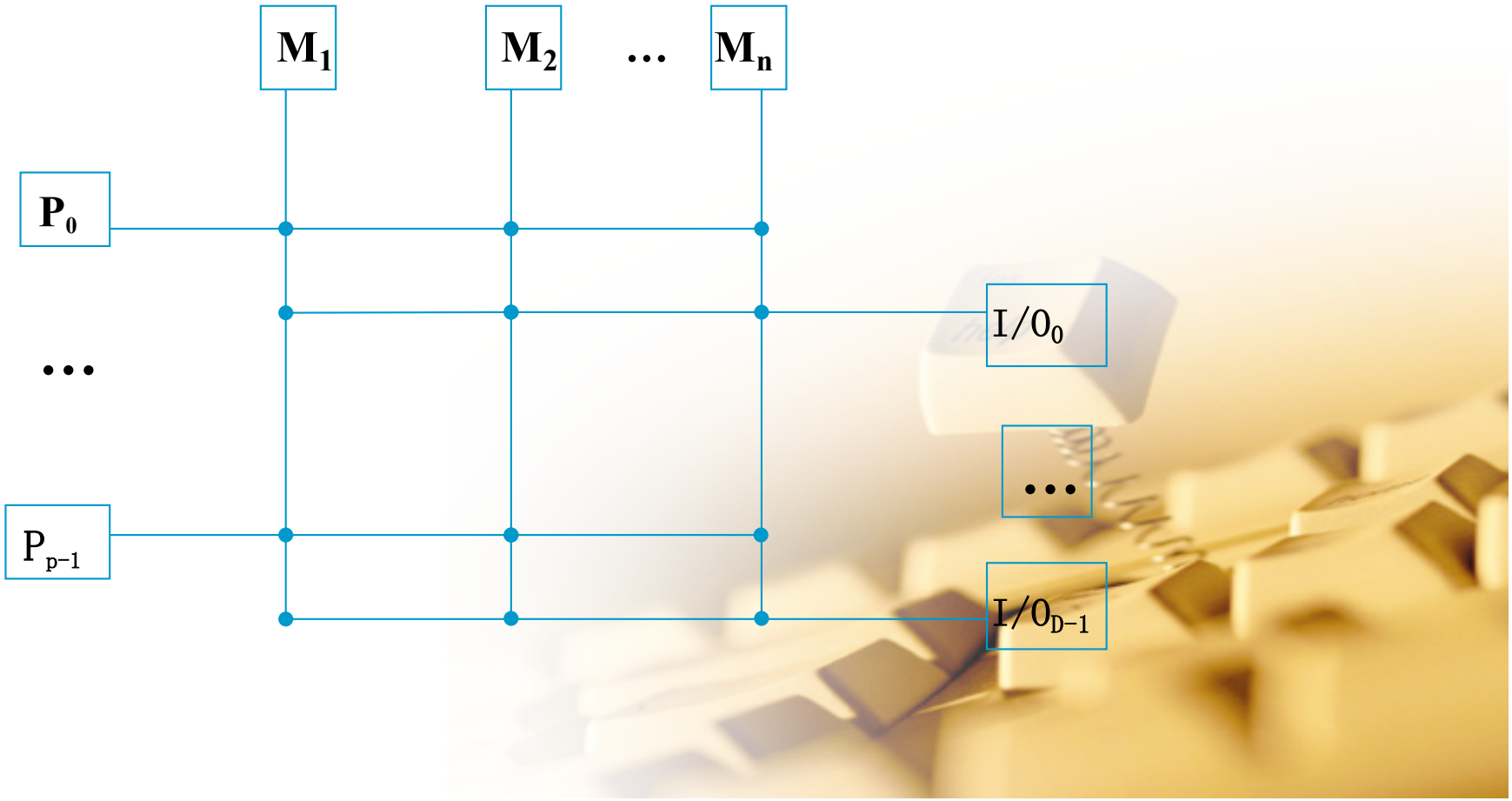
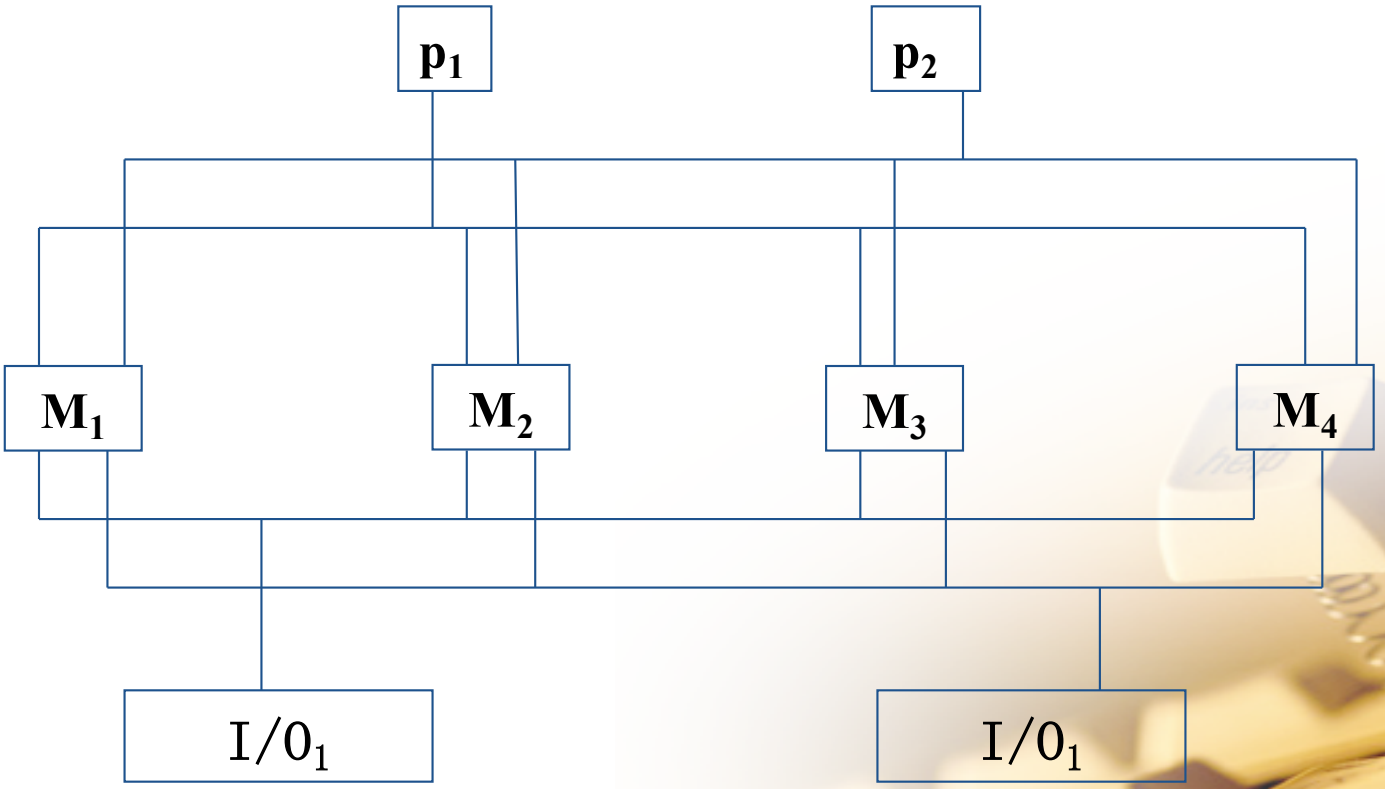
Crossbar Network



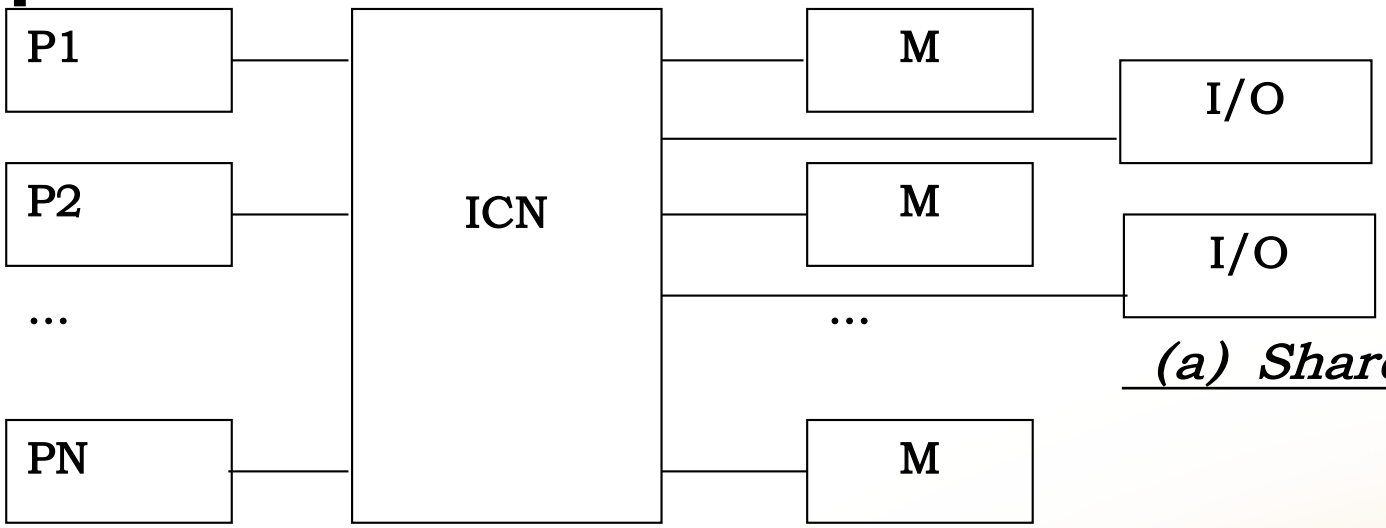
Chapter5 Parallel Processor and Multiprocessor

Multi-Port Memory Network

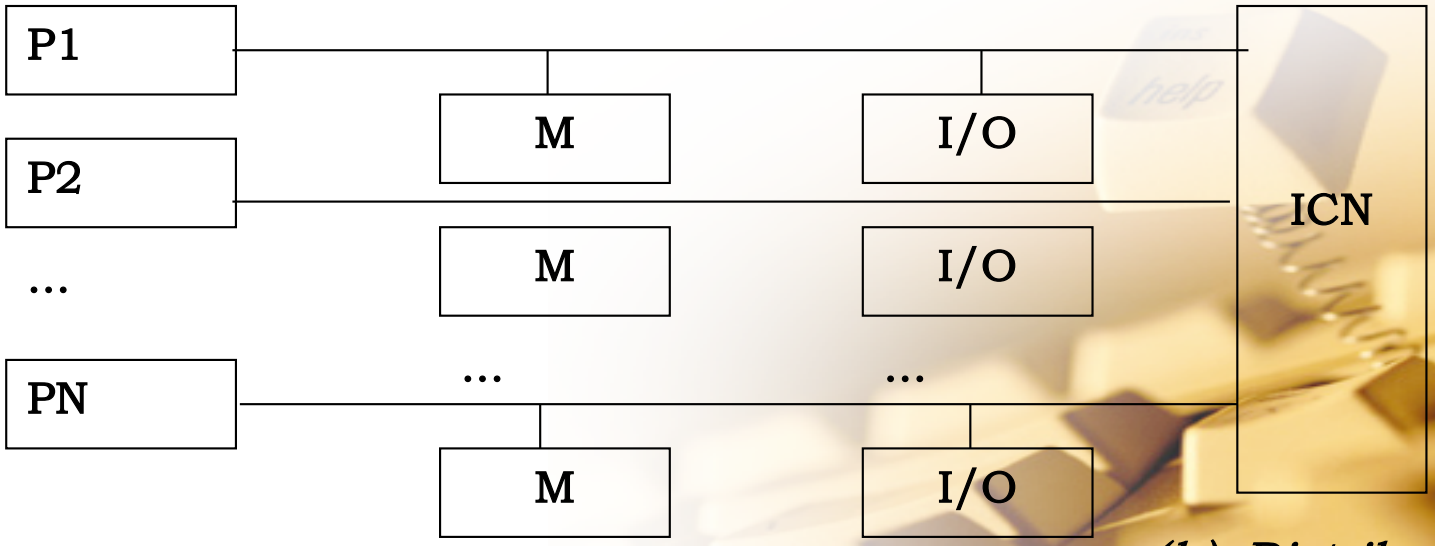


Chapter5 Parallel Processor and Multiprocessor

Multiprocessor Hardware Structure



(a) Shared Memory



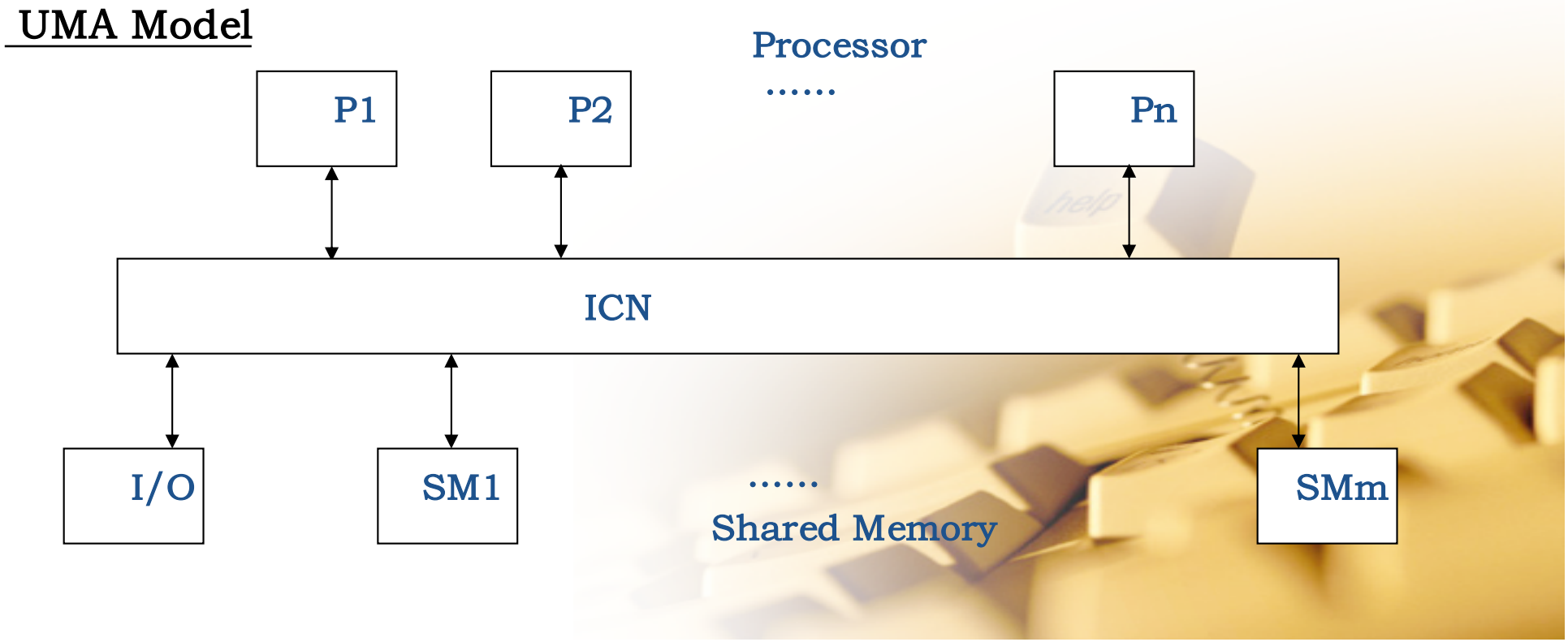
(b) Distributed Memory

Chapter5 Parallel Processor and Multiprocessor

(1) Shared Memory Structure (Tightly Coupled System)

Memory Access Model

1) Uniform-Memory-Access----------UMA
2) Non-uniform-Memory-Access---------- NUMA
3) Cache-Only-Memory Architecture---- COMA



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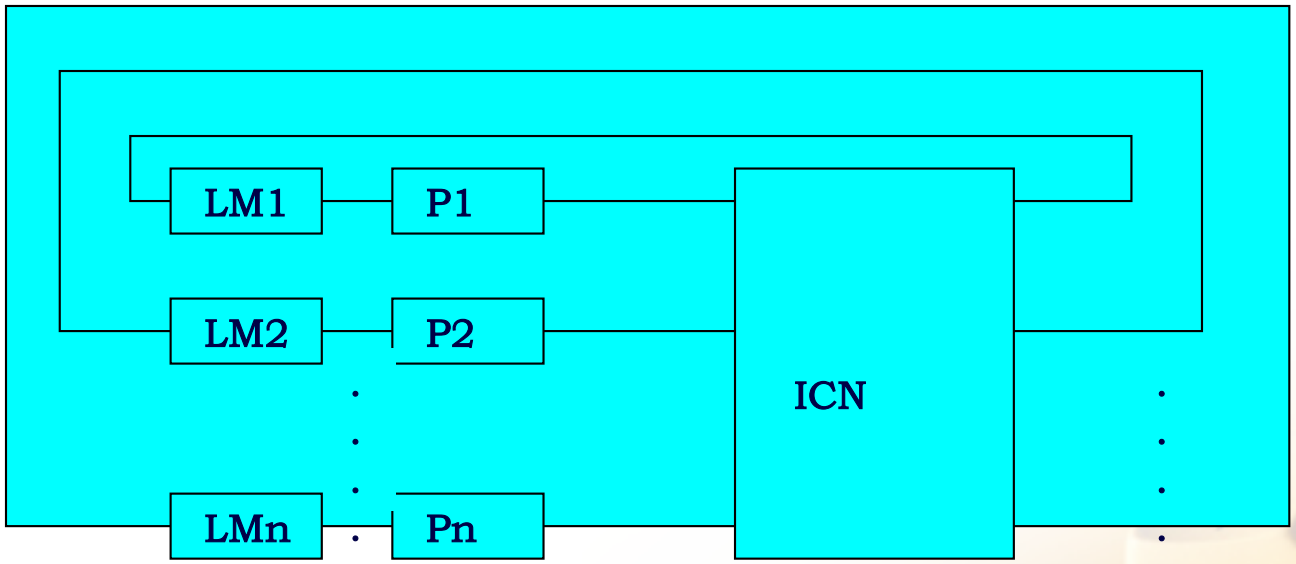
NUMA Model



(a) NUMA--LM
(Ex: BBN Butterfly)

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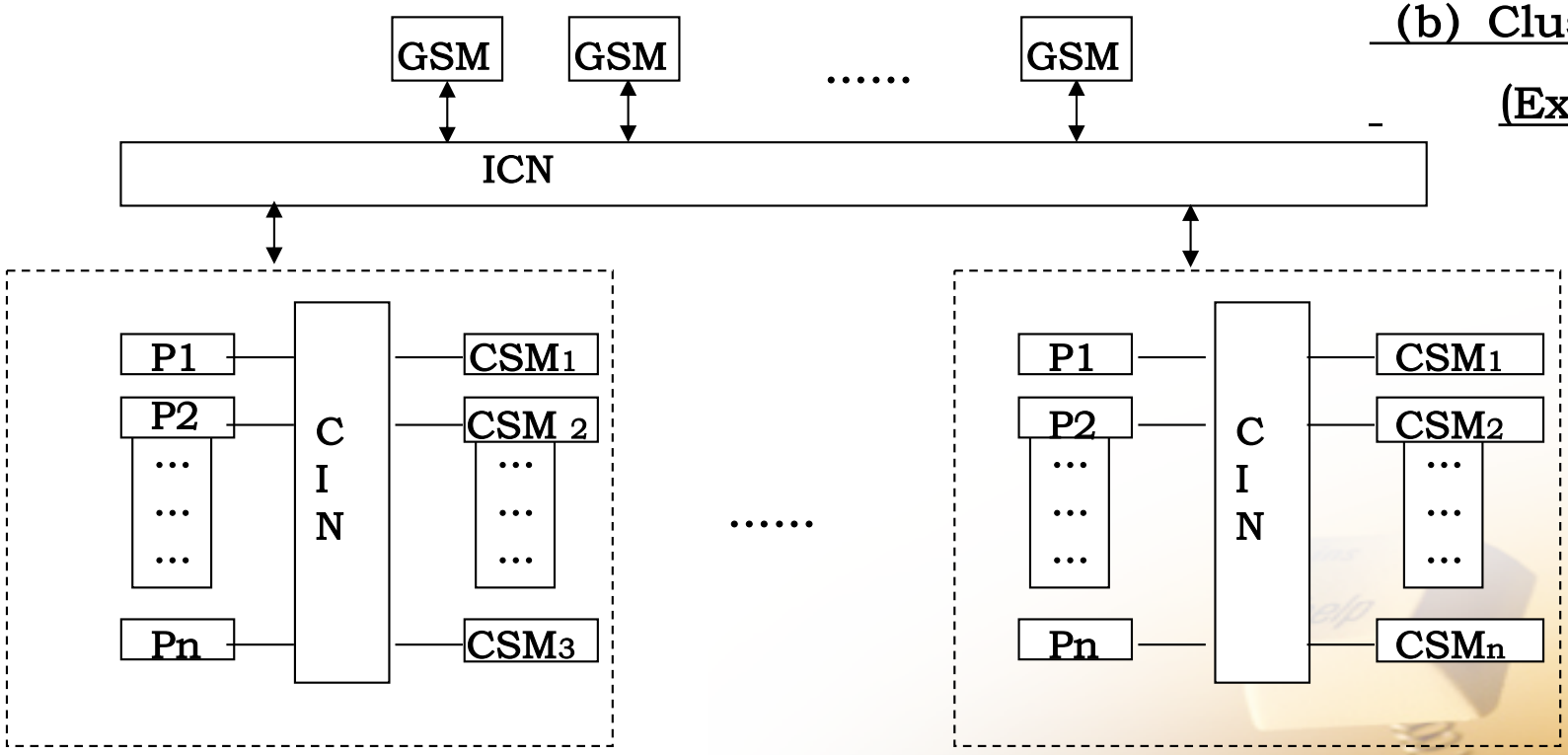
(b) Cluster Model

(Example: Cedar)



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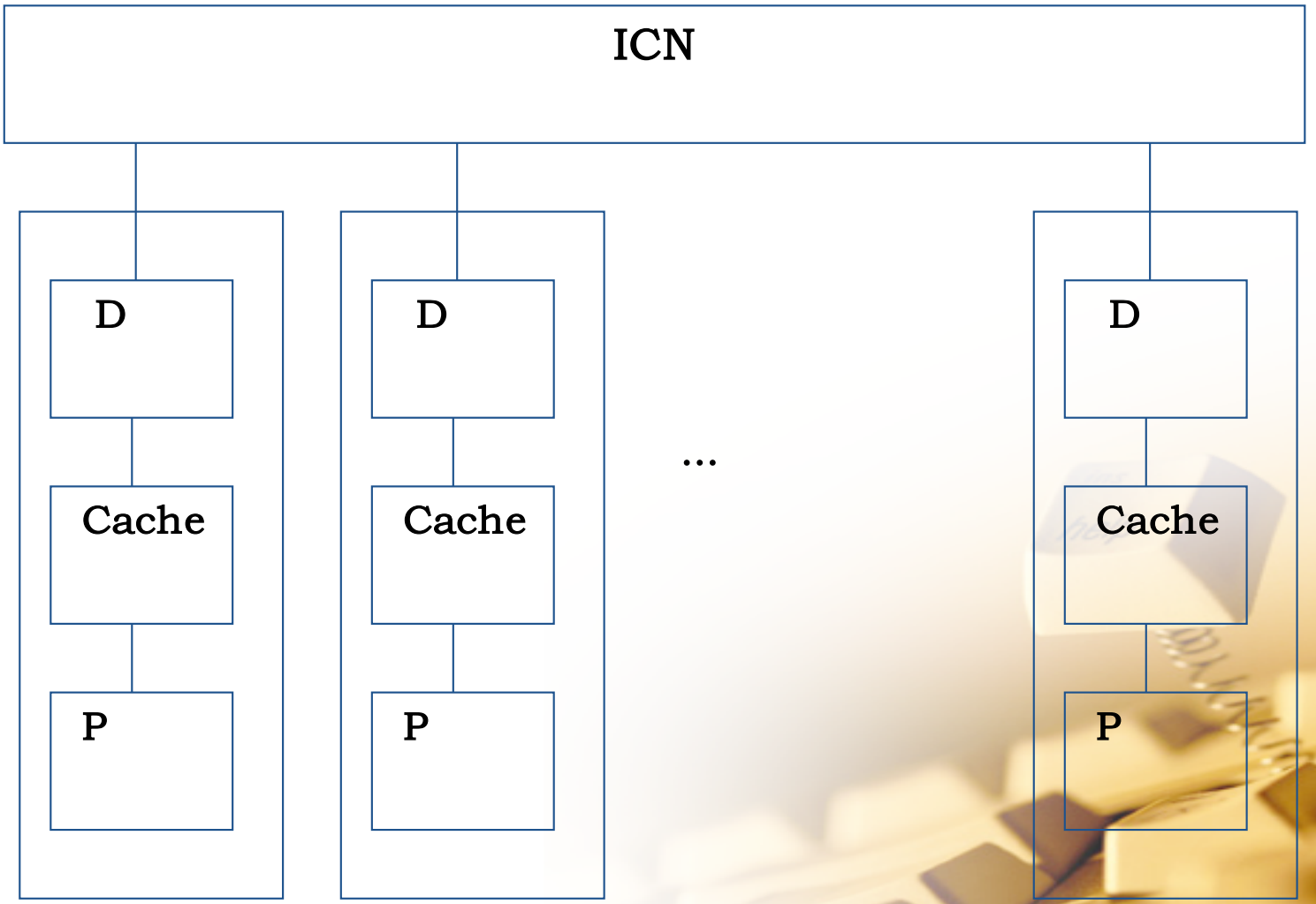
COMA Model



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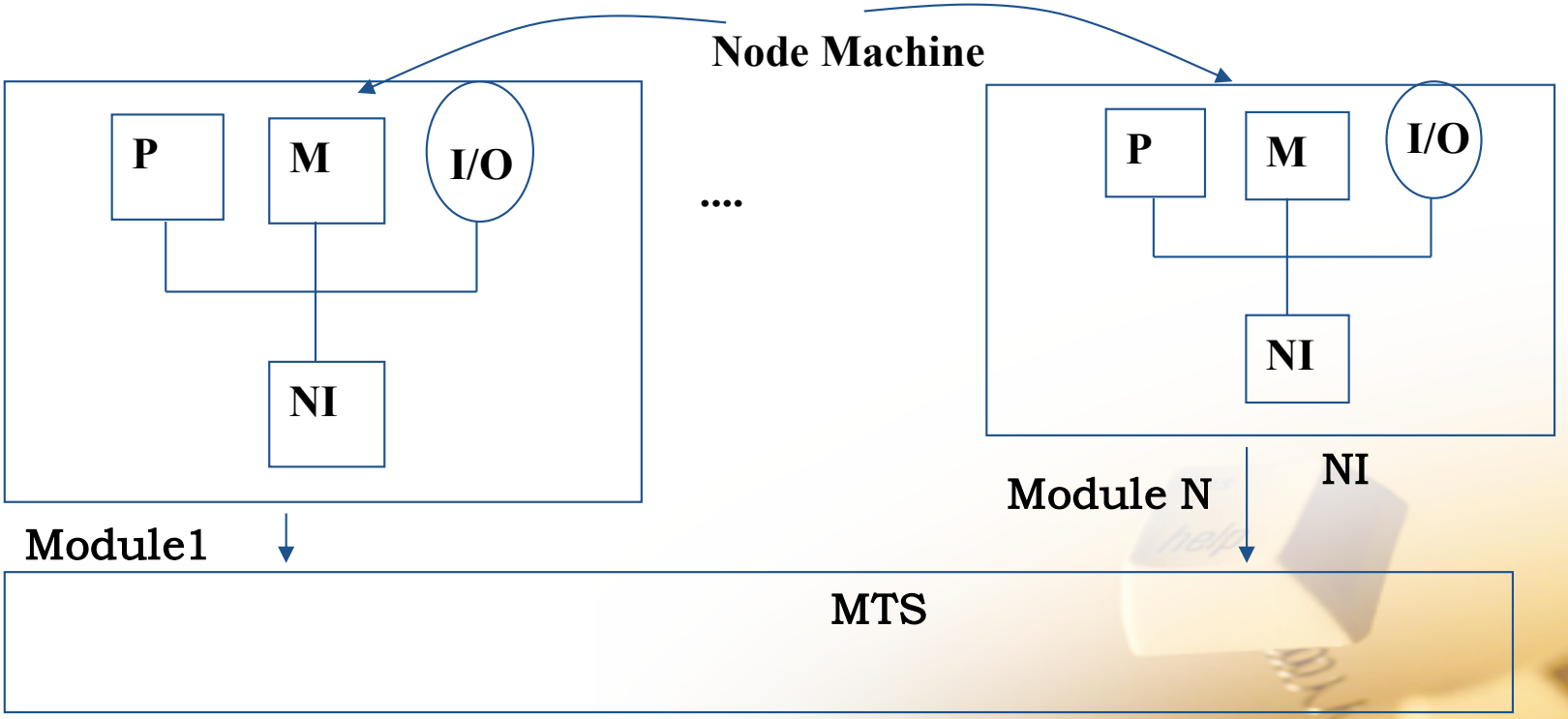
(2) Distributed Memory Structure (Loosely Coupled System)



Chapter5 Parallel Processor and Multiprocessor

Multiprocessor Cache Consistency

Three Factors to make cache contents inconsistent:

(1) Writable Data Sharing

(2) Input/Output Activity

(3) Process Migration

Chapter5 Parallel Processor and Multiprocessor

The ways to solve multiprocessor cache consistency

(1) Hardware Method

a) Snoopy Cache Protocol

- Write-Invalidate
- Write-Update

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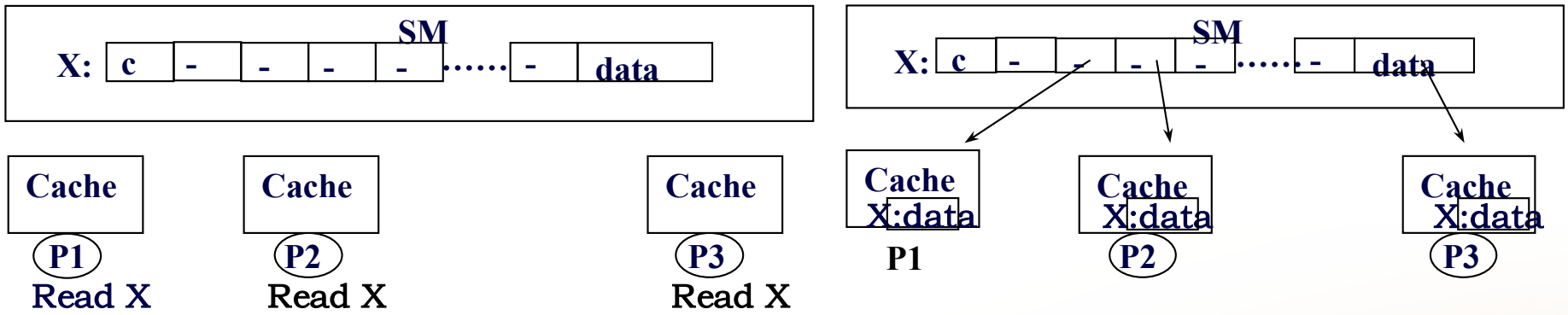
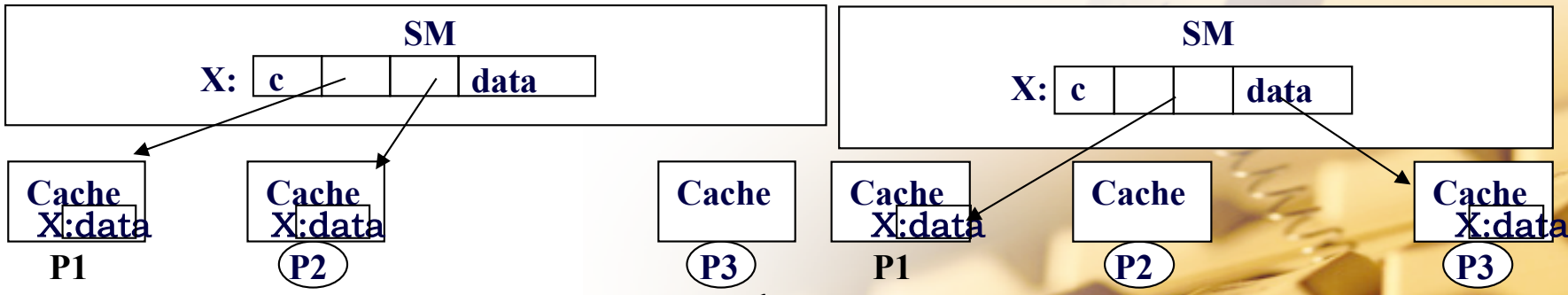
b) Directory Scheme



(a) Whole Directory



(b) Limited Directory

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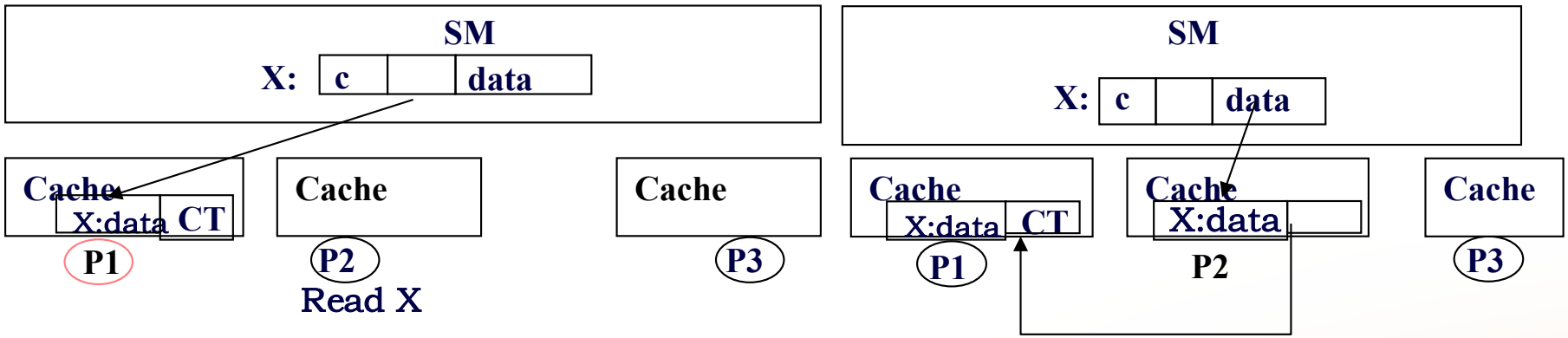

(c) Link Directory

Chapter5 Parallel Processor and Multiprocessor

(2) Software Method

- **Use software to limit some common writable data to store in the cache.**
- **Through the analysis of the compiler, we can divide the data into the cacheable data and non-cacheable data.**

Chapter5 Parallel Processor and Multiprocessor

Multiprocessor Operating System

- ✓Input / Output Load Balancing
- ✓Processor Load Balancing
- ✓System Recombination

OS Classification

- ➢Master-Slave Configuration
- ➢Separate Supervisor
- ➢Floating Supervisor