Project Implement 1-cycle MIPS Processor Using Verilog HDL

1. Design Description

(1) MIPS-Lite ISA：addu，subu，ori，lui，lw，sw，beq，j

(2) 1-Cycle MIPS Processor

2. Design Requirement

(1) The whole system should include Controller, IFU, GPR, ALU, DM, EXT, MUX, shown as Figure1.
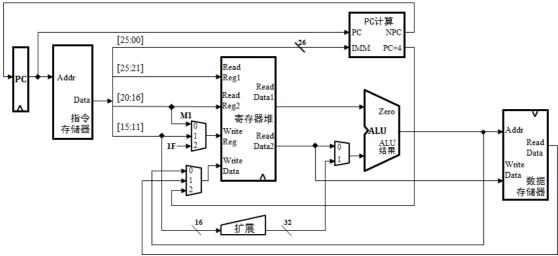
(2) Only clk and reset signal let the system work.

Figure1Top Design
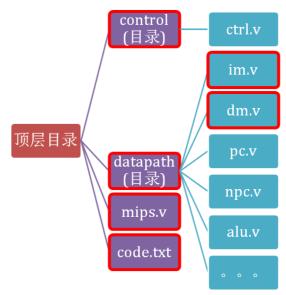
(3) The design structure should be similar as Figure2.

Figure2 Design Structure

3. Functional Component Requirement

(1) IFU

1）PC：Data width is 30bits and PC can be reset. The initial value is 0x0000_0c00.

2）IM：The storage capacity is 1024×32bit.

(2) GPR

(3) ALU

(4) EXT：Can implement zero extension and sign extension.

(5) DM：The storage capacity is also 1024×32bit.

4. Test Requirement

(1) All instructions should be tested.

(2) The test program including 1~20 instructions need to be composed and loaded into IFU. The following is the IM initialization method.

```
reg [31:0] my_memory[1023:0];

initial
    $readmemh( "code.txt", my_memory );
```