Roll No									

NATIONAL INSTITUTE OF TECHNOLOGY GOA

Farmagudi, Ponda, Goa, 403401

Programme Name: B.Tech

Online End Semester Examinations, December-2021

Course Name: Computer Organization and Architecture — Course Code:CS202

Date:08/12/2021 — Time: 09:30 AM-12:30 PM

Duration: 3 Hours — Max. Marks: 100

ANSWER ALL QUESTIONS

1. Using single-precision floating point representation
   a. Add 2.5 and 0.75
   b. Multiply 0.25 by 1.5

   (5+5=10 marks)

2.
   a. Multiply -11 (multiplicand) by 27 (multiplier) using bit pair recoding of multiplier method
   b. Do you agree with the statement "Booth recoding of multiplier method improves the speed of multiplication operation". Justify your answer.

   (6+4=10 marks)

3. Divide 359 (dividend) with 13 (divisor) using non restoring division algorithm.

   (10 marks)

4.
   a. With a neat diagram show the internal structure of a 16x4 bit SRAM chip that uses 2-dimensional address decoding
   b. Compare static RAM with dynamic RAM

   (7+3=10 marks)

5. A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses:
   200, 204, 208, 20C, 2F0, 2F4, 200, 204, 218, 24C,21C, 2F4
   This pattern is repeated two times.
   a. Show the contents of the cache at the end of each reference if a direct-mapped cache is used. Compute the hit rate for this example. Assume that the cache is initially empty.
   b. Repeat part (a) for an associative-mapped cache that uses the LRU (least recently used) replacement algorithm.

   (5+5=10 marks)

6.
   a. What are the different categories of cache miss. Explain them briefly
   b. Explain the concept of virtual memory technique highlighting the difference between the logical and physical address. Also write about the address translation process

   (5+5=10 marks)

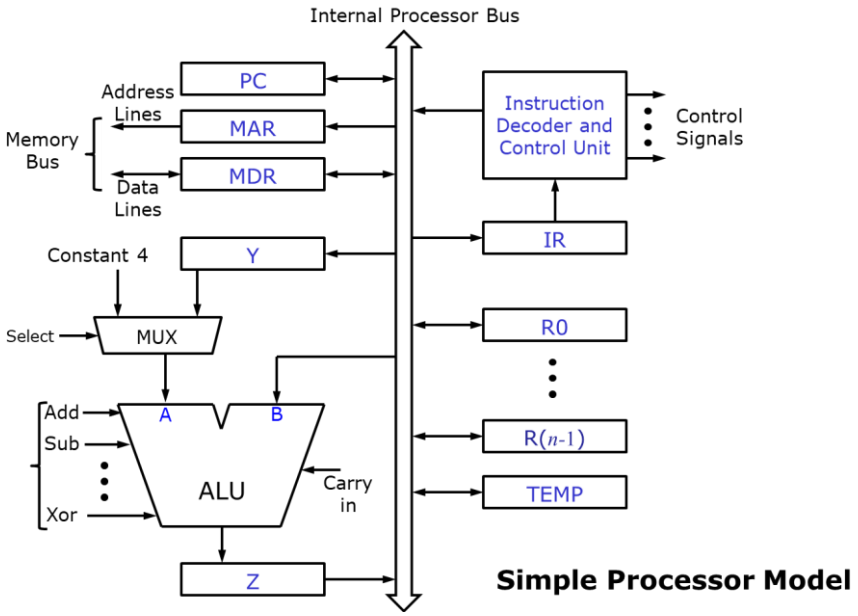
7.

a. What is an I/O interface? What is its role? Explain.
b. What are the approaches to achieve required synchronization between processor and an I/O device?

(4+6=10 marks)

8. Assume that a processor has single internal bus as shown in the Figure below. Give the control sequences for the following
   a. Instruction fetch
   b. Execution of **ADD R3, [R1], [R2]** that corresponds to adding the content of memory location pointed to by R2 to the content of memory location pointed to by R1 and storing the result of addition in R3
   c. Execution of **ADD R1, #NUM** that corresponds to adding the (immediate) number NUM to register R1.
   d. Execution of **JLT LoopBegin** that corresponds to conditional jump to LoopBegin

(10 marks)



Simple Processor Model

9. A hardwired CPU uses 10 control signals S1 to S10 in various time steps T1 to T5 to implement 4 instructions I1 to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1,S3,S5	S2,S4,S6	S1,S7	S10	S3,S8
I2	S1,S3,S5	S8,S9,S10	S5,S6,S7	S6	S10
I3	S1,S3,S5	S7,S8,S10	S2,S6,S9	S10	S1,S3
I4	S1,S3,S5	S2,S6,S7	S5,S10	S6,S9	S10

Derive an expression each to represent the circuit for generating control signals S1, S6, and S9.

(7.5 marks)

10. Draw a neat pipeline flow diagram for the following segment of code.

I1	LOAD R0, N
I2	LOAD R1, X
I3	LOAD R2, Y
I4	MUL R3, R1, R2
I5	ADD R4, R2, R3
I6	STORE Z, R4
I7	FADD F0, F1, F2
I8	FMUL F5, F6, F7

a. Assume that all steps involved in the execution of the instructions are single cycle operations. Mention the total number of clock cycles needed.

b. Assume that the program is running on a hardware that supports 5 stage pipeline (IF, ID, RD, EX, WB). The block containing instructions I1, I2 and I3 is not available in cache. Hence fetching (IF) step of I1 will take 3 cycles and I2 and I3 take 1 cycle. Similarly, the block containing I7 and I8 need to be mapped onto I-cache. Hence, fetching (IF) of I7 will take 2 cycles and I8 1 cycle. Assume that N, X and Z are the locations on L1 cache and Y is the location in main memory. The execution stage of LOAD in I1, I2 and STORE in I6 take 1 clock cycle and LOAD in I3 take 2 clock cycle. The execution stage of MUL and ADD instructions take 3 and 1 clock cycles respectively. The execution stage of FADD and FMUL to take 3 and 4 cycles respectively. Mention the total number of clock cycles needed.

(4+8.5=12.5 marks)

**************************ALL THE BEST*********************************