Basic Electrical Science Lab
Course Code: EE152

Laboratory Manual

Name: Sadat Zubin Aftab Shah

Roll No: 20CSE1030

Section: B

Academic Session: April – August 2021

National Institute of Technology Goa

CERTIFICATE

This is to certify that Mr./ Ms. _____ of Class B.Tech 1st year (2nd Sem), Division Sec A/B, bearing Roll. No._____, has satisfactorily completed the course experiments in the Laboratory Course Basic Electrical Science Lab (EE152) in the academic year 2020-2021 in the Institution of National Institute of Technology Goa.

Course Instructor

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Digital Combinational Logic gates

8. A. Introduction:

This session makes students to understand various digital combinational logic gates- AND, OR, NOT, NAND, NOR, XOR, XNOR - and to verify through the Simulation in MATLAB/Simulink.

8. B. Objectives:

a. Acquire a good knowledge on various digital combinational logic gates- AND, OR, NOT, NAND, NOR, XOR, XNOR.

b. Verification of the theoretical knowledge on these logic gates through simulation in MATLAB/Simulink Platform.

8. C. Theory: Refer to the notes or necessary materials mentioned in EE151 course.

8. D. Statement of Experiments:

Fig. 8.1 represents various logic gates (NOT, AND, NAND, OR, NOR, XOR, XNOR). The input for these gates are digital in nature, i.e., it is either '0' or '1', and the output is also in digital in nature. Based on the theoretical knowledge, a truth table for each gate has to be prepared and that table has to be verified through simulation in Matlab/Simulink.

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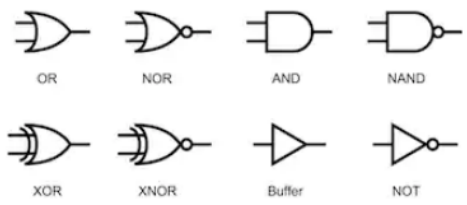


Fig. 8.1

8. E. Procedure:

Prepare the truth table for each logic gates asked in section-8.D theoretically and draw experimental circuit (necessary Measuring instruments are to be incorporated in the circuit) corresponding to the logic gates shown in Fig. 8.1. Construct the experimental circuits in Simulink domain, simulate it, and observe the output and validate corresponding truth table against each logic gates.

8. F. Assignments:

Part-1: Consider Fig. 8.2 and do the same as mentioned in Section - 8.D.

Part-2: Replace the gates shown in Fig. 8.2 by its inverted one and do the same as mentioned in Section - 8.D.

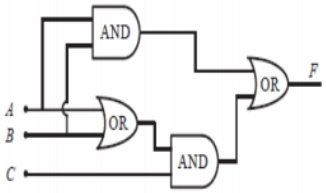


Fig. 8.2

Experiment 8

Digital Combinational Logic Gates

1. **Aim:** To verify the theoretical analysis of various digital combinational logic gates NOT, AND, NAND, OR, NOR, XOR, XNOR

2. **Simulink Blockset used:** Logical operator AND, OR, NOR, NAND, NOT, XOR, XNOR. Display, scope, Pulse generator.

3. **Theory:**

❖ Logic Gate:

A logic gate is a device that acts as a building block for digital circuits. They perform basic logical functions that are fundamental to digital circuits. Most electronic devices we use today will have some form of logic gates in them. For example, logic gates can be used in technologies such as smartphones, tablets or within memory devices.
There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

- AND Gate 

The output is "true" when both inputs are "true." Otherwise, the output is "false."

- OR Gate 

The output is "False" when both inputs are "false." Otherwise, the output is "true."

- NAND Gate 

The output is "false" if both inputs are "true." Otherwise, the output is "true."

- XOR Gate 

The output is "true" if inputs are different, and “false” when the inputs are same.

- NOT Gate 

If the input is "true", then the output is “false”. If the input is “false”, then the output is "true".

- XNOR Gate 

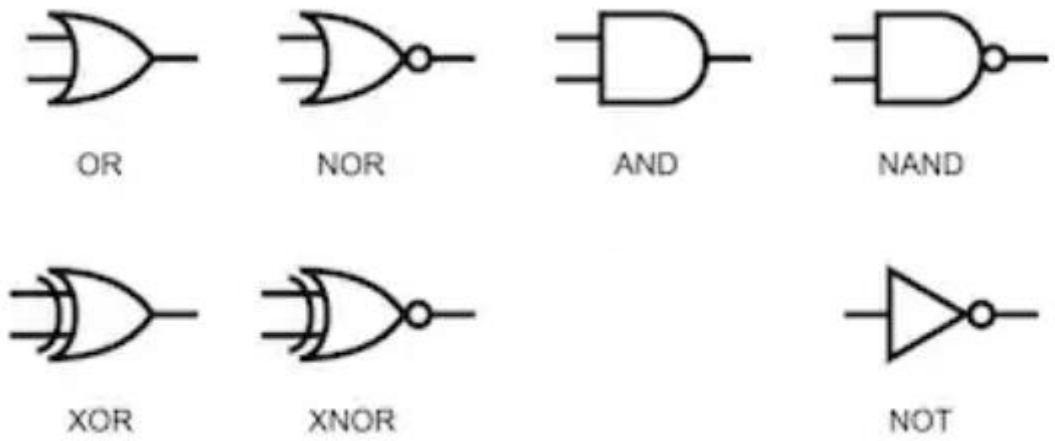
Its output is "true" if the inputs are the same, and "false" if the inputs are different.

- NOR Gate 

Its output is "true" if both inputs are "false." Otherwise, the output is "false."

4. **Statement of Experiments:**

Fig. 8.1 represents various logic gates (NOT, AND, NAND, OR, NOR, XOR, XNOR). The input for these gates are digital in nature, i.e., it is either '0' or '1', and the output is also in digital in nature. Based on the theoretical knowledge, a truth table for each gate has to be prepared and that table has to be verified through simulation in MATLAB/Simulink.



5. **Procedure:**

Prepare the truth table for each logic gates asked in Section-8.D theoretically and draw experimental circuit (necessary Measuring instruments are to be incorporated in the circuit) corresponding to the logic gates shown in Fig. 8.1. Construct the experimental circuits in Simulink domain, simulate it, and observe the output and validate corresponding truth table against each logic gates.

❖ Circuit Diagram:

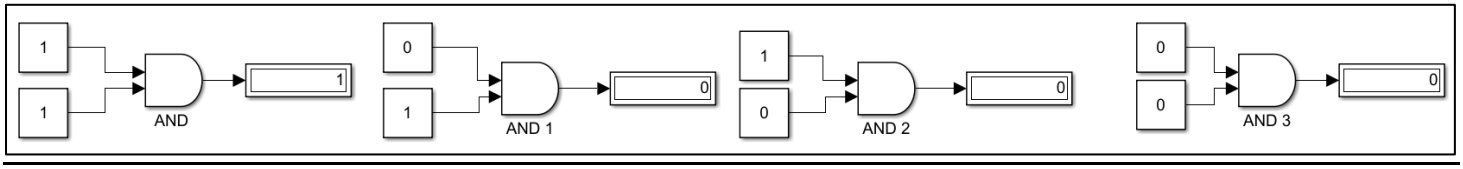


Fig8a: Input Output for AND gate

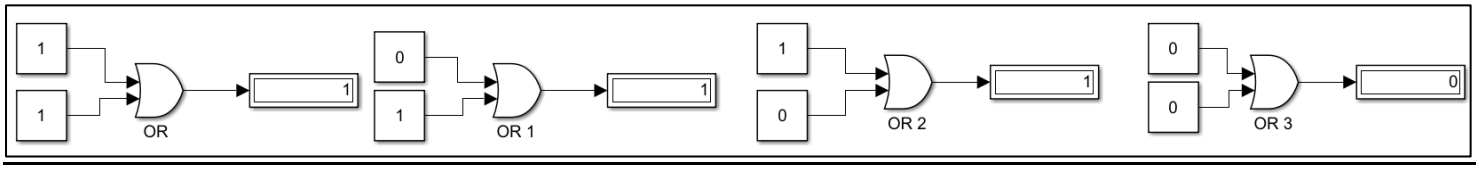


Fig8b: Input Output for OR gate

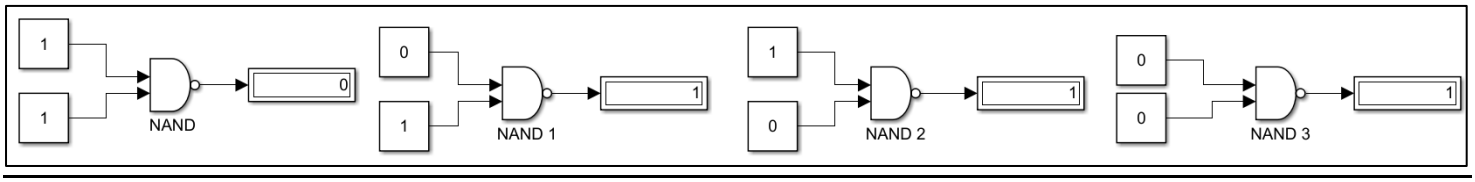


Fig8c: Input Output for NAND gate

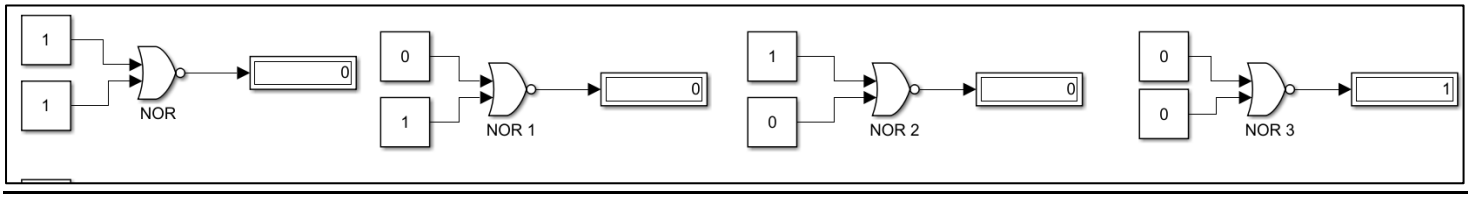


Fig8d: Input Output for NOR gate

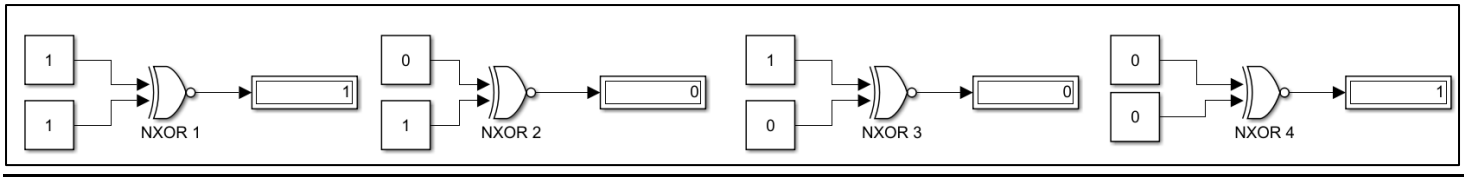


Fig8e: Input Output for XNOR gate

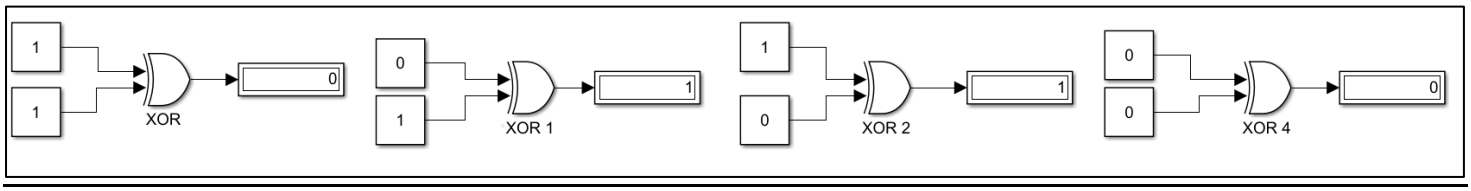


Fig8f: Input Output for XOR gate

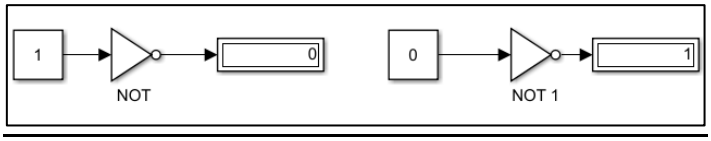


Fig8g: Input Output for NOT gate

Logic Gate	Input	Input	Output	
			Theoretical	Simulated
AND	1	1	1	1
	1	0	0	0
	0	1	0	0
	0	0	0	0

Table8a: Comparison between theoretical and simulated outputs of AND Gate

Logic Gate	Input	Input	Output	
			Theoretical	Simulated
OR	1	1	0	0
	1	0	1	1
	0	1	1	1
	0	0	1	1

Table8b: Comparison between theoretical and simulated outputs of OR Gate

Logic Gate	Input	Input	Output	
			Theoretical	Simulated
NAND	1	1	0	0
	1	0	1	1
	0	1	1	1
	0	0	1	1

Table8c: Comparison between theoretical and simulated outputs of NAND Gate

Logic Gate	Input	Input	Output	
			Theoretical	Simulated
NOR	1	1	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	1

Table8d: Comparison between theoretical and simulated outputs of NOR Gate

Logic Gate	Input	Input	Output	
			Theoretical	Simulated
NXOR	1	1	1	1
	1	0	0	0
	0	1	0	0
	0	0	0	0

Table8e: Comparison between theoretical and simulated outputs of XNOR Gate

Logic Gate	Input	Input	Output	
			Theoretical	Simulated
XOR	1	1	0	0
	1	0	1	1
	0	1	1	1
	0	0	0	0

Table8f: Comparison between theoretical and simulated outputs of XOR Gate

Logic Gate	Input	Output	
		Theoretical	Simulated
NOT	1	0	0
	0	1	1

Table8g: Comparison between theoretical and simulated outputs of NOT Gate

6. Precautions:

a) Ensure that 'powergui' block set is included in the Simulink file
b) Ensure that connections are properly made
c) Ensure that the scale of the graphs should be adjusted to the range in which the readings vary

7. Conclusion: Theoretical Knowledge on digital logic gates is verified through a Simulink platform.

Assignment:

Part-1: Consider Fig. 8.2 and do the same as mentioned in Section - 8.D.

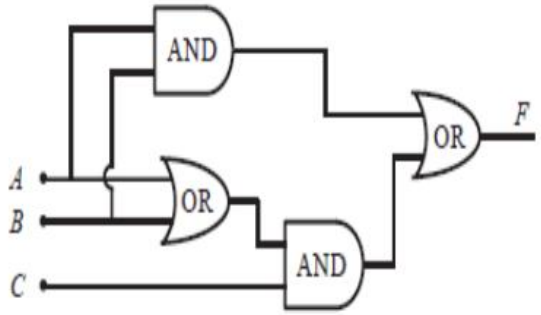


Fig. 8.2

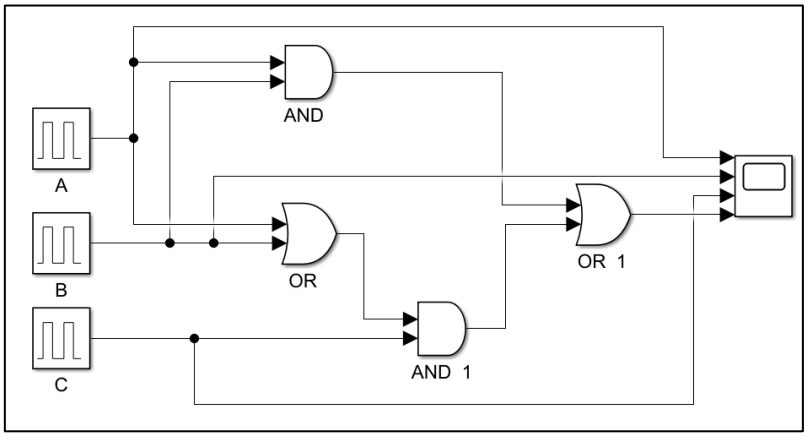
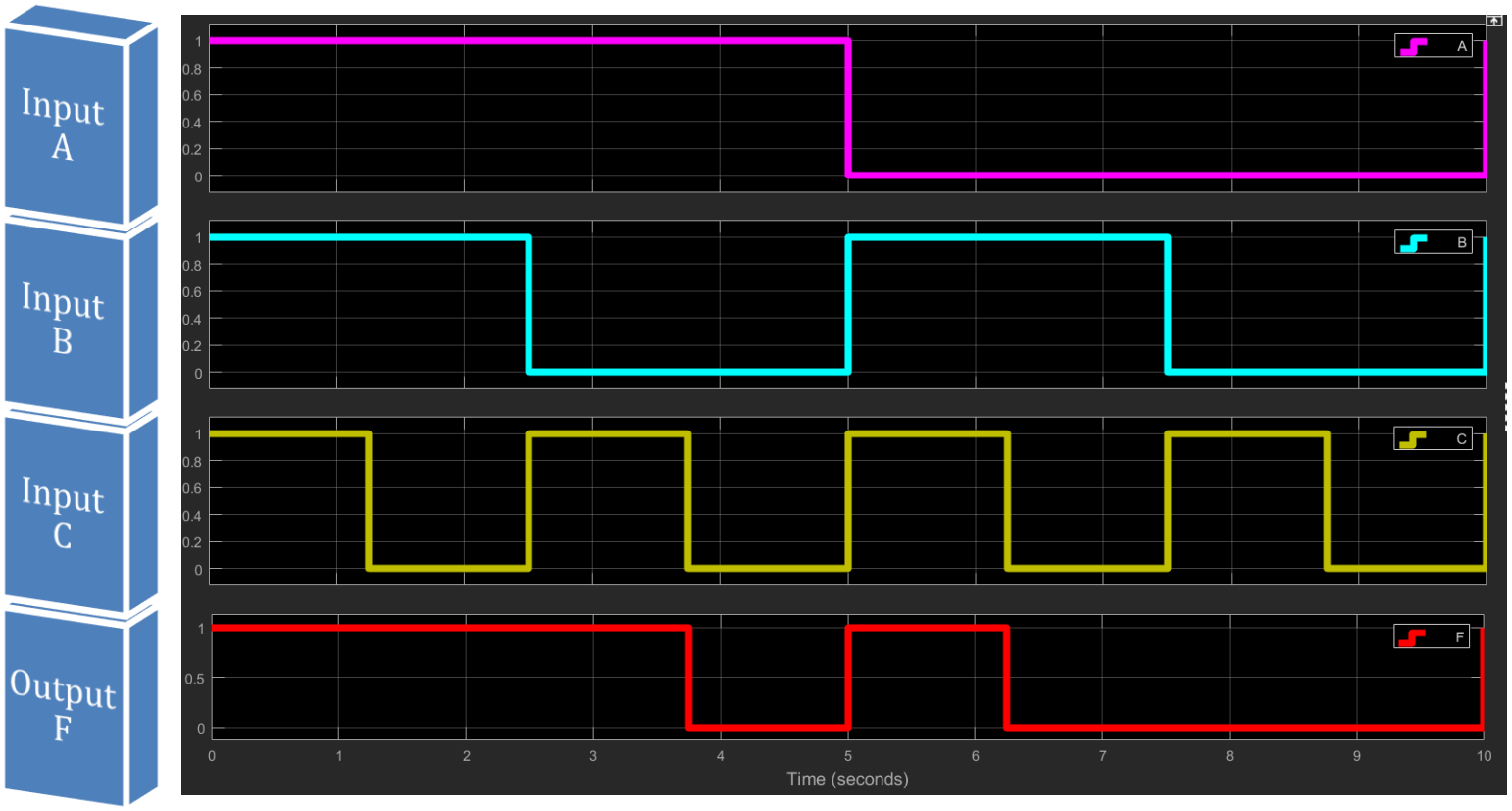


Fig8h: Simulink connections for circuit given in Fig 8.2

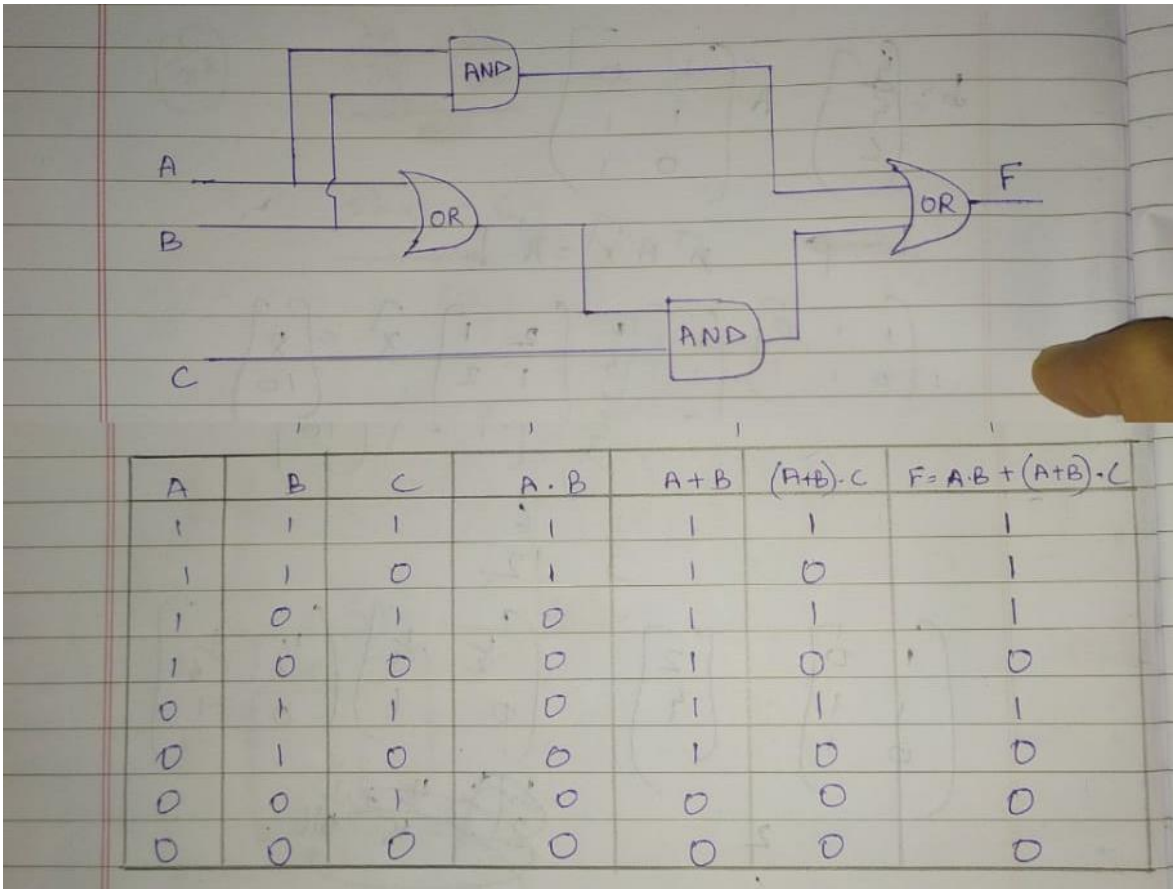
A	B	C	Output F	
			Theoretical	Simulated
1	1	1	1	1
1	1	0	1	1
1	0	1	1	1
1	0	0	0	0
0	1	1	1	1
0	1	0	0	0
0	0	1	0	0
0	0	0	0	0

Table8h: Comparison between theoretical and simulated outputs of circuit in Fig

Graphical Results:



Theoretical Results:



A	B	C	A · B	A + B	(A+B) · C	F = A·B + (A+B)·C
1	1	1	1	1	1	1
1	1	0	1	1	0	1
1	0	1	0	1	1	1
1	0	0	0	1	0	0
0	1	1	0	1	1	1
0	1	0	0	1	0	0
0	0	1	0	0	0	0
0	0	0	0	0	0	0

Assignment:

Part-2: Replace the gates shown in Fig. 8.2 by its inverted one and do the same as mentioned in Section - 8.D.

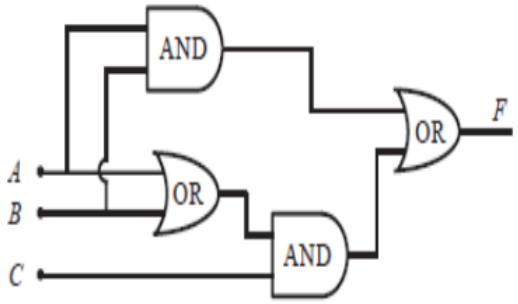


Fig. 8.2

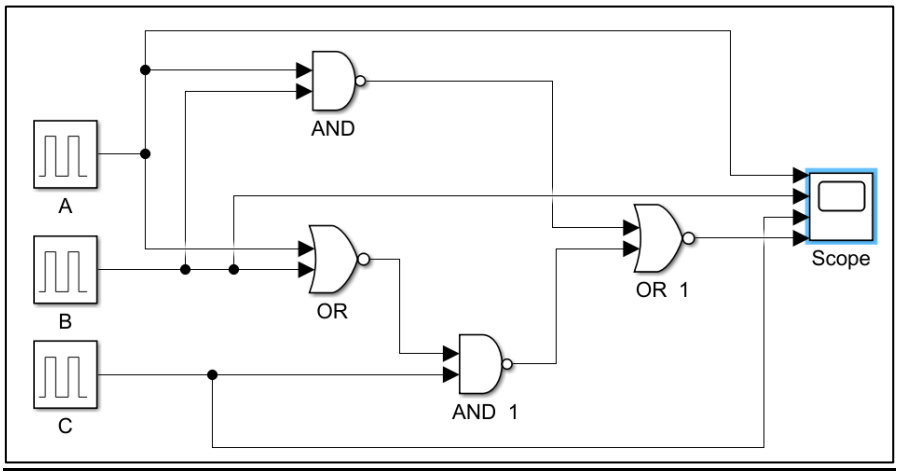
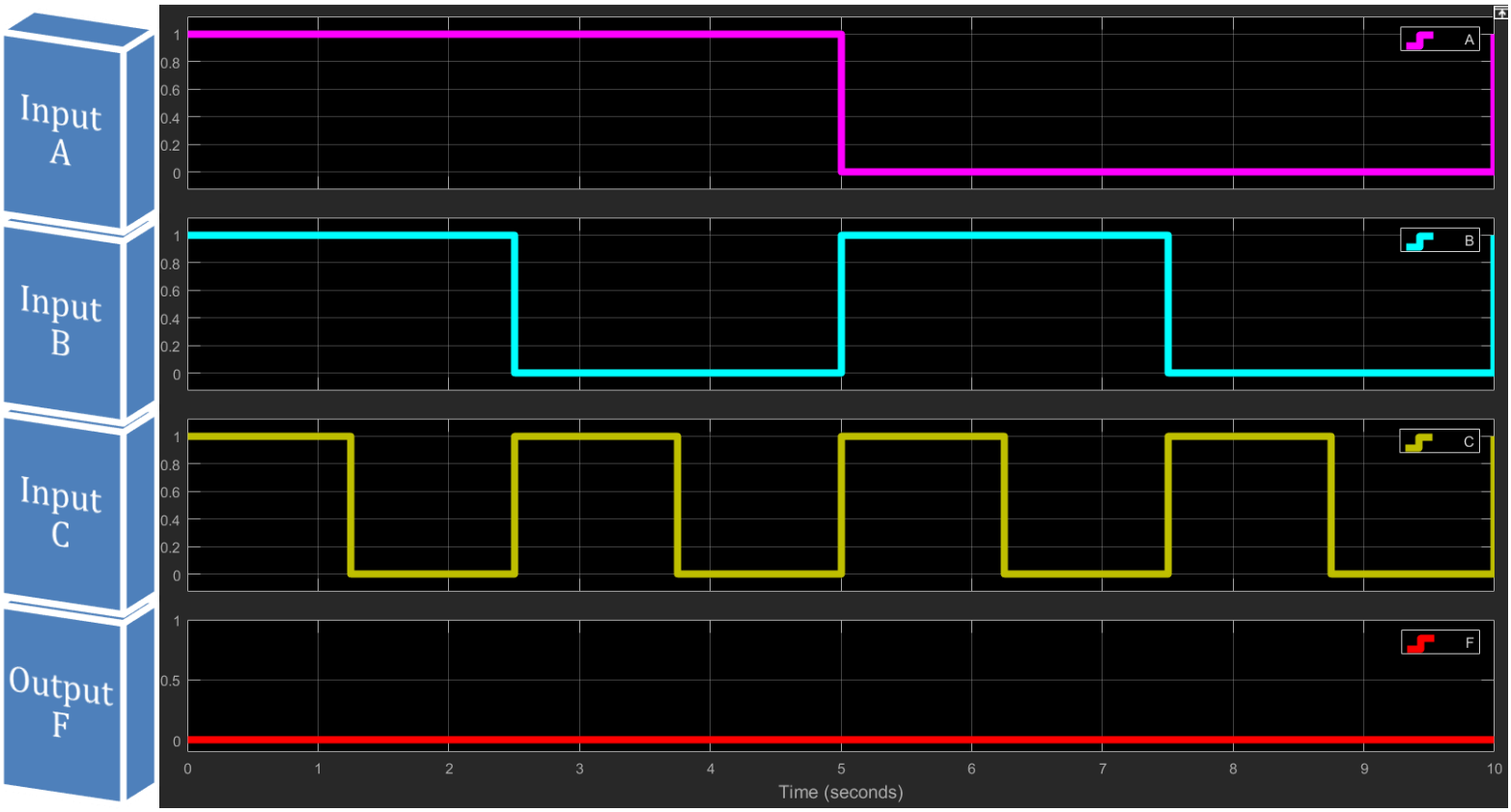


Fig8i: Simulink connections for circuit described as per statement in assignment part 2

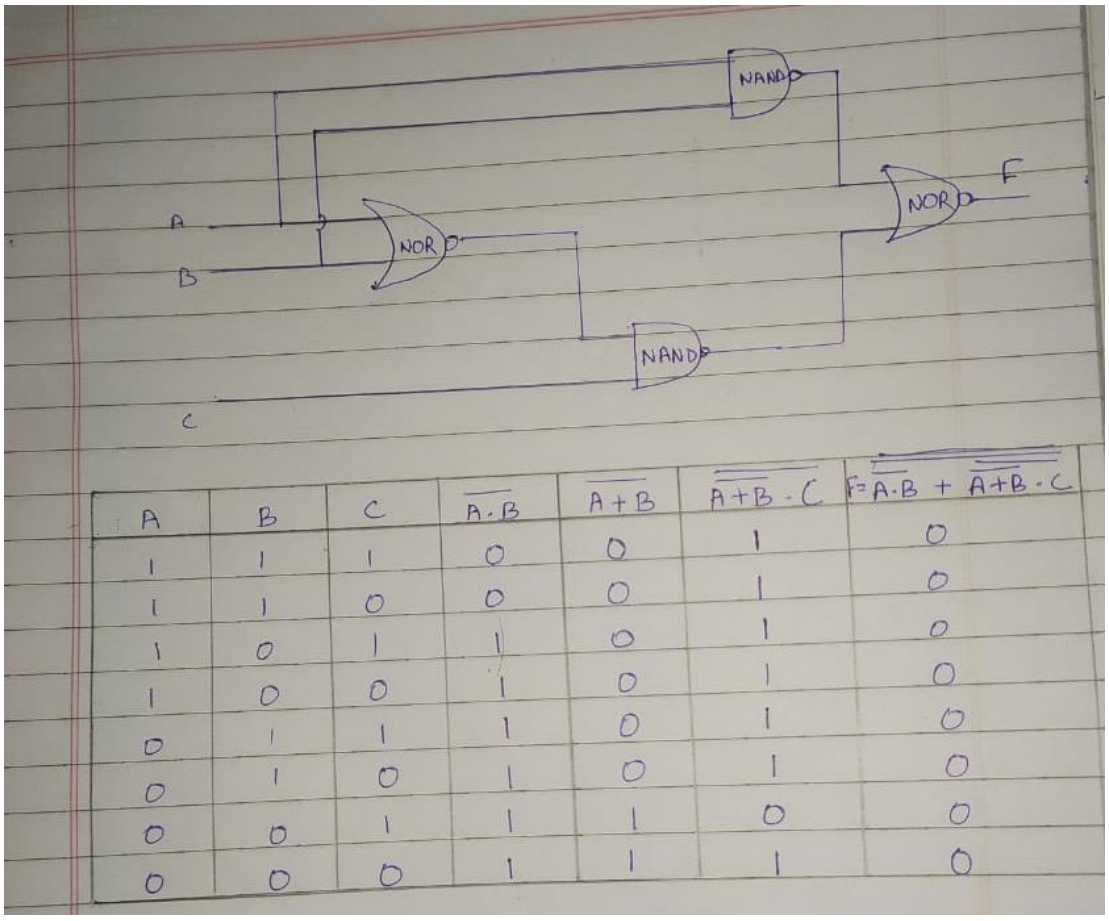
A	B	C	Output F	
			Theoretical	Simulated
1	1	1	0	0
1	1	0	0	0
1	0	1	0	0
1	0	0	0	0
0	1	1	0	0
0	1	0	0	0
0	0	1	0	0
0	0	0	0	0

Table8i: Comparison between theoretical and simulated outputs of circuit in Fig

Graphical Results:



Theoretical Results:



A	B	C	$\overline{A \cdot B}$	$\overline{A+B}$	$\overline{\overline{A+B} \cdot C}$	$F=\overline{A \cdot B} + \overline{\overline{A+B} \cdot C}$
1	1	1	0	0	1	0
1	1	0	0	0	1	0
1	0	1	1	0	1	0
1	0	0	1	0	1	0
0	1	1	1	0	1	0
0	1	0	1	0	1	0
0	0	1	1	1	0	0
0	0	0	1	1	1	0