8. (a) Assuming even parity, find the parity bit for each of the following data units.

   i. 1001011

   ii. 0001100

   iii. 1000000 [3M]

   (b) Suppose we want to store messages made up of 4 characters a, b, c, d with frequencies 60, 5, 30, 5 respectively. What are the fixed-length codes and prefix-free codes that use the least space? [3M]

   (c) A source emits symbols X_i, $1 \leq i \leq 6$, in the BCD format with probabilities $P(X_i)$ as shown in the table below. Apply Shannon-Fano coding procedure to the data characterized in the table.

X_i	$P(X_i)$
A	0.30
B	0.10
C	0.02
D	0.15
E	0.40
F	0.03

   Are there any disadvantages in the resulting code words? Calculate the coding efficiency. [4M]

9. Given the dataword 1010011110 and the divisor 10111

   (a) Show the generation of the codeword at the sender site using binary division.

   (b) Show the checking of the codeword at the receiver site assuming no error has occurred.

   (c) What is the syndrome at the receiver end if the dataword has an error in the 5^{th} bit position counting from the right? Namely: dataword 1010001110 is received. [3+3+4=10M]

10. (a) Compare the data rates for Standard Ethernet, Fast Ethernet, Gigabit Ethernet, and 10 Gigabit Ethernet. [4M]

    (b) Consider five wireless stations, A, B, C, D, and E. Station A can communicate with all other stations. B can communicate with A, C and E. C can communicate with A, B and D. D can communicate with A, C and E. E can communicate with A, D and B.

    i. When A is sending to B, what other communications are possible?

    ii. When B is sending to A, what other communications are possible?

    iii. When B is sending to C, what other communications are possible? [6M]

* * *ALL THE BEST * **

the last signal level has been positive. From the graphs, guess the bandwidth for this scheme using the average number of changes in the signal level.

i. 00000000

ii. 11111111

iii. 01010101

iv. 00110011 [4M]

(b) What are the differences between unipolar, polar and bipolar schemes of line coding? [2M]

(c) Sketch the Manchester encoding on a classic Ethernet for the bit stream 0001110101. [4M]

5. (a) What is the result of scrambling the sequence 10101000000000 using the following scrambling techniques? Assume that the last non-zero signal level has been positive.

i. B8ZS

ii. HDB3 [3M]

(b) Assume we need to create codewords that can automatically correct a one-bit error. What should the number of redundant bits (r) be, given the number of bits in the dataword (k)? After finding the relationship, find the number of bits in r if k is 1, 2, 5, 50, or 1000. [3M]

(c) If we need to correct more than one bit, the number of redundant bits increases. What should the number of redundant bits (r) be to automatically correct one or two bits (not necessarily contiguous) in a dataword of size k? After finding the relationship, find the number of bits in r if k is 1, 2, 5, 50, or 1000. [4M]

6. (a) Determine if the data block and accompanying checksum below are error free. The data block uses a 1's complement checksum.
Data: $06_{16}00_{16}F7_{16}7E_{16}01_{16}52_{16}$
Checksum: 31_{16} [5M]

(b) Generate the CRC checksum to be transmitted with the data stream 1011011010010110_2 using the divisor 11011_2. [5M]

7. (a) To provide more reliability than a single parity bit can give, an error-detecting coding scheme uses one parity bit for checking all the odd-numbered bits and a second parity bit for all the even-numbered bits. What is the Hamming distance of this code? [5M]

(b) Sixteen-bit messages are transmitted using a Hamming code. How many check bits are needed to ensure that the receiver can detect and correct single-bit errors? Show the bit pattern transmitted for the message 1101001100110101. Assume that even parity is used in the Hamming code. [5M]

Roll No								

National Institute of Technology Goa

Programme Name: B.Tech.

End Semester Examination, November-2019

B.Tech CSE
2nd yr
3rd Sem

Course Name: **Principles of Data Communication** Course Code: CS200

Date: 25. 11. 2019 Time: 2:00 PM - 5:00 PM

Duration: 3 Hours Max. Marks: 100

ANSWER ALL QUESTIONS

1. (a) Suppose a computer sends a frame to another computer on a bus topology LAN. The physical destination address of the frame is corrupted during the transmission. What happens to the frame? How can the sender be informed about the situation? [5M]

   (b) Translation, encryption, and compression are some of the duties of the presentation layer in the OSI model. Which layer do you think is responsible for these duties in the Internet model? Explain your answer. [5M]

2. (a) A periodic composite signal with a bandwidth of 2000 Hz is composed of two sine waves. The first one has a frequency of 100 Hz with a maximum amplitude of 20 V; the second one has a maximum amplitude of 5 V. Draw the frequency spectrum and mark the bandwidth. [3M]

   (b) A composite signal contains frequencies from 10 KHz to 30 KHz. The amplitude is zero for the lowest and the highest signals and 30 volts for the 20-KHz signal. Assuming that the amplitudes change gradually from the minimum to the maximum, draw the frequency spectrum. [3M]

   (c) We have a channel with 4 KHz bandwidth. If we want to send data at 100 Kbps, what is the SNR? What is the SNR_{dB}? [4M]

3. (a) In a digital transmission, the sender clock is 0.2 percent faster than the receiver clock. How many extra bits per second does the sender send if the data rate is 1 Mbps? [3M]

   (b) Two signals have the same frequencies. However, whenever the first signal is at its maximum amplitude, the second signal has amplitude of zero. What is the phase shift between the two signals? [3M]

   (c) Which of the three analog-to-analog conversion techniques (AM, FM, or PM) is the most susceptible to noise? Defend your answer. [4M]

4. (a) Draw the graph of the NRZ-L scheme using each of the following data streams, assuming that

Roll No									

NATIONAL INSTITUTE OF TECHNOLOGY GOA

Farmagudi, Ponda, Goa, 403401

B.Tech CSE 2nd yr 3rd Sem

Programme Name: B.Tech

End Semester Examinations, November-2019

Course Name: Computer Organization and Architecture | Course Code: CS202

Date: 28/11/2019 | Time: 02:00 PM-05:00 PM

Duration: 3 Hours | Max. Marks: 100

ANSWER ALL QUESTIONS

NOTE: 1) The diagrams should be neatly drawn
2) Answer to every question should start in a new page

1.

a. We know that IEEE 754 corresponds to the floating-point representation. What may be the reason for such standardization?
b. Using single-precision floating point representation, add and multiply the numbers 2.5 and 0.75.

(2+8=10 marks)

2.

a. With a neat diagram give the design of a 16 bit carry-look ahead adder (CLA) built using 4 bit CLAs. Also give the design of a 32 bit CLA built using the 16 bit CLA according to the specification given in this question.
b. With a neat diagram, explain sequential circuit binary multiplier. Illustrate with an example.

(5+5=10 marks)

3.

a. Compare and contrast a SRAM cell and a DRAM cell
b. What is 2-dimensional address decoding? Explain taking an example and a neat diagram.
c. What is Fast page mode of DRAM and Double Data Rate SDRAM.

(3+4+3=10 marks)

4.

a. We agree that operating system (OS) is the overall manager of a computer system. It implies that OS should always be running and available in memory. When a computer is turned on the OS would not even be loaded in the memory. Then how it is brought into memory?
b. Why computers' memory is typically built as hierarchy?
c. Consider the following analogy for caching. A serviceman comes to a house ti repair the air conditioning system. He carries a toolbox that contains a number of tools that he has used recently in similar job. He uses these tools repeatedly, until he reaches a point where other tools are needed. It is likely that he has the required tools in his vehicle parked outside the house. But, if the needed tools are not in his vehicle, he must go to his shop to get them
Suppose we argue that the toolbox, the vehicle, the shop correspond to the L1 cache, L2 cache, and the main memory of a computer. How good is this analogy? Discuss its correct and incorrect features.

(3+4+3=10 marks)

5.

a. How the read miss and write miss on cache is handled? Explain
b. What is the purpose of virtual memory?
c. What is the need for address translation in virtual memory? How address translation is done? Explain

(4+2+4=10 marks)

6. A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses:
200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4
This pattern is repeated four times.

a. Show the contents of the cache at the end of each pass through this loop if a direct mapped cache is used. Assume that the cache is initially empty.
b. Repeat part (a) for an associative-mapped cache that uses the LRU replacement algorithm.
c. Repeat part (a) for a four-way set-associative cache.

(4+3+3=10 marks)

7.

a. What is an I/O interface? What is its role? Explain.
b. What are the approaches to achieve required synchronization between processor and an I/O device?

(4+6=10 marks)

8.

a. Compare and contrast a micro programmed control unit and a hard wired control unit.
b. Write the complete control sequence (including the instruction fetch) for the following instructions. Assume that every instruction is 2 bytes in length
   i. SUB [R1], R3
   ii. JLT LoopBegin

(3+7=10 marks)

9.

a. A CPU has only three instructions I1, I2 and I3, which uses the following signals in time steps T1-T5:

I1: T1 : Ain, Bout, Cin
T2 : PCout, Bin
T3 : Zout, Ain
T4 : PCin, Bout
T5 : End

I2: T1 : Cin, Bout, Din
T2 : Aout, Bin
T3 : Zout, Ain
T4 : Bin, Cout
T5 : End

I3: T1 : Din, Aout
T2 : Ain, Bout
T3 : Zout, Ain
T4 : Dout, Ain
T5 : End

Write the login functions needed for generating the control signals necessary for execution of the three instructions I1, I2 and I3.

(10 marks)

10.

a. Draw the pipeline execution diagram for the following segment of code

I1		LOAD R0, N
I2		LOAD R1, X
I3		LOAD R2, Y
I4	BL	MUL R3, R1, R2
I5		ADD R4, R2, R3
I6		DEC R0
I7		JNZ BL
I8		STORE Z, R4

Assume that the program is running on a hardware that supports 4 stage pipeline. Assume that the N, X and Z are the locations on L1 cache and Y is the location in main memory. The execution stage of LOAD in I1, I2 and STORE in I8 take 1 clock cycle and LOAD in I3 take 2 clock cycle. The execution stage of MUL and ADD instructions take 3 and 1 clock cycles respectively. Assume that the value stored in location N is 2. Here instruction DEC corresponds to decrementing the operand.

b. What are the hazards in pipeline? Explain briefly.

(6+4=10 marks)

*****************************ALL THE BEST************************************