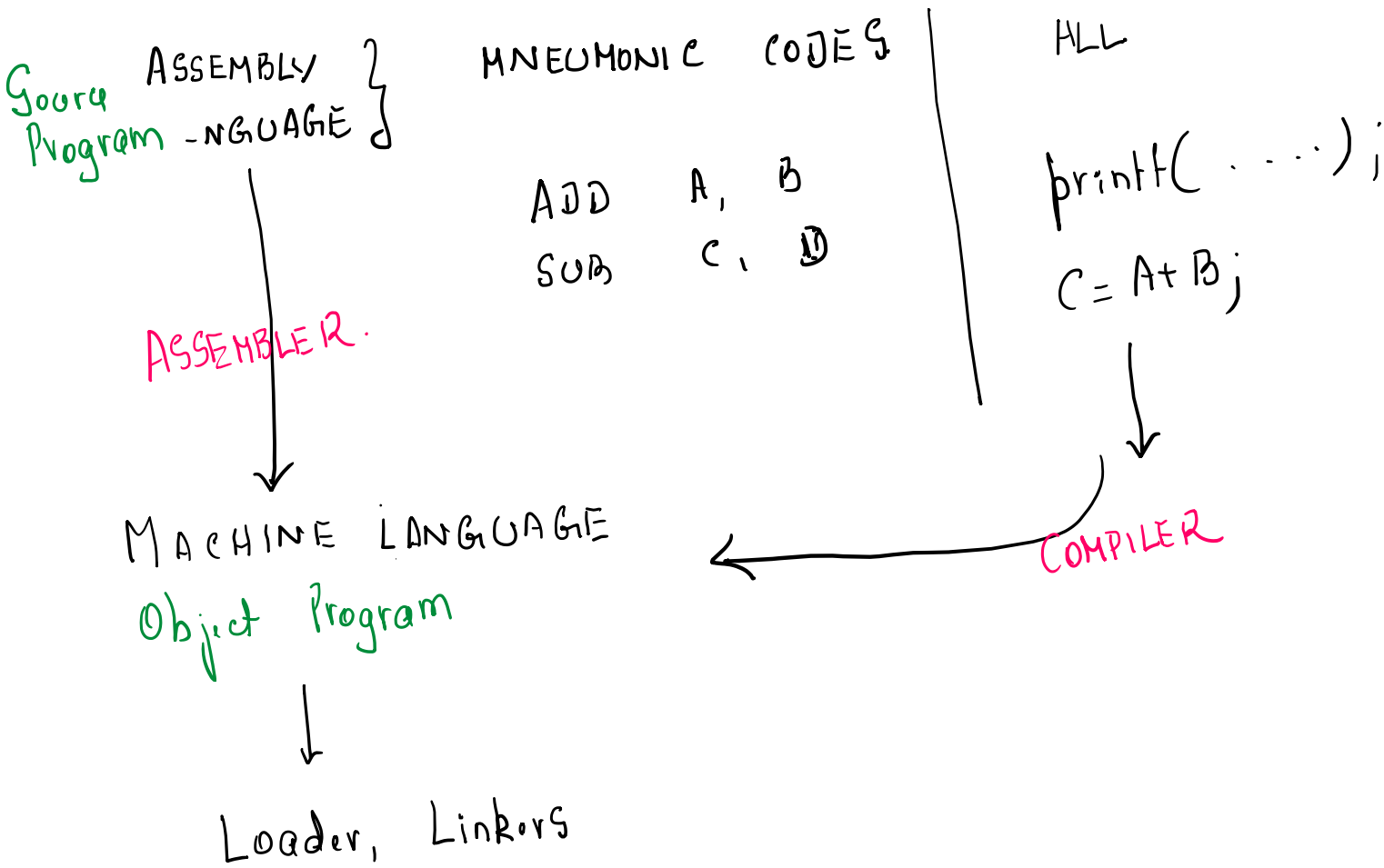
CS251 - Systems Programming

- Assemblers
- Loaders
- Linkers
- Macroprocessor
- Utility Programs



System Program ⟷ Application Program

ASSEMBLER

↳ 0110 011100 001100.

ADD

001100

↑

Lesser dependence on H/W aspects

SP → Machine Architecture-Dependence.

Suitable Architecture.

↓

Hypothetical Machines.

RISC.

SIC: Simplified Instructional Computer

CISC.

SIC/XE

Extra Equipment.

- Memory
- Registers
- Data formats
- Addressing modes
- Instruction set
- I/O

Hexadecimal representation

- base - 16 system.
- Positional numeral system.

Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Deci	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

- Human-friendly representation → Binary coded decimal.

0000 0000.

0 0

4-bits
↳ nibble.
↓
1 hexadecimal digit.

1111 1111

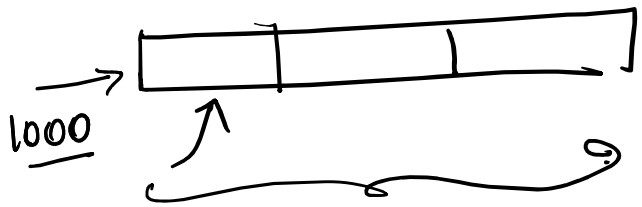
F F

15

0001 1101

SIC

- Memory
  - 8-bit bytes
  - Word → 3-consecutive bytes.
    - 24-bit
  - Byte addressable.



  - Address of a word.
    ↳ lowest numbered byte.
  - Total of 32768 bytes

$$\Downarrow$$

$$2^{15}$$

$2^9 \rightarrow 512$

$2^{10} \rightarrow 1024.$

15-bit address

- Registers
  - 24-bit length
  - 5 registers.

LDA (TEN.)

A ← (TEN)

Mnemonic.	Number.	
A	0	Accumulator. Arithmetic operations
X	1	Index register.

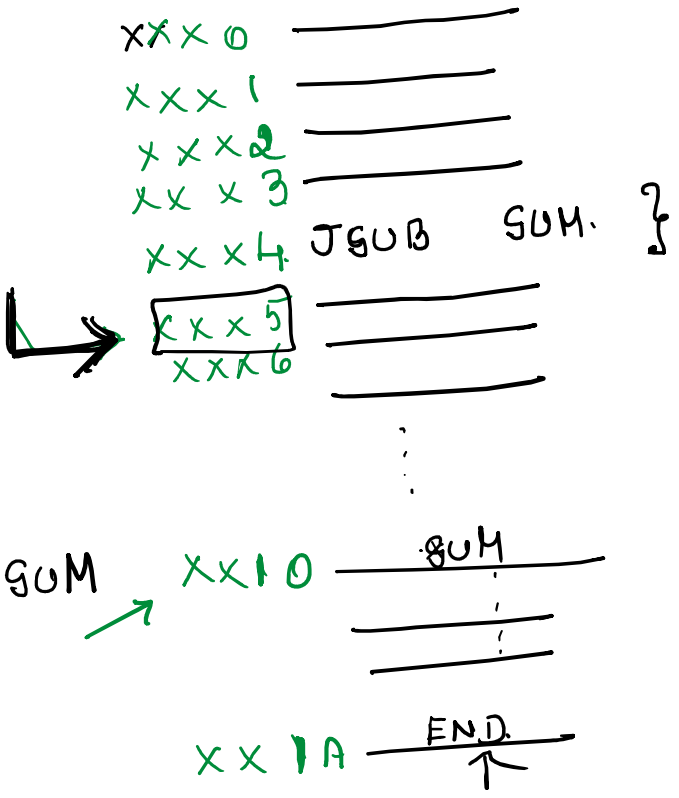
- Sequence of memory.

```
i = 0
i++;
Array[i]
↓ + [X]
```

X → increment

L 2 Linkage register.

Jump to subroutine (JSUB) → return.



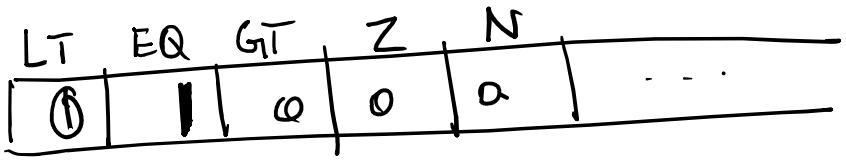
PC 8. Program Counter

SW 9. Status word.

CC

CMP P, Q.

JLT . . .



- Data formats.

① — Integers

— 24-bits.

— 2's complement

② Ascii codes

- 8-bit.

- Instruction formats

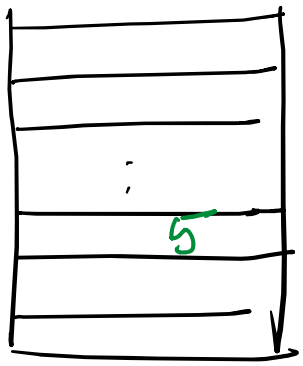
— 24-bit length.

— Addressing modes

— 2 addressing modes.

→ X-flag

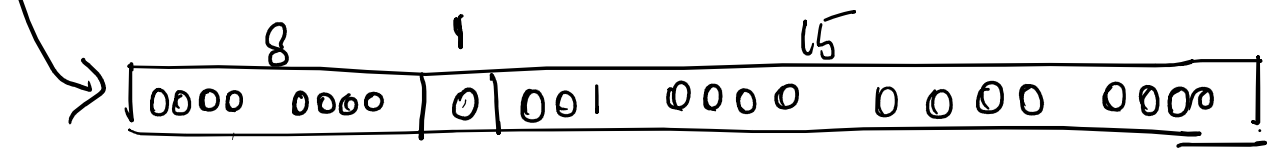
- Direct x=0 TA = Address
- Indexed. X=1 TA = Address + (X).



LDA TEN.
00

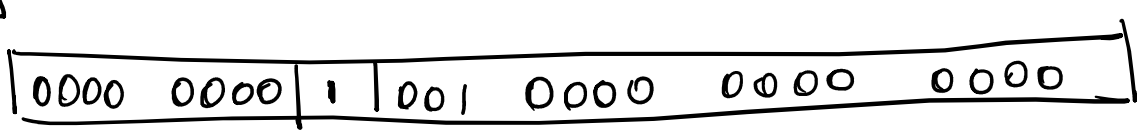
TEN.
→ 1000

A ← 5



LDA TEX, X.

Indexed.



EA = 1000 + (X)

GTCH BUFFER, X