

Representation

- Data & instructions

- Numeric data

- Integer

- Real value

- Integer arithmetic

Unsigned

Signed

- Sign-magnitude

- 1's complement

- 2's complement

$n = 4$

Homework
2.1

Decimal values 5, -2, 14, -10, 26, -19, 51 and -43

→ Signed 7-bit numbers

- Sign-magnitude

- 1's complement

- 2's complement

Sign-Magnitude

1's Complement

2's complement

5

0000101

0000101

0000101

-2

1000010

1111101

1111110

14

-10

1111101 +
1111110

1111101

26

-19

51

-43

Electronic logic gates

2 logic levels:	0	1
	0V	5V
		3.3
		2.3
		1.8
		1.1
		0.5

Supply voltage.

Power consumption \propto
Square of supply
voltage.

— Power consumption ↓

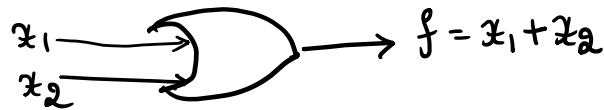
→ Smaller transistor → Length of transistor ↓

⇒ Pack more components on a given area

— Hand-held devices, sensors.

— Transistors → Logic gates

OR gate



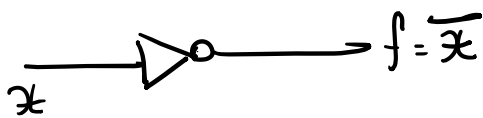
x_1	x_2	$f = x_1 + x_2$
0	0	0
0	1	1
1	0	1
1	1	1

AND



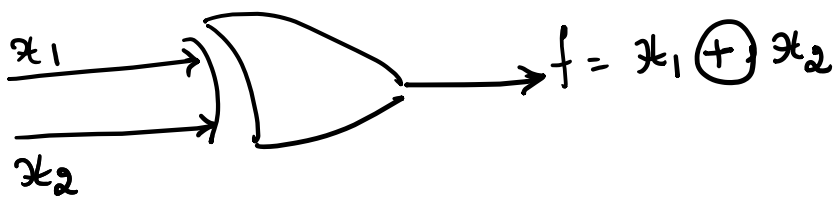
x_1	x_2	$f = x_1 . x_2$
0	0	0
0	1	0
1	0	0
1	1	1

NOT gate



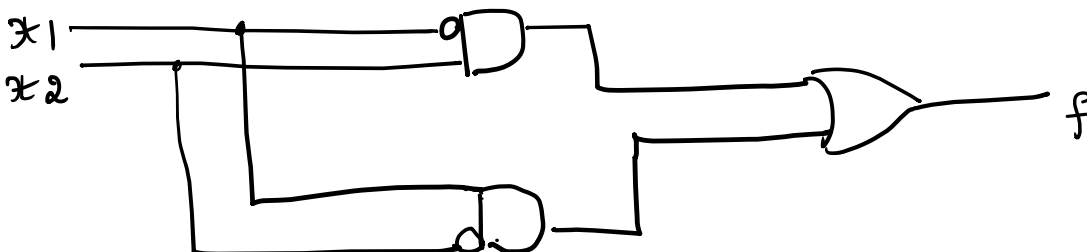
x	$f = \bar{x}$
0	1
1	0

XOR gate



x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

Synthesize - logic functions



x_1	x_2	$\overline{x_1} \cdot x_2$	$x_1 \cdot \overline{x_2}$	$f =$
0	0	0	0	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

XOR

$$f = \overline{x_1} \cdot x_2 + x_1 \cdot \overline{x_2}$$

SOP.

DESIGN OF ADDERS

Unsigned Addition

$$\begin{array}{r} x \\ + y \\ \hline z \end{array}$$

$$\begin{array}{r} 7 \\ + 6 \\ \hline 13 \end{array}$$

$$\begin{array}{r} \text{X} \swarrow \begin{array}{cccc} 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ \hline 1 & 1 & 0 & 1 \end{array} \end{array}$$

Signed 2's complement Addition

$$\begin{array}{r} x \\ + y \\ \hline z \end{array} \quad \begin{array}{r} (+7) \\ + (-3) \\ \hline +4 \end{array}$$

$$\begin{array}{r} \begin{array}{cccc} 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ \hline 0 & 1 & 0 & 0 \end{array} \quad \begin{array}{l} C_i \\ x_i \\ y_i \\ z_i \end{array} \end{array}$$

$$\begin{array}{r} C_{i+1} \quad C_i \\ x_i \\ y_i \\ \hline z_i \end{array}$$

x_i

Carry_{out} $C_{i+1} \leftarrow \boxed{}$

y_i $\boxed{} \leftarrow \text{Carry in @ } C_i$

z_i

INPUT			OUTPUT	
x_i	y_i	C_i	$S_i \mid Z_i$	C_{i+1}
0	0	0	0 $x_i y_i C_i$	0
0	0	1	1 $\bar{x}_i \bar{y}_i C_i$	0
0	1	0	1 $\bar{x}_i y_i \bar{C}_i$	0
0	1	1	0 $x_i \bar{y}_i \bar{C}_i$	1
1	0	0	1 $x_i \bar{y}_i C_i$	0
1	0	1	0 $\bar{x}_i y_i \bar{C}_i$	1
1	1	0	0 $\bar{x}_i \bar{y}_i C_i$	1
1	1	1	1 $x_i y_i C_i$	1

At one bit position

$$S_i = \downarrow +$$

$$() +$$

$$()$$

→ 1-bit adder.