:

SIC/XE Machine Architecture

XE : Extra Equipment

- Memory
  - 2^{20} Bytes
- Registers
  - 5 registers

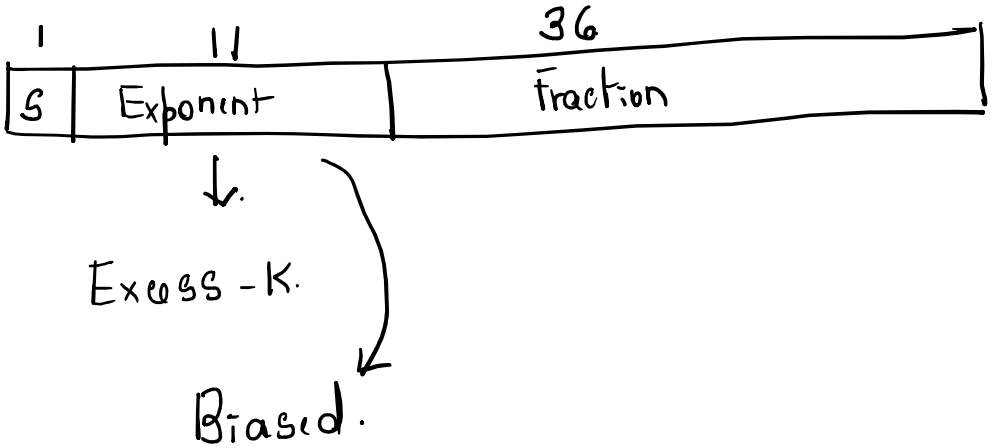
A	0
X	1
L	2
PC	8
SW	9

  - 4 registers

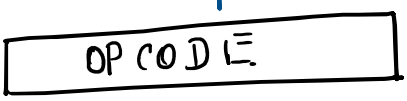
B	3	Base register Addressing

S	4	General working register.
T	5	"
F	6	FP Accumulator.

- Data formats
  - Characters
  - Integers. } 24-bit
  - 48-bit floating point numbers



- Instruction formats
  - Different formats
  - CISC.
    - Relative Addressing
  - 4 formats
    - Format 1 : 1 Byte.

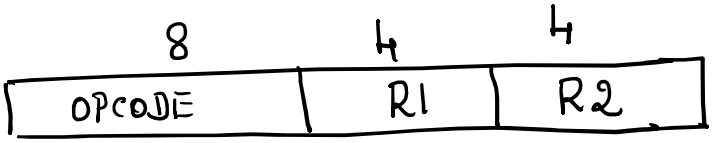


→ FIX (A) ← (F)

→ FLOAT (F) ← (A)

→ HIO

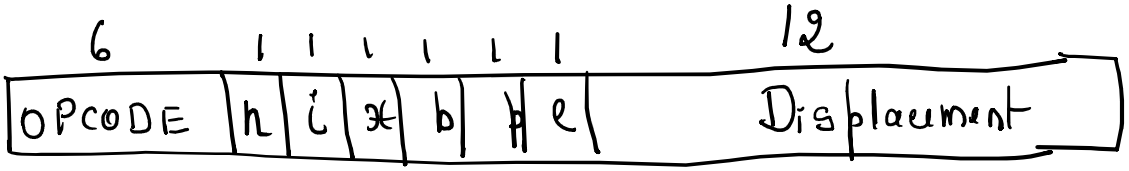
- Format 2: 2 Bytes



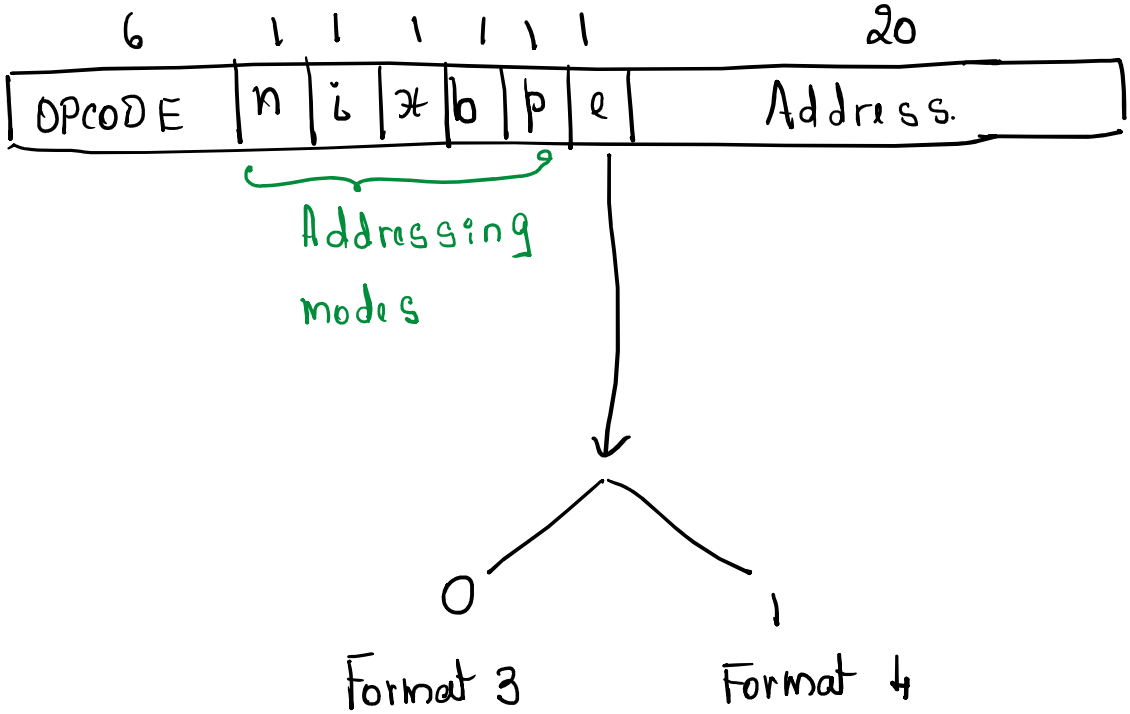
COMPR A, S

A 0 0 4

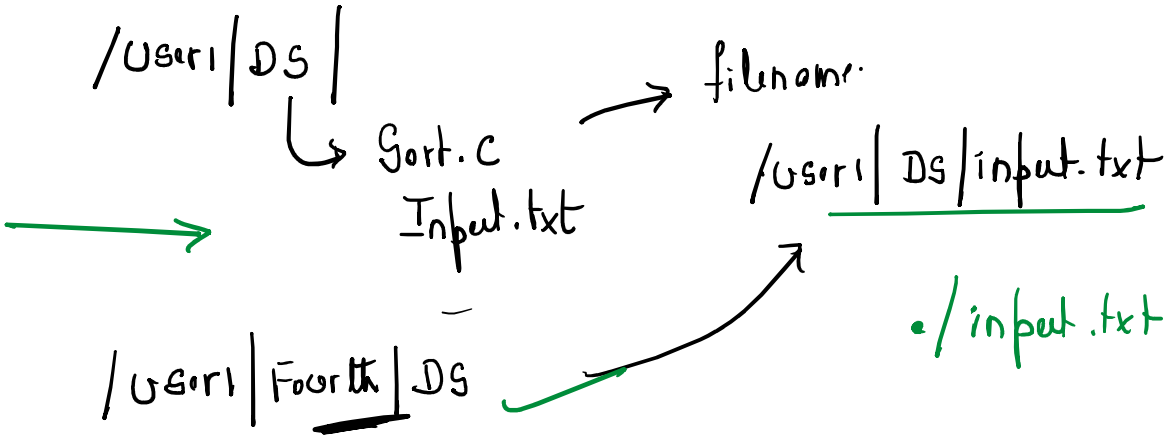
- Format 3: 3 Bytes

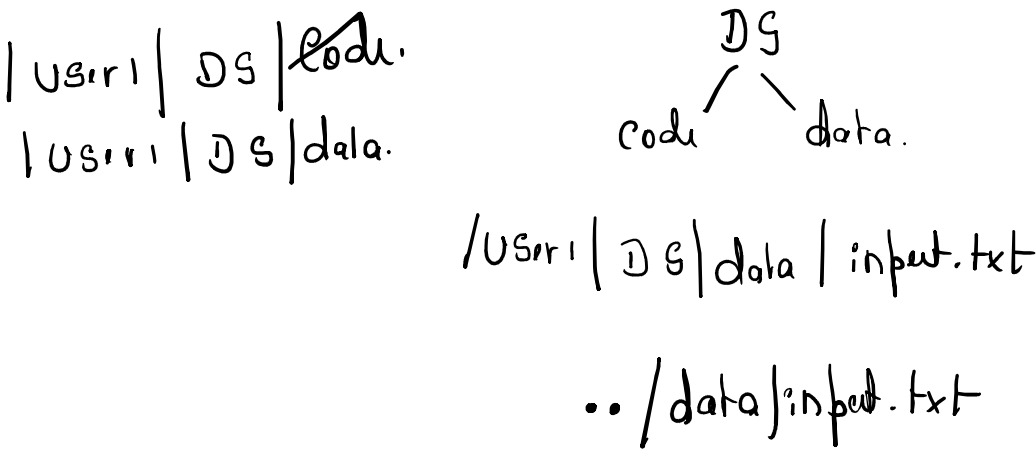


- Format 4: 4 Bytes



- Addressing modes.
  - Relative Addressing
    - Format 3 instruction.

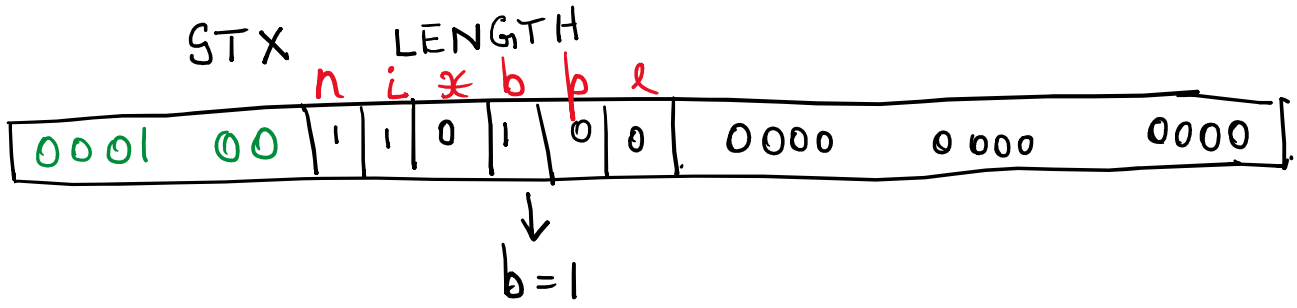




Type.	Indication.	Target Address	
Base Relative.	b=1, p=0	TA = [B] + Disp	0 ≤ disp ≤ 4095
Program Counter (PC) Relative.	b=0, p=1	TA = [PC] + disp	-2048 ≤ disp ≤ 2047

b=0 p=0 | b=1, p=1

– Ex for base relative addressing



[B] ⟺ 0033

x=0 ⇒ Direct

e=0 ⇒ F3

n=1, i=1 ⇒ Simple.

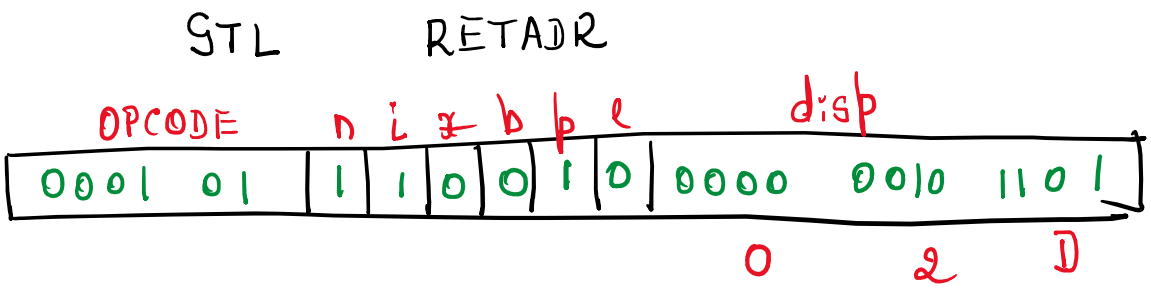
b=1 p=0 ⇒ Base relative Add.

TA = [B] + Disp.

= 0033 + 000

= 0033

– PC : Relative.



x=0 ⇒ Direct addressing

e=0 ⇒ F3

n=1, i=1 ⇒ Simple Addressing

b=0, p=1 ⇒ Pc relative addressing

$TA = [PC] + Disp$ $\quad disp = TA - [PC]$

$PC \leftrightarrow 0003$

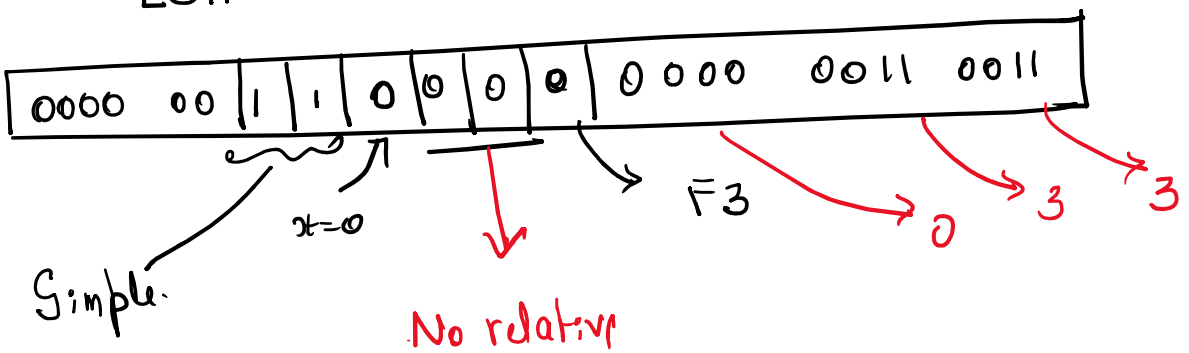
0003
0020
0030

LOOP TD 05
→ JEQ LOOP

PC →

LOOP COMP N
JGT EXIT
A0
⋮
J LOOP
EXIT TD

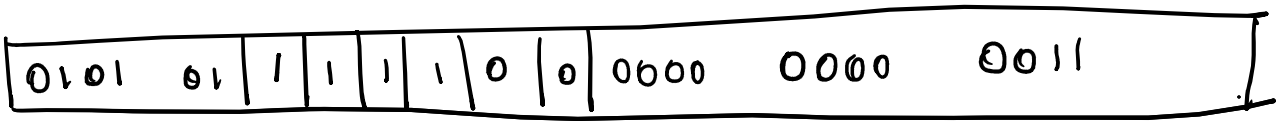
LDA LENGTH



No relative Addressing

⇒ Address directly given.

STCH BUFFER, X



X=1 ⇒ Indexed Addressing

b=1, p=0 ⇒ Base relative addressing

Disp = 003

[B] → 0033

[X] ⇒ 0

TA = Disp + [B] + [X]

Indexing and relative → together

0003
0033
0000
036

ASSEMPLY LANGUAGE

LDA LENGH

ASSEMBLER

0000 0011 0000 0000 0011 0011 ← M/c long

Displacement

TA = [B] + Disp

Disp = TA − [B]

TA = [PC] + Disp

Disp = TA − [PC]