Computer Organization and Architecture

Internal Organization of Memory Chips : DRAM

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Recap

- Memory design
- Internal organization of memory
- SRAM chip design
- SRAM module design

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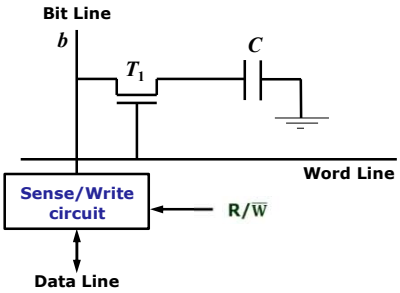
Dynamic RAM (DRAM) Cell

- Less expensive and simpler cell
- Information is stored in the form of a charge on a capacitor (C)
  - Charge in capacitor is stored only for short time
  - However, a cell is required to store information for a much longer time
- To retain information for longer time, content of capacitor mush be periodically refreshed



- Low speed as refresh needed
- Only 1 transistor is used
- Used to build main memory

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Dynamic RAM (DRAM) Chip Organization

- DRAM cells are also arranged in 2-dimensional array form
- Here also, row address lines are used to select row and column address lines are used to select column
- Two important factors influence the design of the DRAM chip are:
  - Number of input/output pins i.e. external pins
  - Need to refresh the cells
- Scheme for saving pins:
  - Row address and column address are transmitted over the same line one after the other
  - This is called time multiplexing
  - This is usually performed by a memory controller circuit
  - It generates the different control signals

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Dynamic RAM (DRAM) Chip Organization

- Two additional control signals are needed to inform the chip when the row address and column address is valid on address line
  - Row address strobe ($\overline{RAS}$):
    - Inform the chip when the row address is valid on address lines
  - Column address strobe ($\overline{CAS}$):
    - Inform the chip when the column address is valid on address lines
  - Both $\overline{RAS}$ and $\overline{CAS}$ are usually active low

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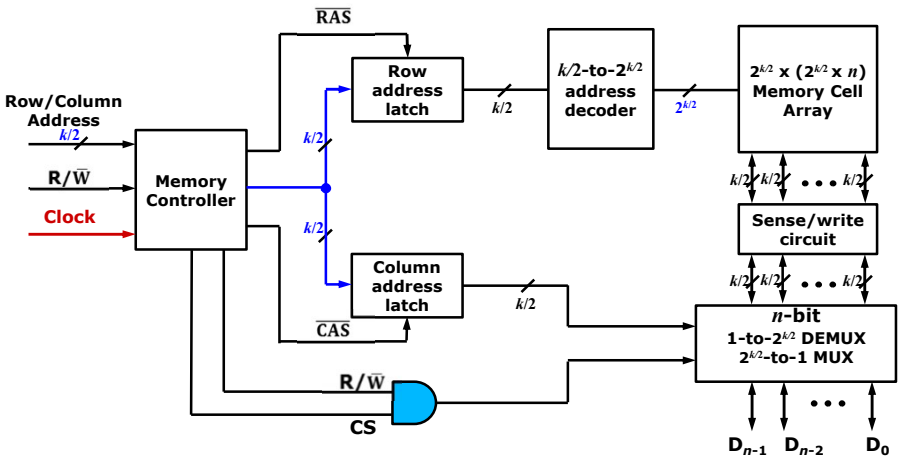
DRAM Chip Organization



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DRAM Chip Organization

- During read or write operation, the row address is applied first
  - It is loaded into row address latch in response to $\overline{RAS}$
  - Then read operation is initiated, in which all cells in a selected row are read and refreshed
- Shortly after row address is loaded, the column address is applied
  - It is loaded onto the column address latch under the control of $\overline{CAS}$
- The information in the column address latch is decoded and appropriate n sense/write circuits are selected
- To ensure that the contents of DRAM are maintained, each row of cells must be accessed and refreshed periodically

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DRAM Chip Organization

- Memory controller circuit provide the necessary signals $\overline{CAS}$ and $\overline{RAS}$ that governs timing
- These operations are directly synchronised with clock signal
- Such a DRAM chip is called Synchronous DRAM (SDRAM)

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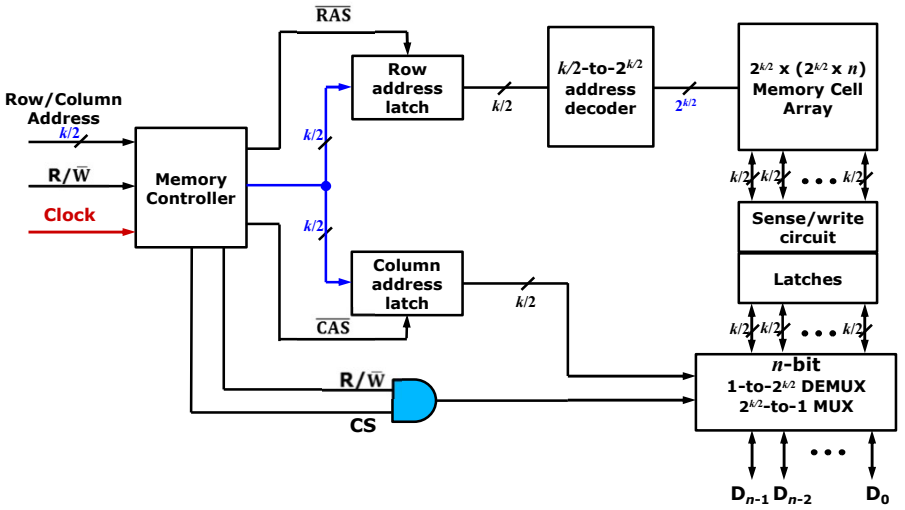
SDRAM Chip Organization



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Fast Page (Burst) Mode Feature of SDRAM

- Transfer capability of SDRAM
- Contents of all $2^{k/2}$ cells in a selected row are sensed in each on the n cell arrays
- Only n bits (one from each of the cells arrays) are placed in the data lines, $D_{(n-1)-0}$
- To access other bytes in the same row, without having to reselect the row, a latch is used at the output of the sense/write circuits in each column
- The row address will load the latches corresponding to all bits in the selected row
- Then different column address are applied to place the different bytes on data lines
- Transfer bytes in sequential order
- This arrangement allows transferring a block of data at much faster rate

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Refresh Overhead in SDRAM

- All dynamic memories need to be refreshed
- In SDRAM typical period of refreshing all rows is ***64ms***
- Each row is refreshed at least in 64*ms*
- Example:
  - *Suppose a SDRAM chip has 8K (8192) rows*
  - *Number of clock cycles to access each row:* 4 clock cycles
  - Number of clock cycles to refresh all rows:

    8192 x 4 = 32768 clock cycles
  - *Suppose clock rate of SDRAM is* 133 MHz
  - Times needed to refresh all rows:

    $32768/133x10^{6} = 246x10^{-6}$ *s* = 0.246 *ms*
  - **Refreshing overhead is *0.246ms* out of *64ms***

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Memory Performance Parameters

- **Access Time**:
  - Time interval between initiation of one operation and completion of that operation
  - Example: Time between assertion of Read signal and MFC signal
- **Memory Cycle Time**:
  - Minimum time delay between the initiation of two successive memory operations
  - Time delay between start of a read/write operation to start of next memory operation
- Memory cycle time is usually slightly larger than access time

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Memory Performance Parameter: Memory Latency

- **Latency:** Amount of time it takes to transfer a word of data to or from the memory
  - While reading and writing single word of data, latency provides a complete indication of memory performance
- In burst operations the time needed to complete the operations depends also on the rate at which successive words can be transferred
- **Latency(block transfers)**: Time to access the first of the sequence of memory words
  - How much time needed to transfer the entire block
  - Blocks are of varying size
  - Number of bits or bytes that can be transferred in one second

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Memory Bandwidth

- **Number of bits or bytes that can be transferred in one second**
  - Depends on the speed of access to the stored data
  - Also depends on the number of bits that can be accessed in parallel
- **Effective bandwidth in a computer**
  - Speed of memory
  - Transfer capability of the links that connect the memory and the processor—speed of bus

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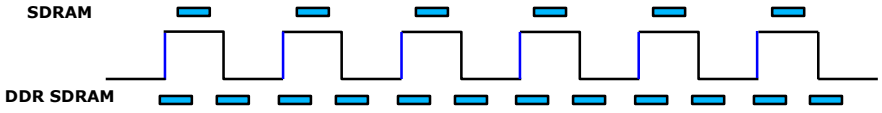
Double-Data-Rate SDRAM (DDR SDRAM)

- Faster version of SDRAM
- The standard SDRAM performs all actions on the raising edge of the clock cycle
- DDR SDRAM access the cell array in the same way, but transfers the data on both edges of the clock
- Hence, their bandwidth is essentially doubled for long burst transfers
- Bandwidth: The number of bits/bytes that can be transferred in one second



BM 33L5039 RAM Module

(1 GB, DDR RAM, 266 MHz, DIMM 184-pin)

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Reference

- **Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", 5th Edition, Tata McGraw Hill, 2002**

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Thank You

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