SEM 2 – 5 (RC 07-08)

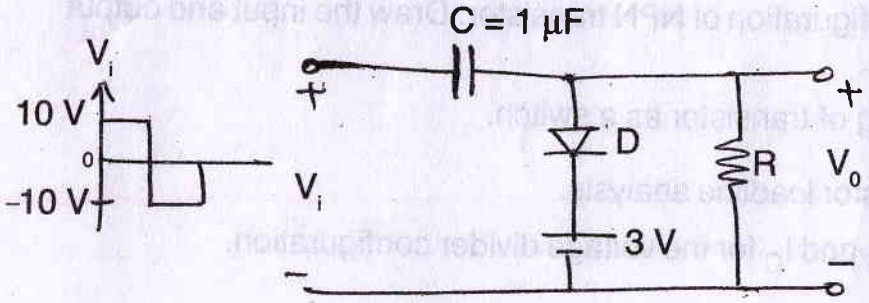
F.E. (Semester – II) (Revised in 2007-08) Examination, Nov./Dec. 2017
BASIC ELECTRONICS ENGINEERING

Duration : 3 Hours | Total Marks : 100

Instructions : *1) Answer **5** questions choosing atleast **one** from **each** Module.*
*2) Assume data **if necessary**.*

MODULE – I

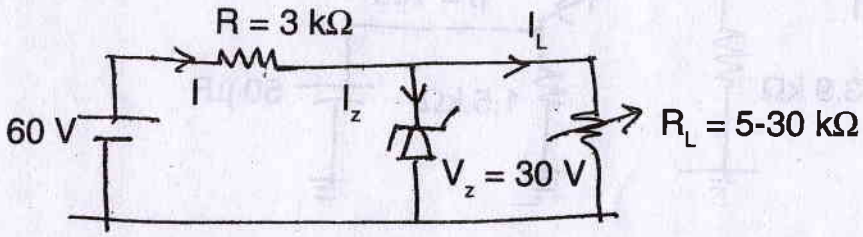
1. a) Determine the output waveform for the following circuit assuming RC time constant is very large and diode is ideal. **4**



b) Using Zener diode approximations find current through the diode of fig. when load resistance R_L is

i) 30 kΩ

ii) 5 kΩ. **6**



c) What is a diode and how is the depletion region formed ? **4**

d) In a center tap full wave rectifier, $R_L = 1\,k\Omega$ and each diode has a forward biased dynamic resistance $r_f = 10\ \Omega$. The voltage across each half of the secondary winding is 220 sinwt. Determine I_m, I_{dc}, I_{rms} and Ripple factor. **6**

P.T.O.

2. a) Explain the working of Half wave rectifier and derive the expression for Ripple factor and Efficiency. 10

   b) Why is a Filter required in a dc power supply ? Draw the circuit of a C filter and explain the output waveform. 5

   c) Draw and explain the operation of a Half wave voltage doubler. 5

MODULE – II

3. a) What do you mean by stabilization of operating point ? Explain the reasons why stabilization of Q point is necessary. 4

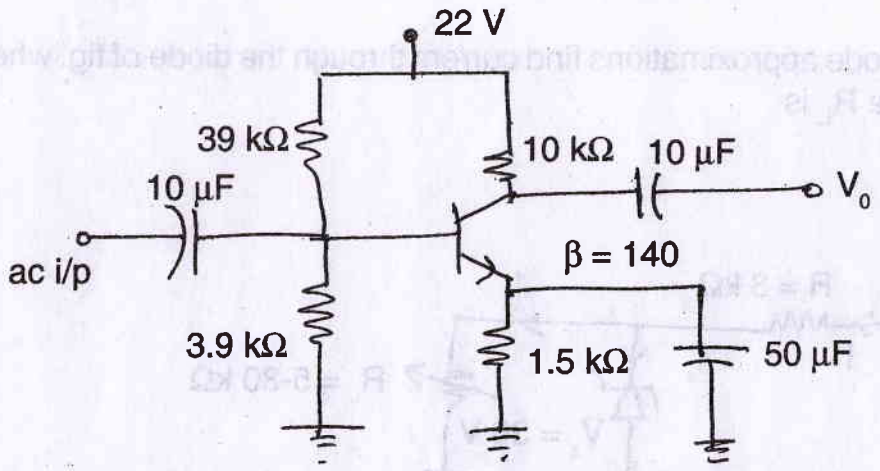
   b) Explain Fixed Bias BJT biasing configuration. 6

   c) Explain CE configuration of NPN transistor. Draw the input and output characteristics. 6

   d) Explain working of transistor as a switch. 4

4. a) Explain Transistor loadline analysis. 5

   b) Determine V_{CE} and I_C for the voltage divider configuration. 5



   c) With the help of circuit diagram and waveforms explain how a transistor works as an amplifier. 5

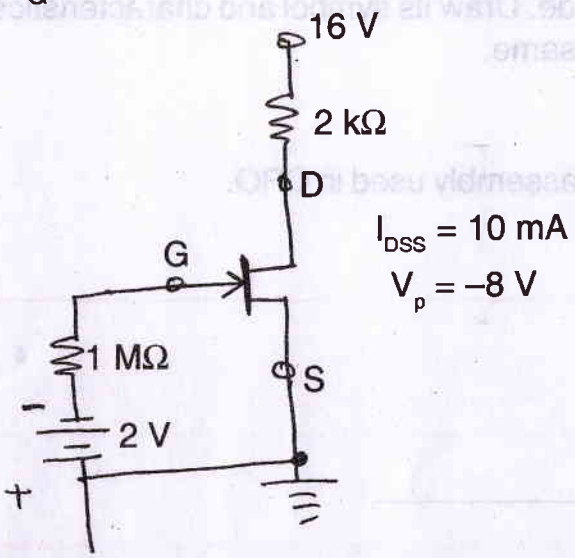
   d) Explain basic transistor construction. 5

MODULE – III

5. a) Draw and explain the drain to source characteristics of P-channel JFET. Also explain how transfer curve is obtained from the output characteristics. 7

b) For Fixed bias configuration given below, determine the following : 6

i) V_{GSQ} ii) I_{DQ}
iii) V_{DS} iv) V_D
v) V_G vi) V_S.



c) Explain the basic construction of n-channel JFET. Apply proper drain to source voltage and sketch the depletion region for $V_{GS} = 0$ and V_{DS} at some positive voltages. 7

6. a) Explain construction of n-channel Enhancement type MOSFET. Also draw its drain characteristics. 8

b) Explain how CMOS can be used as an inverter. 5

c) For the n-channel depletion-type MOSFET shown below determine : 7

i) I_{DQ} ii) V_{GSQ} iii) V_{DS}.