# Basic Electrical Science Lab Course Code: EE152

## **Laboratory Manual**

Name: Sadat Zubin Aftab Shah

Roll No: 20CSE1030

Section: B

Academic Session: April – August 2021

## **National Institute of Technology Goa**



## **CERTIFICATE**

This is to certify that Mr./ Ms	of Class <u>B.Tech</u>
1 <sup>st</sup> year (2 <sup>nd</sup> Sem), Division Sec A/B, bearing Roll. No	, has
satisfactorily completed the course experiments in	the Laboratory
Course Basic Electrical Science Lab (EE152) in the acade	emic year 2020-
2021 in the Institution of National Institute of Technolog	gy Goa.

**Course Instructor** 

## **Table of Contents**

SI. No.	Name of the Experiment	Pg. No.	Date of Experiment	Date of Submission	Marks/Expt. (10 M)
1	Verification of Ohms Law	04-10	20-05-2021	23-05-2021	
2	Verification of Kirchhoff's Laws – KVL and KCL	11-21	27-05-2021	31-05-2021	
3	Verification of Thevenin's and Norton's Theorem				
4	Measurement of AC System quantities – Average, RMS, Form Factor, Peak Factor, P, Q, pf				
5	Measurement of Self, Mutual and Coefficient of Coupling				
6	V-I Characteristics of P- N Junction and Zener Diode				
7	Half-wave Diode Rectifier				
8	Full-wave Diode Rectifier				
9	Transient analysis of RL, RC and RLC Circuits				
10	Digital Gate Circuits				

### **Experiment 1**

#### **Verification of Ohms Law**

- 1. **Aim**: To verify Ohms Law for the given circuit
- 2. **Software tools required:** MATLAB/SIMULINK
- 3. <u>Simulink Block sets Used</u>: Powergui, DC Voltage Source, Series RLC Branch, Current Measurement, Voltage Measurement, Display, Scope, XY Graph, Controlled Voltage Source, Ramp, Group 1 signal builder
- 4. **Theory**: Ohms Law states that the voltage across conducting materials is directly proportional to the current through the material. one arrives at the usual mathematical equation that describes this relationship

Where, V – Voltage across the element

- I Current flowing through the element
- R Resistance offered by the element

R is also the slope of the straight line when V-I characteristics are plotted. Normally resistance is a positive quantity.

5. <u>Circuit Diagram</u>: The considered circuit for Ohms law verification is as given in fig. 1a. The connected circuit in MATLAB/Simulink is given in Fig.1b.

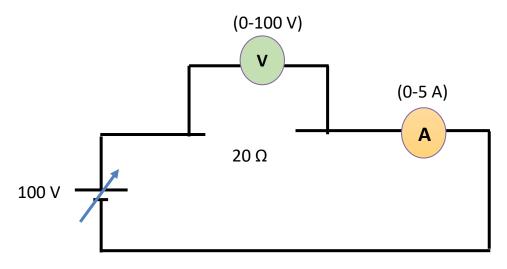


Fig1a: Circuit Diagram

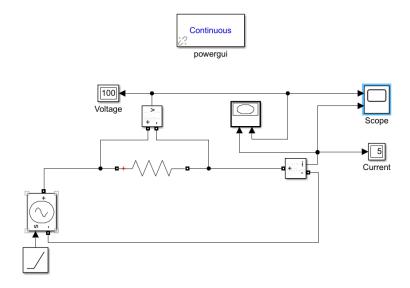


Fig1b: Circuit connections in Simulink

#### 6. **Procedure:**

- i. The mentioned Simulink blocksets are connected as shown in Figure 1b.
- ii. Apply the specified voltage across the specified resistance
- iii. Measure the current flowing through the resistor
- iv. V-t, I-t and V-I plots are generated
- v. The same procedure is repeated for specified types of inputs like Constant DC, Ramp, etc.

#### 7. **Graphical Results:**

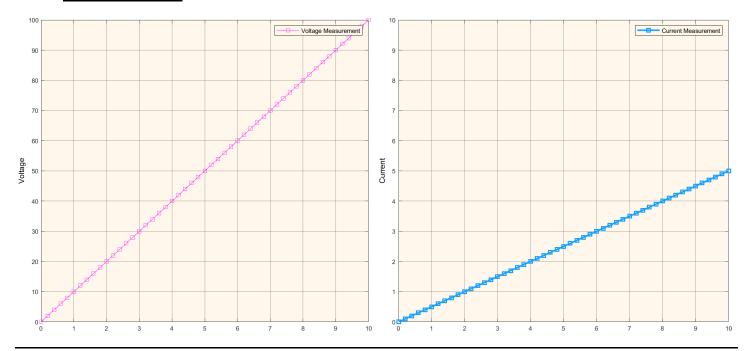


Fig.1c: Voltage Vs Time and Current Vs time Plots

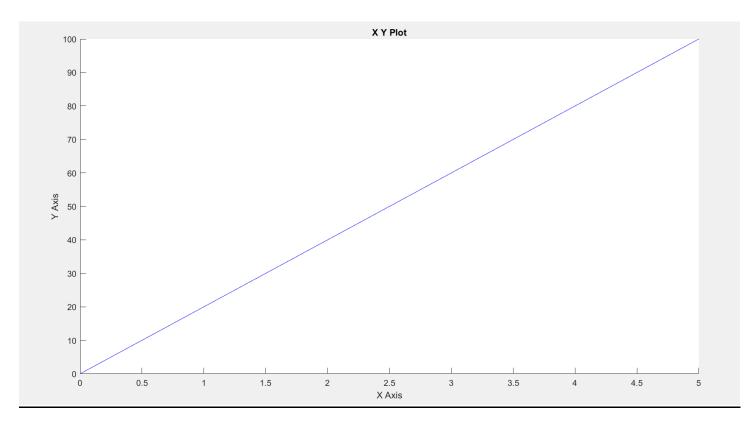


Fig1d: V-I Characteristics

#### 8. **Precautions:**

- a) Ensure that 'Powergui' block set is included in the Simulink file.
- b) Ensure that connections are properly made.
- c) Ensure that the scale of the graphs should be adjusted to the range in which the readings vary.
- 9. <u>Inferences</u>: From the output, it can be inferred that as the input ramp is varied from 0-100 V, the current through the resistance varies from 0-5 A.
- 10. **Conclusion:** The Ohms law is verified for all the specified inputs for the studied resistive network.

#### **Assignment:**

#### a. Consider the below Step function as input with $R = 5\Omega$

 $V(t) = 50V \qquad 0 \le t \le 5 \text{ sec}$  $= -50V \qquad 5 \le t \le 10 \text{ sec}$ 

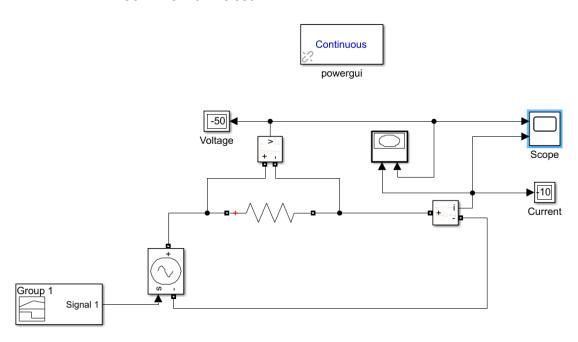


Fig1e: Circuit connections in Simulink

#### **Procedure:**

- 1. The mentioned Simulink blocksets are connected as shown in Figure 1e.
- 2. Connect the Group 1 signal builder with the controlled voltage source to apply the specified voltage across the specified resistance.
- 3. Measure the current flowing through the resistor.
- 4. V-t, I-t and V-I plots are generated.

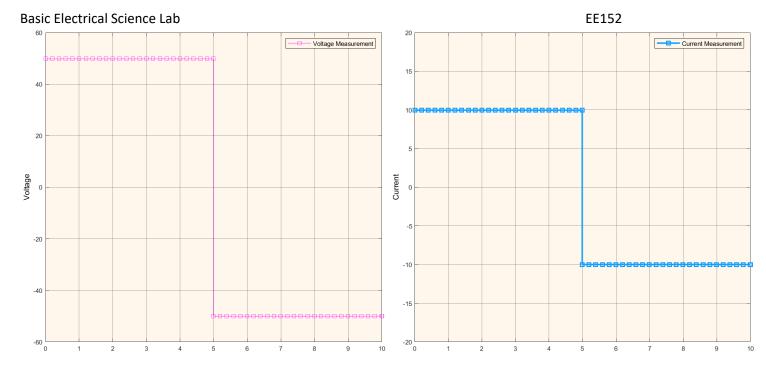


Fig.1f: Voltage Vs Time and Current Vs time Plots

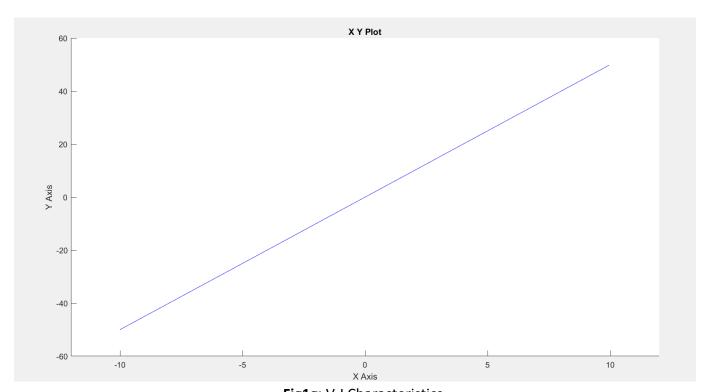


Fig1g: V-I Characteristics

<u>Inferences:</u> From the output, it can be inferred that, as the input voltage is fixed at 50V in first half of simulation, the current remained fixed at 10A and in the second half as the input voltage is fixed at -50V the current remained fixed at -10A, keeping the V/I ratio constant throughout the simulation.

b. Consider the Ramp function varying from 0-200 V as input with R =  $50\Omega$ 

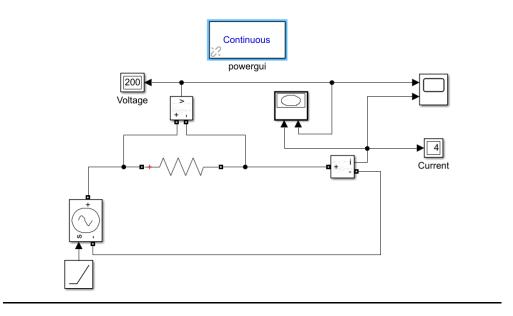


Fig1h: Circuit connections in Simulink

#### Procedure:

- 1. The mentioned Simulink blocksets are connected as shown in Figure 1h.
- 2. Connect the ramp blockset with the controlled voltage source to apply the specified voltage across the specified resistance.
- 3. Measure the current flowing through the resistor.
- 4. V-t, I-t and V-I plots are generated.

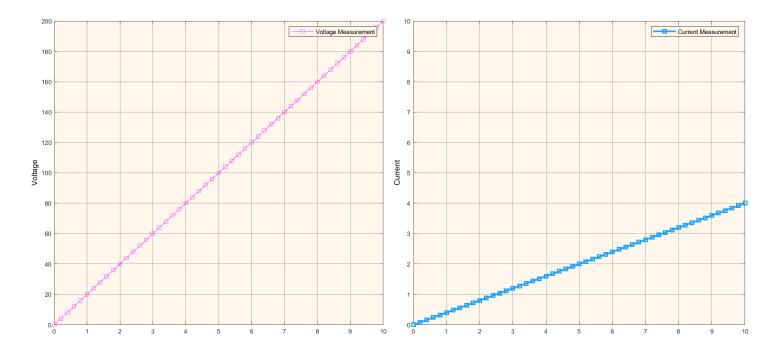


Fig:1i: Voltage Vs Time and Current Vs time Plots

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EF152

X Y Plot

180

160

140

120

80

60

40

20

20

X Y Axis

Fig1j: V-I Characteristics

<u>Inferences</u>: From the output, it can be inferred that as the input ramp is varied from 0-200 V, the current through the resistance varies from 0-4 A.

EE152

#### Verification of Kirchhoff's Laws - KVL and KCL

- 1. Aim: To verify Kirchoff's voltage law and Kirchoff's current law for the given circuit.
- 2. Software tools required: MATLAB/SIMULINK
- 3. <u>Simulink Block sets Used</u>: Powergui, DC Voltage Source, Series RLC Branch, Current Measurement, Voltage Measurement, Display, Scope, XY Graph, Controlled Voltage Source, Ramp, Group 1 signal builder,
- 4. <u>Theory:</u> Kirchoff's voltage law states that the algebraic sum of the potential differences in any loop must be equal to zero. Mathematically,  $\Sigma V = 0$  where V is the potential difference between a loop element. KVL deals with conservation of energy.
  - Kirchoff's current law states that current entering a node is equal to current leaving the node. Mathematically,  $\Sigma I = 0$ , where I is the current entering the node from a particular direction.
- 5. <u>Circuit Diagram</u>: The considered circuit for Kirchoff Voltage law verification is as given in fig. 2a. The considered circuit for Kirchoff Current law verification is as given in fig. 2b. The connected circuit of KVL and KCL in MATLAB/Simulink is given in Fig.2c and Fig.2d.

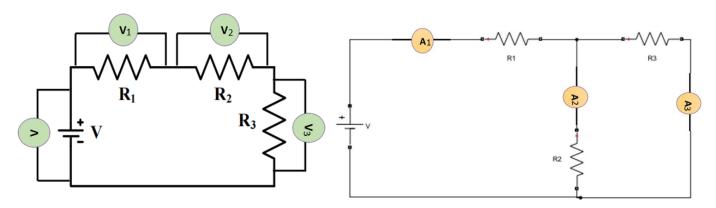


Fig2a: Circuit Diagram for KVL

Fig2b: Circuit Diagram for KCL

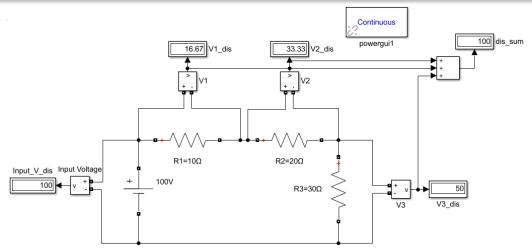


Fig2c: Circuit connections in Simulink for KVL

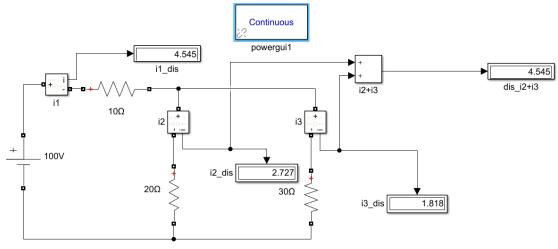


Fig2d: Circuit connections in Simulink for KCL

#### 6. Procedure:

- a. Convert the circuit shown in Fig. 2 into experimental circuit (necessary measuring instruments are to be incorporated in the circuit).
- b. Construct the experimental circuits in MATLAB/Simulink domain, and simulate it.
- c. Based on the simulation, fill up the Table-2.1 for KVL. Similarly, prepare a table for KCL experiment, and fill it.

#### 7. Observations:

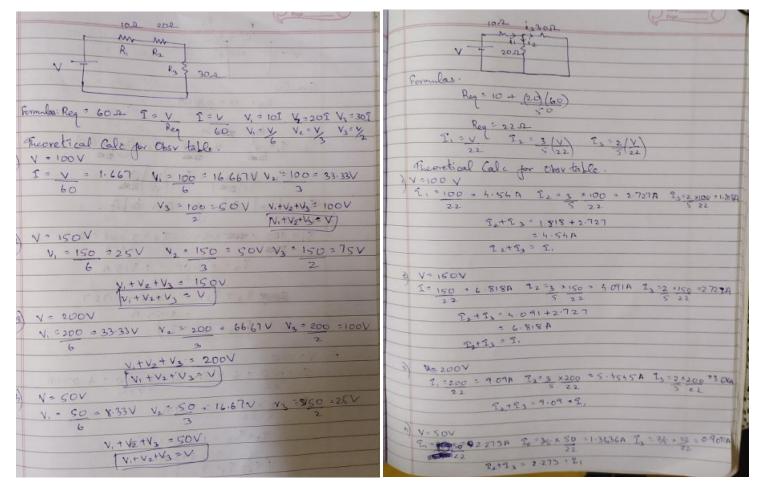
	Applied Voltage V (volts)	Voltage across R <sub>1</sub> (volts) (V <sub>1</sub> )		Voltage across R <sub>2</sub> (volts) (V <sub>2</sub> )		Voltage acros	- ( )	V <sub>1</sub> +V <sub>2</sub> +V <sub>3</sub> (volts)		
Observation No.		Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
1	100	16.67	16.67	33.33	33.33	50	50	100	100	
2	150	25	25	50	50	75	75	150	150	
3	200	33.33	33.33	66.67	66.67	100	100	200	200	
4	50	8.33	8.33	16.67	16.67	25	25	50	50	

Table 2.1: Observation table for KVL

	Applied Voltage	Current through R <sub>1</sub> i1 (Amperes)		Current through R2 i2 (Amperes)		Current the		i2+i3 (Amperes)		
Observation No.	V (volts)	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
1	100	4.545	4.545	2.727	2.727	1.818	1.818	4.545	4.545	
2	150	6.818	6.818	4.091	4.091	2.729	2.729	6.818	6.818	
3	200	9.091	9.091	5.455	5.455	3.636	3.636	9.091	9.091	
4	50	2.273	2.273	1.364	1.364	0.9091	0.9091	2.273	2.273	

Table 2.2: Observation table for KCL

#### 8. Theoretical Calculation Working:



#### 9. Precautions:

- a) Ensure that 'powergui' block set is included in the Simulink file.
- b) Ensure that connections are properly made.
- c) Ensure that the scale of the graphs should be adjusted to the range in which the readings vary.

#### 10. Inferences:

- From the observation table 2.1, it can be inferred that sum of V1+V2+V3 is always equal to V.
- From the observation table 2.2, it can be inferred that sum of i2+i3 is always equal to i1.
- All the theoretical readings match with the simulated readings.

#### 11. Conclusion:

• Kirchoff's voltage law and Kirchoff's current law are hence verified.

#### **Assignment:**

1. Replace constant voltage source by constant current source with the same magnitude in Fig. 2.a & 2.b, do the simulation again.

#### **Circuit Diagram:**

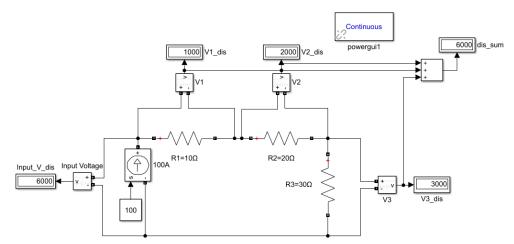


Fig2e: Circuit connections in Simulink for KVL with constant current source

#### **Observations:**

Current Source		Voltage across Current Source V (kVolts)		Voltage across R1 V1 (kVolts)		Voltage across R2 V2 (kVolts)			across R3 Volts)	V1+V2+V3 (kVolts)		
No.	input I (Amperes)	Theoretical	Simulation	Theoretical	Simulation	Theoretical	Simulation	Theoretical	Simulation	Theoretical	Simulation	
1	100	6	6	1	1	2	2	3	3	6	6	
2	150	9	9	1.5	1.5	3	3	4.5	4.5	9	9	
3	200	12	12	2	2	4	4	6	6	12	12	
4	50	3	3	0.5	0.5	1	1	1.5	1.5	3	3	

Table 2.3: Observation table for KVL using constant current source

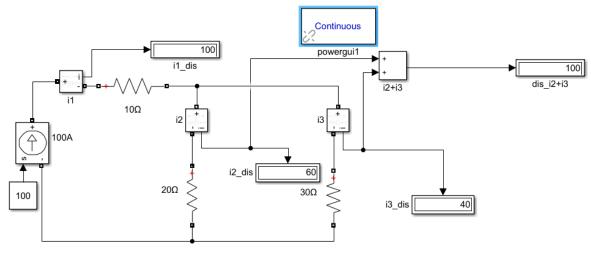


Fig2f: Circuit connections in Simulink for KCL with constant current source

#### **Observations:**

	Current Source input I (Amperes)	Current through R <sub>1</sub> i1 (Amperes)		Current the		Current the		i2+i3 (Amperes)	
Observation No.		Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated
1	100	100	100	60	60	40	40	100	100
2	150	150	150	90	90	60	60	150	150
3	200	200	200	120	120	80	80	200	200
4	50	50	50	30	30	20	20	50	50

**Table 2.4:** Observation table for KCL using constant current source

#### **Inferences:**

- From the observation table 2.3, it can be inferred that sum of V1+V2+V3 is always equal to V.
- From the observation table 2.4, it can be inferred that sum of i2+i3 is always equal to i1.
- All the theoretical readings match with the simulated readings.
- KCL and KVI is verified using constant current source.

2. Replace constant voltage source by variable voltage source (sinusoidal source with the same magnitude, ramp input with slope 1) in Fig. 2.a & 2.b, do the simulation again.

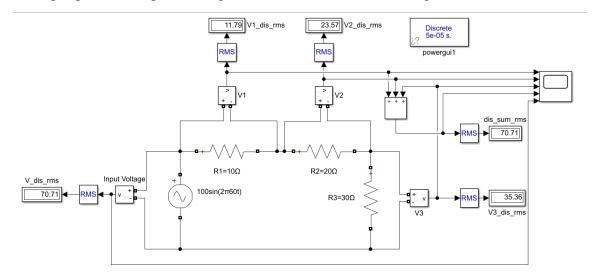
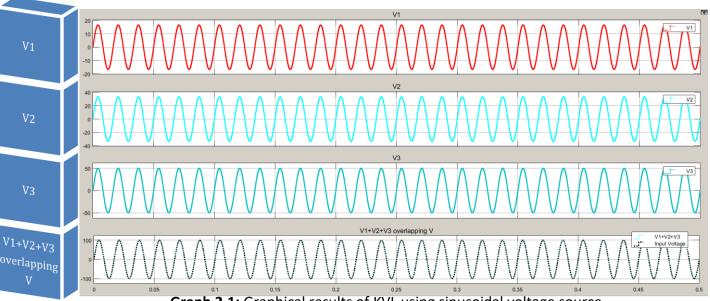


Fig2g: Circuit connections in Simulink for KVL using sinusoidal voltage source

Observation	Input Voltage	V RMS (Volts)		RMS Voltage across R1 V1 (Volts)		RMS V acros V2 (V	s R2	RMS V acros V3 (V	s R3	V1+V2+V3 (Volts)	
No.	V (Volts)	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated
1	100sin(2π60t)	70.71	70.71	11.79	11.79	23.57	23.57	35.36	35.36	70.71	70.71
2	200sin(2π60t)	141.4	141.4	23.57	23.57	47.14	47.14	70.17	70.17	141.4	141.4
3	150sin(2π60t)	106.1	106.1	17.68	17.68	35.36	35.36	70.71	70.71	106.1	106.1
4	50sin(2π60t)	35.36	35.36	5.893	5.893	11.79	11.79	17.68	17.68	35.36	35.36

Table 2.5: Observation table for KVL using sinusoidal voltage source



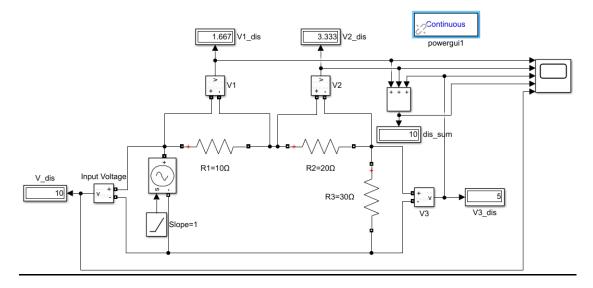


Fig2h: Circuit connections in Simulink for KVL using variable voltage source with ramp

Observation No.	Input Voltage	Voltage V (Volts)		Voltage across R1 at t=5s V1 (Volts)		Voltage across R2 at t=5s V2 (Volts)		Voltage a at t V3 (V	=5s	V1+V2+V3 at t=5s (Volts)		
110.	V slope Theoretical Simulate		Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
1	1	5	5	0.833	0.833	1.677	1.677	2.5	2.5	5	5	
2	2	10	10	1.667	1.667	3.33	3.33	5	5	10	10	
3	3	15	15	2.5	2.5	5	5	7.5	7.5	15	15	
4	4	20	20	3.33	3.33	6.667	6.667	10	10	20	20	

Table 2.6: Observation table for KVL using variable voltage source with ramp

Graph 2.2: Graphical results of KVL using variable voltage source using ramp

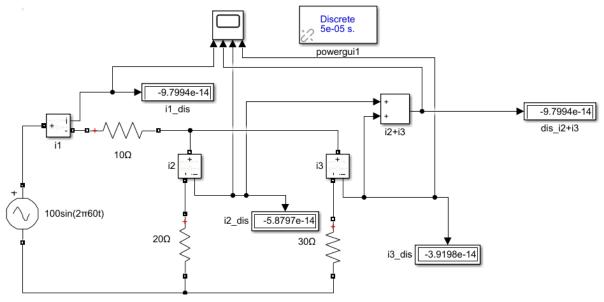
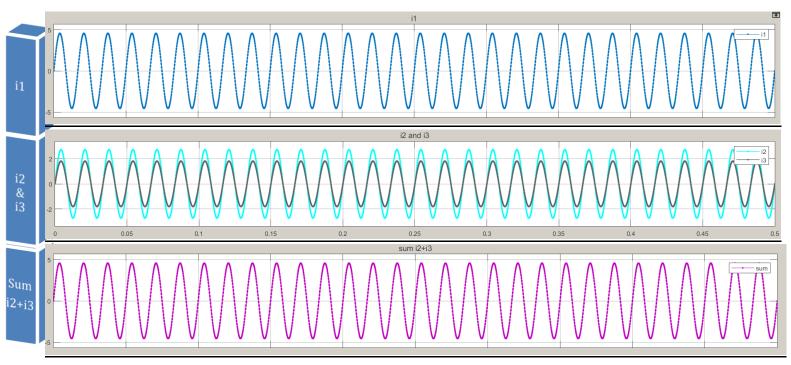


Fig2i: Circuit connections in Simulink for KCL with sinusoidal voltage source

	Current Source input I (Amperes)	Current through R <sub>1</sub> i1 RMS (Amperes)		Current thr i2 RMS (A		Current the i3 RMS (A		i2+i3 RMS (Amperes)		
Observation No.		Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
1	100sin(2π60t)	3.214	3.214	1.928	1.928	1.286	1.286	3.214	3.214	
2	150sin(2π60t)	4.821	4.821	2.893	2.893	1.928	1.928	4.821	4.821	
3	200sin(2π60t)	6.428	6.428	3.857	3.857	2.571	2.571	6.428	6.428	
4	50sin(2π60t)	1.607	1.607	0.9642	0.9642	0.6428	0.6428	1.607	1.607	

Table 2.7: Observation table for KCL using sinusoidal current source



**Graph 2.3:** Graphical results of KCL using sinusoidal voltage source

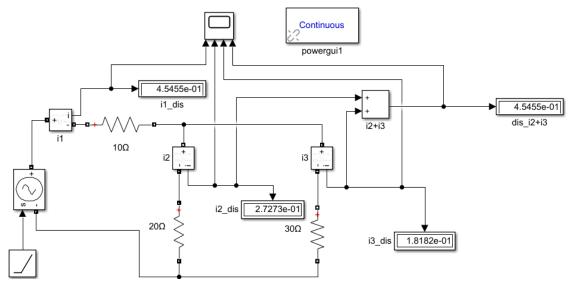
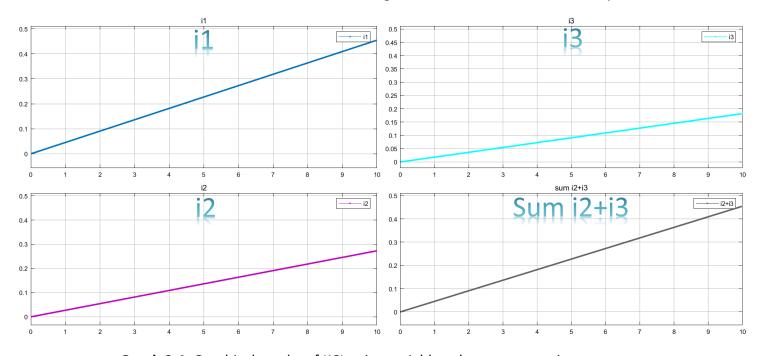


Fig2j: Circuit connections in Simulink for KCL using variable voltage source with ramp

	Current Source input	Current through R <sub>1</sub> i1 (Amperes) at t=5s		Current thi i2 (Ampere		Current the		i2+i3 (Amperes) at t=5s		
Observation No.	I (Ramp Slope)	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
1	1	0.2273	0.2273	0.1364	0.1364	0.09031	0.09031	0.2273	0.2273	
2	2	0.4545	0.4545	0.2727	0.2727	0.1818	0.1818	0.4545	0.4545	
3	3	0.6818	0.6818	0.4091	0.4091	0.2727	0.2727	0.6818	0.6818	
4	4	0.9091	0.9091	0.5455	0.5455	0.3636	0.3636	0.9091	0.9091	

Table 2.8: Observation table for KCL using variable current source with ramp



Graph 2.4: Graphical results of KCL using variable voltage source using ramp

<u>Inferences</u>: From the observation table 2.5 & 2.6, it can be inferred that sum of V1+V2+V3 is always equal to V.

- From the observation table 2.7 & 2.8, it can be inferred that sum of i2+i3 is always equal to i1.
- All the theoretical readings match with the simulated readings.
- KCL and KVI is verified using variable voltage source such as voltage with constant slope and sinusoid voltage

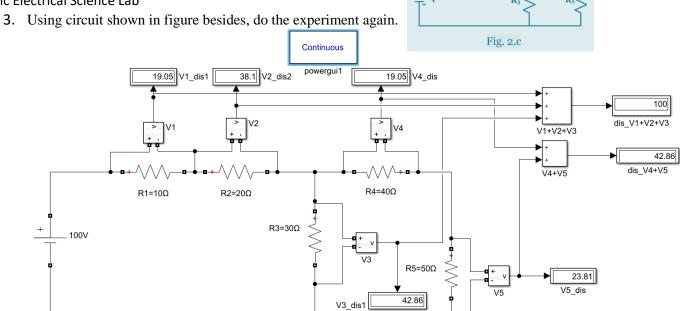


Fig2k: Circuit connections in Simulink for KVL

	Applied Voltage V (Volts)	Voltage across R1 V1 (Volts)		Voltage ac V2 (Vo		Voltage ac R3 (Vo		V1+V2+V3 (Volts)		
Observation No.		Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
Ĩ	100	19.05	19.05	38.1	38.1	42.86	42.86	100	100	
2	150	28.57	28.57	57.14	57.14	28.57	28.57	150	150	
3	200	38.1	38.1	76.19	76.19	85.71	85.71	200	200	
4	50	9.524	9.524	19.05	19.05	21.43	21.43	50	50	

Table 2.9: Observation table for KVL for first loop

	Applied Voltage V (Volts)	Voltage across R3 V3 (Volts)		Voltage across R4 V4 (Volts)		Voltage ac R5 (Vo		V4+V5 (Volts)		
Observation No.		Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	
Ĩ	100	42.86	42.86	19.05	19.05	23.81	23.81	42.86	42.86	
2	150	28.57	28.57	57.14	57.14	28.57	28.57	□150	150	
3	200	64.29	64.29	28.59	28.59	35.71	35.71	64.29	64.29	
4	50	21.43	21.43	9.524	9.524	11.9	11.9	21.43	21.43	

Table 2.10: Observation table for KVL for second loop

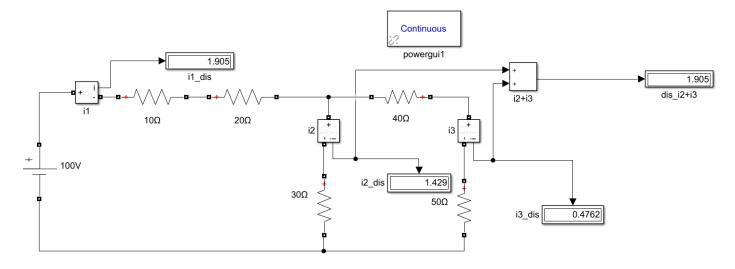


Fig2I: Circuit connections in Simulink for KCL

Observation No.	Applied Voltage V (Volts)	Current through R1 & R2 i1 (Amperes)		Current through R3 i2 (Amperes)		Current through R4 & R5 i3 (Amperes)		i2+i3 (Amperes)	
		Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated	Theoretical	Simulated
ĩ	100	1.905	1.905	1.429	1.429	0.4762	0.4762	1.905	1.905
2	150	2.857	2.857	2.143	2.143	0.7143	0.7143	2.857	2.857
3	200	3.81	3.81	2.851	2.851	0.9524	0.9524	3.81	3.81
4	50	0.9524	0.9524	0.7143	0.7143	0.2381	0.2381	0.9524	0.9524

Table 2.11: Observation table for KCL using constant voltage source for ckt fig

#### Inferences:

- From the observation table 2.9, it can be inferred that sum of V1+V2+V3 is always equal to V.
- From the observation table 2.10, it can be inferred that sum of V4+V5 is always equal to V3.
- From the observation table 2.11, it can be inferred that sum of i2+i3 is always equal to i1.
- All the theoretical readings match with the simulated readings.
- KCL and KVL is verified for the given circuit.