

# System Software - Machine Architecture.

- SIC - RISC
- SIC/XE - CISC

## - SIC

- Memory.

- $2^{15} \rightarrow 15\text{-bit address}$

- Registers

- A, X, L, PC, SW

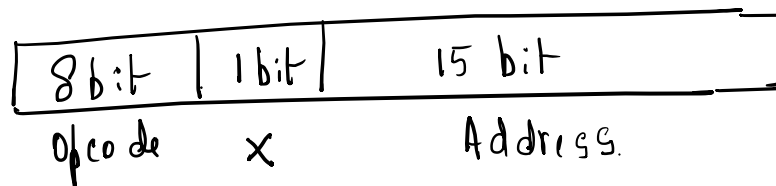
- Data formats

- Integers, Characters

24: Word length.

- Instruction format.

- 24-bit in length



- Addressing modes

- $\rightarrow$  Direct Addressing.

- $\rightarrow X = 0$

- EA = Address mentioned in the

# Addressing field.

## - Indexed Addressing

$$\rightarrow X=1$$

$$EA = [X] + \text{Address field.}$$

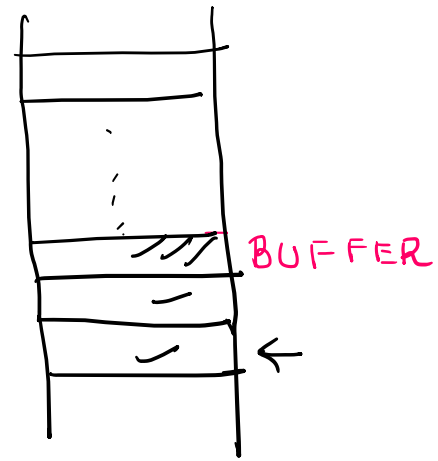
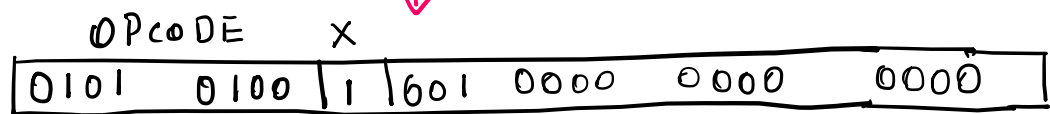
STCH  
54

BUFFER, X.

→ Indexed addressing

→ Direction given to the assembler to use indexed addressing

Assembler



5      4      9      0      0      0

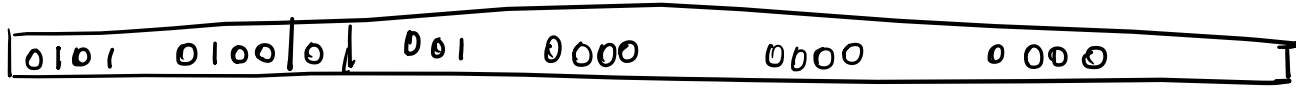
STCH

Indexed.

Address.

Store the character

$$EA = 1000 + [X]$$



# STCH BUFFER

## - Instruction set

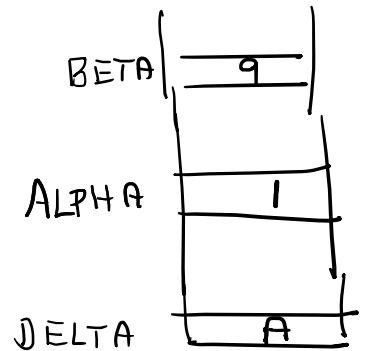
### - (Integer) arithmetic instructions

- ADD
- SUB
- MUL
- DIV

} A

ADD ALPHA

$$(A) \leftarrow (A) + (ALPHA)$$



$$DELTA = ALPHA + BETA$$

ADD DELTA, ALPHA, BETA

## - Load and store.

- LDA, STA
- LDX, STX
- LDCH, STCH

LDA BETA  $A \leftarrow 9$

ADD ALPHA  $A \leftarrow \frac{9+1}{10}$

STA DELTA  $DELTA \leftarrow A$

## - Comparison instruction.

- A  $\rightarrow$  operand.

CMP ALPHA

if  $(ALPHA > A)$

$< A$

$= A$

CC 

EQ	LT	GT	---
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## - Conditional Jump instructions Branch.

- JLT, JGT, JEQ.

While ( )

- J

(Repeat)

## - Subroutine

- JSUB.

- RSUB.

## - Input and Output

- Device is ready.

DEV1

TD  
WD | RD.

EQ. Read TD DEV1  
JEQ Read.  
RD DEV1

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A

WRITE TD DEV2  
JEQ WRITE  
WD DEV2

# SIC/XE - Machine Architecture.



## - Memory

- 24 bit

-  $2^{20}$  bytes

$2^{15}$

## - Registers

A	0
X	1
L	2.
PC	8
SW	9.

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B	3
---	---

S	4.
---	----

T	5
---	---

F	6
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(48 bit)

Base register } Relation-  
Addressing

} General  
Working register.

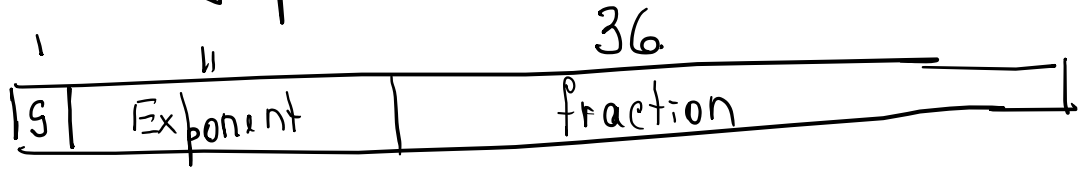
Floating point  
Accumulator.

## — Data formats

— Integers

— Character

— Floating point : 48 bit



## — Instruction formats

— 4 types of instruction formats.