Week 7: Assignment Solutions

1. In 6-bit 2's complement representation, when we subtract the decimal number +6 from +3, the result (in binary) will be:
   a. 111101
   b. 000011
   c. 100011
   d. 111110

   Correct answer is (a).

   Subtracting +6 from +3 is the same as adding the 2's complement of 6 to 3.

   +3: 000011

   -6 (in 2's complement): 111010

   111101

2. For a straightforward two-level implementation (with NOT gates required to invert input variables) of a full adder using AND, OR and NOT gates only, the number of gates required will be ……..

   Correct answer is 12.

   The carry function AB + BC + CA would require 3 AND gates and 1 OR gate.

   The sum function A'B'C + A'BC' + AB'C' + ABC will require 3 NOT gates for complementing the variables, 4 AND gates to generate the product terms, and 1 OR gate to combine them.

   The total number of gates is 3 + 1 + 3 + 4 + 1 = 12.

3. Suppose that the carry output of a full adder is implemented in two-level gate realization using NAND gates only. Assume that the propagation delay of a 2-input gate is 1 nsec, and that of a 3-input gate is 1.5 nsec. The total propagation delay to generate the carry will be ……. nsec.

   Correct answer is 2.5.

   Two-level AND-OR is equivalent to two-level NAND-NAND. In first level we shall have three 2-input NAND gates in parallel, and in the second level there will be one 3-input NAND gate.

   Total delay will be 1 nsec + 1.5 nsec = 2.5 nsec

4. Assume that for a full adder implementation, the delay for sum and carry generation are 6 nsec and 4 nsec respectively. The worst-case delay of a 16-bit ripple carry adder will be:
   a. 96 nsec
   b. 64 nsec
   c. 66 nsec

d. None of the above

Correct answer is (c).

The carry will ripple through the 16 stages, and so the carry propagation time = 16 x 4 = 64 nsec.

In the last adder, generation of sum will require 2 nsec more that generation of carry. So the worst-case delay will be 64 + 4 = 66 nsec.

5. For a full adder stage FA_i in a carry look-ahead adder, which of the following statements are false?
   a. The carry generate function G_i will be 1 if both the inputs A_i and B_i are 1.
   b. The carry propagate function P_i will be 1 if at least one of the inputs A_i and B_i are 1.
   c. The carry generate function G_i will be 1 if exactly one of the inputs A_i and B_i are 1.
   d. None of the above.

   Correct answers are (b) and (c).

   The carry generate function is defined as $G_i = A_i.B_i$

   The carry propagate function is defined as $P_i = A_i$ xor B_i

   The answer follows from the function definitions.

6. Suppose we are using 4-bit carry lookahead adder modules to build a 64-bit adder with two-level carry lookahead, with ripple carry between the modules. If the delay of a basic gate (AND, OR, NOT) is 2 nanoseconds, the worst-case delay of the 64-bit adder will be …….. nanoseconds.

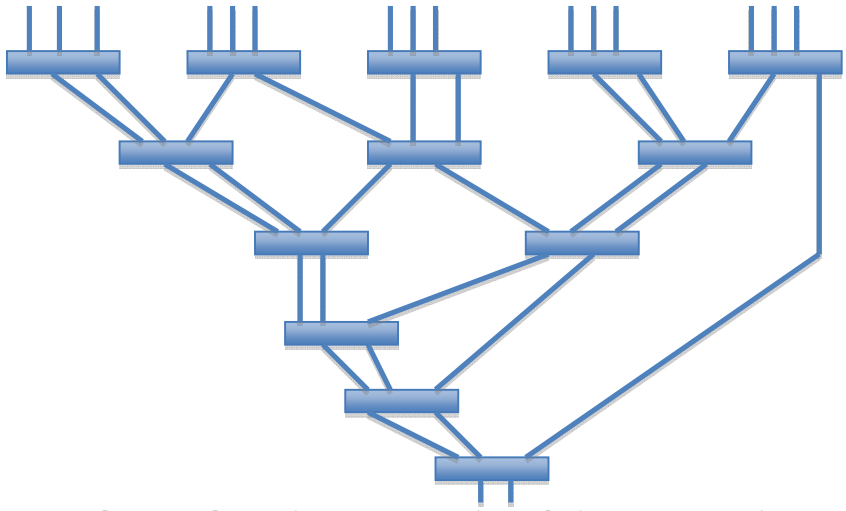
   Correct answer is 24.

   Basic gate delay δ = 2 nsec
   Delay of the 2-level 64-bit carry lookahead adder will be
   $T_{CLA} = (6 + 2 \text{ ceiling}\{\log_4 64\}) \delta = 12 \delta$
   $= 12 \text{ x } 2\text{nsec} = 24 \text{ nsec}$

7. Suppose that we are adding 15 32-bit numbers using 32-bit carry save adder modules and a parallel adder in the last stage of the computation. The minimum number of carry save adders required will be:
    a. 15
    b. 18
    c. 16
    d. 13

    Correct answer is (d).

    Each carry save adder can be used to add a maximum of 3 numbers, and generates 2 numbers as output (a sum word and a carry word).



8. When two 8-bit numbers (A7 A6 … A0) and (B7 B6 … B0) in 2's complement representation (with A0 and B0 as the least significant bits) are added using ripple carry adder, the sum bits obtained are (S7 S6 … S0) and the carry bits are (C7 C6 … C0). An overflow is said to have occurred if:
    a. The carry bit C7 is 1
    b. All the carry bits (C7 C6 … C0) are 1
    c. A7.B7.S7' + A7'.B7'.S7 is 1
    d. A0.B0.S0' + A0'.B0'.S0 is 1

    Correct answer is (c).

    Overflow occurs only when both the numbers are positive or both the numbers are negative, and the sign of the sum gets reversed. Condition (c) states this situation.

9. Why does the MIPS32 architecture does not have any status flags?
    a. It helps in efficient pipeline implementation.
    b. A dedicated register is used to store the status flags.
    c. The status flags are embedded in the instruction encoding.
    d. None of the above.

Correct answer is (a).

In a pipeline implementation, there are several instructions that are in various stages of execution. If there were flag register, we would require one such register for every instruction that is executing in some stage of the pipeline. Moreover, for branch and exception processing, situation becomes more complicated. Hence for ease of pipeline implementation, RISC architectures like MIPS32 do not have any status flags.

10. Which of the following are true for n-bit unsigned multiplication?
    a. The product is (n+1) bits long
    b. The product is 2n bits long
    c. The number of partial products is 2n
    d. The number of partial products is n^2

    Correct answers are (b) and (d).

    The number of bits of the product can be double the number of bits of the number being multiplied (e.g. in 3 bits, 111 x 111 = 110001).

    Every bit of the multiplier will generate a partial product with every bit of multiplicand; the total number will be square of the number of bits.

11. For the binary number 1100110111, the Booth encoding will be:
    a. 0 -1 0 +1 0 -1 0 0 -1
    b. 0 -1 0 +1 0 -1 0 0 0
    c. +1 0 -1 0 +1 0 -1 0 0
    d. None of the above

    Correct answer is (a).

    We take bits pairs (overlapping) from left to right and encode them as follows: 00 or 11 are encoded as 0, 10 is encoded as -1, and 01 is encoded as +1.

12. Which of the following statements are true?
    a. Booth's multiplier is faster than shift-and-add multiplier.
    b. Booth's multiplier with bit-pair recoding is faster than conventional Booth's multiplier.
    c. Carry-save multiplier is faster than Booth's multiplier.
    d. Carry-save multiplier is slower than Booth's multiplier.

    Correct answers are (a), (b) and (c).

    (a) is true since Booth's multiplier do not need addition for bit pairs 00 or 11 in the multiplier.

    (b) is true since bit-pair recoding is guaranteed to reduce the number of operations required.

    (c) is true as carry save multiplication is a combinational multiplier, which is much faster that Booth's multiplier that is based on sequential shift and add.

13. Which of the following is not true for restoring division algorithm?

a. A trial subtraction is carried out in each iteration, followed by a corrective addition if required.
b. A trial addition is carried out in each iteration, followed by a corrective subtraction if required.
c. The next quotient bit is set to 1 if the partial result is negative.
d. None of the above.

Correct answer is (b).

The answer follows from the basic algorithm of restoring division.

14. Which of the following statements are true?
    a. Non-restoring division is faster than restoring division.
    b. The correction step that is required in restoring division is eliminated in non-restoring division.
    c. For n-bit divisor and n-bot dividend, the number of restoring additions will be n/2 on the average.
    d. The data paths required for shift-and-add multiplication and restoring division are somewhat similar.

All the four answers are correct.

The answers directly follow from the restoring and non-restoring division algorithms.