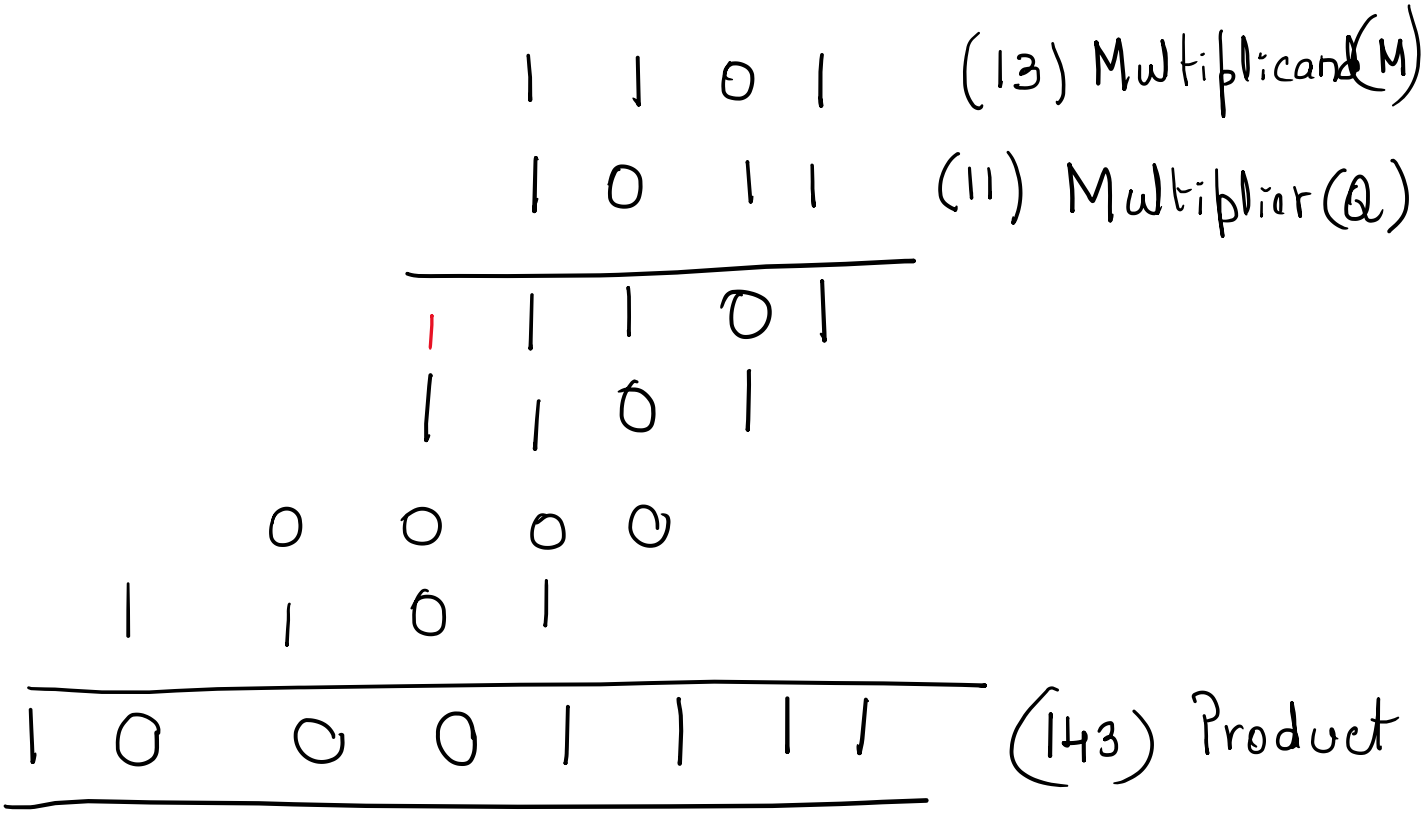
Multiplier for Positive/Unsigned Nos

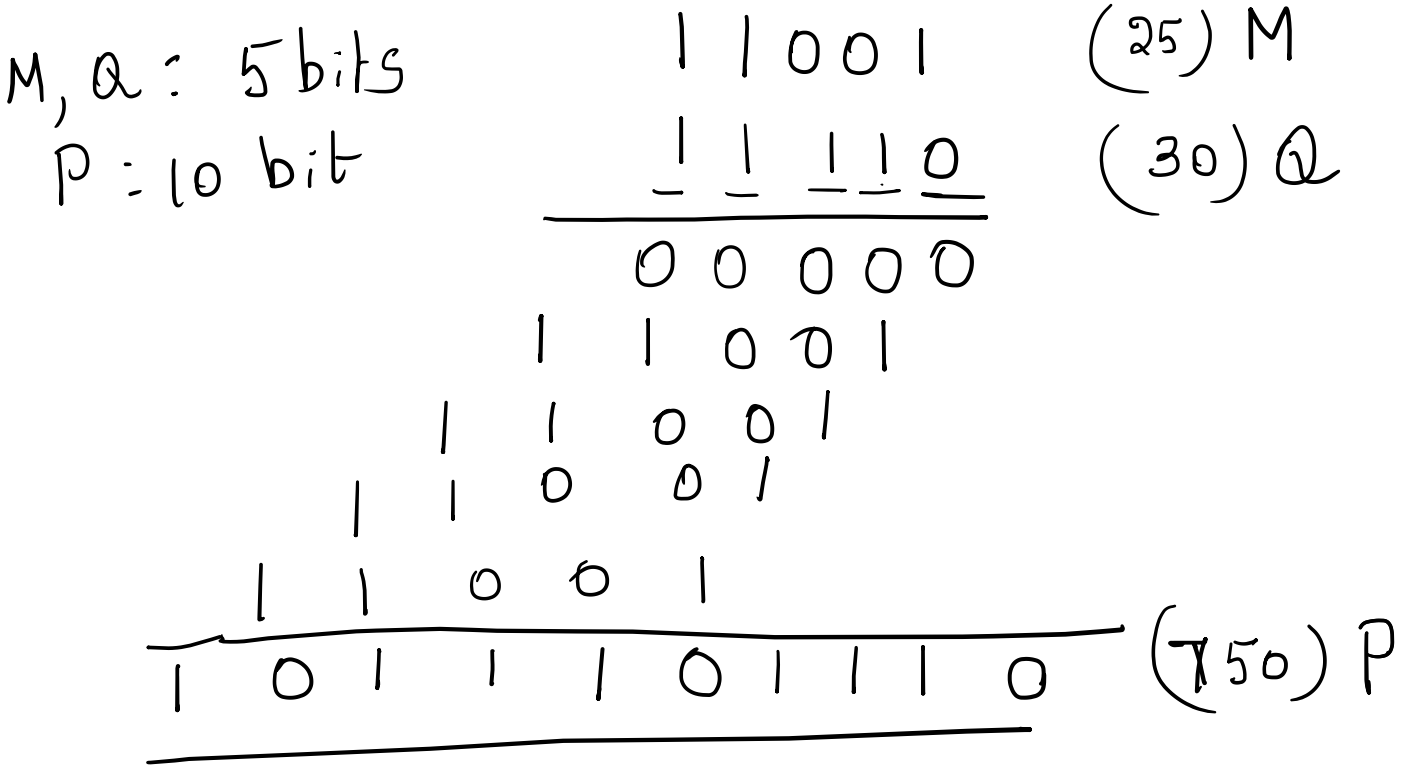


① M, Q : 4-bit numbers | n
P : 8-bit numbers | 2n-bits

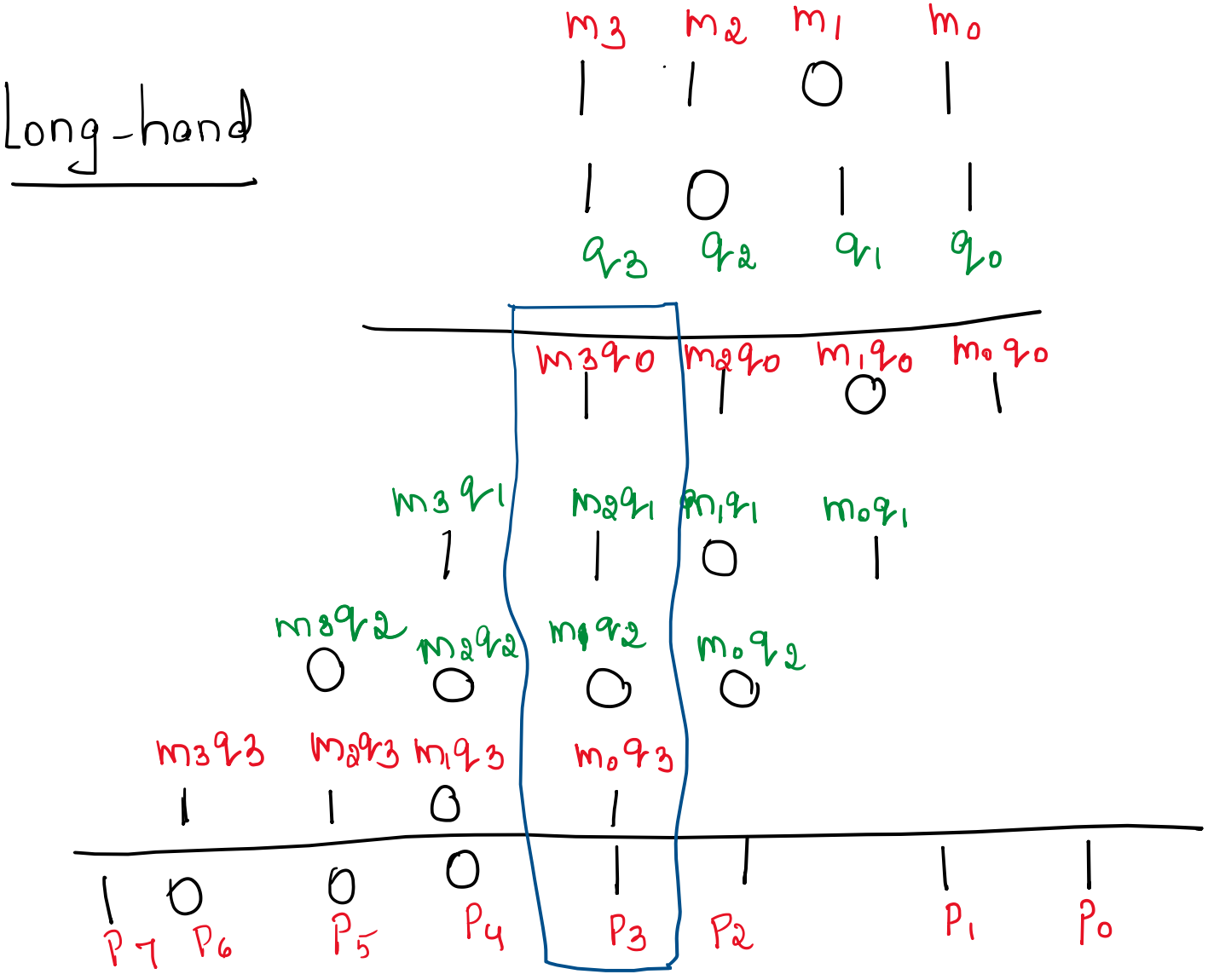
② Multiplier bit
= 1 Multiplicand – suitable shifting
= 0 " Not added.

M, Q : 5 bits

P : 10 bit



Long-hand



$P_0 = m_0 q_0$

$P_1 = m_1 q_0 + m_0 q_1$

$P_2 = m_2 q_0 + m_1 q_1 + m_0 q_2$

$P_3 = m_3 q_0 + m_2 q_1 + m_1 q_2 + m_0 q_3$

$P_4 = m_3 q_1 + m_2 q_2 + m_1 q_3$

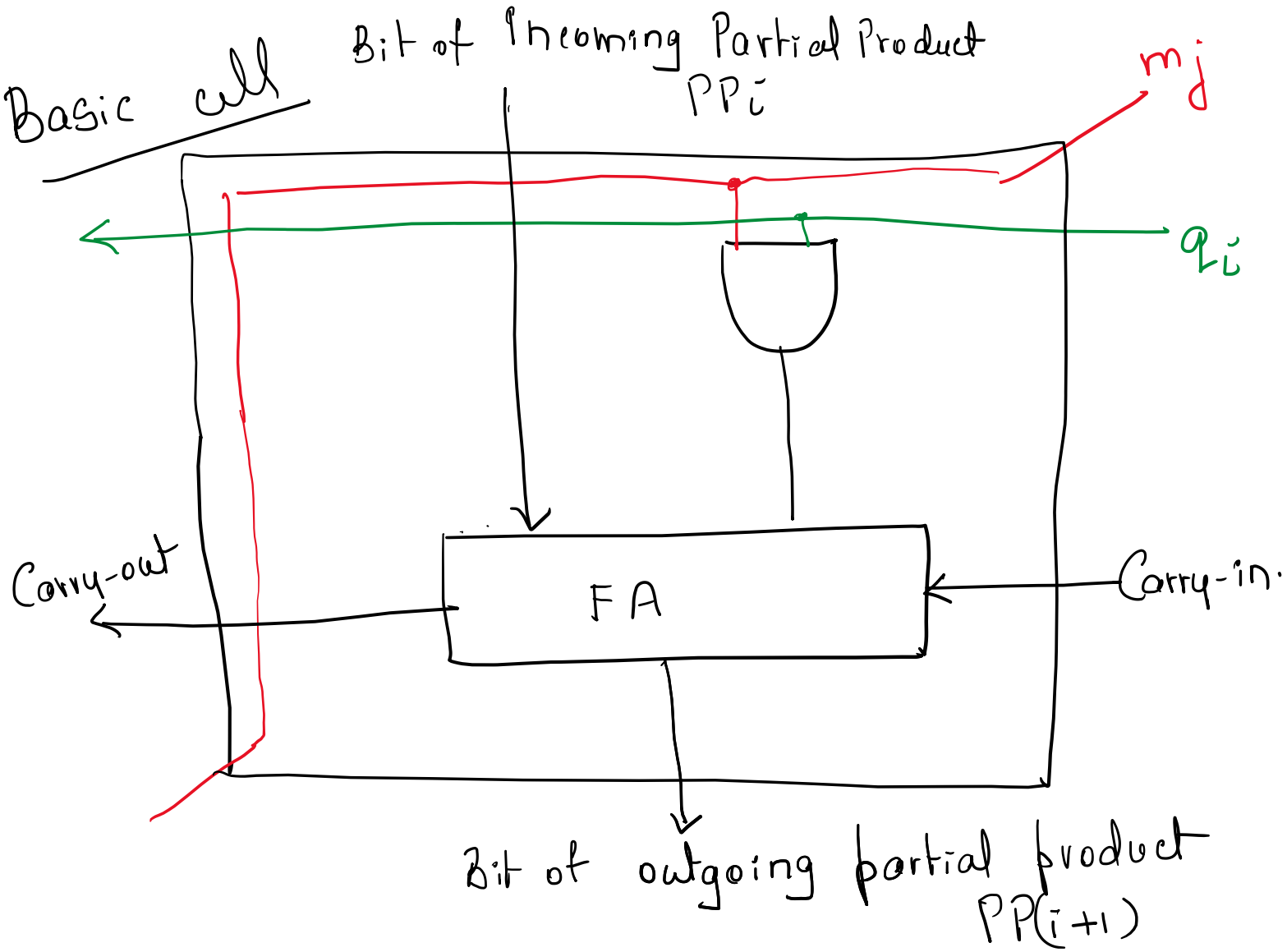
$P_5 = m_3 q_2 + m_2 q_3$

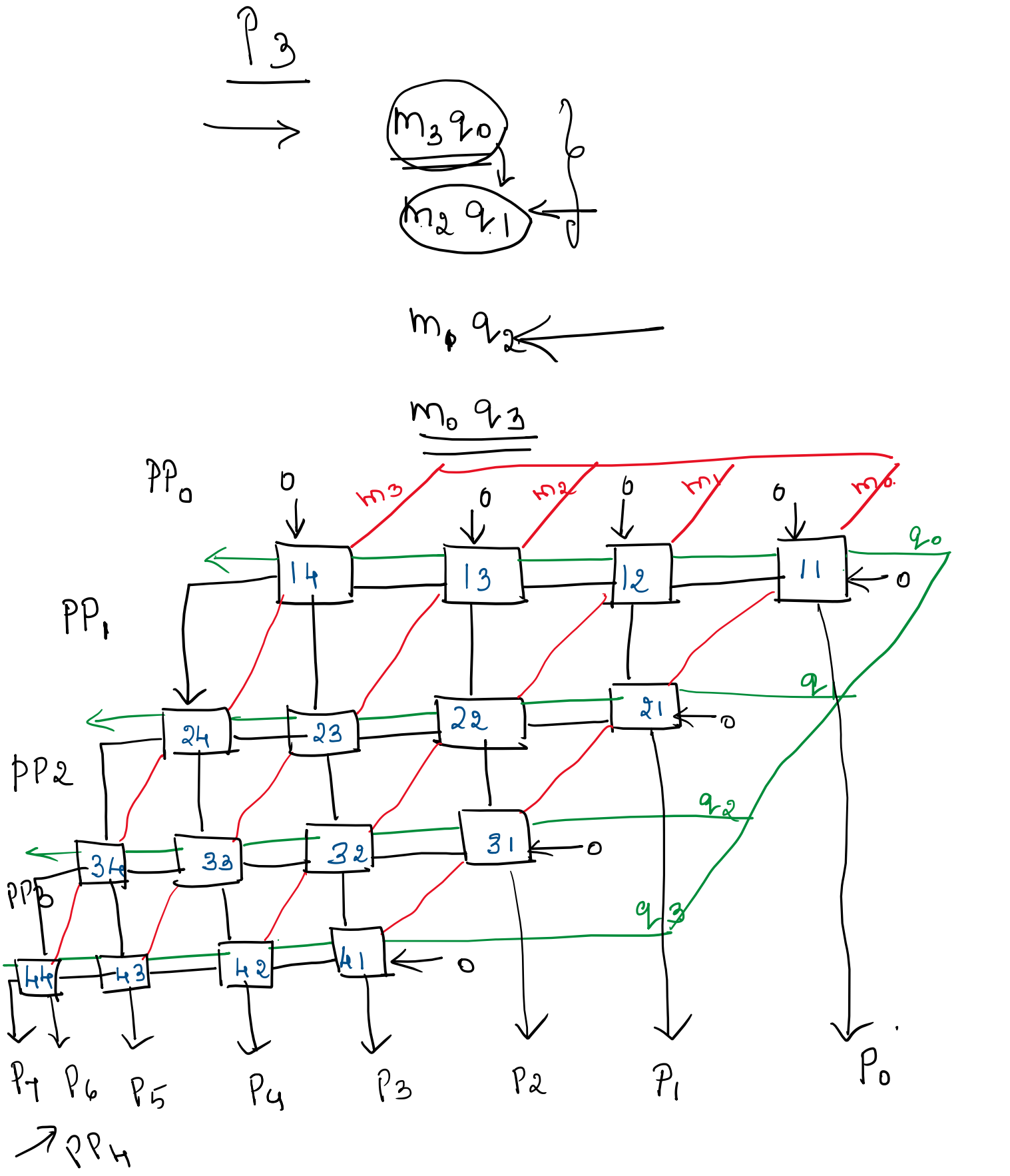
$P_6 = m_3 q_3$

P_7 = Carry-out

AND GATE

FULL ADDER





COMBINATIONAL ARRA MULTIPLIER

$q_i = 1$

Add multiplicand

Delay Computation

First row: Since all incoming PP bits, $PP_0 = 0$,

only AND gates needed:

→ 1 tpd. → (1)

→ 1 tpd → (A)

Rows 2 & 3: Cells 1 & 2 contribute to longest signal path

→ FA

n-2 rows

Each row: 4 tpd. → 2 × 2 = 4 tpd in each

No of rows = 2.

Total → 2 × 4 = 8 tpd.

↳ (2)

(n-2) 4 delay

↳ (B)

Last Row : RCA : 8 tpd. → (3)

n bit : 2n tpd. → (C)

Total delay = ① + ② + ③

1 + 8 + 8

= 17 tpd

Total delay: (A) + (B) + (C)

$= 1 + (n-2)4 + 2n$

$= 1 + 4n - 8 + 2n$

$= 6n - 7$

$= 6n - 6 - 1$

$= 6(n-1) - 1$

Observation

— Easy to understand

— Many gates

Mixture of combinational array technique and sequential technique

↳ less combinational logic

Combinational logic

Sequential logic