DSD - CSE - END SEM QP

ANSWER ALL QUESTIONS ; ALL QUESTIONS CARRY EQUAL MARKS

1> Using Boolean Algebra postulates and theorems, simplify each of the following expressions as disjunctive normal formulas with the fewest number of literals

a) $\bar{w}\bar{x}yz + wxy + \bar{w}\bar{y} + x\bar{y} + \bar{x}\bar{y}$

b) $(\overline{x + yz}) + \bar{y}z$.

2> Show that the 'NAND' operation is not associative i.e. $\text{nand}[x, \text{nand}(y, z)] \neq \text{nand}[\text{nand}(x, y), z]$ Is the nor-operation associative?

3> Using Q-M method and prime implicant chart determine a minimal sum of product for the following Boolean function

a) $f(w, x, y, z) = \Sigma m(3, 4, 5, 7, 10, 12, 14, 15) + dc(2)$

b) $f(w, x, y, z) = \Sigma m(7, 9, 12, 13, 14, 15) + dc(4, 11)$

4> Using K-map simplify the following expressions.

a) $f(v, w, x, y, z) = \Pi M(0, 2, 4, 6, 8, 12, 14, 15, 16, 18, 20, 22, 30 + 31)$

b) $f(w, x, y, z) = \Pi m(0, 3, 4, 11, 13) + dc(2, 6, 8, 9, 10$

5> Realize the Boolean expression

$$f(w, x, y, z) = \Sigma m(4, 5, 7, 8, 10, 12, 15)$$

using a 4-to-1-line multiplexer and external gates.

a> Let w and x appear on select lines S_1 & S_0

b> Let y, z appear on select lines S_1 & S_0

6> Using two 2-to-4 line decoders, construct a 3-to-8 line decoder. You may use any necessary logic gates for the design.

7> Design a master-slave JK flip-flop, and explain its operation using exitation table.

8> Design a D-flipflop & T-flip flop using JK flipflop and explain their operations.

9> Design a 4-bit, universal Shift Register. Explain with appropriate timing diagram.

10> Design a Mod-16 ripple counter and explain with an appropriate timing diagram.