Motivation : 2-Dimensional Address Decoding

- 1-Dimensional Address Decoding

$2^k \times n$: 2^k, n-bit words

k to 2^k : Decoder

2^k AND Gates

Each: k inputs

16x4 : 4 to 16

512x8 : 9 to 2^9 (512)

1M x 4 : 20 to 2^{20}

→ Decoder complexity

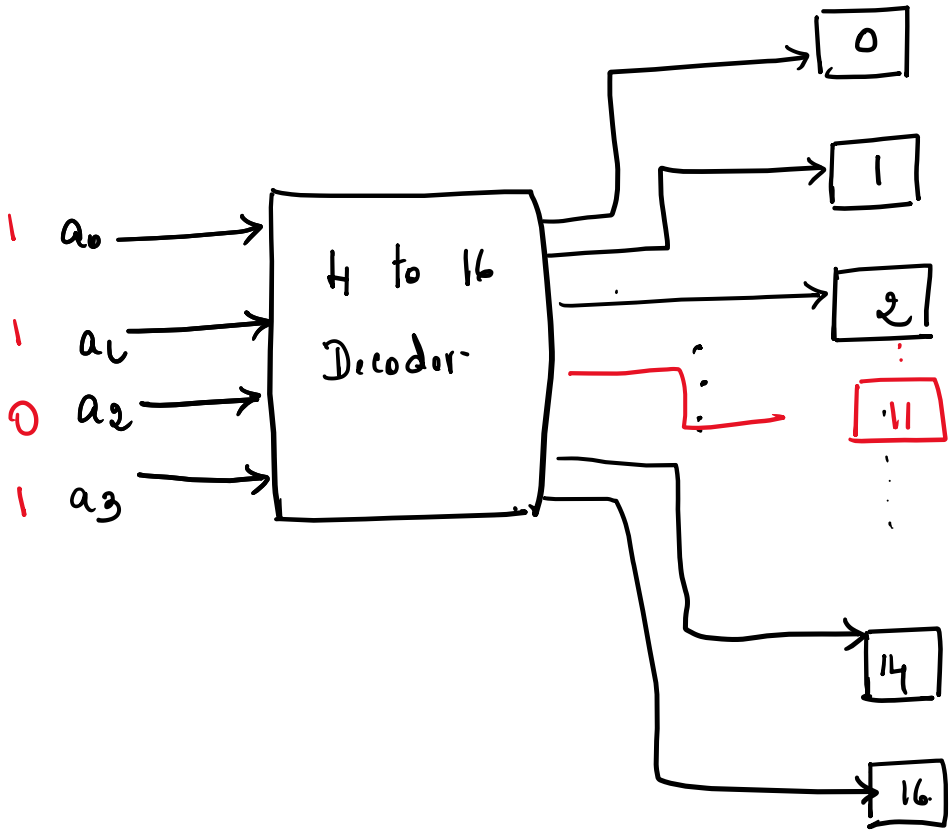
↑

Reduced?

↓

2-Dimensional address decoding

Ex: 16x1 bit memory. word: 1 bit

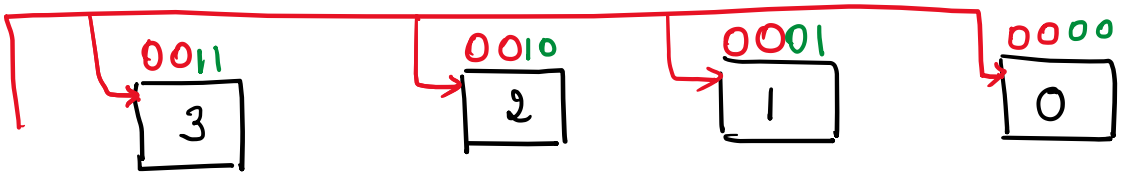


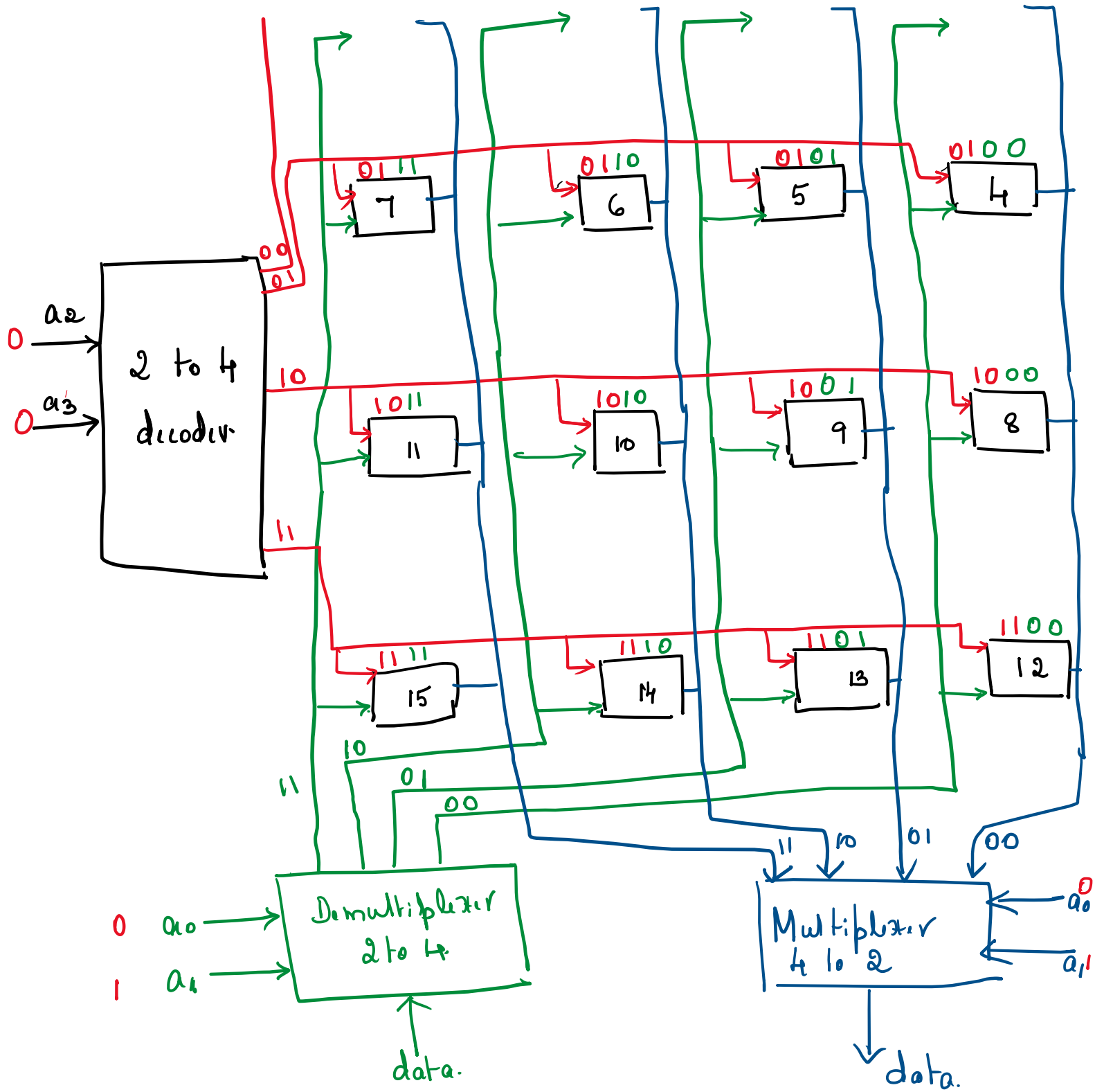
0000 → 0
0001 → 1
0010 → 2
0011 → 3
0100 → 4
0101 → 5
0110 → 6
0111 → 7
1000 → 8
1001 → 9
1010 → 10
1011 → 11
1100 → 12
1101 → 13
1110 → 14
1111 → 15

4 to 16 Decoder

16 - AND gates

Each AND gate → 4 inputs





$a_3\ a_2\ a_1 a_0$

0 0 10

4 tRow 16 decoder

2^k

Row

2 to 4 decoder.

k to

Column

2 to 4.

$k/2 - 2^{k/2}$.

Reduce the complexity of decoding