Control Unit

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Control Unit

- Processor must have some means of generating the control signals needed in the proper sequence
- Two categories of approaches used to generate the control signals in proper sequence:
  - Hardwired control
  - Microprogrammed control

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Hardwired Control

- Control sequence for execution of ADD R1, [R2]:

  T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
  T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
  T3 MDR_{out} , IR_{in}

  T4 $R2_{out}$, MAR_{in} , Read
  T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
  T6 MDR_{out} , Select Y, Add, Z_{in}
  T7 Z_{out} , $R1_{in}$, End

- Counter can be used to keep track of the control steps
- Each state or count, of this counter corresponds to one control step

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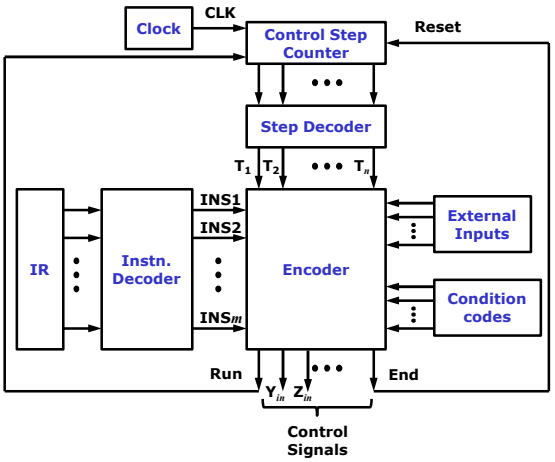
Hardwired Control Unit Organization



- Control signals are obtained using:
  - Contents of control step counter
  - Contents of the instruction register
  - Contents of condition flags
  - External input signals like MFC and interrupt requests
- The decoder/encoder block is a combinational circuit that generates the required control outputs, depending on the state of all its inputs

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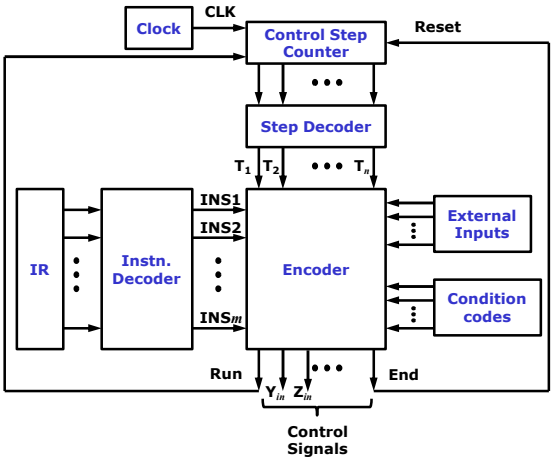
Hardwired Control Unit Organization



- Step decoder:
  - Provides a separate signal line for each step or time slot in the control sequence
- Instruction decoder:
  - Its output consists of separate lines for each machine instruction

- For any instruction in IR, one of the output lines INS1 to INSm is selected (i.e. set to 1) and all other lines are set to 0

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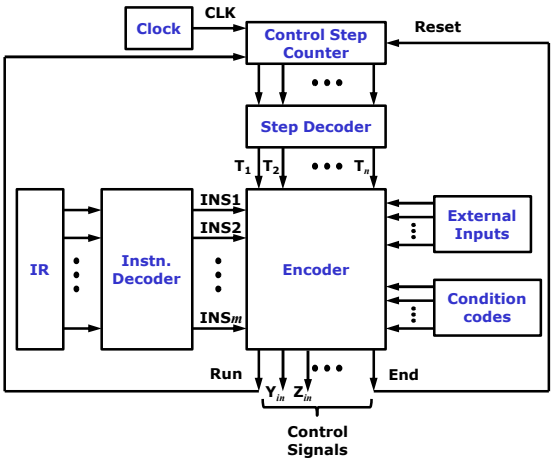
Hardwired Control Unit Organization



- Encoder:
  - Input signals to encoder block are combined to generate individual control signals Y_{in}, Z_{in}, PC_{out}, Add, End and so on

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Design of Encoder

- Control sequence for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End

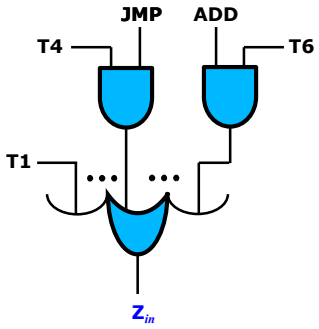
Example: Logic for Generating control signal, Z_{in}

Z_{in} = T1 + T6 . ADD + T4.JMP + …

- Control sequence for JMP next

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $Offset\_filed\_of\_IR_{out}$, Add, Select Y, Z_{in}
T5 Z_{out} , PC_{in} , End



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Design of Encoder

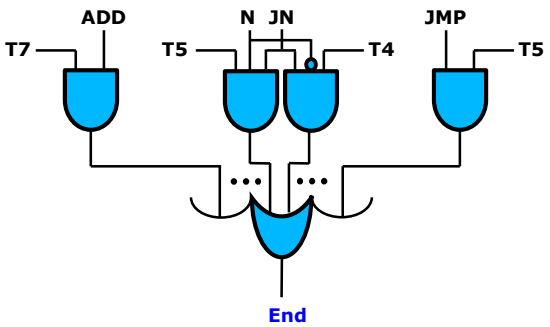
- Example: Generating control signal, End

End = T7.ADD + T5.JMP + (T5.N + T4.$\overline{N}$).JN + …

- Control sequence for JN next

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $Offset\_filed\_of\_IR_{out}$, Add, Select Y, Z_{in} , If N=0 then End
T5 Z_{out} , PC_{in} , End



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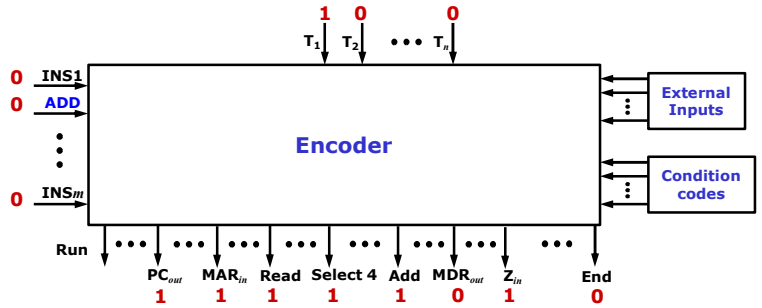
Generation of Control Signals

- Example: T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}

PC_{out} = T1 + …
MAR_{in} = T1 + T4.ADD + …
Select 4 = T1 + …
Add = T1 + T6.ADD + T4.(JMP + JN + …) + …
Z_{in} = T1 + T6.ADD + T4.JMP + …



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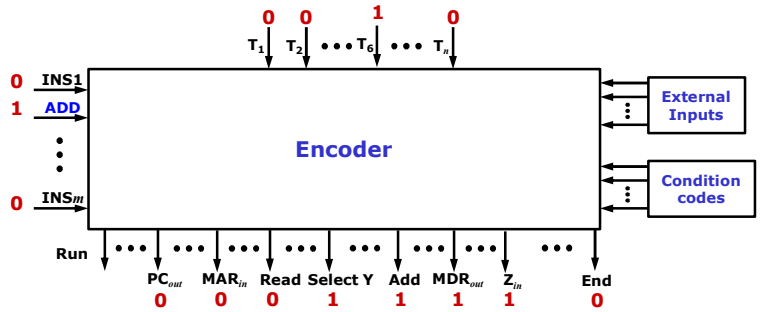
Generation of Control Signals

- Example: ADD R1, [R2]
  T6 MDR_{out} , Select Y, Add, Z_{in}

MDR_{out} = T3 + T6.ADD + …
Select Y = T6.ADD + T4. (JMP + JN + …) + …
Add = T1 + T6.ADD + T4.(JMP + JN + …) + …
Z_{in} = T1 + T6.ADD + T4.JMP + …



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Advantages and Disadvantages

- The hardwired control unit operate in high speed
- Useful when the instructions in the set are limited and simple

- It has less flexibility
- It is used in RISC processors

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Microprogrammed Control Unit

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Microprogrammed Control Unit

- Control signals are generated by a program
- The control signals are stored as control word (CW) in a control memory (control store)
- Control sequence for execution of ADD R1, [R2]:

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End

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Control Word and Control Memory

- Control word is a word whose individual bits represents the various control signals

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	•••
0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	•••
1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	•••
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	•••

- Each control word is called as microinstruction
- All the sequence of control words corresponding to a machine instruction is called microroutine
- All the microinstructions are stored in control memory in a specific location

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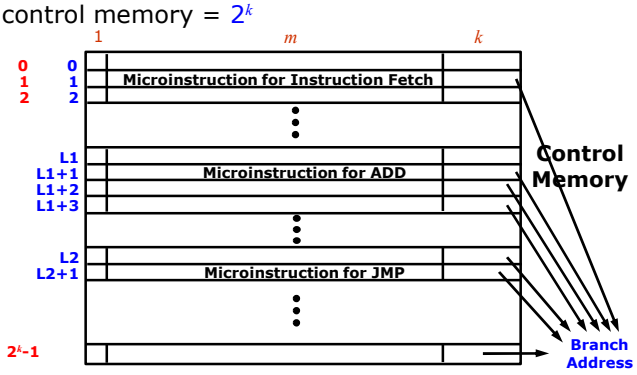
Microprogrammed Control Unit Organization

- m = number of control signals
- k = branch address bits
- Length of a microinstruction = $1+m+k$
- Size of control memory = 2^k



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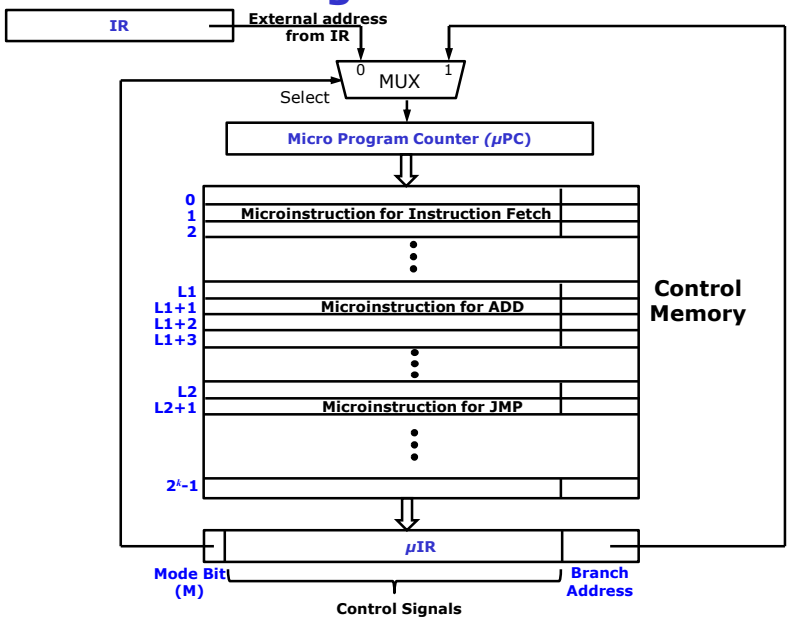
Microprogrammed Control Unit Organization



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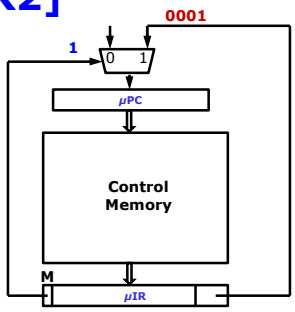
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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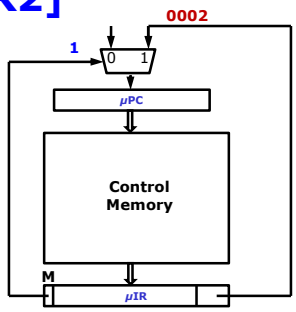
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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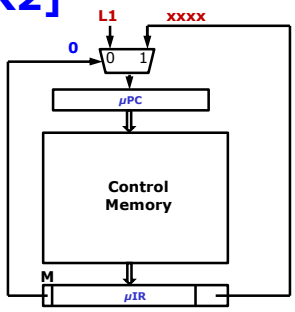
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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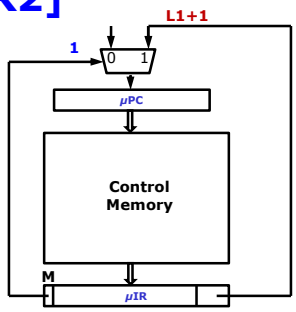
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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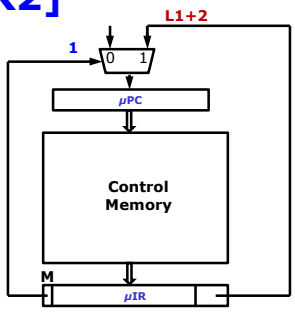
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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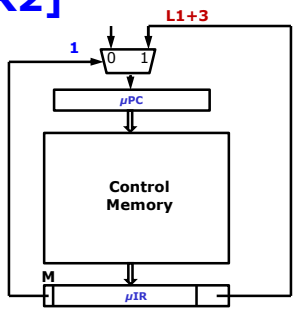
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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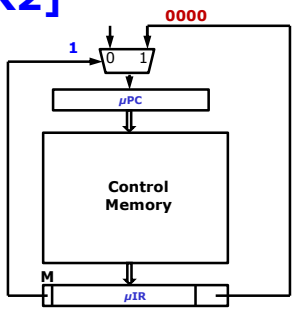
Generation of Control Signals for ADD R1, [R2]

T1 PC_{out} , MAR_{in} , Read, Select 4, Add, Z_{in}
T2 Z_{out} , PC_{in} , Y_{in} , MDR_{inE} , WMFC
T3 MDR_{out} , IR_{in}

T4 $R2_{out}$, MAR_{in} , Read
T5 $R1_{out}$, Y_{in} , MDR_{inE} , WMFC
T6 MDR_{out} , Select Y, Add, Z_{in}
T7 Z_{out} , $R1_{in}$, End



	M	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select 4	Select Y	Add	Z_{in}	Z_{out}	$R1_{in}$	$R1_{out}$	$R2_{out}$	WMFC	End	Branch Address
0000	1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0001
0001	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0002
0002	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	xxxx
L1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	L1+1
L1+1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	L1+2
L1+2	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0	0	L1+3
L1+3	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0000

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Advantages and Disadvantages

- The Microprogrammed control unit is more compact and flexible
- Useful when the instructions in the set are complex and varying in length

- It is slow
- It is used in CISC processors

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