Computer Organization and Architecture

Internal Organization of Memory Chips
2-d Address Decoding

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Recap

- Internal organization of memory chips
- 1-d Address decoding
- Motivation for 2-d address decoding

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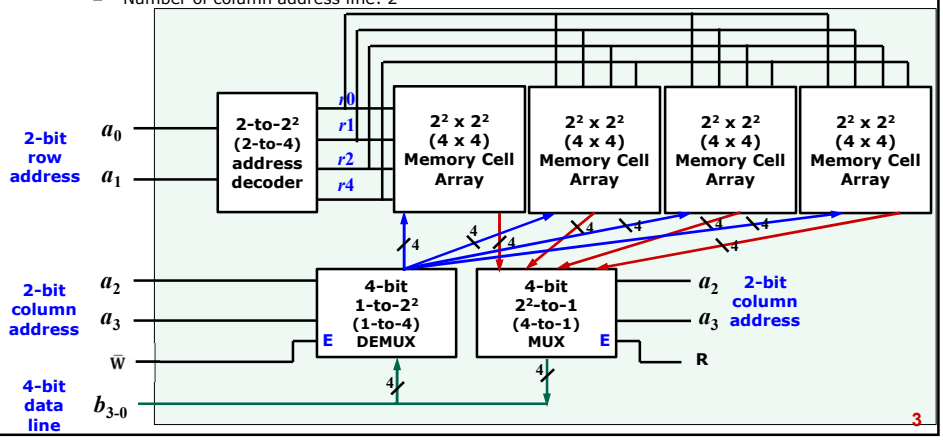
2-dimensional Address Decoding

- k-address line is divided into $k/2$ row address and $k/2$ column address
- Now, memory chip is considered as $2^{k/2}$ x $2^{k/2}$ memory cell array
- Example: Design of 16 x 4 bit memory chip
  - Number of address lines: 4
  - Number of row address lines: 2
  - Number of column address line: 2



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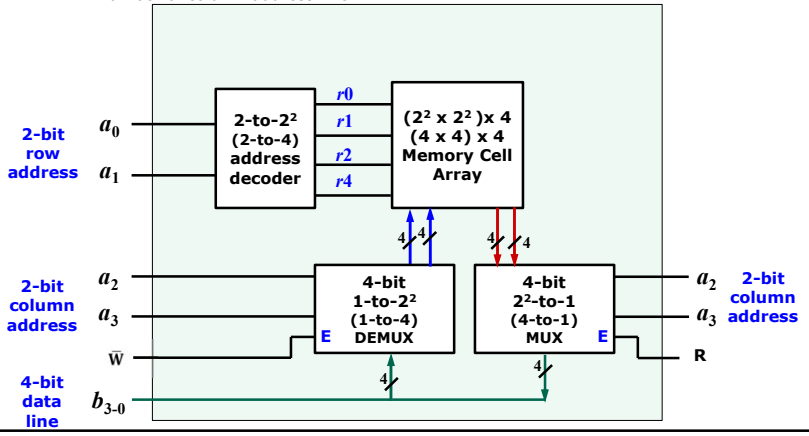

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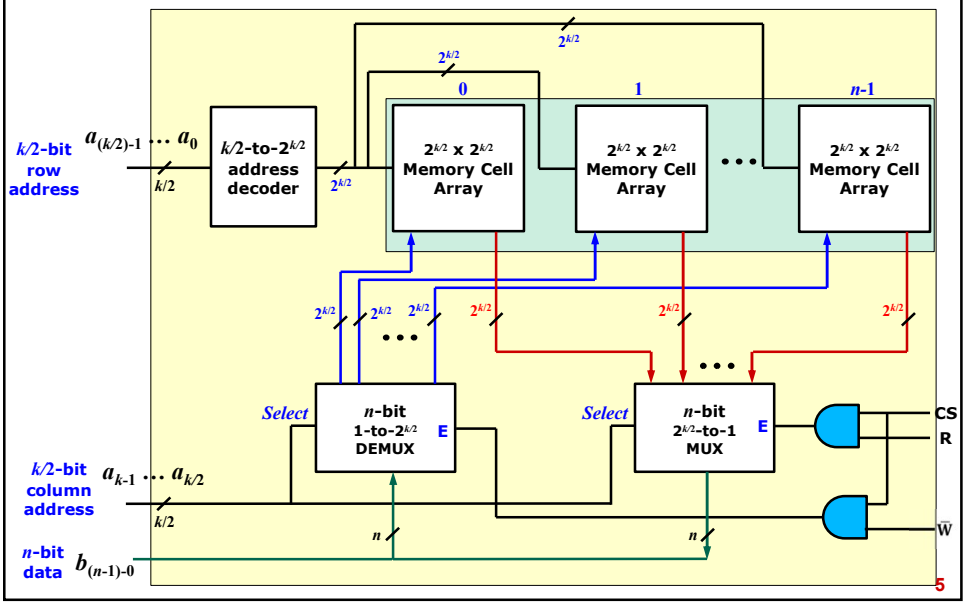
2-dimensional Address Decoding

- **Organization of 2^k x n SRAM Chip**



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2-dimensional Address Decoding

- **Organization of 2^k x n SRAM Chip**
  - The number of cell array depends on the width of the memory chip (word length) expected

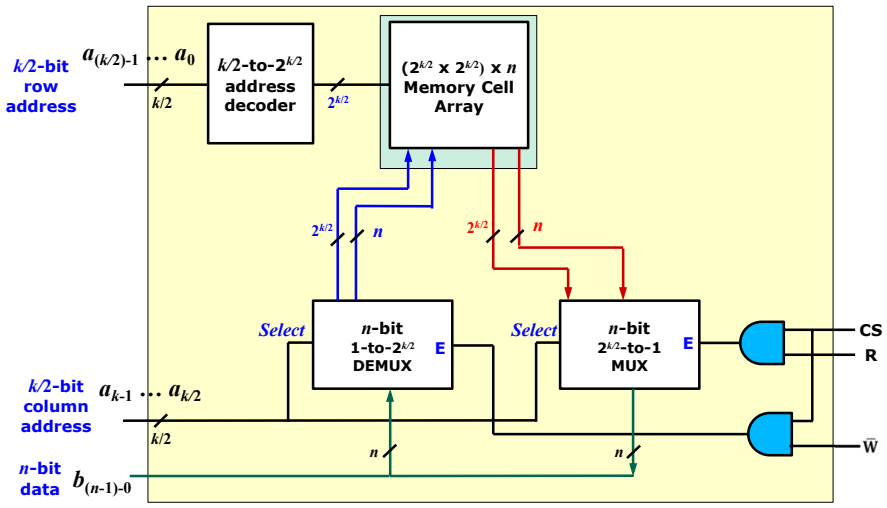

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Illustration: Design of 1MB SRAM Chip

- Capacity of memory: 1 MB
- Word length: 8 bits
- Memory organization: 1M x 8

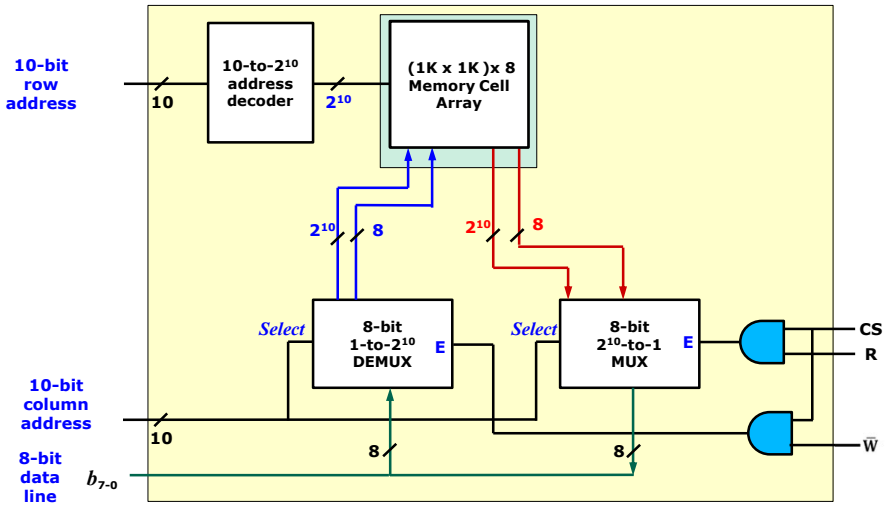

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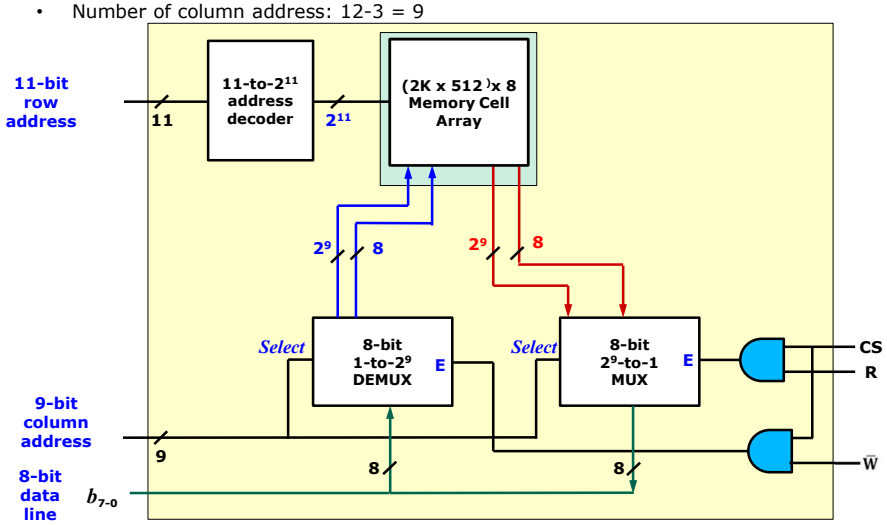
Illustration: Design of 1MB SRAM Chip

- Capacity of memory: 1 MB (2^{20} B = 2^{23} b)
- Word length: 8 bits
- Number of row address: 11
- Number of column address: 12-3 = 9



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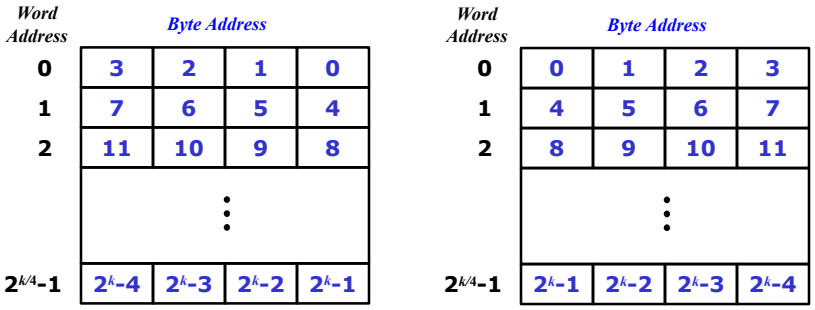
Byte Addressable Memory



Example: Intel Processors **Motorola Processors**

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Static RAM Module

- **Byte Addressable Memory**
- Illustration:
  - Task: Design SRAM with capacity 8MB (2^{23} **B**)
  - Requirements:
    - Memory organization depends on the word size and word size decides the width of the data bus
      - Let word size be 32 bit (**4 B**)
      - Now, memory organization: 2M x 32 bit
    - Memory should be byte addressable
      - Let the organization of cell array to incorporate byte addressability be 1M x 8 bit
  - Organization include:
    - 2 rows of chips, each of size 1M x 8 bit
    - Each row contain 4 chips
  - Number of address lines: 23 (2^{23} **B**)

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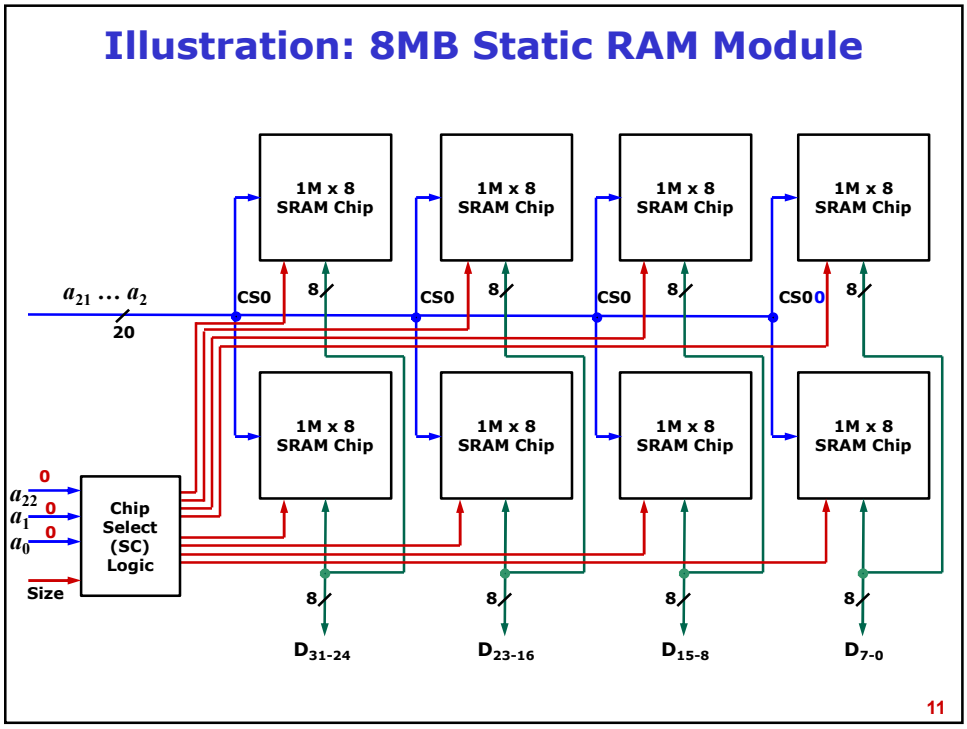


Illustration: 8MB Static RAM Module
1M x 8 SRAM Chip
$a_{21} \ldots a_2$
20
CS0
8
Chip Select (SC) Logic
0
a_{22}
0
a_1
0
a_0
Size
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
11

11

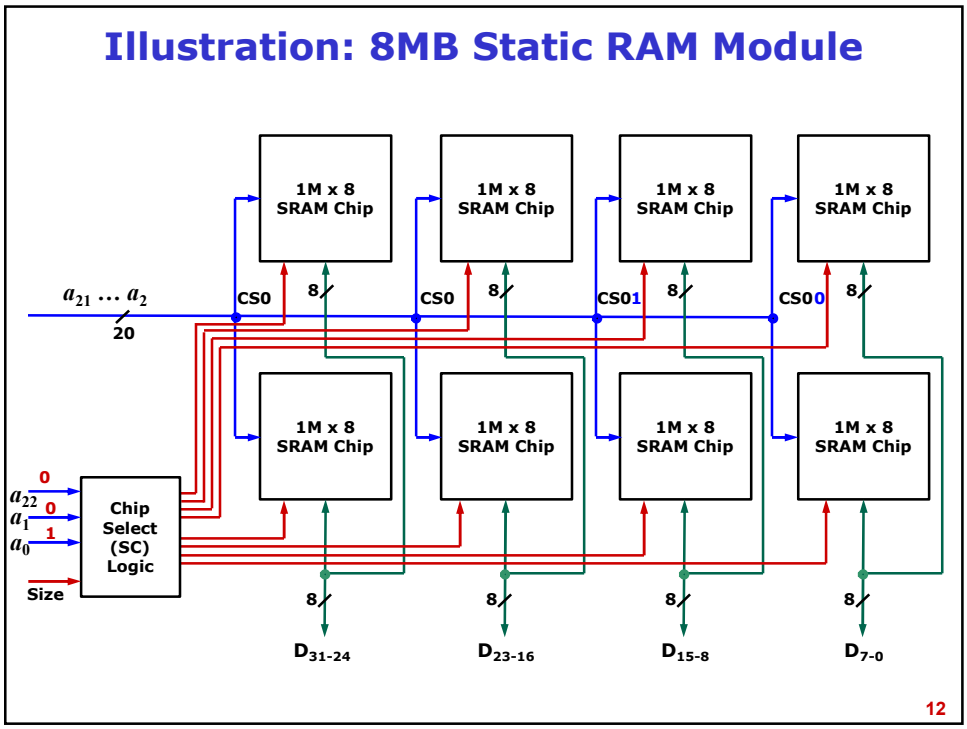


Illustration: 8MB Static RAM Module
1M x 8 SRAM Chip
$a_{21} \ldots a_2$
20
CS0
CS01
CS00
8
Chip Select (SC) Logic
0
a_{22}
0
a_1
1
a_0
Size
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
12

12

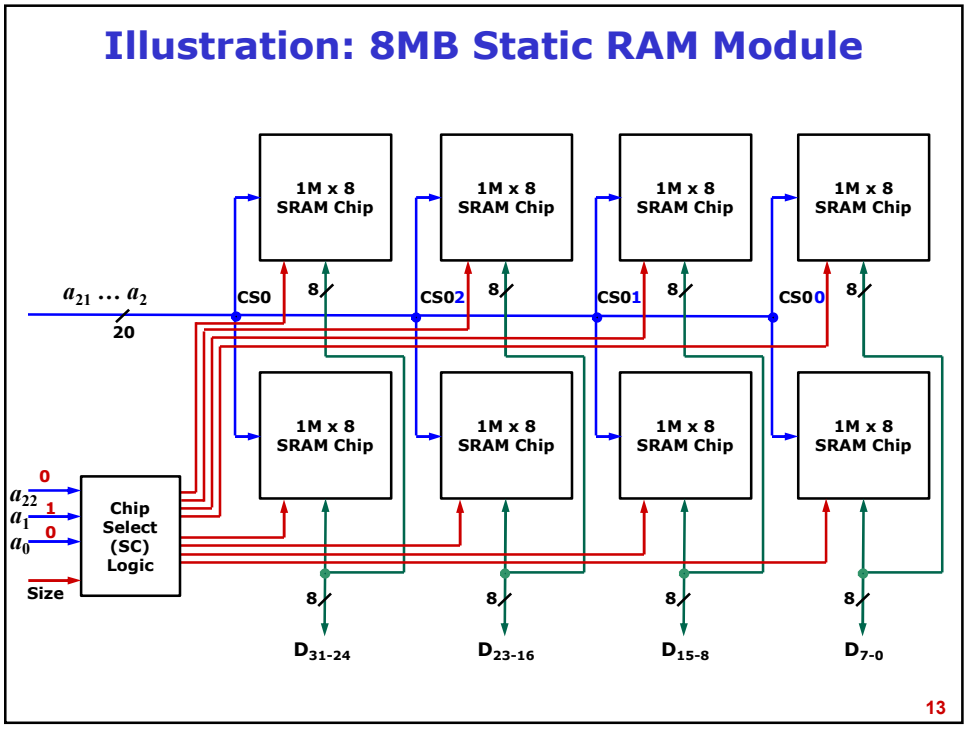


Illustration: 8MB Static RAM Module
1M x 8 SRAM Chip
$a_{21} \ldots a_2$
20
CS0
CS02
CS01
CS00
8
0
a_{22}
1
a_1
0
a_0
Chip Select (SC) Logic
Size
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
13

13

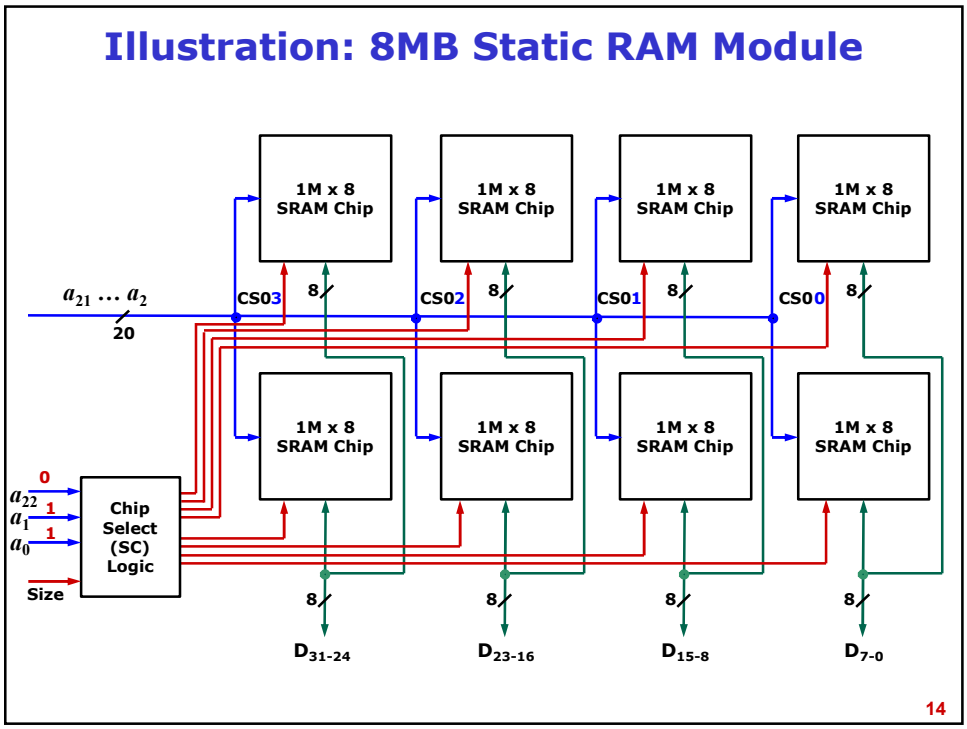
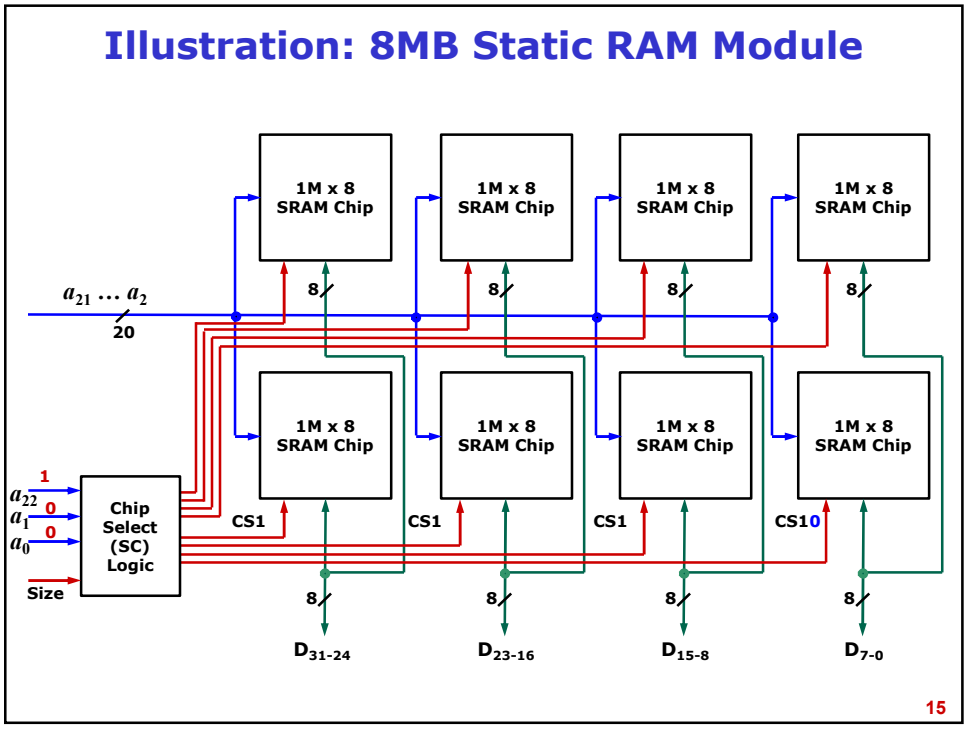


Illustration: 8MB Static RAM Module
1M x 8 SRAM Chip
$a_{21} \ldots a_2$
20
CS03
CS02
CS01
CS00
8
0
a_{22}
1
a_1
1
a_0
Chip Select (SC) Logic
Size
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
14

14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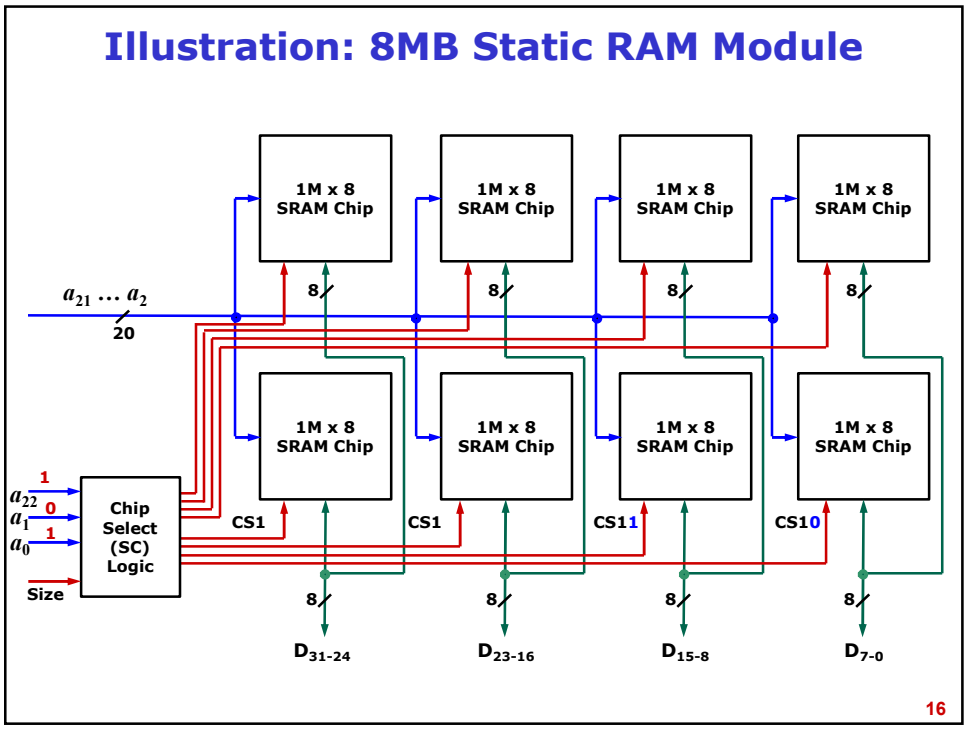
1M x 8 SRAM Chip
$a_{21} \ldots a_2$
20
8
1
a_{22}
0
a_1
0
a_0
Chip Select (SC) Logic
Size
CS1
CS1
CS1
CS10
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
15

15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20
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a_1
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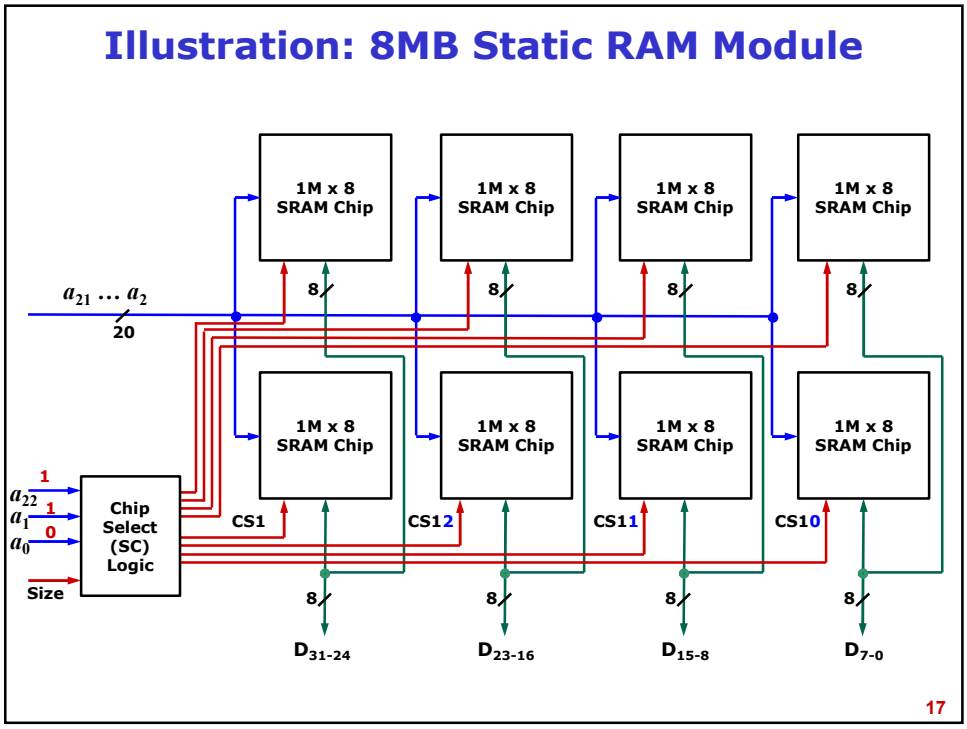
Chip Select (SC) Logic
Size
CS1
CS1
CS11
CS10
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
16

16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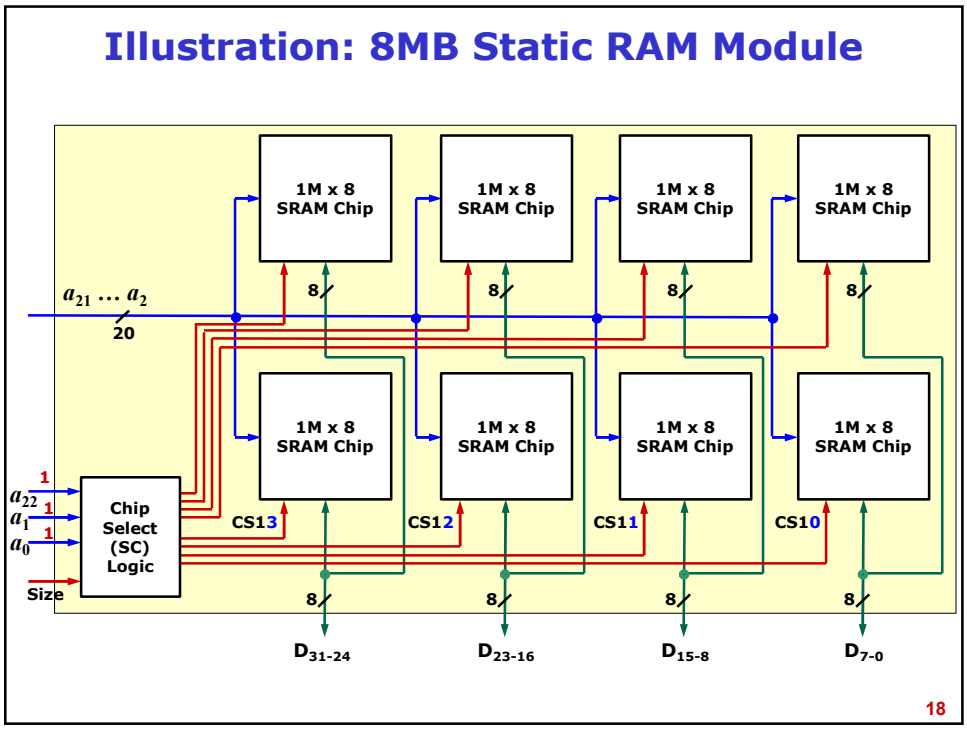
$a_{21} \ldots a_2$
20
8
Chip Select (SC) Logic
a_{22} 1
a_1 1
a_0 0
Size
CS1
CS12
CS11
CS10
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
17

17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Chip Select (SC) Logic
a_{22} 1
a_1 1
a_0 1
Size
CS13
CS12
CS11
CS10
D_{31-24}
D_{23-16}
D_{15-8}
D_{7-0}
18

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Static RAM Module

- **4MB SRAM Module**

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Static RAM Module

- N: Capacity of SRAM
- n bits: Width of SRAM
- M: Capacity of one SRAM chip
- m bits: Width of SRAM chip
- Number of rows of memory chips: N/M
- Number of chips in a row: n/m
- According to the number of rows of memory chips and number of chips in a row, Chip Select (CS) logic is designed
- Higher order bits in address select a row of memory chips
- Lower order bits in address select a byte in a word
- Size line in CS logic indicates how many bytes in a word need to be selected

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Reference

- **Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", 5th Edition, Tata McGraw Hill, 2002**

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Thank You

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