CS202 Computer Organization and Architecture

Online Mid Sem Examination : 06/10/2021

①

ADD A, B, C

- LOAD Address of instruction into MAR (PC)
  - MAR → Address lines
  - Read signal to MU
  - Instruction word to MDR
  - MDR → IR
- → A → MAR
- → Read.
- [A] → MDR
- → MDR → I/P of ALU.
- → B → MAR
- → Read.
- [B] → MDR
- Add signal to ALU.
- ALU - Addition.
- C → MAR
- Result of Add → MDR
- Write.
- WMFC

IF → 1

ID → 1

OF → 1

EX → 1

WB → 1

IF, ID - 1

Remarks

2.

(a)

	Sign-magnitude	1's complement	2's complement
7	000000111	000000111	000000111
-44	100101100	111010011	111010100
-13	100001101	111110010	111110011
27	000011011	000011011	000011011
-64	101000000	110111111	111000000

(1 x 5 = 5 marks)

(b) $X = 010.110111$ (188)

$X' = 101001000 + 1$

$X' = 101001001$

$Y = 011101001$ (233)

$Y' = 100010110 + 1$ (-233)

$Y' = 100010111$

(i) $X' + Y' = 101001001 + 100010111 = 1001100000$ ✓ 2½

Only x'', y'' – (2 marks)

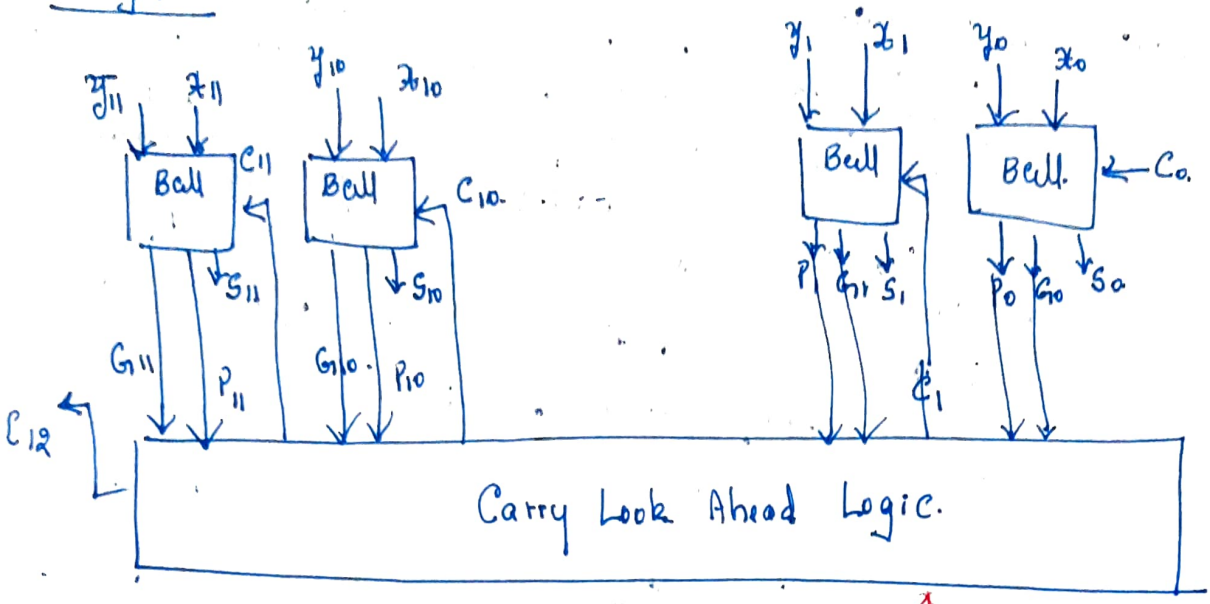
(ii) $Y'' = 011101000 + 1$

$Y'' = 011101001$

$X' - Y' = X' + Y'' = 101001001 + 011101001 = 000110010$ ✓ 2½

(c) Design of a 12-bit adder using CLA

Design 1.



— Crude approach.

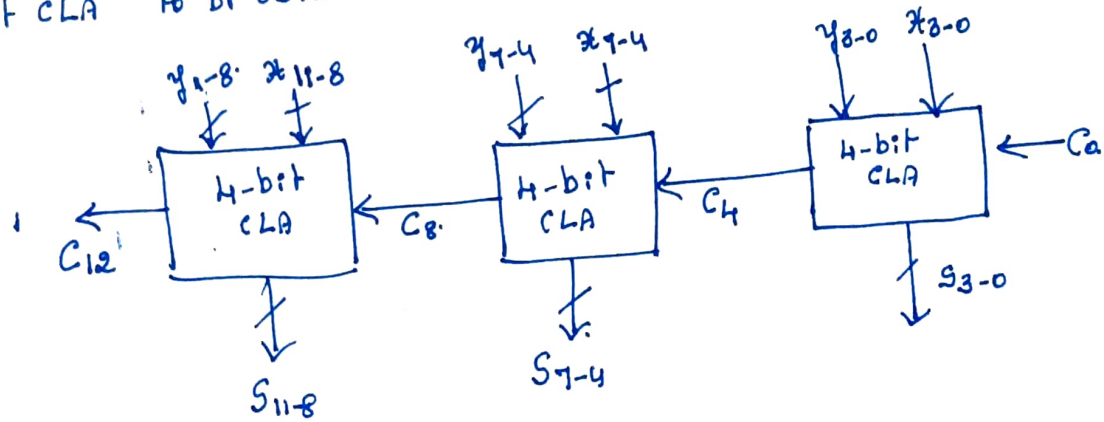
→ C_{12} expression: 12 terms
- 13 input AND gate.

→ Drawback

4 marks
idea – 1 mark
Drawback – 1 mark
6 marks

Design 2: Cascade Style I

3, 4-bit CLA to be used.



Drawback

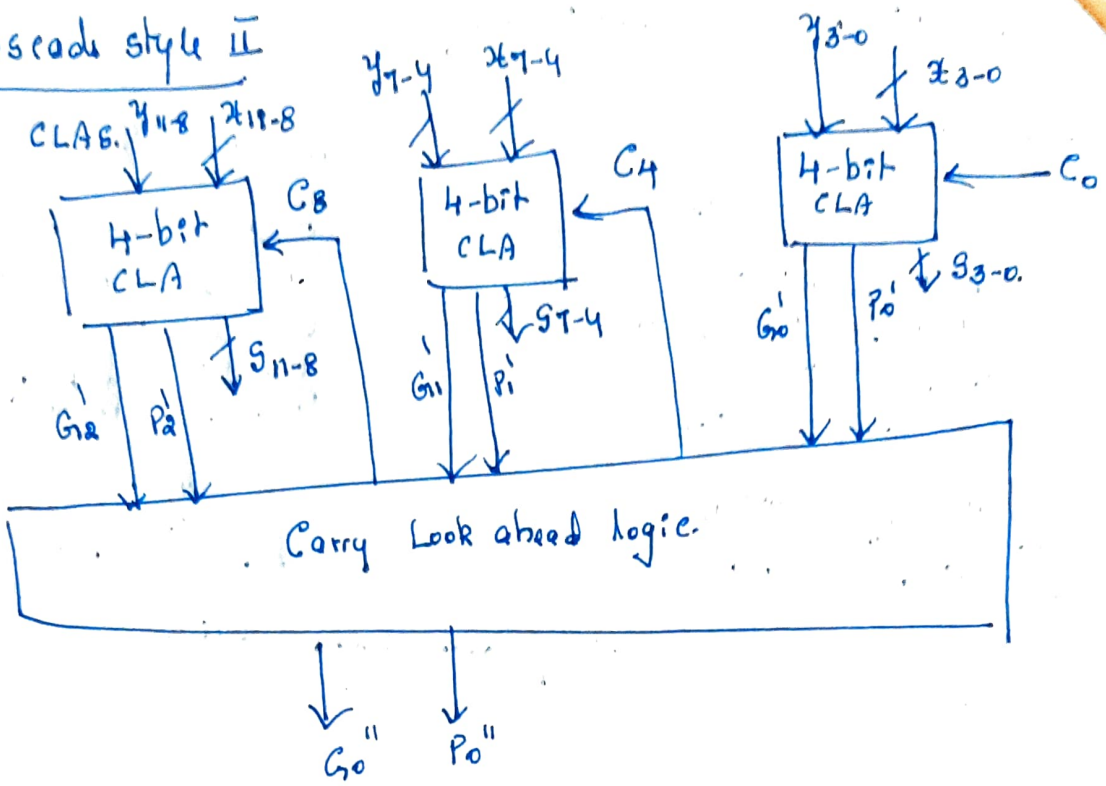
Ripple Carry style.

2, 6 bit CLA may be used.

idea – 1 mark
Design – 4 mark
Drawback – 1 mark
6 marks

Design 3: Cascade style II

3, 4-bit CLAs.



2, 6-bit CLA may be used

to

Idea - 1 mark
Design - 4 mark
Discussion - 1 mark
6 marks

Any one complete design to be presented

(a) Many gates
Complexity of electronic circuits involved.
Handling - Positive and negative numbers alike.
} Explanation
3 marks

(b) Multiplicand, M = 11 = 0 0 1 0 1 1

Multiplier, Q = -27

= 1 0 0 1 0 1

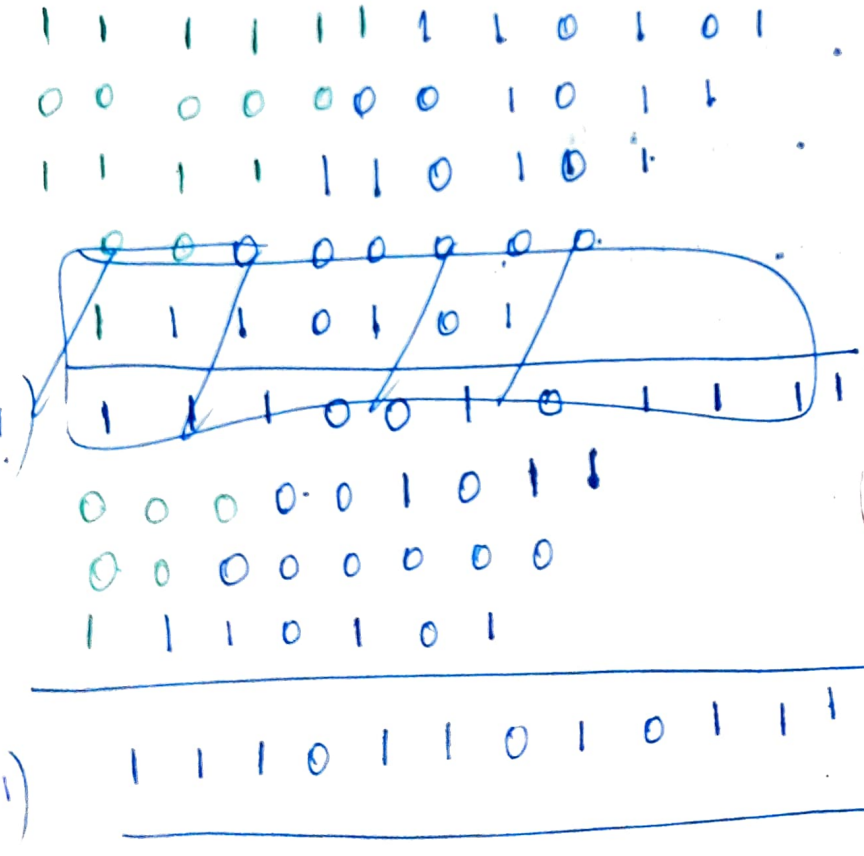
$\bar{Q}$ = -1 0 +1 -1 +1 -1

1 marks

$M'' = 1\,1\,0\,1\,0\,0 +$
$\quad\quad\quad\quad\quad\quad 1$
$1\,1\,0\,1\,0\,1$

$0\,1\,1\,0\,1\,1$
$1\,0\,0\,1\,0\,0 +$
$\quad\quad\quad\quad 1$
$1\,0\,0\,1\,0\,1$

0 0 1 0 1 1 (M)
-1 0 +1 -1 +1 -1 ($\bar{Q}$) → 1 mark



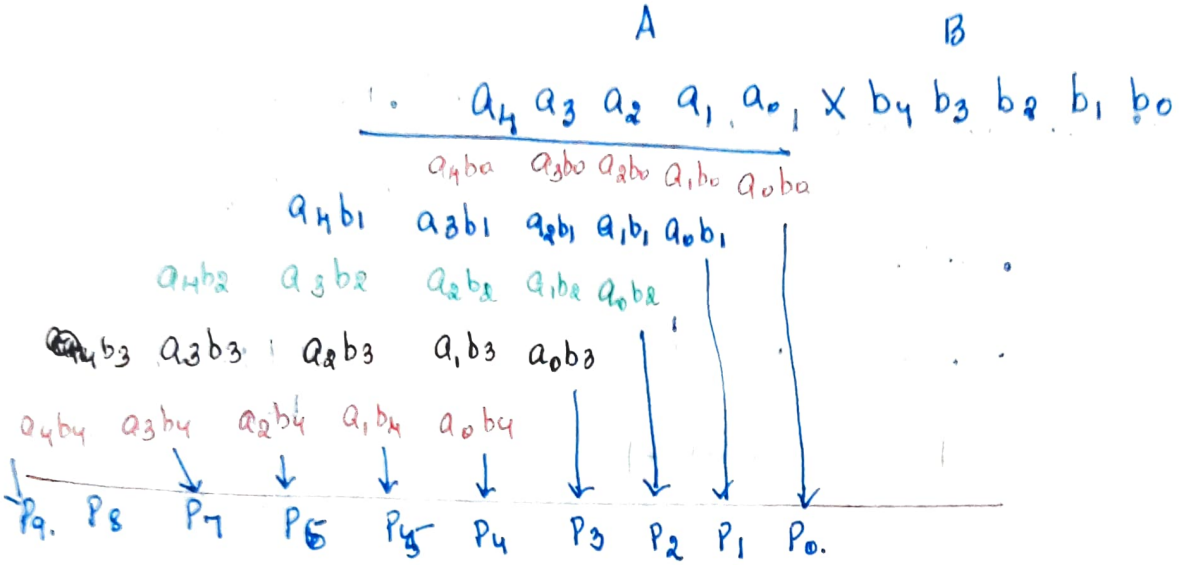
6 x 0.5 = 3 marks

2 marks

4 marks

(4) $A = a_4 a_3 a_2 a_1 a_0$.

$B = b_4 b_3 b_2 b_1 b_0$.



$P_0 = a_0 b_0$

$P_1 = a_1 b_0 + a_0 b_1$

$P_2 = a_2 b_0 + a_1 b_1 + a_0 b_2$.

$P_3 = a_3 b_0 + a_2 b_1 + a_1 b_2 + a_0 b_3$

$P_4 = a_4 b_0 + a_3 b_1 + a_2 b_2 + a_1 b_3 + a_0 b_4$

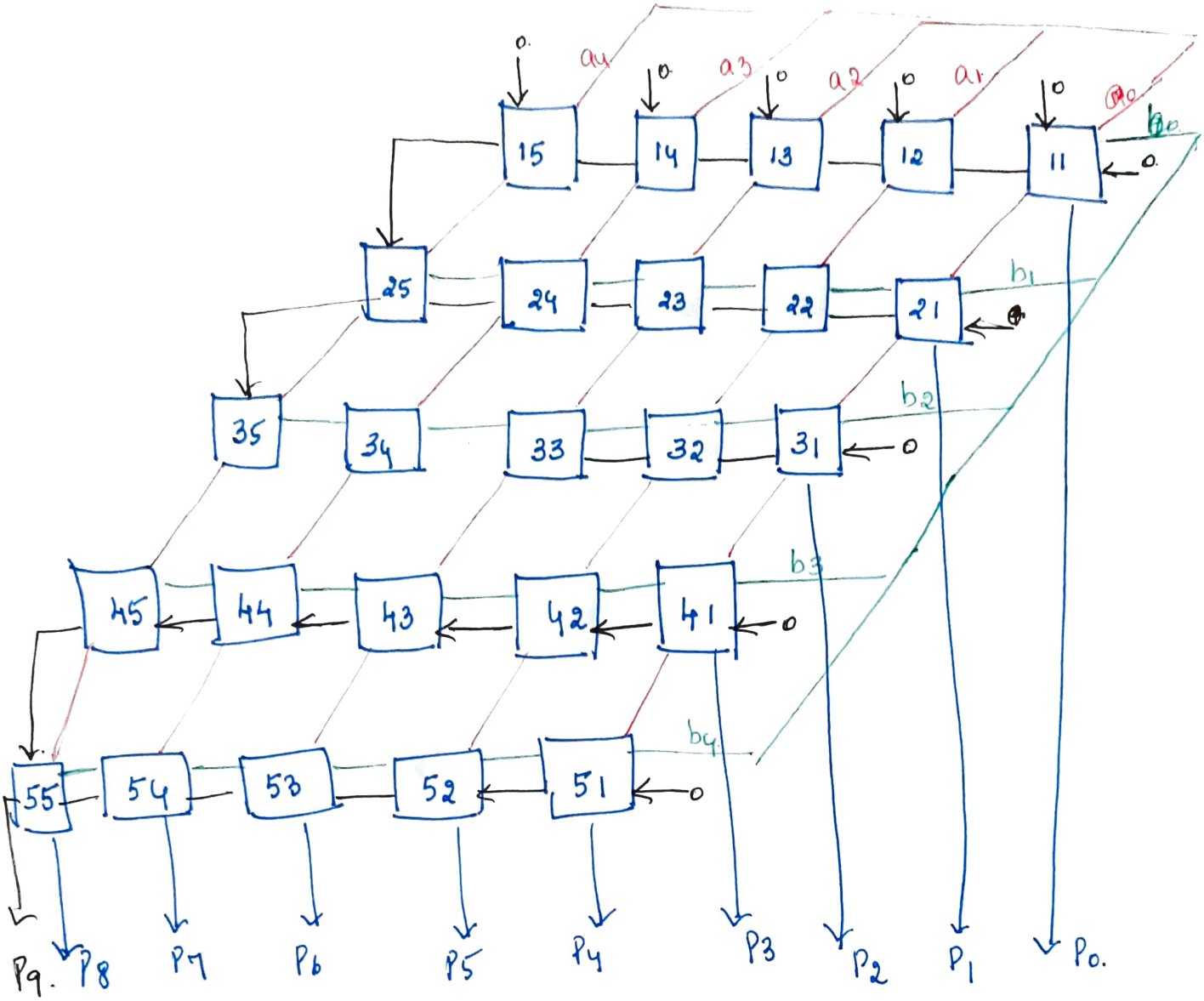
$P_5 = a_4 b_1 + a_3 b_2 + a_2 b_3 + a_1 b_4$.

$P_6 = a_4 b_2 + a_3 b_3 + a_2 b_4$

$P_7 = a_4 b_3 + a_3 b_4$.

$P_8 = a_4 b_4$.

$P_9 =$ Carry out



5

CSA based. — 5 marks

5) Restoring division

Perform 359 ÷ 11 Using Restoring algorithm

Dividend Q = $359_{(10)}$

= $101100111_{(2)}$ ← 9 bits

n = 9

Divisor M = $11_{(10)}$

= $00000\ 1011_{(2)}$

(n+1) bit rep. = 000000 1011

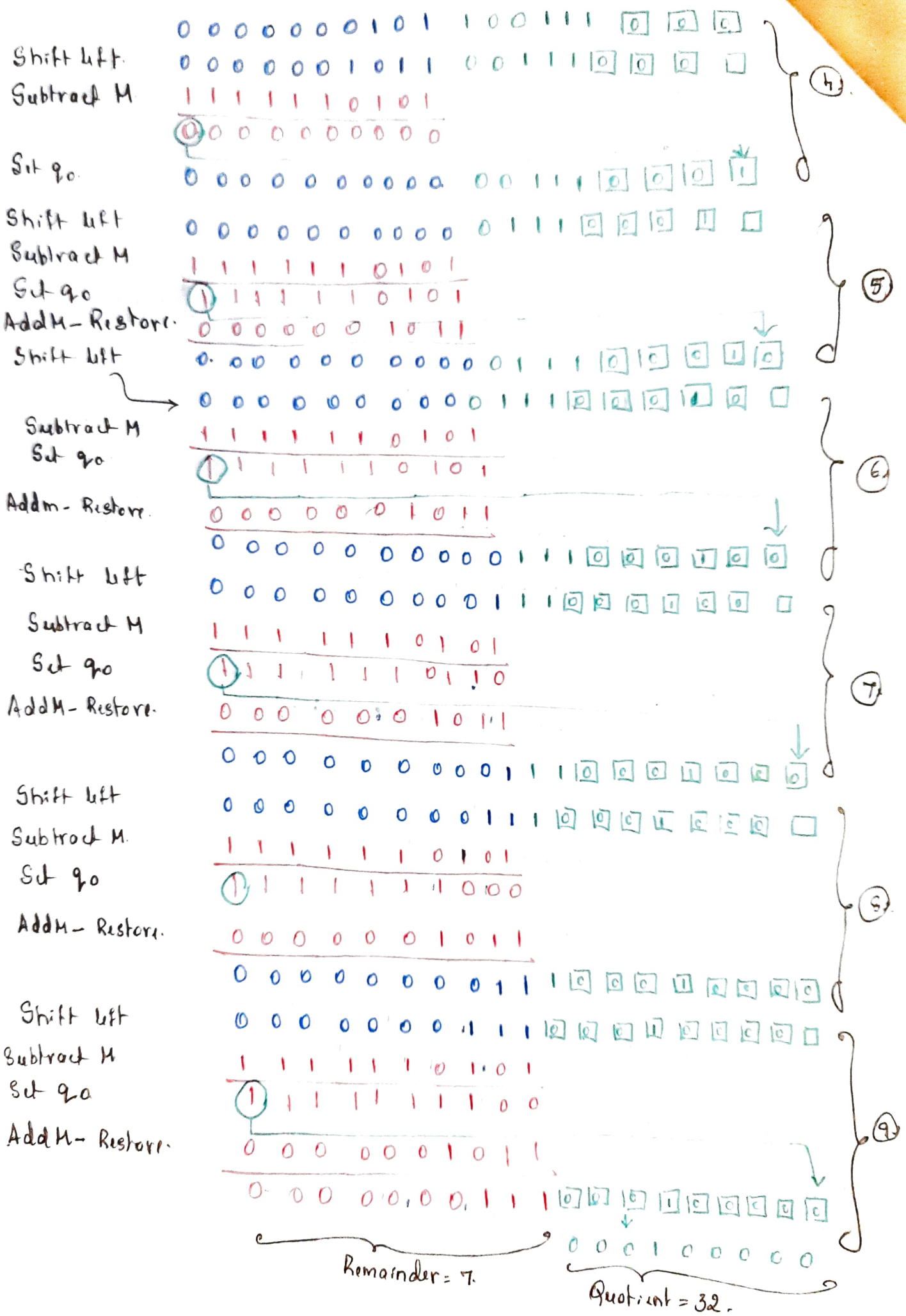
M' = 1111110100 + 1

= 1111110101

```
       3 2
  11 ) 3 5 9
       3 3
         2 9
         2 2
           7
```

2	359	
2	179	1
2	89	1
2	44	1
2	22	0
2	11	0
2	5	1
2	2	1
	1	0

Step	A	Q	
Initialization	0 000000000	101100111	①
Shift left	0 000000001	01100111□	
Subtract M	1111110101		
Set q_0	1111110110		
Add M – Restore	0000001011		
	0000000001	01100111[0]	
Shift left	0000000010	1100111[0]□	②
Subtract M	1111110101		
Set q_0	1111110111		
Add M – Restore	0000001011		
	0000000010	1100111[0][0]	
Shift left	0000000101	100111[0][0]□	③
Subtract M	1111110101		
Set q_0	1111111010		
Add M – Restore	0000001011		
	0000000101	100111[0][0][0]	


Shift left
Subtract M
Set q0
4
Shift left
Subtract M
Set q0
Add M - Restore
5
Shift left
Subtract M
Set q0
Add m - Restore
6
Shift left
Subtract M
Set q0
Add M - Restore
7
Shift left
Subtract M
Set q0
Add M - Restore
8
Shift left
Subtract M
Set q0
Add M - Restore
9
Remainder = 7
Quotient = 32