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EE152 Basic Electrical Science Lab

Session – 8

Digital Combinational Logic gates

8. A. Introduction:

This session makes students to understand various digital combinational logic gates- AND, OR, NOT, NAND, NOR, XOR, XNOR - and to verify through the Simulation in MATLAB/Simulink.

8. B. Objectives:

a. Acquire a good knowledge on various digital combinational logic gates- AND, OR, NOT, NAND, NOR, XOR, XNOR.

b. Verification of the theoretical knowledge on these logic gates through simulation in MATLAB/Simulink Platform.

8. C. Theory: Refer to the notes or necessary materials mentioned in EE151 course.

8. D. Statement of Experiments:

Fig. 8.1 represents various logic gates (NOT, AND, NAND, OR, NOR, XOR, XNOR). The input for these gates are digital in nature, i.e., it is either '0' or '1', and the output is also in digital in nature. Based on the theoretical knowledge, a truth table for each gate has to be prepared and that table has to be verified through simulation in Matlab/Simulink.

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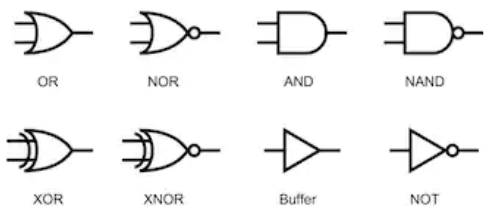

Fig. 8.1

8. E. Procedure:

Prepare the truth table for each logic gates asked in section-8.D theoretically and draw experimental circuit (necessary Measuring instruments are to be incorporated in the circuit) corresponding to the logic gates shown in Fig. 8.1. Construct the experimental circuits in Simulink domain, simulate it, and observe the output and validate corresponding truth table against each logic gates.

8. F. Assignments:

Part-1: Consider Fig. 8.2 and do the same as mentioned in Section - 8.D.

Part-2: Replace the gates shown in Fig. 8.2 by its inverted one and do the same as mentioned in Section - 8.D.

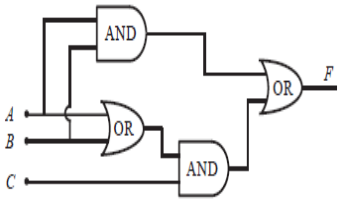

Fig. 8.2