Computer Organization and Architecture

Internal Organization of Memory Chips

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Recap

- Introduction to memory unit
  - Important memory operations
  - Hierarchical organization
- Semiconductor memory cells
  - SRAM
  - DRAM

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Internal Organization of Memory

- The memory is organised such that a group of n-bits can be stored or retrieved in a single basic operation
- Each group of n-bits is referred as one **memory word**
- Accessing the memory to store or retrieve information require address for each location
- Possible number of address locations are decided by the number of address lines in the processor
- For k-address lines, there will be 2^k locations, each of n-bit memory word
- 2^k addresses constitute address space of computer
- Example: Let k=10 and n=32
  - Number of locations: 2^{10}
  - Size of the memory: 2^{10} x 2^5 bits = 2^{15} bits
    = 2^{12} Bytes
    = 4 KB

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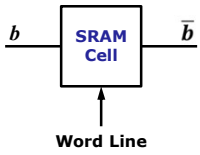
Internal Organization of SRAM Chip

- SRAM cell (block diagram):



- Memory cells are usually organised in the form of an array
- At each memory location, n SRAM cells are placed next to each other to form n-bit memory word
- Example: 4-bit memory word

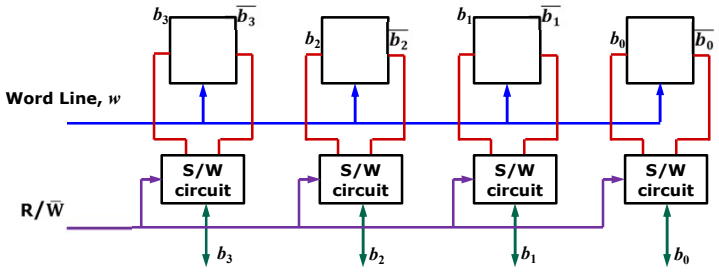


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Illustration: 16 x 4 bit Memory Chip

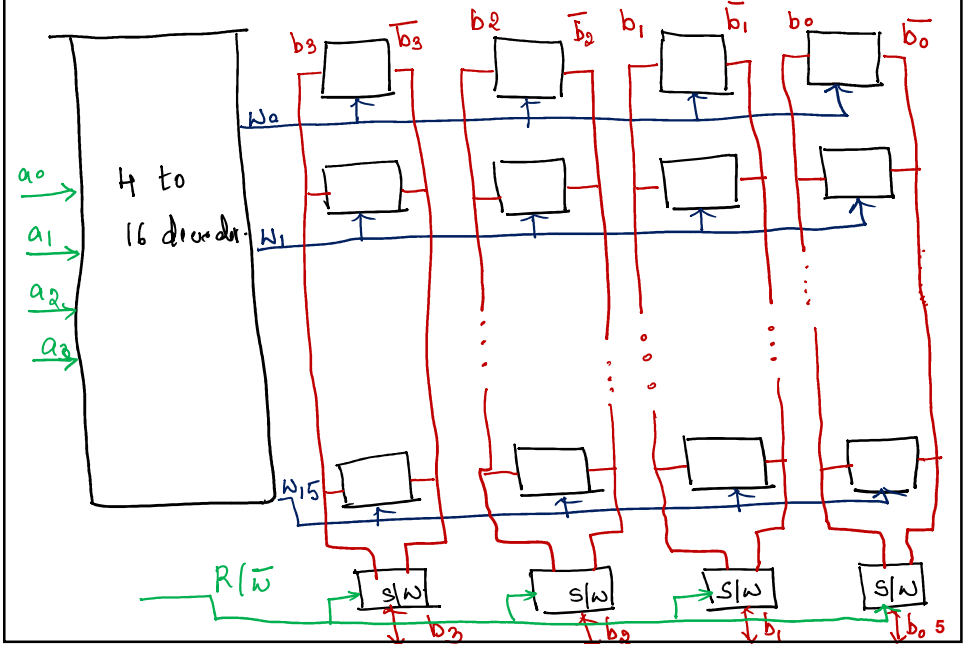

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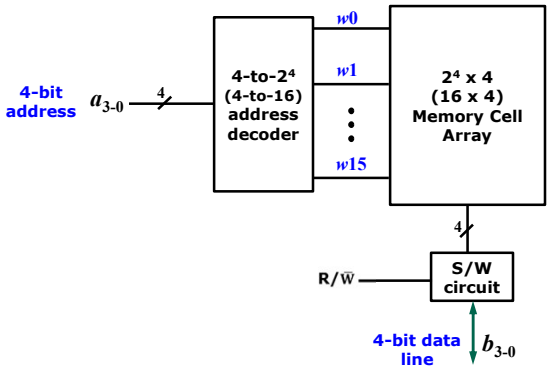
Illustration: 16 x 4 bit Memory Chip

- 1-dimensional address decoding:
  - *Example*: ***Design of 64b memory chip***
  - Number of address line be : 4
  - Address decoder configuration : 4-to-2^4



4 address
4 data.
1 R/$\bar{W}$
1 CS
2 PS
12

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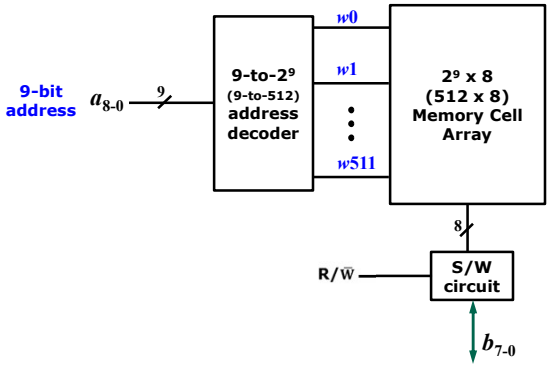
Illustration: 512 x 8 bit Memory Chip

- 1-dimensional address decoding:
  - *Example*: ***Design of 4Kb memory chip***

Memory chip organization : 512 x 8
Memory Size : 512B
Number of address line be : 9
Address decoder configuration : 9-to-2^9



- Example:
  - Memory capacity: 4 MB
  - Word length: 32 bits
  - Organization: 1M x 32
  - Number of address line: 20

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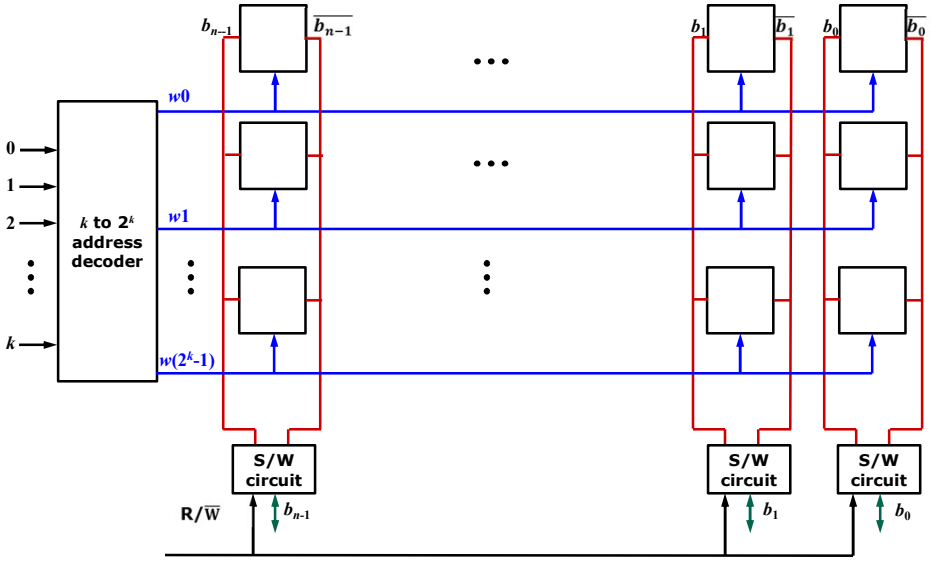
Internal Organization of 2^k x n SRAM Chip



- 1-dimensional address decoding
- This design is not actually used for RAM of any size

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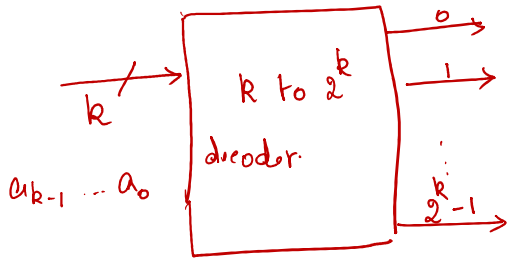
Limitation of 1-dimensional address decoding

→ $2^k \times n$ bit memory



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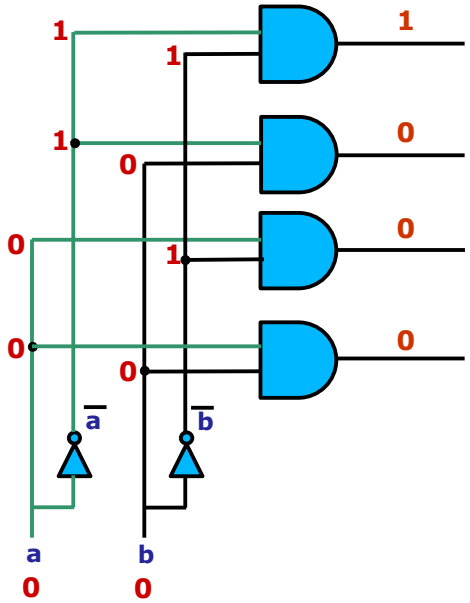
Limitation of 1-dimensional address decoding



2 to 4 decoder

4 - And gates.

2-input AND

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Limitation of 1-dimensional address decoding

→ k to 2^k

→ 2^k AND gates, k input

→ 512 × 8 bit memory

→ 9 to 2^9 address decoder

→ 16 × 4 bit

↓

1M × 4 bit

$2^{20} \times 4$. 20 to 2^{20} decoder.

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Motivation for 2-dimensional address decoding

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Reference

- **Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", 5th Edition, Tata McGraw Hill, 2002**

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Thank You

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