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National Institute of Technology Goa

Programme Name: **B.Tech.**

End Semester Examinations, May-2022

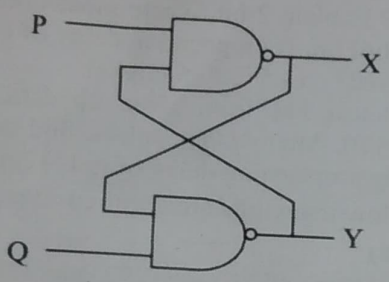
Course Name: Digital Systems Design (DSD) | Course Code: CS 250

Date: **20.5.22** | Time:9:30 AM-12:30 PM

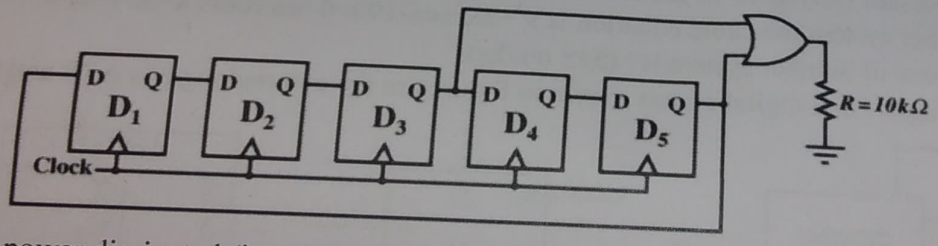
Duration: **3 Hours** | Max. Marks: **100**

ANSWER ALL QUESTIONS

1. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = "0". If the input condition is changed simultaneously to P = Q = "1", the outputs X and Y are (5 marks)



2. Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor $R = 10$ $k\Omega$ and the supply voltage is 5 V. The D flip-flops D1, D2, D3, D4 and D5 are initialized with logic values 0, 1, 0, 1 and 0, respectively. The clock has a 30% duty cycle. (5 marks)

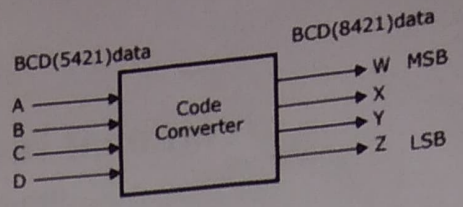


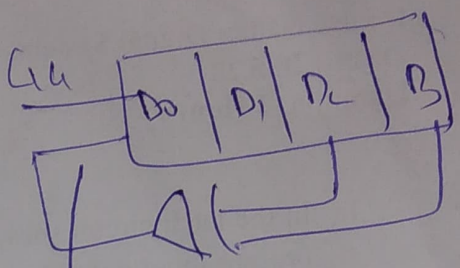
The average power dissipated (in mW) in resistor R is _____.

3. A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 seconds, YELLOW is turned on for 5 seconds and the RED is turned on for 75 seconds. This traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock of 5 second period. The minimum number of flip-flops required to implement this FSM is _____. (5 marks)

4. A 'code converter' is to be designed to convert from the BCD (5421) to the normal BCD (8421). The input BCD combinations for each digit are below. A block diagram of the converter is shown in figure. (5 marks) 7 4 m

Decimal	BCD(5421)			
	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	0	0
6	1	0	0	1
7	1	0	1	0
8	1	0	1	1
9	1	1	0	0





(A) Draw K-map for outputs, W, X, Y, and Z.
(B) Obtain minimized expression for the outputs W, X, Y, and Z.

5. What is Decade Counter? Explain 2-bit Synchronous counter by JK flip-flops? A 4 bits mod 16 counter is made by JK FlipFlip. If propagation delay of each FlipFlop is 50 nsec, the maximum clock frequency can be used? (3.5+3.5+5 marks).
6. Make a circuit which detect 111 from given i/p data, X=101111011111? A 4-bit serial in parallel shift register is 0110. After 4 clock pulses, find the content of shift register? (5+3 marks)
7. A certain JK flip-flop has propagation delay of tpd=12 nsec. The largest ripple counter that can operate at 10 MHz is? How many bits are required to represent (i) 10 digit decimal (ii) 11 digit with base 5? (5+5 marks)
8. Perform Hexadecimal addition $(IF2E)_{16}+(2F31)_{16}+(3C2A)_{16}$. List some applications of NOT gate? (2+3 marks)
9. Minimum number of 2x1 MUX required to implement AND and NOR gate? Represent the given ASCII code "Bb48" in binary? (3+2 marks)
10. Represent $(231.75)_{10}$ in IEEE 754 floating point single precision 32 bit format? In a particular number system the cubic equation is $x^3+bx^2+cx-190=0$ has roots x=5, x=8, x=9. On the base 10, the base of number system is? (5+5 marks)
11. The inputs to a digital circuit shown in Figure are the external signals A, B and C. (6 marks)

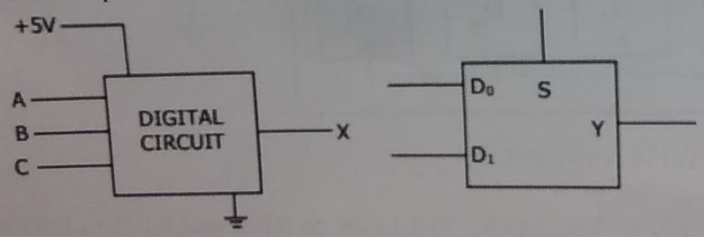


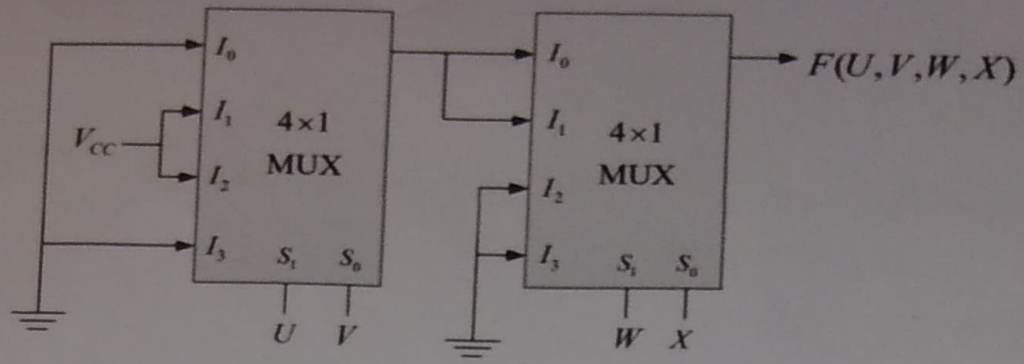
Table1	
S	Y
0	D_0
1	D_1

($\overline{A}$ $\overline{B}$ and $\overline{C}$ are not available). The +5V power supply (logic 1) and the ground (logic 0) are also available.

The output of the circuit is $X=\overline{A}B+\overline{A}\,\overline{B}\,\overline{C}$

- Write down the output function in its canonical SOP and POS forms.
- Implement the circuit using only two 2:1 multiplexers shown in the Figure where S is the data-select line, D_0 and D_1 are the input data lines and Y is the output lines. The function table for the multiplexer is given in table 1.

12. A certain JK flip-flop has propagation delay of t_{pd}=12 nsec. The largest ripple counter that can operate at 10 MHz is? (4 marks)
13. 5 bits data 01101 is given, Represent given data in hamming code representation. (5 marks)
14. A four-variable Boolean function is realized using 4x 1 multiplexers as shown in the figure. The minimized expression for F (U, V, W, X) is? (5 marks)



15. A 16 Kb (=16,384 bit) memory array is designed as a square with an aspect ratio of one (number of rows is equal to the number of columns). The minimum number of address lines needed for the row decoder is _____ ? Justify how NAND gate qualifies to be called as universal gate? (2+3 marks)
16. Design TTL NAND gate with Totempole output? (5 marks)