

# Multiplier for Positive/Unsigned Nos

$$\begin{array}{r}
 \begin{array}{cccc}
 1 & 1 & 0 & 1 \\
 1 & 0 & 1 & 1
 \end{array}
 \begin{array}{l}
 (13) \text{ Multiplicand (M)} \\
 (11) \text{ Multiplier (Q)}
 \end{array} \\
 \hline
 \begin{array}{cccc}
 1 & 1 & 0 & 1 \\
 1 & 1 & 0 & 1 \\
 0 & 0 & 0 & 0 \\
 1 & 1 & 0 & 1
 \end{array} \\
 \hline
 \begin{array}{cccccc}
 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1
 \end{array}
 \begin{array}{l}
 (143) \text{ Product}
 \end{array}
 \end{array}$$

① M, Q : h-bit numbers  
P : 2h-bit numbers

② Multiplier bit  
= 1 Multiplicand - suitable shifting  
= 0 Not added.

$M, Q: 5 \text{ bits}$

$p = 10 \text{ bit}$

$$\begin{array}{r} 11001 \\ \underline{11110} \end{array}$$

(25) M

(30) Q

0 0 0 0 0

1 1 0 0 1

1 1 0 0 1

1 1 0 0 1

1 1 0 0 1

1 0 1 1 1 0 1 1 1 0 (750) P

Long-hand

$$m_3 \quad m_2 \quad m_1 \quad m_0$$

1 1 0 1

1 0 1 1

$$q_3 \quad q_2 \quad q_1 \quad q_0$$

$M_3 \rho_0$   $M_2 \rho_0$   $M_1 \rho_0$   $M_0 \rho_0$

1 1 0 1

$$m_3 q_1 \quad m_2 q_1 \quad m_1 q_1 \quad m_0 q_1$$

1101

$m_1 g r_2$     $m_2 g r_2$     $m_1 g r_2$     $m_0 g r_2$

$m_3 q_3$     $m_2 q_3$     $m_1 q_3$     $m_0 q_3$

1

$\begin{array}{ccccccc} | & \bigcirc & \bigcirc & \bigcirc & | & | & | \\ P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0 \end{array}$

$$P_0 = m_0 q_0$$

$$P_1 = m_1 q_0 + m_0 q_1$$

$$P_2 = m_2 q_0 + m_1 q_1 + m_0 q_2$$

$$P_3 = m_3 q_0 + m_2 q_1 + m_1 q_2 + m_0 q_3$$

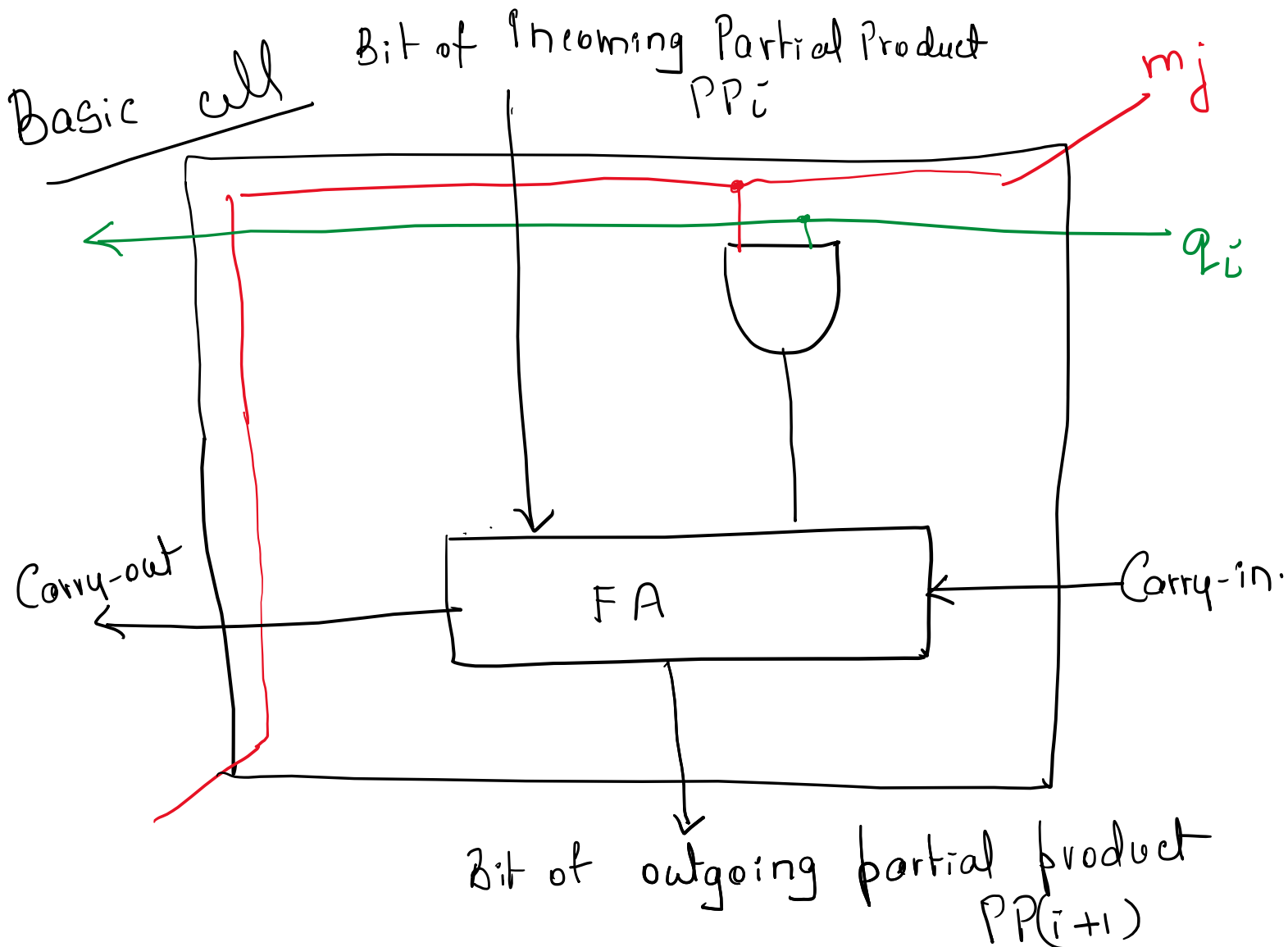
$$P_4 = m_3 q_1 + m_2 q_2 + m_1 q_3$$

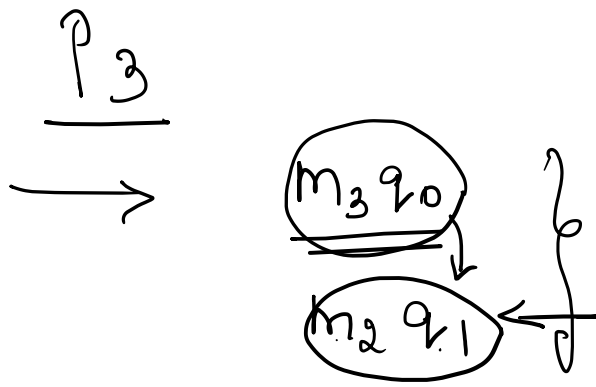
$$P_5 = m_3 q_2 + m_2 q_3$$

$$P_6 = m_3 q_3$$

$$P_7 = \text{Carry-out}$$

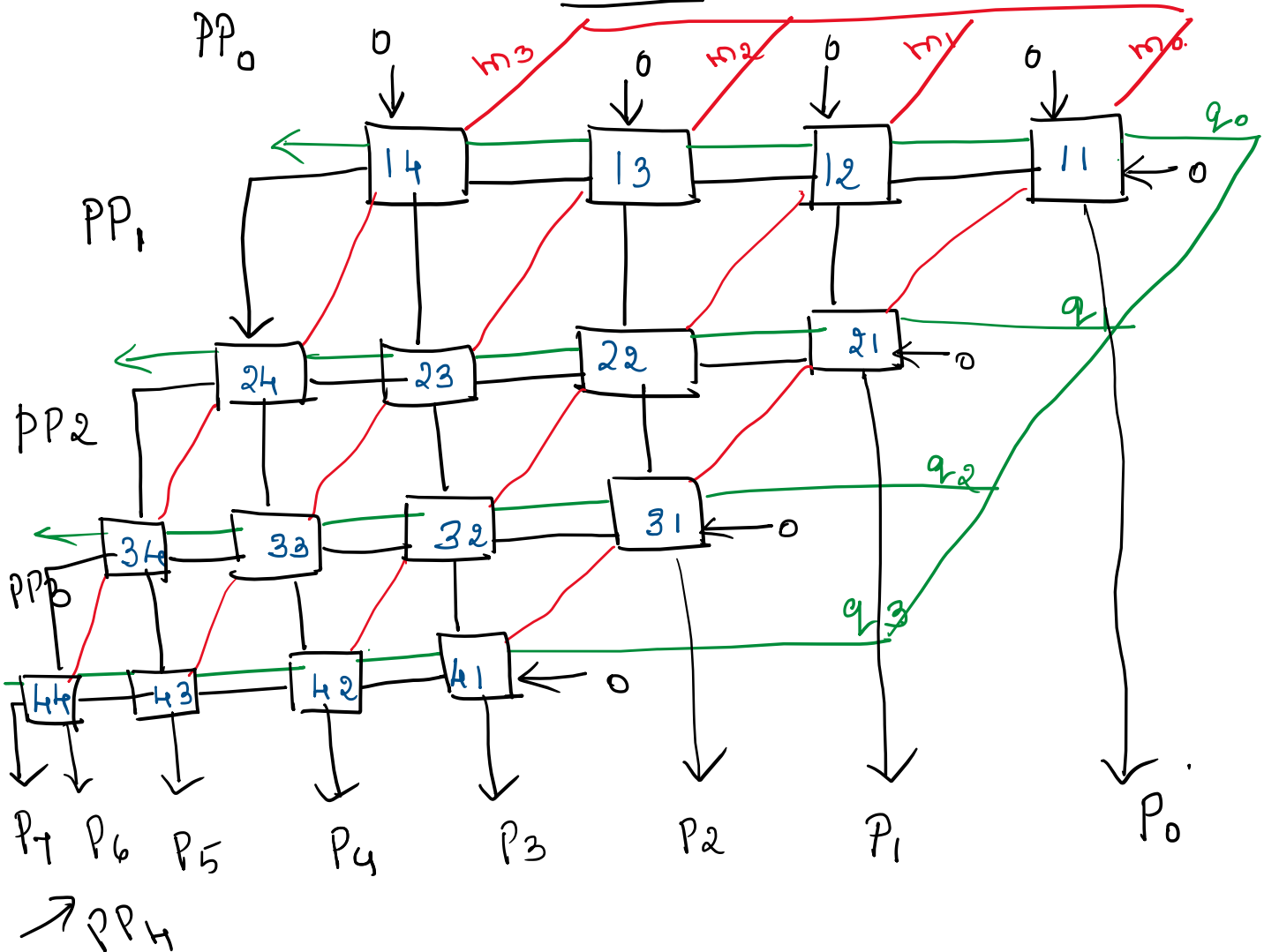
AND GATE  
FULL ADDER





$m_1 q_2$  ←

$m_0 q_3$



COMBINATIONAL ARRAY MULTIPLIER

$$\underline{q_i = 1}$$

Add multiplicand

## Delay Computation

First row: Since all incoming PP bits,  $PP_0 = 0$ ,  
only AND gates needed;

→ 1 tpd. → (1)

→ 1 tpd → (A)

Rows 2 & 3: CUs 1 & 2 contribute to longest  
Signal path

→  $\bar{F}A$

$n-2$  rows

Each row: 4 tpd.

→  $2 \times 2 = 4$  tpd in each

No of rows = 2.

Total →  $2 \times 4 = 8$  tpd.

$(n-2) 4$  delay.

→ (B)

→ (2)

Last Row : RCA : 8 tpd. → (3)

$n$  bit :  $2n$  tpd. → (C)

$$\begin{aligned}\text{Total delay} &= \textcircled{1} + \textcircled{2} + \textcircled{3} \\ &= 1 + 8 + 8 \\ &= \underline{17 \text{ tpd.}}\end{aligned}$$

$$\begin{aligned}\text{Total delay: } &\textcircled{A} + \textcircled{B} + \textcircled{C} \\ &= 1 + (n-2)4 + 2n \\ &= 1 + 4n - 8 + 2n \\ &= 6n - 7 \\ &= 6n - 6 - 1 \\ &= \underline{6(n-1) - 1}\end{aligned}$$

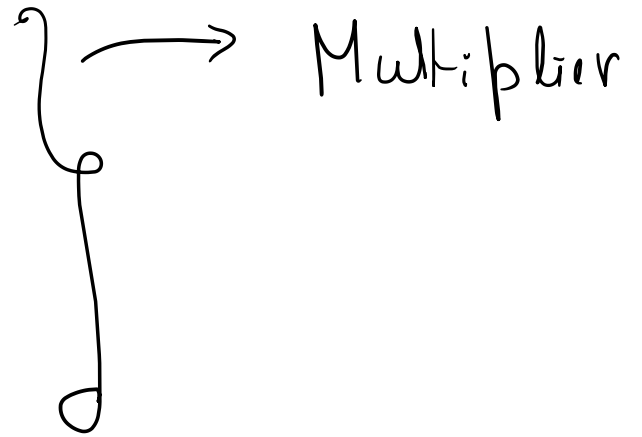
### Observation

- Easy to understand
- Many gates

Mixture of combinational array techniques  
and sequential techniques  
↳ less combinational logic

Combinational logic

Sequential logic



Multiplier