INTRODUCTION

The IC is a single chip driver & controller LSI for graphic dot-matrix liquid crystal display systems. This chip can be connected directly to a microprocessor, accepts serial or 8-bit parallel display data from the microprocessor, stores the display data in an on-chip display data RAM of 65 x 132 bits and generates a liquid crystal display drive signal independent of the microprocessor. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. It contains 65 common driver circuits and 132 segment driver circuits, so that a single chip can drive a 65 x 132 dot display.

This chip is able to minimize power consumption because it performs display data RAM read / write operation with no external operation clock. In addition, because it contains power supply circuits necessary to drive liquid crystal, which is a display clock oscillator circuit, high performance voltage converter circuit, high-accuracy voltage regulator circuit, low power consumption voltage divider resistors and OP-Amps for liquid crystal driver power voltage, it is possible to make the lowest power consumption display system with the fewest components for high performance portable systems.

FEATURES

Power Supply
- Logic Power VDD1 –GROUND = 2.4V ~ 3.6V
- Analog Power VDD2 –GROUND = 2.4V ~ 3.6V
- LCD Driving V0 – GROUND = 13.5V (Max)

Display Driver Output Circuits
- 65 common outputs / 132 segment outputs
- Display Duty = 1/33,1/49,1/55 1/65 select by SEL0/SEL1
- Applicable Bias: 1/5 ~ 1/9,select by SEL0/SEL1

On-chip Display Data RAM
- RAM size : 65x132 =8,580 bits

Built-in Analog Circuit
- Reduced external parts (1 capacitors only)
- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter (with booster ratios x4/x5)
- High accuracy reference voltage generator
- Electronic contrast control (64 steps)
- Embedded V0 Voltage regulator
- High performance voltage follower (V1 ~ V4 voltage generator with output buffer inside)
- Temperature compensation on V0 voltage

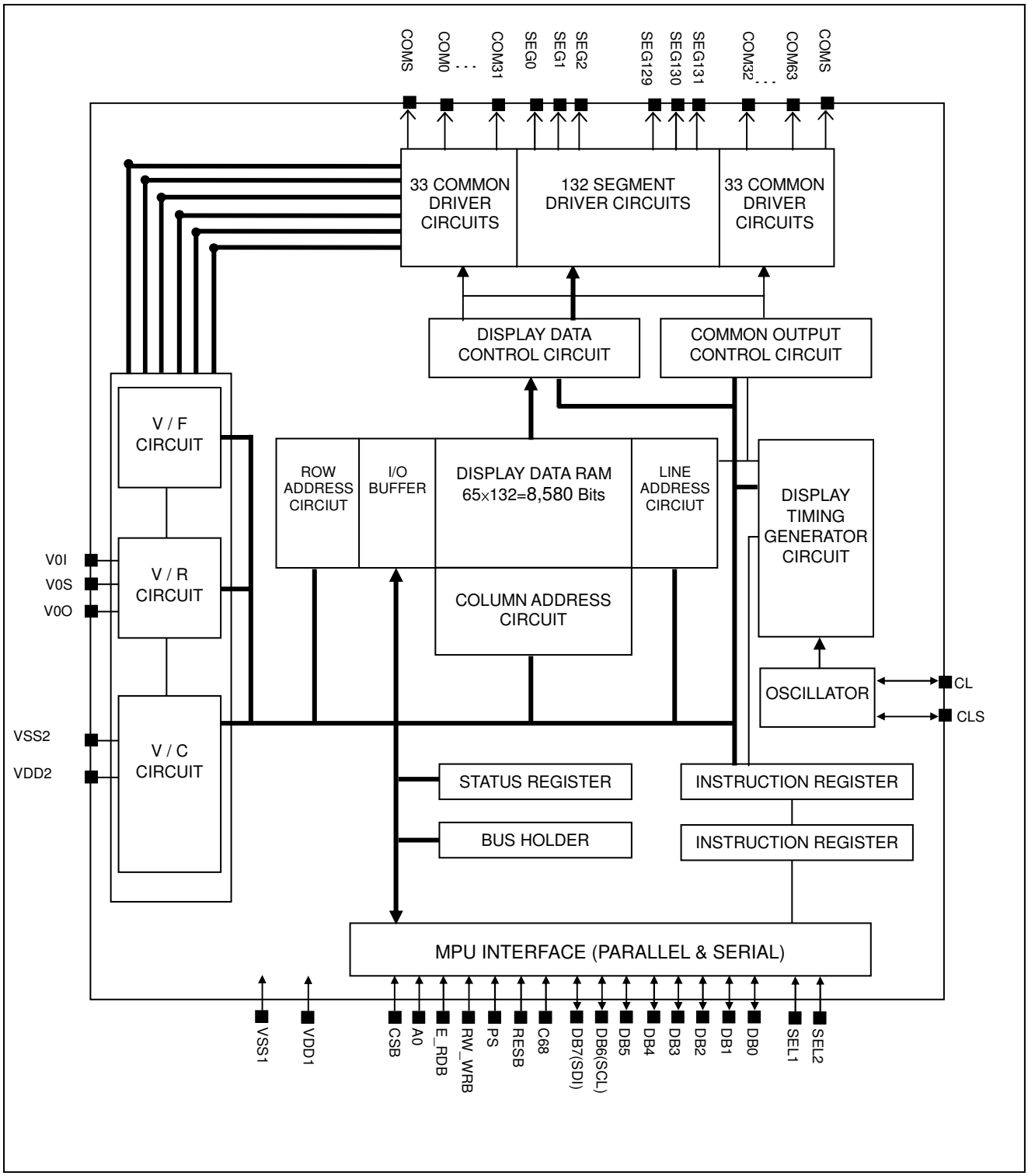
Microprocessor Interface
- High-speed 8080/6800-series 8-bit parallel bi-directional interface
- Serial 4 line Write/Read interface

Various Function Set
- Display On/Off control
- Set display starting line,
- Set row/column address
- Software reset
- Reverse display
- COM/SEG output direction control
- Display power control
- LCD Contrast (V0) control

Operating Temperatures
- Wide range of operating temperatures from -30℃ to 80℃

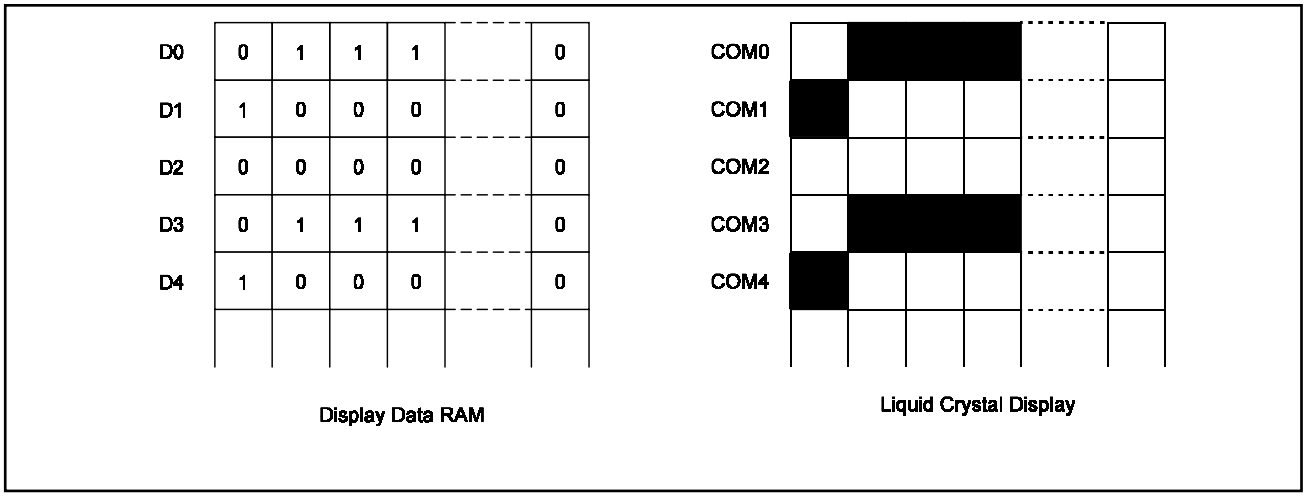
Package Type
- COG(Gold-bumped bared chip)

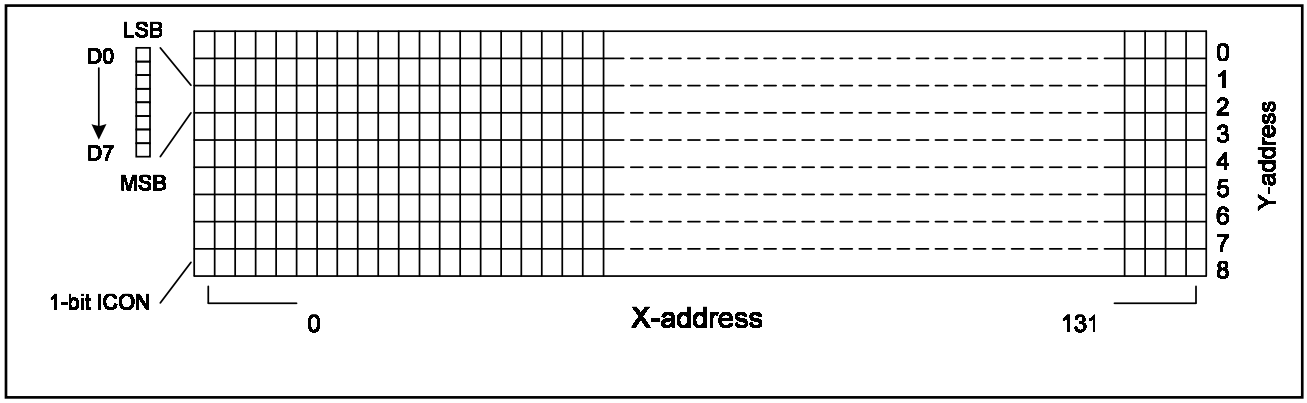
BLOCK DIAGRAM

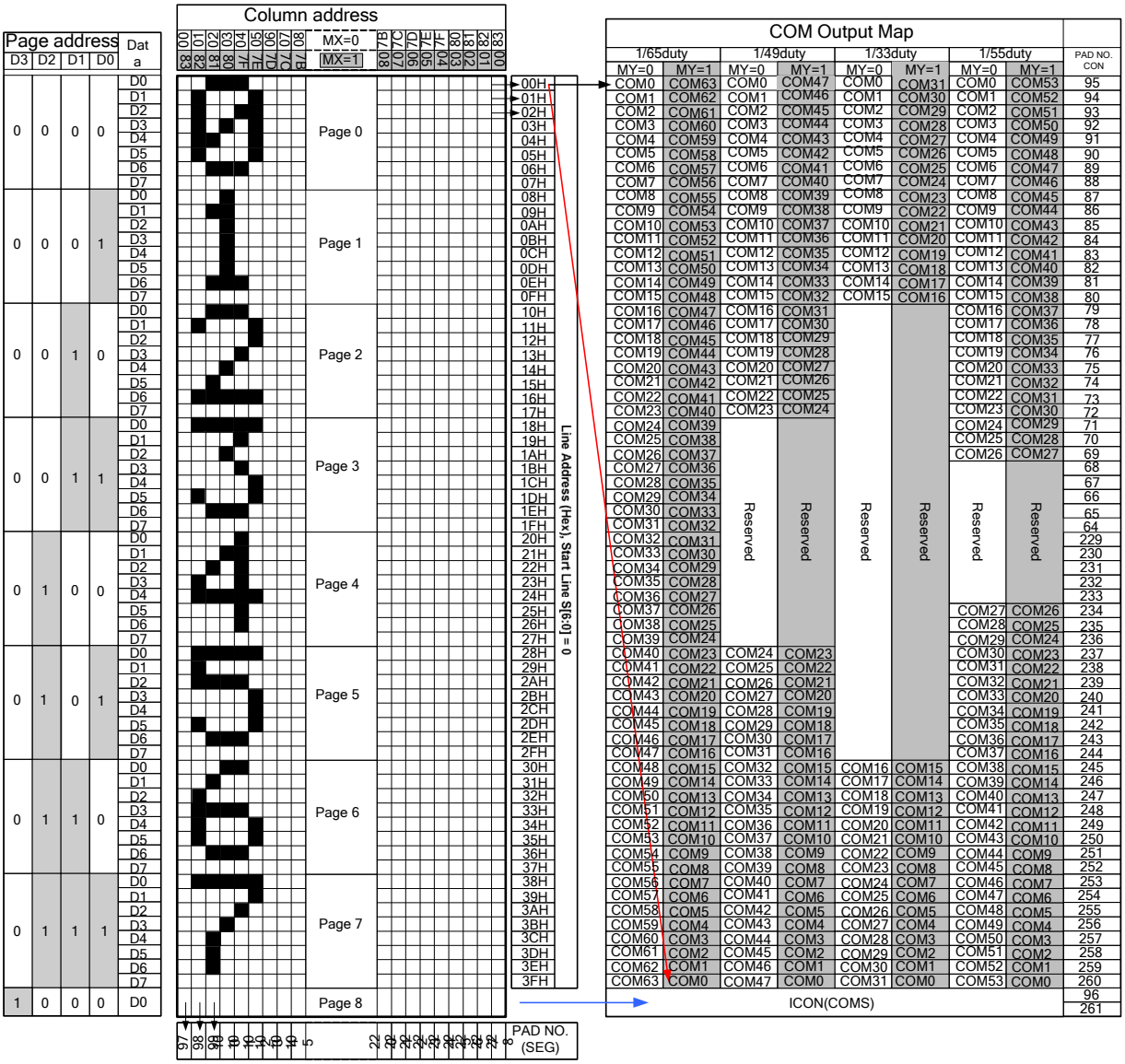


Display RAM Address Mapping

IC is built-in a RAM with 65X132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Fig 7 for detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Fig 8 for detailed illustration. The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.



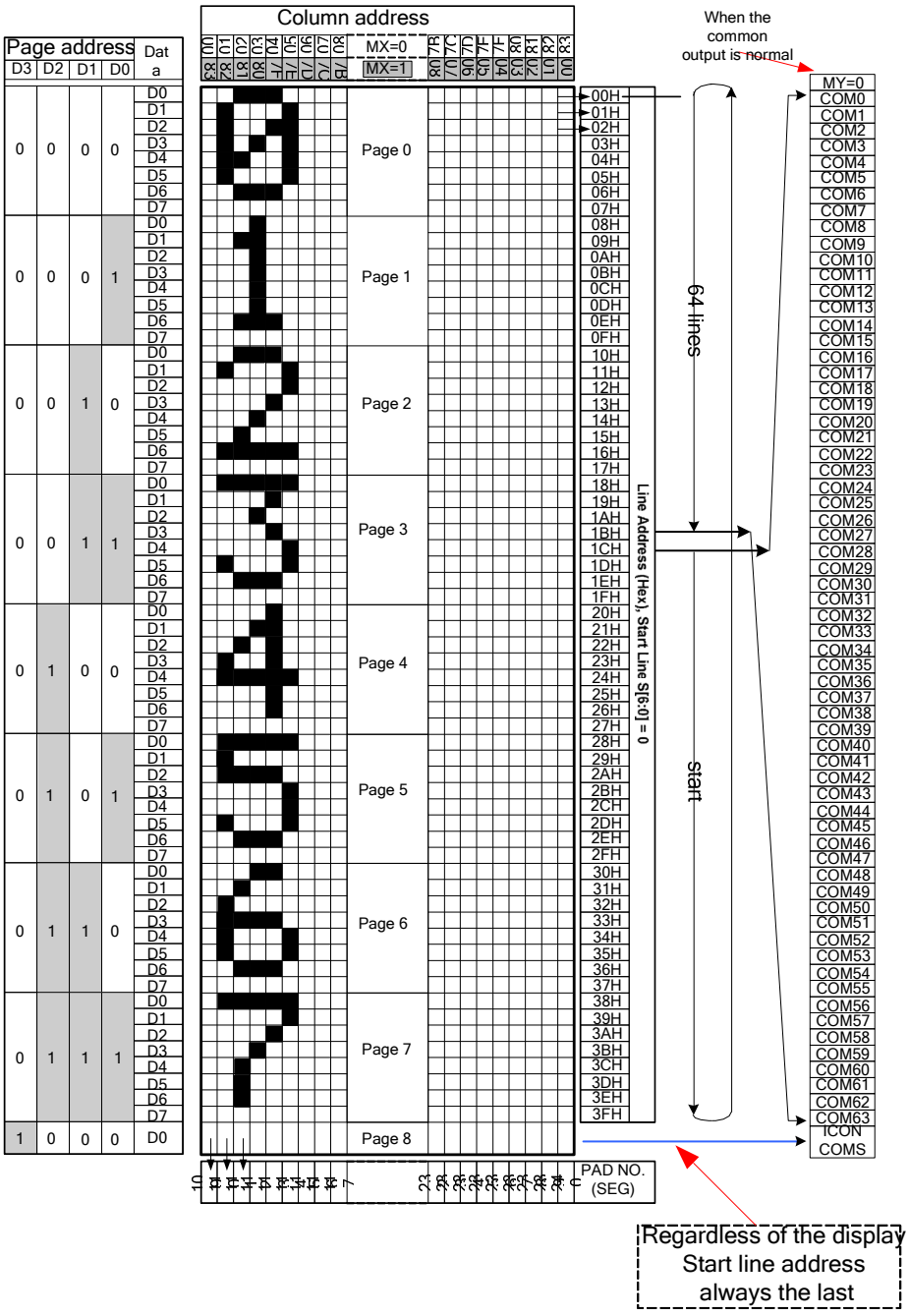




DDRAM and Output Map（COM/SEG）

Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the "Display Start Line Set" instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, IC can realize the screen scrolling without changing the contents of DDRAM as shown in bellow. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.



Reset Initialization

The IC provides both hardware (H/W) reset and software (S/W) reset function. When the RESB is setting to "L", the H/W reset will be activated, or user can use S/W reset instruction to initialize the internal registers' configurations, but the H/W reset and S/W reset covered range is different, please check the table listed as below.

The default H/W reset initializing settings are listed as below:

No.	Register	Description
1.	AY=0	Page address
2.	AX=0	Column address
3.	ST=0	Display start line address = 0
4.	MY=0	COM output direction COM0 → COM63
5.	RR[2:0]=(1,0,0)	V0 Regulation Ratio
6.	EV[5:0]=(0,0,0,0,0,0)	Electronic volume register
7.	Exit Test Mode	
8.	DON=0	Display OFF, SEG/COM output GROUND level
9.	REV=0	Reverse display OFF
10.	AP=0	Entire display OFF
11.	MX=0	SEG output direction SEG0 → SEG131
12.	(internal status)	Serial interface internal register data clear
13.	BS=0	LCD bias
14.	BL=0	Booster Level
15.	Exit Power Saving Mode	
16.	VB=0;VR=0;VF=0	Power Control OFF

★ For S/W reset , only the 1 ~ 7 items above will be reinitialized.

When doing the H/W reset (RESB = "L"), the V0 will also discharge to GROUND level internally, so when using external LCD power sources, please input these power sources only when the H/W reset process has been finished (RESB is backing to "H") .

Command Table

NO.	INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
1	Display on/off	0	0	1	0	1	0	1	1	1	DON	DON=1, display ON DON=0, display OFF
2	Set start line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Set Display start line
3	Set page address	0	0	1	0	1	1	AY3	AY2	AY1	AY0	Set page address
4	Set column address	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set column address
		0	0	0	0	0	1	AX7	AX6	AX5	AX4	
5	Write data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
6	Read data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
7	SEG direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
8	Inverse display	0	0	1	0	1	0	0	1	1	INV	INV =0, normal display,INV =1, inverse display
9	ALL pixel on	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
10	Bias select	0	0	1	0	1	0	0	0	1	BS	Select bias setting,0=1/9; 1=1/7 (at 1/65 duty)
11	Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
12	END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
13	RESET	0	0	1	1	1	0	0	0	1	0	Software reset
14	COM Direction	0	0	1	1	0	0	MY	0	0	0	Set output direction of COM MY=1, reverse direction MY=0, normal direction
15	Power control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
16	Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
17	SET EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
		0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
18	Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL=0: 5X BL=1: 4X
				0	0	0	0	0	0	0	BL	
19	Power save	Compound Command										Display OFF + All Pixel ON
20	Nop	0	0	1	1	1	0	0	0	1	1	No operation (dummy command)
21	Spi4 Read Ram	0	0	0	0	1	1	0	1	1	1	spi read ram data command

COMMAND DESCRIPTION

Display ON / OFF

LCD display ON / OFF select

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1 Display ON
DON = 0 Display OFF

Display Starting Line

Set the starting line address for the first common output.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
…	…	…	…	…	…	…
1	1	1	1	1	1	63

Note: When DON=0, set Start line command

Set Page Address

AY[3:0] defines the Y address vector address of the display RAM

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	AY3	AY2	AY1	AY0

AY3	AY2	AY1	AY0	Page Address	Valid Bit
0	0	0	0	Page0	DB0~DB7
0	0	0	1	Page1	DB0~DB7
0	0	1	0	Page2	DB0~DB7
. .	. .	. .	. .	. .	. .
0	1	1	0	Page6	DB0~DB7
0	1	1	1	Page7	DB0~DB7
1	0	0	0	Page8(icon page)	DB0

Set AX Address

Sets the Column Address of display data RAM for MPU Write/Read access. After setting the row and/or Column address, user can write/read the internal display RAM consecutively. The Column address will auto-incremented by +1 .

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	AX7	AX6	AX5	AX4
0	0	0	0	0	0	AX3	AX2	AX1	AX0

Write Display Data

8-bit display data can be written to the display RAM location specified by the column address and row address by this instruction. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed rows.

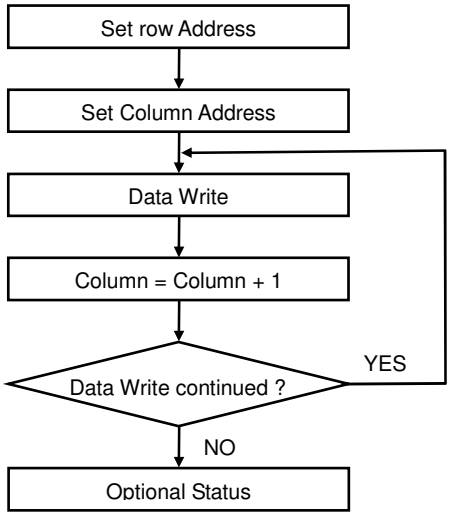
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

Data Read Display Data

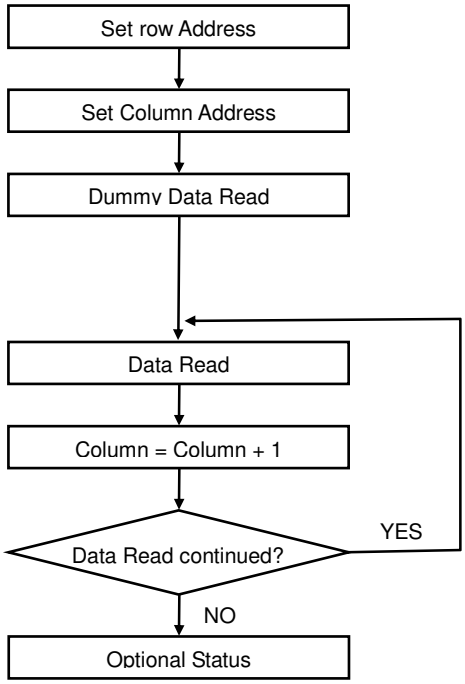
8-bit display data RAM specified by the column address and row address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously can continuously read data from the addressed row. A dummy read is required after specified the target column and/or row address.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Display RAM Write Sequence



Display RAM Read Sequence



SEG Direction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: Normal direction(SEG0->SEG131) MX=1: Reverse direction (SEG131->SEG0)

Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (white -> Black, Black-> White) while the display data in the Display Data RAM is never changed.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV=1: Inverse display

All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP =0: Normal display AP =1: All pixels ON

Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	BS

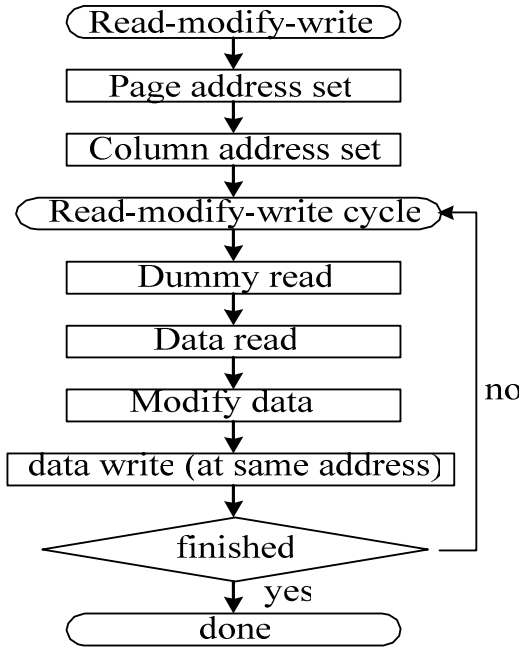
Duty	Bias	
	BS=0	BS=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

Read-modify-Write

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address . (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

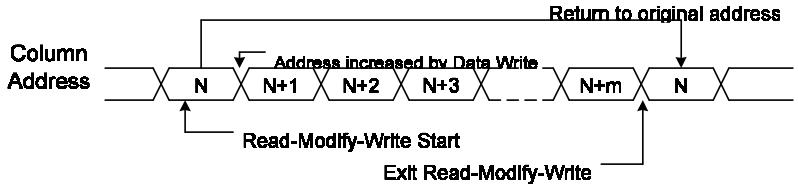
* In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used



END

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address. it was when the Read-modify-Write instruction was entered.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0



S/W Reset

This instruction will activate the internal S/W reset operation. The covered ranged is different with H/W reset, for details please refer to the “Reset Initialization” section.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

COM Direction

This instruction controls the common output status which changes the vertical display direction. The detailed information can be found in Fig 9

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	MY	0	0	0

Flag	Description
MY	MY=0: Normal direction (COM0->COM63) MY=1: Reverse direction (COM63->COM0)

Power Control

This instruction controls the built-in power circuits. Typically, these 3 flags are turned ON at the same time.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VB	VR	VF

Flag	Description
VB	VB=0: Built-in Booster OFF VB=1: Built-in Booster ON
VR	VR=0: Built-in Regulator OFF VR=1: Built-in Regulator ON
VF	VF=0: Built-in Follower OFF VF=1: Built-in Follower ON

Regulation Ratio

This instruction controls the regulation ratio of the built-in regulator.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	RR2	RR1	RR0

RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	3.0
0	0	1	3.5

0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

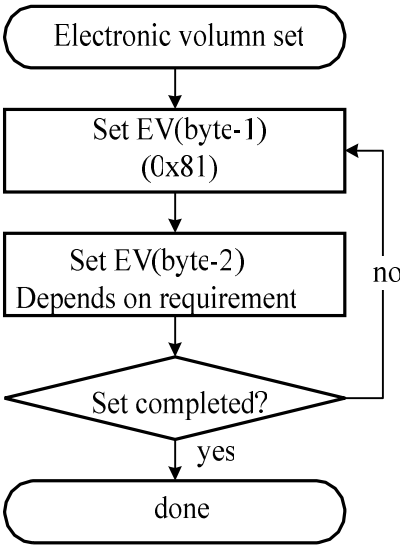
The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])
V0 = RR X [1 – (63 – EV) / 162] X 2.1, or V0 = RR X [(99 + EV) / 162] X 2.1

SYMBOL	REGISTER	VALUE
RR	RR[2:0]	3, 3.5, 4, 4.5, 5, 5.5, 6 and 6.5
EV	EV[5:0]	0~63

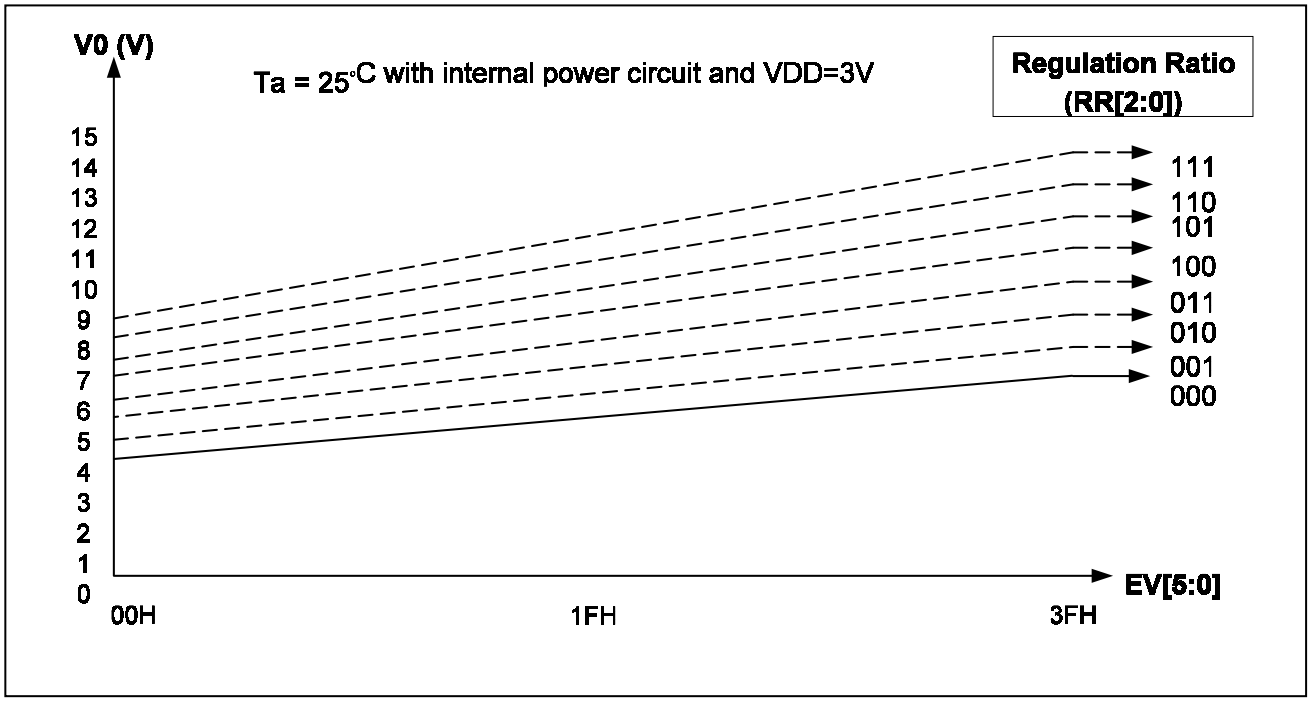
Set EV

This is double byte instruction. The first byte set IC into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1
0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0



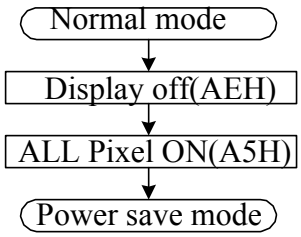
The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curves can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment. Please refer to the "Selection of Application Voltage" section for detailed information



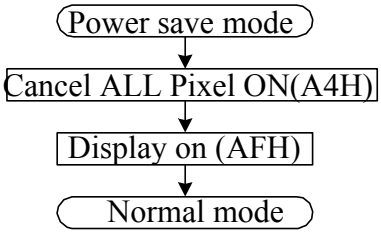
Power Save (Compound Instruction)

This is compound instruction. The 1st instruction is Display OFF (DON=0) and the 2nd instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.



Enter power save mode



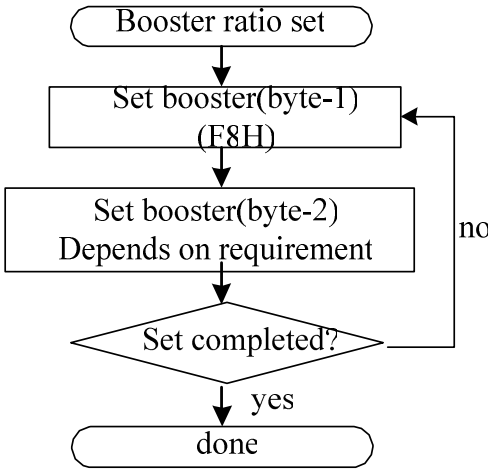
Exit power save mode

Set Booster

This is double byte instruction. The first byte set IC into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. IC booster is built-in booster capacitors. The only external component is a keep capacitor between V0 and GND. Booster level can be changed with instruction only without changing hardware connection

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	0	BL

BL	Boost Level
0	X5
1	X4



NOP

"No Operation" instruction. IC will do nothing when receiving this instruction.

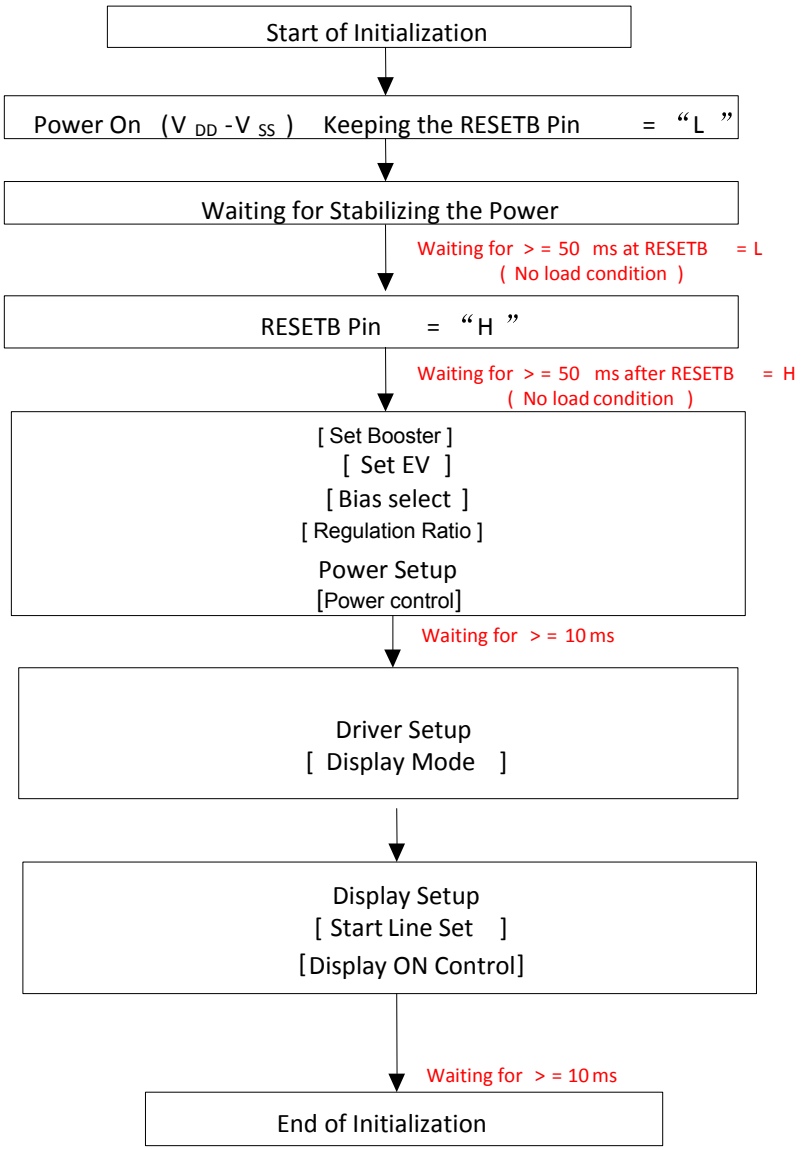
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

SPI4 READ RAM DATA

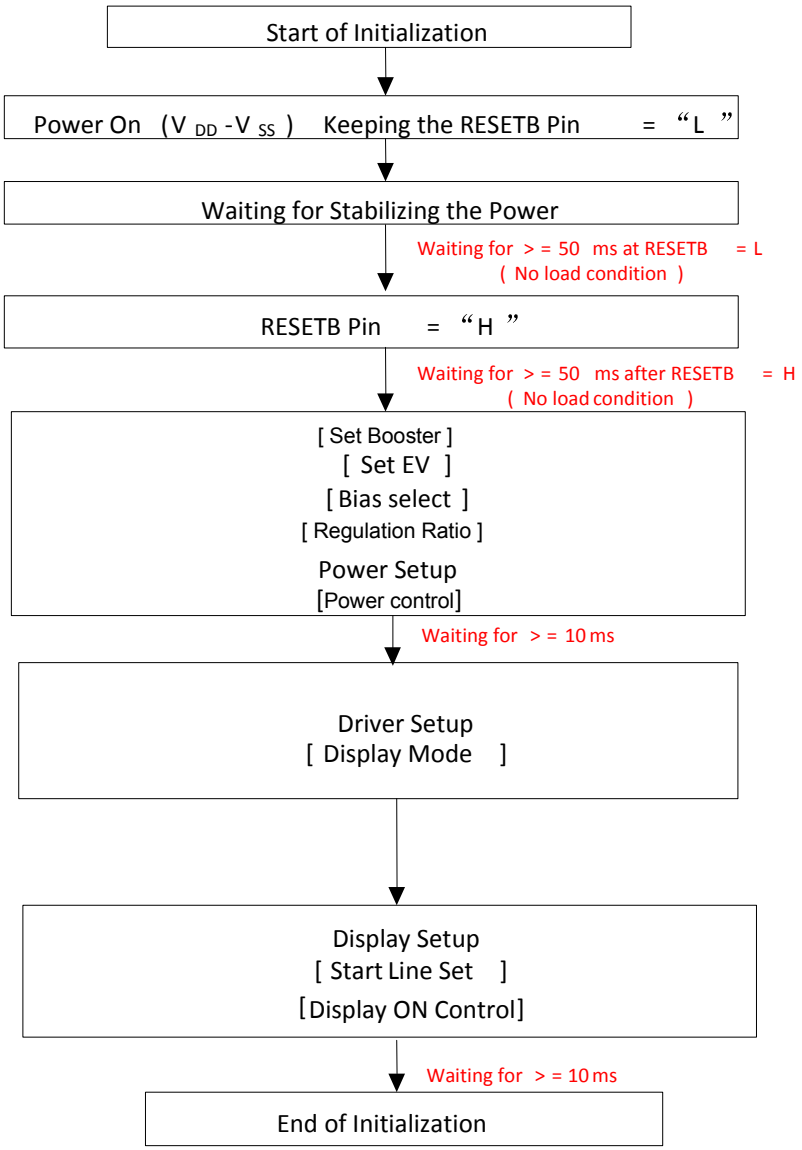
Spi4 read ram data. IC will read ram data after setting this command.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	1	1	1

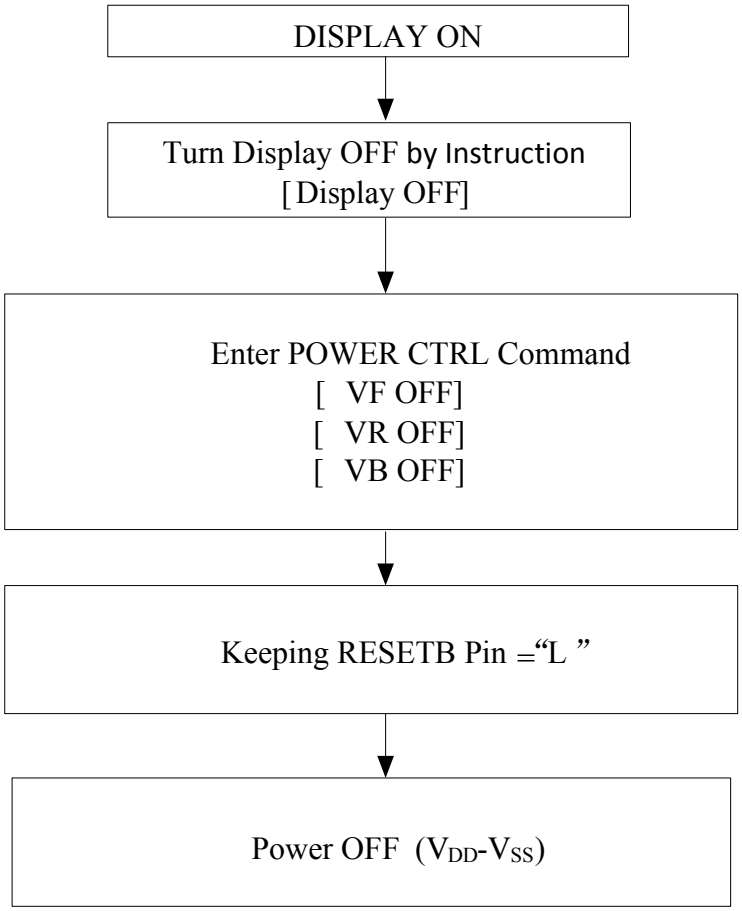
Power On Sequence (VDD>=2.4)



Power on Sequence (VDD1=VDD2=1.8V)



Power off Sequence



APPLICATION WITH VDD1=VDD2=1.8V

When VDD1/VDD2/=1.8V, It needs new equation to calculate the V0 voltage:

V0=RR*1.9*(99+CT)/162
NOTE: V0<7.5, AND CT<49 is necessary to keep equation accurate and linear

Booster and RR and CT could adjust and get enough V0 for LCD DRIVER.

Power Supply Circuits

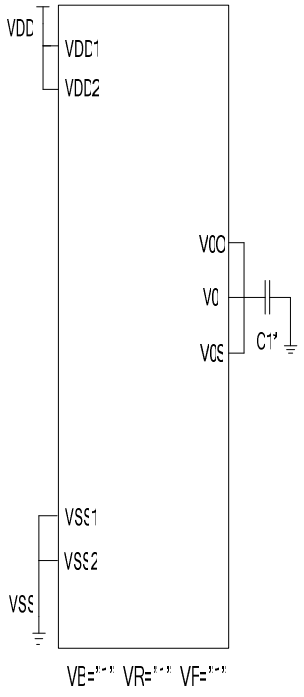
The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are two modules, voltage converter circuits (VB) and voltage follower circuits (VF). They are valid only in master operation and controlled by power control instruction. The possible LCD power supply configurations are listed as below.

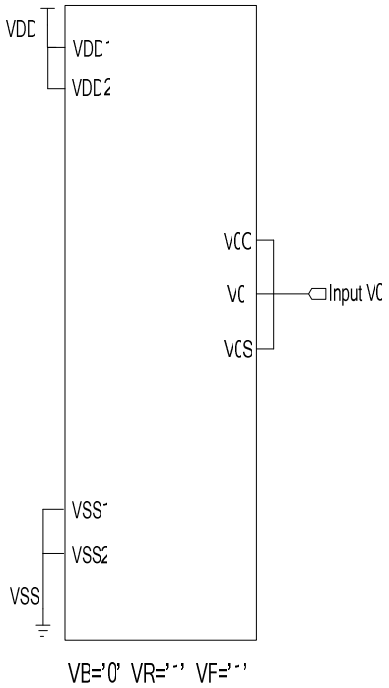
Power Supply Configurations

Power Configuration	Instruction (VB VR VF)	VB circuits	VR circuits	VF circuits	V0O V0I V0S
Internal power supply circuits are used	(1 1 1)	ON	ON	ON	Open*1
Only the voltage follower circuits are used	(0 1 1)	OFF	ON	ON	External input

<Note>

* 1 V0O, V0I and V0S are short together by ITO. When VB="1", connect external stabilizing capacitors to GROUND.





C1*=0.01~4.7uF

Voltage Follower Circuits

The Voltage Follower circuits resistively divide the liquid crystal operating voltage (V0) into four voltage levels (V1, V2, V3 and V4) and these voltage levels will be buffered output to serve as the LCD driving power sources.

Bias	V1	V2	V3	V4
1/9*	8/9 x V0*	7/9 x V0*	2/9 x V0*	1/9 x V0*
1/8	7/8 x V0	6/8 x V0	2/8 x V0	1/8 x V0
1/7	6/7 x V0	5/7 x V0	2/7 x V0	1/7 x V0
1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0

* Default Value

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VDD1/VDD2	-0.3 ~ 7	V
	V0O/V0I/V0S	-0.3 ~ 13.5	V
Input voltage range	V_{IN}	-0.3 to V_{DD1} + 0.3	V
Operating temperature range	T_{OPR}	-40 to +85	℃
Storage temperature range (Bare chip)	T_{STR}	-55 to +125	℃

NOTES:

1. VDD1/VDD2 and V0 are based on VSS1/VSS2 = 0V
2. The Voltage levels relation V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥VSS1/VSS2 = 0V must always be satisfied.
3. If supply voltage exceeds the absolute maximum range, this LSI may be damaged permanently.

DC CHARACTERISTICS

(Ta = -30 to 80℃)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage(1)		VDD1		2.4	-	3.6	V	VDD1 *1
Operating Voltage(2)		VDD2~3		2.4	-	3.6	V	VDD2~3 *9
Operating Voltage(3)		V0O/V0I/ V0S		4.0	-	13.5	V	V0O/V0I/ V0S *2
Input voltage	High	V_{IH}		0.8*V_{DD1}	-	V_{DD1}	V	*3
	Low	V_{IL}		V_{SS1}	-	0.2*V_{DD1}		
Output voltage	High	V_{OH}	I_{OUT} = 1mA, VDD1=2.4V	0.8*V_{DD1}	-	V_{DD1}	V	*4
	Low	V_{OL}	I_{OUT} = -1mA, VDD1=2.4V	V_{SS1}	-	0.2*V_{DD1}		
Input leakage current		I_{IL}	V_{IN} = V_{DD1} or V_{SS1}	-1.0	-	+1.0	µA	*5
Output leakage current		I_{OL}	V_{IN} = V_{DD1} or V_{SS1}	-3.0	-	+3.0	µA	*6
LCD driver ON Resistance		R_{ON}	Ta = 25℃, V0 = 8.5V	-	0.6	0.8	kΩ	COMx *7
				-	1.3	1.5	kΩ	SEGx *7
Oscillator frequency (internal)		F_{OSC}	Ta = 25℃	2.8	3.0	3.2	MHz	
Oscillator frequency (External)		F_{CL}	Ta = 25℃	-	3.0	-	MHz	CL
Frame Frequency		FR	Duty=1/65, V0=8.5V, Ta=25℃	60	66	75	Hz	
LCD operation Voltage		V0	CT=3F,RR=4 Booster X5, VDD1=VDD2 =3V					

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Pin used
			Min.	Typ.	Max.		
Dynamic current consumption	Idd	VDD1=VDD2 =3.0V Booster X5 V0 = 8.5V, Bias=1/9 Ta=25℃	-	300	400	μA	*8 $I_{VDD1+VDD2+}$
Display OFF	Idd	VDD1=VDD2 =3.0V Booster X5 V0 = 8.5V, Bias=1/9 Ta=25℃	-	95	190	μA	
Power Down	Idd	VDD1=VDD2 =3.0V Ta=25℃	-	1	5	μA	

NOTE

*1. Although the wide range of DC operating voltages is guaranteed, but if the voltage fluctuation is too large during MPU accessing, the performance can't be guaranteed.

*2. In case of external power supply is applied.

*3. CSB, A0, DB0~ DB7, E_RDB, RW_WRB, RESB, C68, PS, CLS, CL, pins.

*4. DB0 ~ DB7

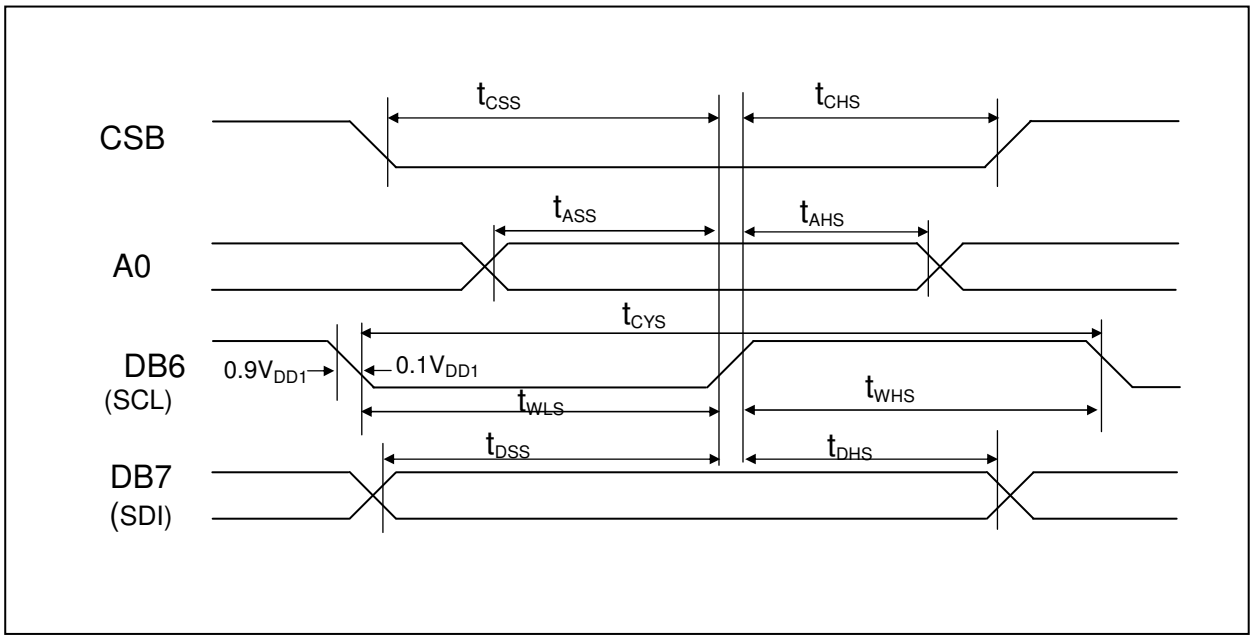
*5. CSB, A0, DB [7:0], E_RDB, RW_WRB, RESB, C68, PS, CLS, CL pins.

*6. Applies when the DB0 ~ DB7pins are in high impedance.

*7. Resistance value when 0.1mA is applied during the ON status of the output pin SEGx or COMx.
RON= ΔV / 0.1 [KΩ] (ΔV: voltage change when 0.1mA is applied in the ON status.)

*8. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU & the LCD outputs (COMx, SEGx) are just floating, without any loading

Serial Interface Characteristics

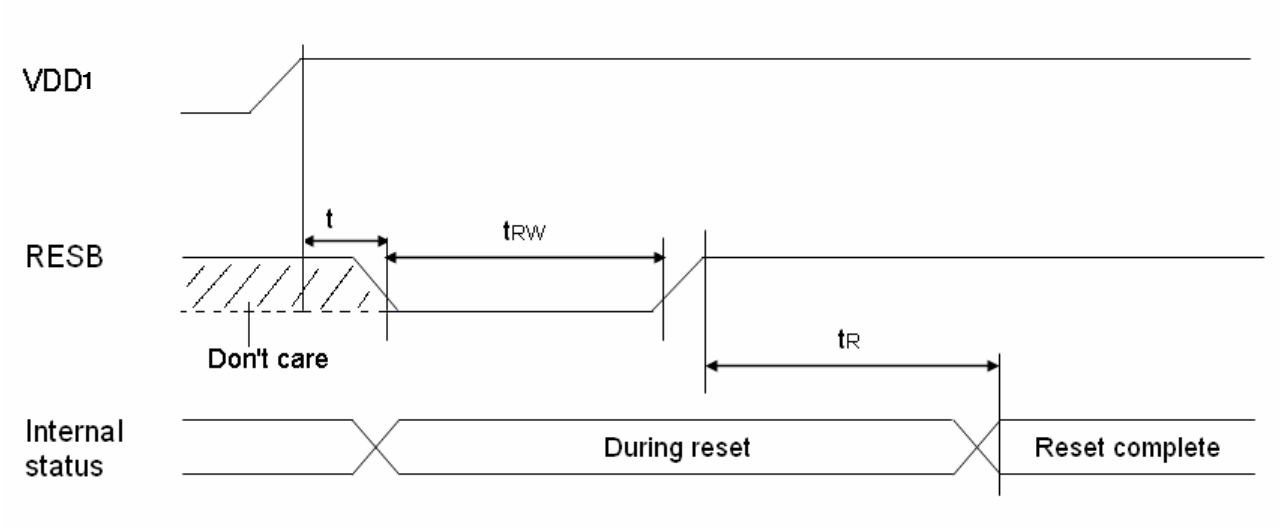


(V_{DD1} = 2.4 ~ 3.6V, Ta = -30~80℃℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB6 (SCL)	t**CYS** t**WHS** t**WLS**	200 90 90	- - -	- - -	ns	
Address setup time Address hold time	A0	t**ASS** t**AHS**	45 45	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	t**DSS** t**DHS**	45 45	- -	- -	ns	
CSB setup time CSB hold time	CSB	t**CSS** t**CHS**	90 90	- -	- -	ns	

Note: All signal Rising time and falling Time <15ns

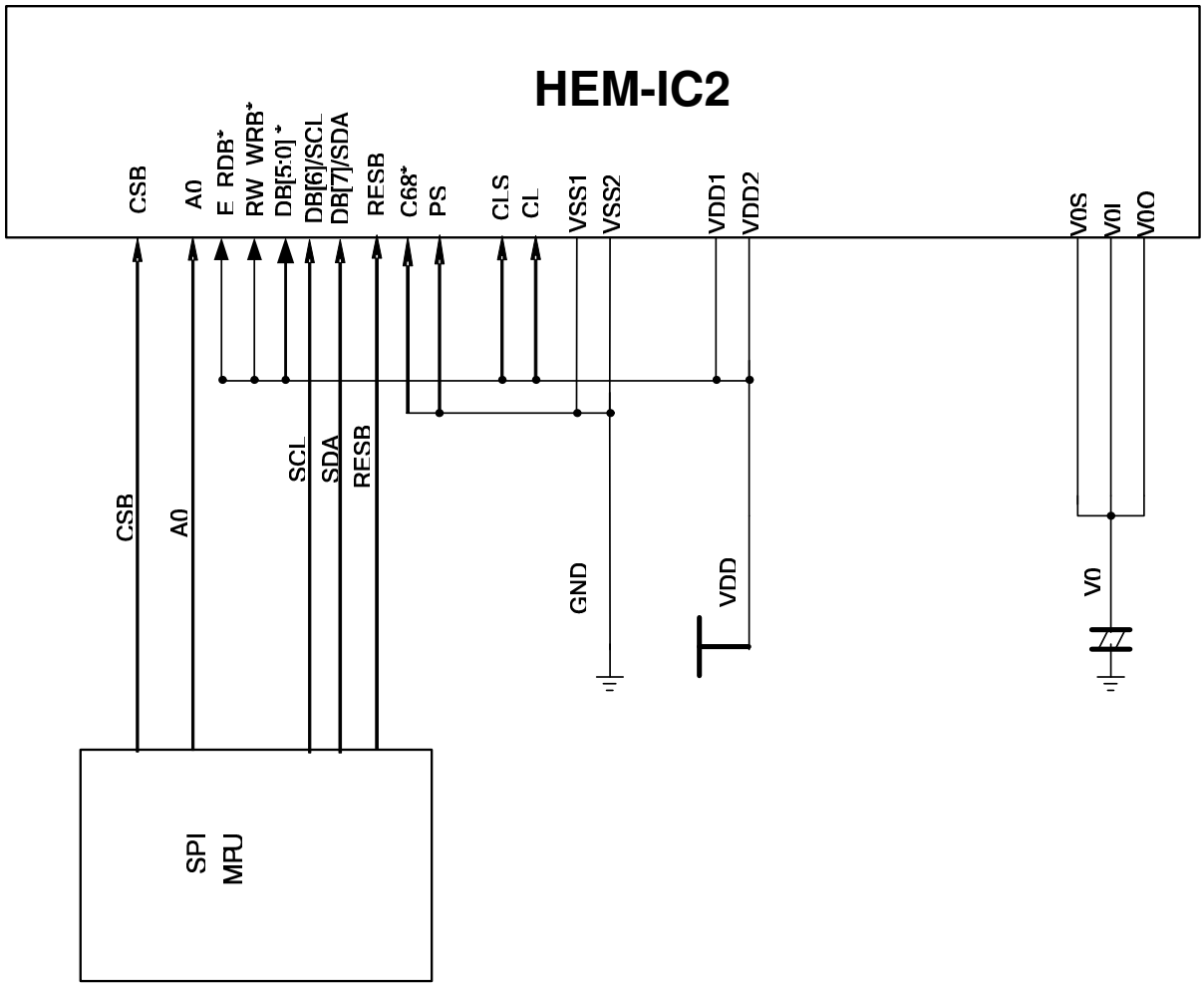
Reset Input Timing



(V**DD1** = 2.4V ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	t**RW**	2	-	-	us	
Reset time	-	t**R**	-	-	2	us	
Reset time	RESB	t	0	-	-	us	

In Case of Serial Interface 4 (PS = "L")



*: No use pin must fix to VSS1 or VDD1

SEL [1:0] refer to the pin definition