Intel® Time Coordinated Compute (TCC) User Guide

June 2024

Intel Confidential

Document Number: 786715

Figures

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Revision History

Date	Revision	Description
August 2023	1.0	Initial External Release
September '23	1.1	Updated with Precision Time Coordination
February'24	1.2	Updated with 14th Gen Intel® Core™ S-Series Processor information and additional content updates
March'24	1.3	Added Intel Atom® X7000RE/C Series processor (Amston Lake) data
May '24	2.0	Added TGPIO pin info, cyclic test command line info, additional information on power management settings and several advanced tuning options; Addition of Intel® Xeon™ D-2896TER KPI data
June'24	2.1	Added enveloping usecase for Intel® Speed Shift Technology for edge compute on 13th Generation Intel® Core™ H-Series processor

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1.0 Introduction

A major shift is happening at the edge in markets such as Manufacturing and Energy, both for Oil & Gas and Utilities, as well as many other market segments spanning Health, Aviation, Retail and many more. This transformation towards software-defined solutions is driven by multiple factors such as reducing cost, new technologies such as AI & 5G, improving quality and efficiency, and changes in the workforce. A key element of this transformation is to support operational workloads on general purpose compute platforms which drives a need to support real-time workloads along with best-effort workloads on the same system. Intel® Time Coordinated Compute (TCC) enabled platforms deliver optimized compute- and time-performance for real-time applications and include support for IEEE** 802.1 Time Sensitive Networking (TSN) over converged networks (wireless and wired).

Intel's Time Coordinated Compute offering comprises of a comprehensive set of optimizations throughout the complete platform stack all the way from Intel silicon to the application layer. These optimizations are designed to make Intel platforms with real-time support achieve high determinism in the presence of best effort workloads running on the same system.

Time Coordinated Compute provides the following key values:

- Timely & reliable data processing: Better out-of-box real-time performance for deterministic workloads
- Doing more with the same system: Maximum efficiencies by aggregating
  real-time and best-effort applications on a single system
- Timely & reliable data delivery: Support for IEEE Time Sensitive Networking (TSN) over converged networks

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* Other names and brands may be claimed as the property of others.

- Future-proofing designs: Scale between Intel Atom® processors, Intel® Core™ processors, and Intel® Xeon® processors as well as across processor generations

The current version of this document describes real-time features and optimizations across several processor families and generations. Some features are not available on all product stock keeping units (SKUs) and product families. Contact your Intel representative for details.

Real-time applications (also called "workloads") must execute within a certain amount of time, consistently, across numerous iterations. While specific requirements vary by use case, real-time applications typically perform the following sequence of tasks:

1. Process new input such as a sensor measurement or camera video streams.
2. Perform a computation such as a new motion vector or object detection bounding box of a computer vision workload.
3. Control an actuator or render a result.
4. Ensure actions are tightly synchronized or happen at the exact same time.

Furthermore, these applications often have a deadline. They must complete the tasks within a certain time, which may range in typical applications from microseconds to milliseconds.

On processors with TCC support, Intel provides the following support for real-time applications:

- Selected processors with features to minimize worst-case execution time (WCET) within the system.
- Selected processors with time synchronization optimizations.
- Ethernet controllers and wireless connectivity solutions that support IEEE 802.1 Time-Sensitive Networking (TSN) standards.
- Validated configuration guidance as the base for Intel's key performance indicators (KPIs) of time performance.
- Reference software to help development of real-time systems using Intel processors and connectivity solutions.

1.1 About This Document

This document provides guidance on how to utilize Intel's platforms for real-time usages, including some technology background as well as recommendations and examples on how to prepare Intel's real-time capable edge platforms for use with real-time applications. This document is for anyone working on these components, such as:

- System engineers preparing a system to support real-time applications.
- Engineers at ODMs and OEMs setting up systems and preparing the base platform software as well as validating its readiness for real-time.
- Software developers developing and validating SW applications and middleware with real-time requirements to work on Intel systems.

Consider this document the starting point for understanding how to best use Intel platforms for real-time usages. This document:

- Introduces the basics of running real-time workloads on Intel systems.
- Provides recommendations and examples on how to achieve the desired real-time performance on Intel platforms.
- Introduces the KPIs that Intel uses to measure real-time performance.
- Introduces real-time hardware features and related software.
- Provides information for advanced tuning of Intel platforms for users with very stringent real-time requirements.

Note: This document is not intended to provide a comprehensive specification for real-time features or software implementations. Where feasible, reference documentation has been cited that gives further technical detail for the topics discussed.

2.0 Real-time Capabilities Overview

2.1 Hardware Features

Intel® Core™ Processors, Intel Atom® Processors and Intel® Xeon® Processors with Intel® Time Coordinated Computing (TCC) provide hardware features to optimize real-time compute performance and support ethernet controllers with IEEE TSN support to optimize network traffic.

In this chapter, the hardware features are described at a high level. These features include HW-, FW- and SW-level optimizations throughout Intel's platform stack. For information about hardware features beyond the scope of this document, see the External Design Specification (*EDS) Addendum* listed in the Reference Documents.

2.1.1 Hardware Optimizations Overview

Intel's Time Coordinated Compute offering comprises of many optimizations throughout Intel's processors and connectivity solutions targeted at improving real-time performance in a mixed criticality environments comprised of real-time workloads as well as best-effort workloads running concurrently on Intel platforms and utilizing the same network connections and networks.

2.1.1.1 Time Synchronization Optimizations

- Precision Time Coordination: Clocks from SOC subsystem can be more precisely correlated in software via hardware time-stamping.
- Timed-GPIO: GPIO output that can be precisely coordinated in software (via Platform Sync) leveraging pulse-per-second (PPS)
- PCI Express* Precision Time Measurement (PTM): enables precise coordination of events across multiple components with independent local time clocks.

- IEEE 1588 (PTP) support in all Intel end-point connectivity solutions. IEEE 802.1AS TSN profile of IEEE 1588 supported in many Intel end-point connectivity solutions.

2.1.1.2 Timeliness Optimizations

- Power State Transition Optimizations: Enable CPU to keep executing instructions while its frequency is increasing or decreasing. While on early platforms with TCC support, e.g. Intel Atom® x6000 Series Processors and 11th Generation Intel® Core™ Processors), Intel recommended disabling many power management capabilities, subsequent additional improvements have changed such recommendations to allow some power management features to remain enabled with minimal impact to real-time behavior. In addition, Intel® Speed Shift technology together with other P-State options may be used to boost real-time performance by increasing the core frequency on select cores.
- Memory/Cache Allocation Optimizations: Partitioning of shared caches at the way level between classes of service (L2 & L3 Cache) - Intel® Cache Allocation Technology (CAT); Limit amount of cache available to GPU.
- Interrupt Request (IRQ) Optimizations: Optimize processor microcode & other overhead in the critical path for interrupts in the CPU core; Allow devices to deliver interrupts directly to the guest OS without requiring preprocessing by the hypervisor.
- Fabric and PCIe Virtual Channels: Virtual channels on Fabric and PCIe available to high priority workloads.

Time Sensitive Networking: Support of IEEE 801.1AS, 802.1Qbv, 802.1Qav, 802.1Qbu/3br in all end-point connectivity solutions to take advantage of TSN features becoming common in edge networks.

2.2 Supported Hardware

Intel offers real-time support on a wide variety of platforms and SKUs. Time Coordinated Compute support includes a set of optimizations in the SOC hardware and processor microcode including support for L2 and LLC (L3) Cache Allocation Technology (CAT) as well as IEEE Time Sensitive Networking (TSN) support in our connectivity offering.

2.2.1 Intel processors with Time Coordinated Compute support

A wide variety of Intel processors support Time Coordinated Compute capabilities including many versions and SKUs of Intel® Xeon® processors, Intel ® Core™ processors, and Intel Atom® processors. Appendix A provides a detailed list of processors and SKUs offering TCC support.

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: https://www.intel.com/content/www/us/en/products/details/embedded-processors.html.

2.2.2 TSN-capable Ethernet Controllers

Intel platforms with real-time support feature TSN over Ethernet via Intel's discrete i226-LM/IT Ethernet Controllers and on select processor SKUs and product families via integrated Ethernet MACs (for Intel® Core™ S-Series processors the R680E SKU of PCH is required for integrated 2.5Gb Ethernet with TSN support)

Table 1: TSN-capable Ethernet Controllers

Ethernet solution	Number of Ports	Media-Access Control (MAC)	Base-T PHY	Supported on
Discrete Intel® Ethernet Controller i226 LM/IT (2.5GbE with TSN and vPro support)	1 port per i226	Discrete PCIe device (MAC/PHY combo)		All TCC supported processors
Integrated 2.5GbE MAC	1 port	Yes	3rd Party	• 11th Generation Intel® Core™ UP3-Series Processors • 13th Generation Intel® Core™ U-, P-, H- Series Processors • Intel Atom® x7000E series processors
Integrated 2.5GbE MACs	2 ports	Yes (1 per port)	3rd Party	• 13th Generation Intel® Core™ S-Series Processors (R680E SKU of PCH only) • 12th Generation Intel® Core™ S-Series Processors (R680E SKU of PCH only) • Intel® Xeon® W-11000E Series Processors

Ethernet solution	Number of Ports	Media-Access Control (MAC)	Base-T PHY	Supported on
Integrated 2.5GbE MACs	3 ports	Yes (1 per port)	3rd Party	• Intel Atom® x6000E series processors

The ethernet controllers with TSN support can operate at multiple speeds: 10Mbps, 100Mbps, 1Gbps, and 2.5Gbps and in either full duplex or half duplex mode.
The integrated ethernet MAC with TSN support is accessed by Intel's processor cores through system software as a PCI express Root Complex Integrated Endpoint (RCiEP) via PCH I/O Fabric (PSF2) and only supports the SGMII interface.
To support Ethernet with TSN, the integrated ethernet MACs require 3rd party Ethernet PHYs external to the SOC. Supported PHYs are generally listed in the product briefs of the processor families.
Note: Many other Intel® Ethernet Controllers support IEEE 1588 and PTM but have limitations on other TSN aspects, e.g. IEEE 802.1Qbv or 802.1Qav (See product specifications for details).

2.2.3 TSN capable Altera® FPGA solutions

Intel provides various FPGA products that include Time Sensitive Networking support, some of them specifically targeted at switched endpoints. The following products are currently offered:

FPGA product	Number of Ports	TSN support
Cyclone® V	3x/5x 1Gb/s port Switch	Yes (TTTech IP) IEEE802.1AS, Qbv, Qbu, Qcc, CB, Qci
Cyclone® 10	5x-7x 1 Gbps	Yes (TTTech IP) IEEE802.1AS, Qbv, Qbu, Qcc, CB, Qci
Arria® 10	5x-7x 1 Gbps	Yes (TTTech IP) IEEE802.1AS, Qbv, Qbu, Qcc, CB, Qci

2.2.4 TSN-capable Wireless Solutions

Intel is working on providing TSN support over 5G and Wi-Fi on select Intel platforms. This section will be updated as such TSN capabilities will be available.

2.3 TCC enabled Software

Intel provides software that enables developers to access TCC hardware features, including BIOS support, Linux* kernel driver and user-space patches, and sample applications. In addition, Intel is working with ecosystem partners to deliver TCC and IEEE TSN support as part of 3rd party SW solutions.

2.3.1 Operating System Support

Intel provides Linux* OS support by upstreaming Linux kernel driver and user space patches to open-source libraries and utilities (iproute2, ethtool, linuxptp, etc.). In addition, Intel is working with commercial Linux distribution vendors to integrate upstreamed patches in their commercial distributions. For early access samples of upcoming Intel platforms Intel will provide overlays supporting the latest features to use in combination with the latest available Ubuntu* distributions.

2.3.2 Hypervisor Support

Intel enables 3rd party Hypervisors for real-time support and validates select capabilities with opensource ACRN and KVM Hypervisors.

2.3.3 UEFI-BIOS Support

Many of the control registers involved in configuring a platform for real-time usage are accessible through the BIOS.
Intel's reference BIOS includes various TCC enhancements including an option called Time Coordinated Computing Mode (TCC Mode), a single BIOS switch that optimizes the firmware settings for low latency. If your BIOS vendor has included support for TCC Mode, enabling this setting is a quick way to optimize your firmware configuration for real-time support.

2.3.4 Slim Bootloader Support

Like the UEFI-BIOS, Intel's Slim Bootloader (SBL) reference provides a configuration option to enable or disable TCC Mode. This configuration option is found in the following configuration file in the SBL source directory:

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* Other names and brands may be claimed as the property of others.

Platform\CommonBoardPkg\CfgData\CfgData_Tcc.yaml
You can override the enable or disable TCC Mode using the ConfigEditor tool. For more information on updating the settings using this tool, refer to the SBL wiki:
https://slimbootloader.github.io/how-tos/enable-intel-tcc.html#open-sbl-defaultconfiguration-data
For generic ConfigEditor info, refer to:
https://slimbootloader.github.io/tools/ConfigTools.html?highlight=configeditor#configeditor

2.3.5 Other Analysis and Profiling Tools

Other tools are available to help developers detect and analyze areas of the system negatively affecting real-time performance.

Table 2: Other Analysis and Profiling Tools

Tool	Description
Intel® VTune™ Profiler	Detect and analyze sources of system jitter. For information specific to real-time applications, see *Tutorial: Profile Applications with Intel® VTune™ Profiler* listed in Reference Documents.
Inter-event histogram triggers tool	A tool in the Linux kernel that can assist with latency profiling and analysis. This tool is platform independent. See Section 2.2 of the kernel document Event Histograms in Reference Documents.

2.3.6 Time-Sensitive Networking Reference Software

Intel provides a small set of TSN sample/reference applications available at https://github.com/intel/iotg_tsn_ref_sw.

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3.0 Time Coordinated Compute Quick Start Guide

3.1 Getting started with Intel® TCC

As mentioned in Chapter 2, Intel platforms are designed to support various applications and workloads and serve a broad range of markets. Intel's Time Coordinated Compute offering is designed to expand these markets to add support for workloads requiring real-time capabilities (low latencies, deterministic processing, and accurate time synchronization).

Many elements influence the real-time performance of a platform including HW and SW choices, BIOS and SW settings as well as ways to configure shared resources on the platform. As described in the previous chapters, TCC is comprised of many optimizations in hardware and software. The level of determinism required strongly depends on the real-time workload. Hence, not every implementation will require all the TCC optimizations available on Intel platforms to be enabled. This chapter describes some of the basic considerations of running real-time workloads on Intel platforms.

The following table provides guidance on how to approach usage of the capabilities offered.

1	Choose an Intel platform with TCC support	This ensures your platform has all the needed capabilities to support real-time workloads. This generally also includes choosing a connectivity solution with IEEE TSN support.
2	SW stack selection	Select the best RTOS and Hypervisor to fit your needs (e.g., Linux Preempt-RT)
3	Apply Real-time kernel boot parameters	Follow the directions for low latency configuration of your OS by your OS vendor (kernel boot parameters)
4	Pin your real-time workload to cores	Pinning a real-time workload to a core takes away some real-time performance variance. In a Hybrid system pinning allows allocating the real-time workload to the type of core best fitting the needs of the workload.
5	Configure platform for Time Coordinated Computing via BIOS, providing the most	Evaluate the overall performance of your system as well as your ability to support your real-time workloads after enabling **TCC Mode** in your BIOS. If your system does not support TCC Mode,

	flexibility for mixed criticality applications	please refer to alternate BIOS configurations detailed in Appendix B For many applications enabling TCC Mode or equivalent BIOS settings will likely be sufficient!
6	**If needed:** Allocate L2/3 cache to high priority workloads	Use Intel® Cache Allocation Technology to allocate an amount of cache for the real-time workload to utilize.
7	**If needed:** **Configure Intel® Speed Shift to increase real-time performance**	Use Intel® Speed Shift technology to boost core frequency on cores with high priority real-time workloads.

3.2 Hardware Configuration

Intel processors are designed to be configurable to address many unique customer requirements. Such requirements can come in the form of form factor (layout), thermal, performance, and cost. The combination of these requirement categories will ultimately determine board characteristics like memory type & speed, memory layout, and I/O layout. Regardless, for best real-time performance, Intel recommends:

- Populating ≥ 1 DIMM/channel for each available memory channel on the board (populating more DIMMs and more memory generally allows for quicker access to more data)
- Utilizing PCI Express slots attached to CPU die for lowest latency / highest throughput network connections. Note that the other available PCIe slots will also be sufficient for many real-time workloads and do also support many real-time optimizations (e.g. Precision Time Measurement - PTM).

Note: Refer to the documentation provided by the board or system vendor to identify which PCI Express connectors route to the CPU die.

3.3 Firmware Configuration

Intel's reference BIOS includes multiple knobs relevant to configure the BIOS for real-time performance. Such knobs include enabling and disabling specific functionalities that tend to impact real-time performance, such as some power-, frequency-, and thermal-management features, Hyperthreading and capabilities like PCIe Precision Time Measurement.

3.3.1 TCC Mode

TCC enabled platforms generally offer *TCC Mode*, a single BIOS knob that optimizes the firmware settings for low latency. TCC mode includes a wide range of real-time optimizations including the following:

- Power states and frequency transition optimizations
- Configuration of TCC features, e.g.:
  - Limit amount of cache available to GPU.
  - Optimize IO device utilization of Cache (for select platforms).
  - Set up virtual channels for VC-capable endpoints.

The TCC Mode option is generally found in the following BIOS menu, but specific naming may vary in your BIOS:

Intel Advanced Menu > Intel® Time Coordinated Computing

If your BIOS vendor has included support for TCC Mode, Intel recommends enabling this setting as a starting point for optimizing the firmware settings for real-time.

When Intel TCC Mode is enabled, it configures various existing BIOS settings to predetermined values, however, those values can be changed independently. We recommend not deviating from the default Intel TCC Mode values to ensure consistent configuration that is optimized for general real-time performance.

Due to TCC mode optimizing the platform for Time Coordinated Computing including changing some SOC power settings, enabling TCC mode adds approximately 1 Watt to the TDP of the processor.

When TCC Mode is disabled, the settings can be set independently for granular control of specific capabilities.

In cases where your BIOS does not include support for TCC Mode, please see Appendix B for platform specific settings that can be used to manually implement the equivalent TCC Mode functionality.

Note: BIOS configuration for some options can be overridden by the operating system. Specifically, when using Linux, the relevant kernel parameters should be supplied during boot to prevent the OS from altering the BIOS settings.

Note: Altering hardware and software power management features can negatively affect real-time performance and general compute performance for various I/O paths.
For specific register specifications, see the *BIOS Specification* (formerly BIOS Writer's Guide) listed in Reference Documents.

3.3.2 Power Management settings

As mentioned in Chapter 2, Intel has optimized power management capabilities on recent platforms resulting in improvements of Time Coordinated Compute performance even with some power management enabled. Starting with the 12th Generation Intel® Core™ processors and the Intel Atom® x7000 Series processors, TCC Mode no longer changes the default settings of Intel® Speed Shift Technology and Intel® Speed Step Technology. In addition, we keep Intel® Turbo Boost technology enabled during our real-time performance measurements on those platforms, as highlighted in Chapter 4: Key Performance Indicator Measurements.

3.4 Operating System Configuration

The operating system is a critical element for real-time optimization and options depend heavily on the particular operating system used. For Linux, there are some key parameter settings Intel uses for real-time performance measurements which will be spelled out in Chapter 4, but Linux distribution vendors offer their own guidance on how to optimize their Preempt-RT capable OS versions for real-time operation.
Canonical Real-time Ubuntu*: Tuning a real-time kernel
RedHat RHEL*: Understanding RHEL for Real-time
SuSE*: SUSE Linux Enterprise Real Time

The above links provide guidance for those Linux distributions. In general Intel recommends a properly configured BIOS, which will eliminate the need for the OS to redundantly disable known sources of jitter. As such the following Linux boot command could be used to ensure the timestamp counter in the CPU is used and interrupts to the cores reserved for real-time are avoided:

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* Other names and brands may be claimed as the property of others.

clocksource=tsc tsc=reliable nmi_watchdog=0 nosoftlockup idle=poll isolcpus=X-Y

[1] rcu_nocbs=X-Y nohz_full=X-Y irqaffinity=0

where X and Y are the range of cores dedicated to real time tasks

3.5 Optimal Clock Synchronization Accuracy

IO devices that support PCIe Precision Time Measurement (PTM) provide the highest degree of clock synchronization accuracy. Intel platforms support Precision Time Coordination out of the box, enabling accurate clock synchronization within the SOC. The configuration and use of Timed-GPIO is outside of the scope of this quick start guide, however more details can be found in Chapter 5.

3.5.1 Enabling PTM

Most Intel processors support PCIe PTM. PTM functionally can generally be enabled/disabled in BIOS. In most cases PTM functionality is enabled by default. If not already enabled, there are generally two ways to enable PTM:

1) If your BIOS supports Intel TCC Mode, the easiest way is to enable TCC mode. Enabling Intel TCC Mode was described in Chapter 3.3. TCC mode will automatically enable PTM on all PCIe connections on the processor.
2) If your BIOS does not support TCC Mode you can enable PTM for each PCIe connection separately (This may not be supported on all SOCs). The BIOS Menu items can generally be found at **Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration** and **Intel Advanced > PCH-IO Configuration > PCI Express Configuration.** The action generally needs to be repeated for any PCIe the user wishes to enable.

To take advantage of PTM all devices connected to a PCIe port will need to also support PTM. For example, if a PCIe-switch is used to connect several ethernet controllers to a single PCIe port on the SOC,

[1] While icolcpus use is not generally advised as it cannot changed at run-time, for real-time applications it is still the standard for CPU isolation.

the PCIe switch as well as the etherent devices will need to support PTM.

3.6 Cache Allocation for Real-time Workloads

In real-time system designs, it is often necessary to have control over shared resources to ensure that an adequate amount of that resource is available when needed by the application. Failure to allocate sufficient resources can lead to a performance degradation of the real-time application, causing it to miss execution deadlines.
System caches are one of the shared resources that, depending on the amount of contention, can drastically affect the performance of a real-time application. Intel provides the ability to partition cache resources using Cache Allocation Technology (CAT), which, depending on processor family and generation, may be available on both the L2 Cache and LLC Cache. Both L2- and LLC-CAT are available on TCC enabled Intel processors, however on TCC enabled Intel® Core™ processors and Intel Atom® processors, LLC (L3) cache is non-architectural. This document describes methodologies to configure CAT on those processors that are available for non-architectural CAT. Intel configures a simple Cache partitioning scheme using CAT when running real-time performance measurements. This simple scheme divides the cache in half, creating one half dedicated to the real-time application(s) and the other for best effort application(s). While not covered in this chapter beyond some basic allocation of cache to cores, additional details about using Cache Allocation Technology can be found in Chapter 5.

3.7 Setting up Intel's connectivity solutions as part of a TSN based network.

Setting up a TSN based network and how to best link Intel's connectivity solutions with TSN support is outside the scope of this document. Intel is offering some guidance for TSN in a Linux environment using Intel's ethernet solutions in the Ethernet Time-Sensitive Networking on Linux* for Intel® Processors & Ethernet Controller i225/i226 – Get Started Guide which can be found in RDC, document number: 6164446.

3.8 Example: Configuring a 13th Generation Intel® Core™ i7-13800HRE platform for real-time

This example outlines the high-level steps of preparing a 13th Generation Intel® Core™ platform for real-time usage.

Hardware selection:

- Intel® Core™ i7-13800HRE Processor
  - 14 Cores, 6 performance cores & 8 efficiency cores
  - 24MB of LLC (L2 Cache)
  - Integrated graphics
- Memory: Populate all DIMM slots
- Intel® Ethernet Controller I226 on PCIe port PEG (Port 1)

Configuring the Firmware

Enable TCC Mode in BIOS which will configure various BIOS menus for best real-time performance. In addition, it will configure all PCIe slots for Precision Time Measurement (PTM) and enable GT-CLOS, which limits the amount of cache the integrated graphics has access to.

Choosing and Configuring the Operating System

In the example we assume Real-time Ubuntu* optimized for Intel platforms is used.[1]

Apply kernel parameters to isolate cores for real-time workloads and correct clock usage. In this example we are planning to use P cores 4 & 5 for real-time usage and P-cores 0 - 3 as well as E-cores 6 - 13 for housekeeping and best effort workloads:

clocksource=tsc tsc=reliable nmi_watchdog=0 nosoftlockup idle=poll isolcpus=4-5 rcu_nocbs=4-5 nohz_full=4-5 irqaffinity=0[2]

Cache partitioning.

[1] Please contact Canonical for access to Real-time Ubuntu

[2] Follow Canonical's guidance on configuring other kernel boot parameter settings on real-time Ubuntu

In this example we are following the simple cache partitioning scheme described previously, dividing the cache in half: one half dedicated to the real-time application(s) and the other for best effort application(s). The Intel® Core™ Processor i7-13800HRE Processor contains 24MB of LLC (L3) cache that can be partitioned using the model specific, non-architectural implementation of L3 Cache Allocation Technology found on Intel® Core™ processors that support Time Coordinated Computing. (See Figure 1)

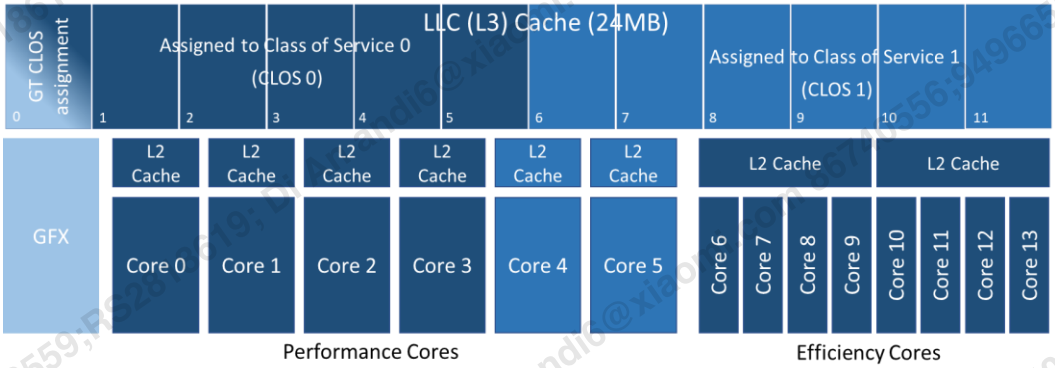


Figure 1 Cache allocation example for 13th Gen Intel® Core™ Processor i7-13800HRE example with GT CLOS enabled via TCC Mode in BIOS

Table 3 shows how the 24MB last level cache can be partitioned in half, with P cores 0-3 and all E cores being assigned a non-overlapping portion of the cache from P cores 4, and 5 which will be used for real-time workloads. For completeness, the equivalent commands for programming the MSRs directly are also shown. The MSR's used for configuring the cache masks are L3_MASK_0 (address 0xC90) and L3_MASK_1 (address 0xC91). The MSR used for associating a class of service to a core is PQR_ASSOC (address 0xC8F).
The 13th Gen Intel® Core™ Processor i7-13800HRE last level cache has a capacity bitmask (CBM) length of 12 (0xFFF), so each class of service will be assigned a CBM length of 6 (0x3F and 0xFC0, respectively) when partitioning the cache in half.

Table 3: Partitioning the cache in half on the 13th Gen Intel® Core™ Processor i7-13800HRE.

Using intel-cmt-cat "pqos" utility	Model Specific Register (MSR) programming	Comments
pqos --iface=msr -e "llc:0=0x3F;llc:1=0xFC0"	wrmsr 0xC90 0x3F wrmsr 0xC91 0xFC0	Assign ½ the cache to CLOS 0 Assign ½ the cache (non-overlapping) to CLOS 1
pqos --iface=msr -a "llc:0=0-3, 6-13;llc:1=4,5"	wrmsr -p 0 0xC8F 0x000000000 wrmsr -p 1 0xC8F 0x000000000 wrmsr -p 2 0xC8F 0x000000000 wrmsr -p 3 0xC8F 0x000000000 … wrmsr -p 4 0xC8F 0x100000000 wrmsr -p 3 0xC8F 0x100000000	Assign CLOS 0 to Cores 0-3 (performance cores) Also assign CLOS 0 to all efficiency cores (6-13) using the same command (not shown) Assign CLOS 1 to Cores 4 and 5

Note: The "–iface=msr" extension is necessary to make the pqos command work on non-architectural CAT.

Pinning real-time workloads to specific cores.

During run-time any real-time workloads should be pinned to the cores designated for high priority workloads (in this example Cores 4 and 5). This applies to the actual real-time workloads as well as any needed IRQ interrupt handling for such workloads. For best performance you pin the real-time workload to one Core (e.g. Core 4) and the real-time IRQ handling to the other (Core 5).

Note: Please refer to guidance from your OS vendor on how to pin workloads to cores.

4.0 Key Performance Indicator Measurements

This chapter describes the real-time performance benchmarks Intel utilizes to measure real-time performance of our SOCs. It is meant to provide high level guidance to our customers of the expected real-time performance on an Intel platform optimized for real-time usage as well as guidance on how Intel configured the platforms for the provided measured data.

4.1 Real-Time Key Performance Indicators (KPIs)

Real-time Key Performance Indicators (KPIs) are real-time performance metrics. Intel provides information about KPIs, including measurements and configurations for replicating the tests on a given platform in the following chapter.
The Performance Report describes:

- Real-time capabilities enabled at product launch of select real-time capable processor SKUs.
- Real-time KPI requirements using Linux with Preempt-RT.

The information is expected to cover the following two benchmarks:

Cyclictest: a latency test designed to measure a system's real-time performance and event responsiveness. Cyclictest's latency is defined as the time between a thread's intended wake-up time and its actual wake-up time. For more information on Cyclictest, please refer to https://wiki.linuxfoundation.org/realtime/documentation/howto/tools/cyclictest/test-design as well as to https://git.kernel.org/pub/scm/utils/rt-tests/rt-tests.git/.

- **Real-Time Compute Performance (RTCP):** a KPI developed by Intel measuring the total elapsed time from when a synthetic sensor data packet is received, to when a synthetic actuator command packet is sent (including the elapsed time for the execution of a predefined compute workload).

For both benchmarks, MAX and AVERAGE observed values as well as Jitter (Difference between Min and Max observed value) are provided.

- The MAX observed value expresses the works case result observed, generally over a 24hour test period and millions of iterations. In general, the MAX value is most relevant to real-time edge workloads.
- The average and jitter (difference between MIN and MAX) value are provided as reference.

4.2 General System Configuration for KPI measurements:

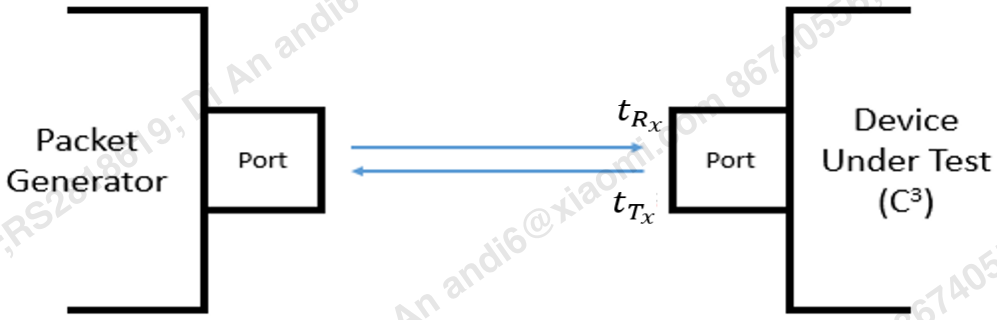


Figure 2 Real-time performance test set-up

Measuring real-time performance generally involves a real-time capable system to generate data, the packet generator, as well a real-time capable system that is being tested, the device under test, connected via a network connection. Depending on the real-time performance test utilized, real-time performance is often measured comparing the time when data is received at the device under test (t_{Rx}) and the time data is sent out from the device under test (t_{Tx}). This time expresses how long it takes the device under test to receive, process, and transmit the data.

To represent a realistic load of the system, the device under test is generally running best-effort background applications at the same time. This background loading is critical to correctly determine the time coordinated compute performance of a real-time workload.

Before running the performance benchmarks Intel configures the system for real-time, applying kernel boot parameters, enabling TCC mode in BIOS, pinning real-time workloads to cores and assigning part of the cache to high priority queues. Details of this configuration are documented in the following chapters.

4.3 Platform specific real-time performance measurements

4.3.1 KPI data for Intel® Xeon® Processors with real-time support

4.3.1.1 Real-time configuration for Intel® Xeon® D-2896TER Processor KPI measurements

Hardware		
Motherboard		Moro City
CPU	**Product**	Intel® Xeon™ D-2896TER
	Speed (MHz)	2000
	Number of CPUs	20 Cores
	Stepping	B1
	LLC Cache	30MB
Chipset		Eddy Lake
Memory	**Vendor**	Hynix
	Type	DDR4-3200
	Size (GB)	2x32GB
	Channel	2
BIOS	**Vendor**	Intel Corporation
	Version	IDVICRB1.SBT.0027.D98.2401090837
OS	**Release**	meta-intel-ese Reference Distro 1.0-ESE (kirkstone) 20240215072049
	Kernel version	6.1.69-rt21-intel-ese-standard-lts-rt x86_64

Ethernet Controller:
Intel® Ethernet Controller i226 LM connected to PEG PCIe

Test settings for Intel® Xeon® D-2896TER Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> PCI-E Port Clock Gating <Disabled> PCI-E ASPM Support <Disabled> Uncore Frequency Scaling <Disabled Uncore Freq [21]> Energy Efficient Turbo <Disabled> SpeedStep (Pstates) <Enabled> Hardware Pstates <Native Mode> Native ASPM <Disabled> Package C State <C0/C1 state> Enhanced Half State (CIE) <Disabled>
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_requests=1 rcu_nocb_poll irqaffinity=0 hpet=disable numa_balancing=disable efi=runtime iommu=pt nmi_watchdog=0 hugepages=1024 nohz_full=2,3 mce=off
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XFFFF • Best-effort workload: Run on CLOS 0 with Waymask 0XF0000

RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us)
	• Buffer Size (Instructions Executed)
	  ○ 264KB = 12K instructions
	  ○ 1296KB = 60K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git Example • **Board A:** ./rtcp.sh -p icxd -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p icxd -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

RT Test Configuration on device under test:

- Real-Time Workload (Cyclictest): Run on Core 2 and 3
- Real-Time Workloads (RTCP) : Real-Time Control Loop on core 3
- Real-Time interrupt handler (IRQ) on core 2
- Simultaneous Workloads: Core-to-memory stress workload on all remaining P-Cores.
- Simultaneous Workloads: Core-to-memory stress workload on core 0 and 1
    - stress-ng on all remaining P-Cores., example:
        - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0

C

KPI results for Intel® Xeon® D-2896TER Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using discrete Ethernet i225	1ms RTCP 60k IPCL	TCC Mode enabled. No outliers (CPU contention)	324 µs	423 µs	120 µs	86 million (24 hours)
	125us RTCP 12k IPCL	TCC Mode enabled. No outliers (CPU contention)	60 µs	80 µs	38 µs	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet i225	1ms RTCP 60k IPCL	TCC Mode enabled. No outliers (CPU contention)	217 µs	244 µs	30 µs	86 million (24 hours)
	100us RTCP 12k IPCL	TCC Mode enabled. No outliers (CPU contention)	29 µs	47 µs	18 µs	691 million (24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled. (CPU contention)	2 µs	6 µs	5 µs	345 million (24 hours)

Ethernet Controller:

Intel® Ethernet Controller i226 LM connected to PEG PCIe

4.3.1.2 Real-time configuration for Intel® Xeon® D-2752TER Processor KPI measurements

Hardware		
Motherboard		Brighton City
CPU	Product	Intel® Xeon™ D-2752TER
	Speed (MHz)	1800
	Number of CPUs	12 Cores
	Stepping	B1
	LLC Cache	20MB
Chipset		Ice Lake
Memory	Vendor	Micron
	Type	DDR4-2666
	Size (GB)	4x16GB
	Channel	3
BIOS	Vendor	Intel Corporation
	Version	IDVICRB1.SBT.0023.P54.2208251316
OS	Release	meta-intel-ese Reference Distro 1.0-ESE (kirkstone) 20220810200651
	Kernel version	5.10.131-rt72

Ethernet Controller:
Intel® Ethernet Controller i226 LM connected to PEG PCIe

Test settings for Intel® Xeon® D-2752TER Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> PCI-E Port Clock Gating <Disabled> PCI-E ASPM Support <Disabled> Uncore Frequency Scaling <Disabled> Energy Efficient Turbo <Disabled> Hardware P-State <Native Mode> Native ASPM <Disabled> Package C-State <C0/C1 state>
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_requests=1 rcu_nocb_poll irqaffinity=0 hpet=disable numa_balancing=disable efi=runtime iommu=pt nmi_watchdog=0 hugepages=1024 nohz_full=2,3 mce=off
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XFFFF

Item	Description
	• Best-effort workload: Run on CLOS 0 with Waymask 0XF0000

RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us)
	• Buffer Size (Instructions Executed)
	  ○ 264KB = 12K instructions
	  ○ 1296KB = 60K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p icxd -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p icxd -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:** ./rtcp.sh -S (Set's up the environment) • **Board A and board B:** ./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

RT Test Configuration on device under test:

- Real-Time Workload (Cyclictest): Run on Core 2 and 3
- Real-Time Workloads (RTCP) :
  - Real-Time Control Loop on core 3
  - Real-Time interrupt handler (IRQ) on core 2
- Simultaneous Workloads: Core-to-memory stress workload on core 0 and 1
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0

C

KPI results for Intel® Xeon® D-2752TER Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using discrete Ethernet i226	1ms RTCP 60k IPCL	TCC Mode disabled. No outliers (CPU and GFX contention)	NA	NA	NA	86 million (24 hours)
	1ms RTCP 60k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	374 µs	456 µs	109 µs	86 million (24 hours)
	125us RTCP 12k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	68 µs	99 µs	43 µs	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet i226	1ms RTCP 60k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	286 µs	441 µs	169 µs	86 million (24 hours)
	100us RTCP 12k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	37 µs	72 µs	35 µs	691 million (24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled. (CPU and GFX contention)	3 µs (Avg. latency)	15 µs (Max latency)	14 µs	345 million (24 hours)

4.3.1.3 Real-time configuration for Intel® Xeon® W-11865MRE Processor KPI measurements

Hardware		
Motherboard		Intel® Customer Reference Board for Tiger Lake H DDR4
CPU	Product	Intel® Xeon® W-11865MRE Processor
	Speed (MHz)	2600 nominal / 4700 turbo
	Number of CPUs	8 Cores / 16 Threads
	Stepping	PRQ
	LLC Cache	24 MB
Chipset		Tiger point
Graphic		Intel® UHD Graphics for 11th Gen Intel® Processors
Memory	Vendor	Samsung
	Type	DDR4-3200
	Size (GB)	2x16GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	TGLIFUI1.R00.4163.A05.2105091335
OS	Release	TGL-H Yocto BSP ER#85
	Kernel version	5.4.115-rt57-intel-ese-standard-lts-rt

Ethernet Controller:

- Integrated Ethernet port in PCH with 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-time workload (Cyclictest): Run on core 2 and 3.
- Real-time workload (RTCP):
  - Real-time control loop run on core 3,
  - Real-time interrupt handler (IRQ) run on core 2
- Simultaneous workloads: core-to-memory stress workload on core 0 & 1, graphics workload on core 1
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0
  - gfxbench on core 1

Test settings for Intel® Xeon® W-11865MRE Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> VTD <Enabled>

Item	Description
	TSN GBE Configuration - PCH TSN LAN Controller <Enabled> TSN GBE Configuration - PCH TSN Link Speed <38.4MHz 1Gbs >
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_requests=1 rcu_nocb_poll irqaffinity=0 hpet=disable numa_balancing=disable efi=runtime iommu=pt nmi_watchdog=0 hugepages=1024 nohz_full=2,3 mce=off
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XF • Best-effort workload: Run on CLOS 0 with Waymask 0XFF0

RTCP Settings	• RT Control Loop Period (1ms, 300us)
	• Buffer Size (Instructions Executed)
	  ○ 220 KB = 10K instructions
	  ○ 1080KB = 50K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p tgl -h dwmac -i <ethernet interface> -c rtcp1a -n 2400000 -d 300000 • **Board B:** ./rtcp.sh -p tgl -h dwmac -i <ethernet interface> -c rtcp1b -n 2400000 -d 300000 • **Board A and board B:** ./rtcp.sh -S (Set's up the environment) • **Board A and board B:** ./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel® Xeon® W-11865MRE Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms cycle RTCP KPI using a 50k IPCL real-time workload	TCC Mode disabled	250µs	504µs	330µs	70 Million (24 hours)
	1ms cycle RTCP using a 50k IPCL	TCC Mode enabled, 2 outliers removed*	206µs	252µs*	130µs	100 Million (24 hours)

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
	real-time workload	TCC Mode enabled	206µs	1208µs	1010µs	691 million (24 hours)
Linux_RT	300µs RTCP using 10k IPCL real-time workload	TCC Mode enabled	49µs	176µs	54µs	720 Million (24 hours)
	Cyclictest	250µs wakeup interval. TCC mode enabled	N.A	17µs (Max latency)	N.A	345 Million (24 hours)

*One outlier removed – root caused to specific scenario

4.3.2 KPI data for Intel® Core™ Processors with real-time support

4.3.2.1 Real-time configuration for Intel® Core™ i9-14900Processor KPI measurements (Raptor Lake Refresh S)

Hardware		
Motherboard		Intel® RPL-S ADP-S DDR5 SODIMM CRB
CPU	Product	14th Gen Intel(R) Core(TM) i9-14900 65W
	Speed (MHz)	2000
	Max Turbo Speed (MHz)	5800
	Number of CPUs	24 Cores (8 performance+ 16 efficiency)
	LLC Cache	36MB
Chipset		Raptorlake Refresh
Graphics		GT1
Memory	Vendor	SK Hynix
	Type	DDR5-4800
	Size (GB)	2x16GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	IOTG_RPL_SR17_B0B1-ADPSADL_RPSF_SEP0_03D82592_2023 WW13.2.01_BE4115_25Mhz_TSN0.bin
OS	Release	RPL-SR Yocto BSP RC01 (ER#25)
	Kernel version	6.1.38-rt12-intel-ese-standard-lts-rt

Ethernet Controller:

- Intel® Ethernet Controller i226 LM connected to PCIe port PEG
- Integrated Ethernet port in PCH 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-Time Workload (Cyclictest): Run on Core 2 and 3
- Real-Time Workloads (RTCP):
  - Real-Time Control Loop on core 3
  - Real-Time interrupt handler (IRQ) on core 2
- Simultaneous Workloads: Core-to-memory stress workload on core 0, 1, 4, 5, 6, 7, 8, and 9. Graphics workload on core 1.
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0
  - gfxbench on core 1

Test settings for Intel® Core™ i9-14900 Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> Intel® Turbo Boost Technology <Enabled> Intel SpeedStep® <Enabled> VTD <Enabled> TSN GBE Configuration - PCH TSN LAN Controller <Enabled> TSN GBE Configuration - PCH TSN Link Speed <38.4MHz 1Gbs>
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 clocksource=tsc tsc=reliable nowatchdog intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_suppress=1 rcu_nocb_poll irqaffinity=0 i915.enable_rc6=0 i915.enable_dc=0 i915.disable_power_well=0 mce=off hpet=disable numa_balancing=disable igb.blacklist=no efi=runtime art=virtallow iommu=pt nmi_watchdog=0 nosoftlockup hugepages=1024 rdt=!mba i915.enable_guc=7
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0X3F • Best-effort workload: Run on CLOS 0 with Waymask 0XFC0

RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us)
	• Buffer Size (Instructions Executed)
	  ○ 242 KB = 11K instructions
	  ○ 1188KB = 55K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p rpls -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p rpls -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel® Core™ i9-14900 Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using discrete Ethernet i226	1ms RTCP 55k IPCL	TCC Mode disabled. No outliers (CPU and GFX contention)	380 µs	568 µs	406 µs	86 million (24 hours)
	1ms RTCP 55k IPCL	TCC Mode enabled. (CPU and GFX contention)	176 µs	217 µs	65 µs	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. (CPU and GFX contention)	64 µs	97 µs	42 µs	691 million (24 hours)
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms RTCP 55k IPCL	TCC Mode enabled. (CPU and GFX contention)	172 µs	230 µs	78 µs	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. (CPU and GFX contention)	46 µs	96 µs	65 µs	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet i226	1ms RTCP 55k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	160 µs	188 µs	95 µs	86 million (24 hours)
	100us RTCP 11k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	37 µs	45 µs	22 µs	691 million (24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled. (CPU and GFX contention)	1 µs (Avg. latency)	6 µs (Max latency)	5 µs	345 million (24 hours)

4.3.2.2 Real-time configuration for Intel® Core™ i9-13900E Processor KPI measurements (Raptor Lake S)

Hardware		
Motherboard		Intel® RPL-S ADP-S DDR5 SODIMM CRB
CPU	Product	13th Gen Intel(R) Core(TM) i9-13900E
	Speed (MHz)	1800
	Number of CPUs	24 Cores (8 performance+ 16 energy efficient)
	Stepping	B1
	LLC Cache	36MB
Chipset		Raptorlake
Graphic	Driver cores	GT1
Memory	Vendor	SK Hynix
	Type	DDR5-4800
	Size (GB)	2x16GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	RPLISRPLISFI1.R00.3441.A02.2212120717FI1.R00.
OS	Release	RPL-S Yocto BSP ER22 with rt-kernel-5.19
	Kernel version	5.19.0-rt10-intel-ese-preempt-rt-mainline-tracking-rt-519

Ethernet Controller:

- Intel® Ethernet Controller i226 LM connected to PCIe port PEG
- Integrated Ethernet port in PCH 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-Time Workload (Cyclictest): Run on Core 2 and 3
- Real-Time Workloads (RTCP):
  - Real-Time Control Loop on core 3
  - Real-Time interrupt handler (IRQ) on core 2
- Simultaneous Workloads: Core-to-memory stress workload on core 0, 1, 4, 5, 6, 7, 8, and 9. Graphics workload on core 1.
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0

- gfxbench on core 1

Test settings for Intel® Core™ i9-13900E Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> Intel® Turbo Boost Technology <Enabled> Intel SpeedStep® <Enabled> VTD <Enabled> TSN GBE Configuration - PCH TSN LAN Controller <Enabled> TSN GBE Configuration - PCH TSN Link Speed <38.4MHz 1Gbs>
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 clocksource=tsc tsc=reliable nowatchdog intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_suppress=1 rcu_nocb_poll irqaffinity=0 i915.enable_rc6=0 i915.enable_dc=0 i915.disable_power_well=0 mce=off hpet=disable numa_balancing=disable igb.blacklist=no efi=runtime art=virtallow iommu=pt nmi_watchdog=0 nosoftlockup hugepages=1024 rdt=!mba i915.enable_guc=7
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0X3F • Best-effort workload: Run on CLOS 0 with Waymask 0XFC0

RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us)
	• Buffer Size (Instructions Executed)
	  ○ 242 KB = 11K instructions
	  ○ 1188KB = 55K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p rpls -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p rpls -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel® Core™ i9-13900E Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using discrete Ethernet i226	1ms RTCP 55k IPCL	TCC Mode disabled. No outliers (CPU and GFX contention)	402 µs	586 µs	461 µs	86 million (24 hours)
	1ms RTCP 55k IPCL	TCC Mode enabled. (CPU and GFX contention)	138 µs	167 µs	48 µs	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. (CPU and GFX contention)	47 µs	71 µs	41 µs	691 million (24 hours)
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms RTCP 55k IPCL	TCC Mode enabled. (CPU and GFX contention)	137 µs	255 µs	135 µs	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. (CPU and GFX contention)	41 µs	97 µs	69 µs	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet i226	1ms RTCP 55k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	N.A	180 µs	N.A	86 million (24 hours)
	100us RTCP 11k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	N.A	59 µs	N.A	691 million (24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled. (CPU and GFX contention)	2 µs (Avg. latency)	12 µs (Max latency)	N.A	345 million (24 hours)

4.3.2.3 Real-time configuration for Intel® Core™ i7-13800HRE Processor KPI measurements (Raptor Lake -P)

Hardware		
Motherboard		Intel® RPL-P DDR5 SODIMM CRB
CPU	Product	13th Gen Intel(R) Core(TM) i7-13800HRE 65W
	Speed (MHz)	2500
	Max Turbo Speed (MHz)	5000
	Number of CPUs	14 Cores (6 performance+ 8 efficiency)
	LLC Cache	24MB
Chipset		Raptorlake
Graphics		GT1
Memory	Vendor	SK Hynix
	Type	DDR5-4800
	Size (GB)	2x16GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	IOTG_RPL_CRB_PR05_J0B1-XXXADPP_RPSF_SEP0_03F724A8_2023WW23.3.01_BE427202.bin
OS	Release	RPL-P Ubuntu BSP WW31.1 PV2+ RC01 ER30
	Kernel version	linux-image-5.19rt-intel 230725t153817z-r1

Ethernet Controller:

- Intel® Ethernet Controller i226 LM connected to PCIe port PEG
- Integrated Ethernet port in PCH 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-Time Workload (Cyclictest): Run on Core 2 and 3
- Real-Time Workloads (RTCP):
  - Real-Time Control Loop on core 3
  - Real-Time interrupt handler (IRQ) on core 2
- Simultaneous Workloads: Core-to-memory stress workload on core 0, 1, 4, 5. Graphics workload on core 1.
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0
  - gfxbench on core 1

Test settings for Intel® Core™ i7-13800HRE Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> Intel® Turbo Boost Technology <Enabled>

Item	Description
	Intel SpeedStep® <Enabled> VTD <Enabled> TSN GBE Configuration - PCH TSN LAN Controller <Enabled> TSN GBE Configuration - PCH TSN Link Speed <38.4MHz 1Gbs>
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 clocksource=tsc tsc=reliable nowatchdog intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_suppress=1 rcu_nocb_poll irqaffinity=0 i915.enable_rc6=0 i915.enable_dc=0 i915.disable_power_well=0 mce=off hpet=disable numa_balancing=disable igb.blacklist=no efi=runtime art=virtallow iommu=pt nmi_watchdog=0 nosoftlockup hugepages=1024 rdt=!mba i915.enable_guc=7
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0X3F • Best-effort workload: Run on CLOS 0 with Waymask 0XFC0

RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us)
	• Buffer Size (Instructions Executed)
	  ○ 242 KB = 11K instructions
	  ○ 1188KB = 55K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p rpls -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p rpls -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel® Core™ i7-13800HRE Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using discrete Ethernet i226	1ms RTCP 55k IPCL	TCC Mode disabled. No outliers (CPU and GFX contention)	239 µs	450 µs	235 µs	86 million (24 hours)
	1ms RTCP 55k IPCL	TCC Mode enabled. (CPU and GFX contention)	209 µs	384 µs	200 µs	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. (CPU and GFX contention)	40 µs	65 µs	36 µs	691 million (24 hours)
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms RTCP 55k IPCL	TCC Mode enabled. (CPU and GFX contention)	288 µs	423 µs	173 µs	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. (CPU and GFX contention)	54 µs	87 µs	56 µs	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet i226	1ms RTCP 55k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	134 µs	351 µs	N.A	86 million (24 hours)
	100us RTCP 11k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	26 µs	54 µs	N.A	691 million (24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled. (CPU and GFX contention)	1 µs (Avg. latency)	11 µs (Max latency)	N.A	345 million (24 hours)

4.3.2.4 Real-time configuration for Intel® Core™ i7-12700E Processor KPI measurements

Hardware		
Motherboard		Intel® Customer Reference Board for Alderlake-S DDR4
CPU	Product	12th Gen Intel(R) Core(TM) i7-12700E
	Speed (MHz)	4200 (BIOS Turbo + IST Enabled)
	Number of CPUs	12 Cores (8 performance+ 4 energy efficient)
	Stepping	C1
	LLC Cache	25 MB
Chipset		Alderlake
Graphic	Driver cores	GT1
Memory	Vendor	Crucial Technology
	Type	DDR4-3200
	Size (GB)	4x8GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	ADLSFWI1.R00.2355.B00.2108270706
OS	Release	ADL-S Yocto BSP ER71a with lts-rt-5.10-kernel
	Kernel version	5.10.78-rt55-intel-ese-standard-lts-rt

Ethernet Controller:

- Intel® Ethernet Controller i226 LM connected to PCIe port PEG
- Integrated Ethernet port in PCH 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-time workload (Cyclictest): Run on core 2 and 3.
- Real-time workload (RTCP):
  - Real-time control loop run on core 3,
  - Real-time interrupt handler (IRQ) run on core 2
- Simultaneous workloads: core-to-memory stress workload on core 0 & 1, graphics workload on core 1
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0
  - gfxbench on core 1

Test settings for Intel® Core™ i7-12700E Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> Intel® Turbo Boost Technology 3.0 <Enabled> Intel SpeedStep® <Enabled> VTD <Enabled> TSN GBE Configuration - PCH TSN LAN Controller <Enabled> TSN GBE Configuration - PCH TSN Link Speed <38.4MHz 1Gbs>
Kernel Boot Settings	i915.force_probe=* udmabuf.list_limit=8192 processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 clocksource=tsc tsc=reliable nowatchdog intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_suppress=1 rcu_nocb_poll irqaffinity=0 i915.enable_rc6=0 i915.enable_dc=0 i915.disable_power_well=0 mce=off hpet=disable numa_balancing=disable igb.blacklist=no efi=runtime art=virtallow iommu=pt nmi_watchdog=0 nosoftlockup hugepages=1024 rdt=!mba i915.enable_guc=7
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0X3E0 • Best-effort workload: Run on CLOS 0 with Waymask 0X1F

RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us)
	• Buffer Size (Instructions Executed)
	  ○ 242 KB = 11K instructions
	  ○ 1188KB = 55K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p adls -h dwmac -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p adls -h dwmac -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a2-3 -t2 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel® Core™ i7-12700E Processor

Configura-tion	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms RTCP 55k IPCL	TCC Mode disabled. No outliers (CPU, memory, and gfx contention)	426.2 us	470.8 us	245.6 us	86 million (24 hours)
	1ms RTCP 55k IPCL	TCC Mode enabled. No outliers (CPU, memory, and gfx contention)	241.1	297.5 us	73.2 us	86 million (24 hours)
	125us RTCP 11k IPCL	TCC Mode enabled. No outliers (CPU, memory, and gfx contention)	45.3	94.8 us	67.9	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet	1ms RTCP 55k IPCL	TCC Mode enabled. No outliers (CPU, memory, and gfx contention)	N.A	189.9 us	N.A	(24 hours)
	100us RTCP 11k IPCL	TCC Mode enabled. No outliers (CPU, memory, and gfx contention)	N.A	49.7 us	N.A	(24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled	N.A	11 us (Max latency)	N.A	(24 hours)

4.3.2.5 Real-time configuration for Intel® Core™ i7-1185GRE Processor KPI measurements

Hardware		
Motherboard		Intel® Customer Reference Board for Tiger Lake U DDR4
CPU	Product	Intel(R) Core(TM) i7-1185GRE CPU
	Speed (MHz)	1800 (config TDP up)
	Number of CPUs	4 Cores / 8 Threads
	Stepping	B2
	LLC Cache	12 MB
Chipset		Tiger point
Graphic	Driver cores	GT2
Memory	Vendor	Samsung
	Type	DDR4-3200
	Size (GB)	4x4GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	TGLIFUI1.R00.3313.A03.2008071806
OS	Release	TGL-U Yocto BSP ER#50
	Kernel version	5.4.59-rt36-intel-preempt-rt

Ethernet Controller:

- Integrated Ethernet port in PCH with 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-time workload (Cyclictest): on core 3
- Real-time workloads (RTCP):
  - Real-time control loop on core 3
  - Real-time interrupt handler (IRQ) on core 2

Test settings for Intel® Core™ i7-1185GRE Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> VTD <Enabled>

Item	Description
	TSN GBE Configuration - PCH TSN LAN Controller <Enabled> TSN GBE Configuration - PCH TSN Link Speed <38.4MHz 1Gbs>
Kernel Boot Settings	processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_requests=1 rcu_nocb_poll irqaffinity=0 hpet=disable numa_balancing=disable efi=runtime iommu=pt nmi_watchdog=0 hugepages=1024 nohz_full=2,3 mce=off
Cache allocation settings	L2 CAT: not configured (L2 cache not shared) L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XF • Best-effort workload: Run on CLOS 0 with Waymask 0XFF0

RTCP Settings	• RT Control Loop Period (1ms, 300us)
	• Buffer Size (Instructions Executed)
	  ○ 220 KB = 10K instructions
	  ○ 1080KB = 50K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p tgl -h dwmac -i <ethernet interface> -c rtcp1a -n 2400000 -d 300000 • **Board B:** ./rtcp.sh -p tgl -h dwmac -i <ethernet interface> -c rtcp1b -n 2400000 -d 300000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a3 -t1 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel® Core™ i7-1185GRE Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms cycle RTCP KPI using a 50k IPCL real-time workload	TCC Mode disabled	164µs	645µs	481µs	100 Million (24 hours)
	300µs RTCP KPI using a 10k IPCL	TCC Mode enabled, 1 outlier above 300us	60µs	373µs	313µs	300 Million (24 hours)

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
	real-time workload	TCC Mode enabled, 1 outlier removed	60µs	165µs*	105µs*	300 Million (24 hours)
Linux_RT	Cyclictest	250µs wakeup interval. TCC mode enabled	N.A	15µs (Max latency)	N.A	345 Million (24 hours)

*One outlier removed – root caused to specific usage scenario

4.3.3 KPI data for Intel Atom® Processors with real-time support

4.3.3.1 Real-time configuration for Intel Atom® X7000RE Processor KPI measurements (Amston Lake)

KPI configurations and measurement data will be available soon.

4.3.3.2 Real-time configuration for Intel Atom® x7425E Processor KPI measurements

Hardware		
Motherboard		AlderLake-N DDR5 CRB
CPU	Product	Intel(R) Atom® Processor x7425E
	Speed (MHz)	1500
	Number of CPUs	4 Cores / 4 Threads
	Stepping	N0
	LLC Cache	6MB
Chipset		Alder Lake
Memory	Vendor	SK Hynix
	Type	DDR5-4800
	Size (GB)	1x16GB
	Channel	1
BIOS	Vendor	Intel Corporation
	Version	ADLNFWI1.R00.4031.A00.2301180153
OS	Release	ADL-N Yocto BSP ER46 with rt-kernel-5.15
	Kernel version	5.15.85-rt55-intel-ese-preempt-rt-lts-rt-bullpen-rt

Ethernet Controller:

- Intel® Ethernet Controller i226 LM connected to PCIe port (PCH)
- Integrated Ethernet port in PCH with 3rd party PHY (TI*)

RT Test Configuration on device under test:

- Real-Time Workload (Cyclictest): Run on Core 2 and 3
- Real-Time Workloads (RTCP) :
  - Real-Time Control Loop on core 3
  - Real-Time interrupt handler (IRQ) on core 2
- Simultaneous Workloads: Core-to-memory stress workload on core 0, 1, 4, 5, 6, 7, 8, and 9. Graphics workload on core 1.
  - stress-ng on core 0 and core 1, example:
    - stress-ng --taskset 0-1 --cpu 2 --cpu-load 100 -t 0

- gfxbench on core 1

Test settings for Intel Atom® x7425E Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> Intel® Turbo Boost Technology <Enabled> Intel SpeedStep® <Enabled> VTD <Enabled>
Kernel Boot Settings	i915.force_probe=* udmabuf.list_limit=8192 nopcid processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 clocksource=tsc tsc=reliable nowatchdog intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_suppress=1 rcu_nocb_poll irqaffinity=0 i915.enable_rc6=0 i915.enable_dc=0 i915.disable_power_well=0 mce=off hpet=disable numa_balancing=disable igb.blacklist=no efi=runtime art=virtallow iommu=pt nmi_watchdog=0 nosoftlockup hugepages=1024 rdt=!mba i915.enable_guc=7
Cache allocation settings	L2 CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XFF00 • Best-effort workload: Run on CLOS 0 with Waymask 0XFF L3/LLC CAT: configured • RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XFC0 • Best-effort workload: Run on CLOS 0 with Waymask 0X3F
RTCP Settings	• RT Control Loop Period (1ms, 125us, 100us) • Buffer Size (Instructions Executed) ○ 132 KB = 6K instructions ○ 648 KB = 30K instructions
RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p adln -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p adln -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a3 -t1 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel Atom® x7425E Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT with XDP-ZC TSN driver using discrete Ethernet i226	1ms RTCP 30k IPCL	TCC Mode disabled. No outliers (CPU and GFX contention)	395 µs	935 µs	357µs	86 million (24 hours)
	1ms RTCP 30k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	412 µs	703 µs	354µs	86 million (24 hours)
	125us RTCP 6k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	73 µs	96 µs	24µs	691 million (24 hours)
Linux_RT with XDP-ZC TSN driver using integrated Ethernet	1ms RTCP 30k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	324 µs	400 µs	105µs	86 million (24 hours)
	125us RTCP 6k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	75 µs	85 µs	27µs	691 million (24 hours)
Linux_RT with DPDK TSN driver using discrete Ethernet i226	1ms RTCP 30k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	142 µs	529 µs	402 µs	86 million (24 hours)
	100us RTCP 6k IPCL	TCC Mode enabled. No outliers (CPU and GFX contention)	44 µs	61 µs	35 µs	691 million (24 hours)
Linux_RT	Cyclictest	250us wakeup interval. TCC mode enabled. (CPU and GFX contention)	3 µs (Avg. latency)	12 µs (Max latency)	11 µs	345 million (24 hours)

4.3.3.3 Real-time configuration for Intel Atom® x6427FE Processor KPI measurements

Hardware		
Motherboard		EHL RVP / CRB (XDP)
CPU	Product	Intel Atom(R) x6427FE Processor
	Speed (MHz)	1.90GHz
	Number of CPUs	4 Cores / 4 Threads
	Stepping	B1
	LLC Cache	4 MB
Chipset		Mule Creek Canyon
Graphic	Driver cores	GT2
Memory	Vendor	Micron Technology
	Type	LPDDR4
	Size (GB)	2x4GB
	Channel	2
BIOS	Vendor	Intel Corporation
	Version	EHLSFWI1.R00.2463.A14.2012290454
	Microcode	0xE
OS	Release	EHL PV Candidate 12
	Kernel version	5.4.61-rt37-intel-preempt-rt #1 SMP PREEMPT_RT

Ethernet Controller:

- Integrated Ethernet port on PCH with 3rd party PHY (Marvell*)

RT Test Configuration on device under test:

- Real-time workload (Cyclictest): on core 3
- Real-time workloads (RTCP):
  - Real-time control loop on core 3
  - Real-time interrupt handler (IRQ) on core 2

Test settings for Intel Atom® x6427FE Processor KPI measurements

Item	Description
BIOS	Intel TCC Mode <Enabled> VTD <Enabled>
Kernel Boot Settings	i915.force_probe=* udmabuf.list_limit=8192 processor.max_cstate=0 intel.max_cstate=0 processor_idle.max_cstate=0 intel_idle.max_cstate=0 clocksource=tsc tsc=reliable nowatchdog intel_pstate=disable idle=poll noht isolcpus=2,3 rcu_nocbs=2,3 rcupdate.rcu_cpu_stall_suppress=1 rcu_nocb_poll irqaffinity=0 i915.enable_rc6=0 i915.enable_dc=0 i915.disable_power_well=0 mce=off hpet=disable numa_balancing=disable igb.blacklist=no efi=runtime art=virtallow iommu=pt nmi_watchdog=0 nosoftlockup hugepages=1024 i915.enable_guc=7 mmio_stale_data=force

Cache allocation settings	L2 CAT: configured
	• RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XFF0
	  • Best-effort workload: Run on CLOS 0 with Waymask 0XF
	L3/LLC CAT: configured
	• RTCP/Cyclic test: Run on CLOS 1 with Waymask 0XFFF0
	  • Best-effort workload: Run on CLOS 0 with Waymask 0XF

RTCP Settings	• RT Control Loop Period (1ms, 300us)
	• Buffer Size (Instructions Executed)
	  ○ 110 KB = 5K instructions
	  ○ 540KB = 25K instructions

RTCP Command Line	• git clone https://github.com/OTCShare2/rtcp-xdp.git **Example** • **Board A:** ./rtcp.sh -p ehl -h i225 -i <ethernet interface> -c rtcp1a -n 2400000 -d 125000 • **Board B:** ./rtcp.sh -p ehl -h i225 -i <ethernet interface> -c rtcp1b -n 2400000 -d 125000 • **Board A and board B:**./rtcp.sh -S (Set's up the environment) • **Board A and board B:**./rtcp.sh -R (Triggers the execution run)
Cyclictest Execution Command	• sudo chrt -f 99 ./cyclictest -a3 -t1 -m -p99 -i250 -h700 -q -D 24h

KPI results for Intel Atom® x6427FE Processor

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
Linux_RT	1ms cycle RTCP KPI	TCC Mode disabled	575µs	896 µs	321 µs	120 Million

Configuration	KPI	Notable Details	Observed Average Cycle Time	Observed MAX Cycle Time	Jitter (MAX-MIN)	Iterations run
with XDP-ZC TSN driver using integrated Ethernet	using a 25k IPCL real-time workload	(CPUmem + 3D Navi)				(24 hours)
	250us RTCP KPI using a 5k IPCL real-time workload	TCC Mode enabled (CPUmem + 3D Navi)*	69µs	171 µs	102 µs	180 Million (24 hours)
Linux_RT	Cyclictest	TCC mode enabled 250-µs wakeup interval	N.A	14 µs (Max latency)	N.A	346 Million (24 hours)

5.0 Advanced Real-time Capabilities and Tuning

This chapter provides additional options for optimizing Intel platforms for real-time usage that go beyond the basic configurations described in previous chapters. Such options are considered more advanced and generally require more in-depth knowledge of processor architecture.

5.1 Configuration of Shared Resources

If the basic real-time configuration does not address all real-time needs some customers may want to try out configuring shared resources like L2/L3 Cache to achieve their expected real-time performance. This chapter provides guidance on how to configure cache to improve real-time performance for those advanced usages where this may be beneficial. Configuring cache in a manner that provides an overall improvement of real-time performance without major impact on overall system performance requires advanced system knowledge and a deep understanding of the cache architecture of your system.

5.1.1 Caches

Enumerating and understanding the cache topology can be an important step when making decisions on workload placement. Cache, both L2 and Last-Level (LLC/L3) may be shared between processor cores.

Cache is an integral part of modern processors and can be critical to reduce latencies, as it allows much quicker access to frequently or recently used data, avoiding the need to fetch the data from memory. As such the availability of sufficient cache is critical for workloads requiring low latencies and determinism. For many applications, including many real-time applications, the default configuration of cache on Intel platforms as well as additional technologies to help with smart usage of the available cache will be sufficient.

For advanced real-time applications cache partitioning has proven to be an effective approach for mitigating multi-workload interference, but when done incorrectly can also negatively affect both real-time and general compute performance.

5.1.1.1 Overview of common cache architectures found on Intel SoC's

Cache topology varies between processors, but in general Cache, both L2 and LLC are generally shared to some degree among compute cores. The following provides 3 examples of Cache topology found on Intel platforms.

For Performance Cores, L2-cache is generally dedicated to a core, whereas for efficiency cores L2-cache may be shared. L3 cache is generally shared among most cores. The following chapter provides guidance on how to understand the cache topology on Intel systems.

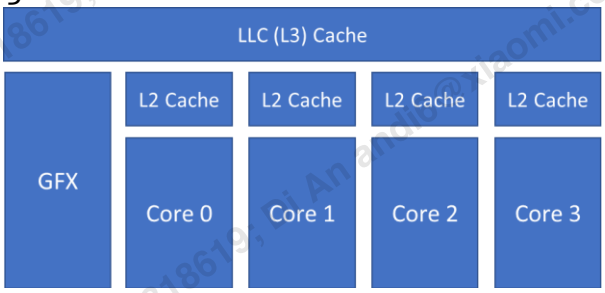


Figure 3: Cache architecture of 11th Gen Intel® Core™ Processor I7-1185GRE (Tiger Lake UP3)

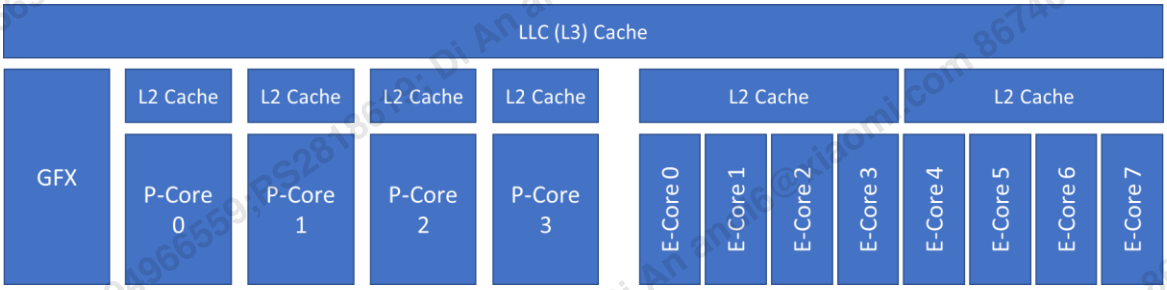


Figure 4: Cache Architecture of 13th Gen Intel® Core™ Processor i5-1350PRE (Raptor Lake P)

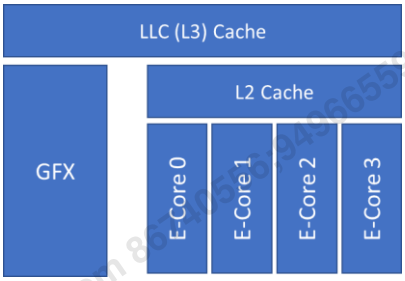


Figure 5: Cache architecture of Intel Atom® X7425E Processor (Alder Lake-N)

5.1.1.2 Enumerating Cache Topology

Enumerating and understanding the cache topology is an important step when making decisions on workload placement.

Intel communicates information about caches such as size, hierarchy, inclusivity, and associativity through CPUID. In Linux, multiple utilities exist for gathering this information and presenting it in a human readable format. Refer to Hardware Locality (hwloc), available through many package managers and also on GitHub (open-mpi/hwloc: Hardware locality (hwloc) (github.com), which provides the *lstopo* utility. Lstopo provides an easy-to-read ascii representation of the caches in the system and CPU cores associated with a cache instance.

When running lstopo, consider using the following parameters:

```
--of ascii      # Output format set to ascii
--no-io         # Hide I/O devices to improve readability
```

Note: As core counts increase, additional screen real estate is required to properly view the output. If the output is not legible, revert to '--of console' instead of '--of ascii'.

5.1.2 LLC (L3) Cache Partitioning

The default cache allocation scheme shares the entire LLC cache between all agents (all cores allocated to CLOS 0), which can result in increased jitter in some applications due to cache thrashing. Applying a simple cache partitioning scheme could minimize this source of jitter. However, in some cases, reducing the amount of cache available to an application can adversely affect performance. As a result, Intel recommends testing applications with both the default configuration (all Cache-Ways shared) and a simple partitioning scheme.

The simplest partitioning scheme is to divide the cache in half, creating one half dedicated to the real-time application(s) and the other for best effort application(s). Intel provides the ability to partition caches at various levels in the caching hierarchy through Cache Allocation Technology (CAT), part of Intel® Resource Director Technology (Intel® RDT).

Note: Certain platforms with support for TCC Mode BIOS may optionally have "GT CLOS", a BIOS setting that modifies the default cache partitioning scheme for the integrated GPU. When set to Enabled, the integrated GPU will use only a small portion of the last level cache versus sharing all of the cache by default.

5.1.2.1 Using L3 CAT for real-time performance optimization

Cache Allocation Technology feature enables more cache resources (i.e., cache space) to be made available for high priority applications based on guidance from the execution environment as shown in Figure 6. The architecture also allows dynamic resource reassignment during runtime to further optimize the performance of the high priority application with minimal degradation to the low priority app. Additionally, resources can be rebalanced for system throughput benefit across use- cases of OSes, VMMs, containers and other scenarios by managing the CPUID and MSR interfaces. This section describes the hardware and software support required in the platform including what is required of the execution environment (i.e., OS/VMM) to support such resource control. Note that in Figure 2 the L3 Cache is shown as an example resource.

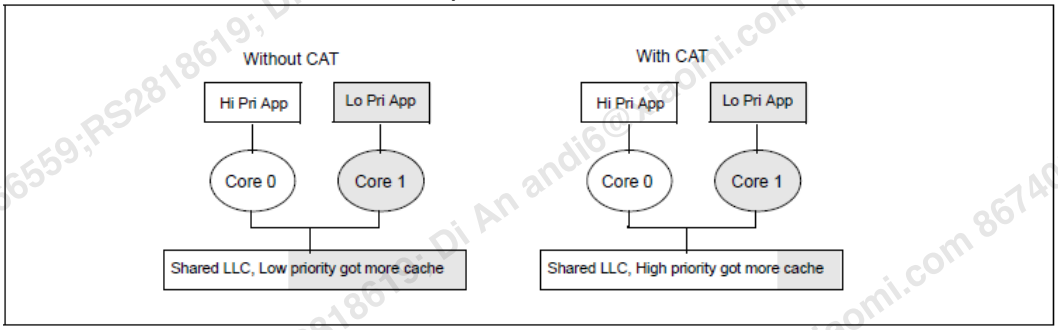


Figure 6: Cache Allocation Technology Enables Allocation of More Resources to High Priority Applications

5.1.2.2 Using intel-cmt-cat

The Intel® RDT software package, intel-cmt-cat, is available on Github (intel/intel-cmt-cat: User space software for Intel(R) Resource Director Technology (github.com) and provides support for configuring Cache Allocation Technology. Follow the instructions in the repository for obtaining and compiling the pqos utility executable.

Usage examples for configuring resource allocations can be found on the intel-cmt-cat wiki:

Usage Examples · intel/intel-cmt-cat Wiki (github.com)

5.1.2.2.1 Example L3 cache partitioning for an 11th Gen Intel® Core™ Processor i7-1185GRE

The 11th Gen Intel® Core™ Processor i7-1185GRE contains 4 cores and 12MB of cache that can be partitioned using the model specific, non-

architectural implementation of L3 Cache Allocation Technology found on Intel® Core™ processors that support Time Coordinated Computing. In this example Cores 2 &3 are used for processing real-time workloads.

Table 4 shows how the 12MB last level cache can be partitioned in half, with cores 0,1 being assigned a non-overlapping portion of the cache from cores 2,3. For completeness, the equivalent commands for programming the MSRs directly are also shown. The MSR's used for configuring the cache masks are L3_MASK_0 (address 0xC90) and L3_MASK_1 (address 0xC91). The MSR used for associating a class of service to a core is PQR_ASSOC (address 0xC8F).

The i7-1185GRE last level cache has a capacity bitmask (CBM) length of 12 (0xFFF), so each class of service will be assigned a CBM length of 6 (0x3F and 0xFC0, respectively) when partitioning the cache in half.

Note: This example matches the cache allocation utilized in the KPI data for 11th Gen Intel® Core™ Processor i7-1185GRE provided in the earlier chapter.

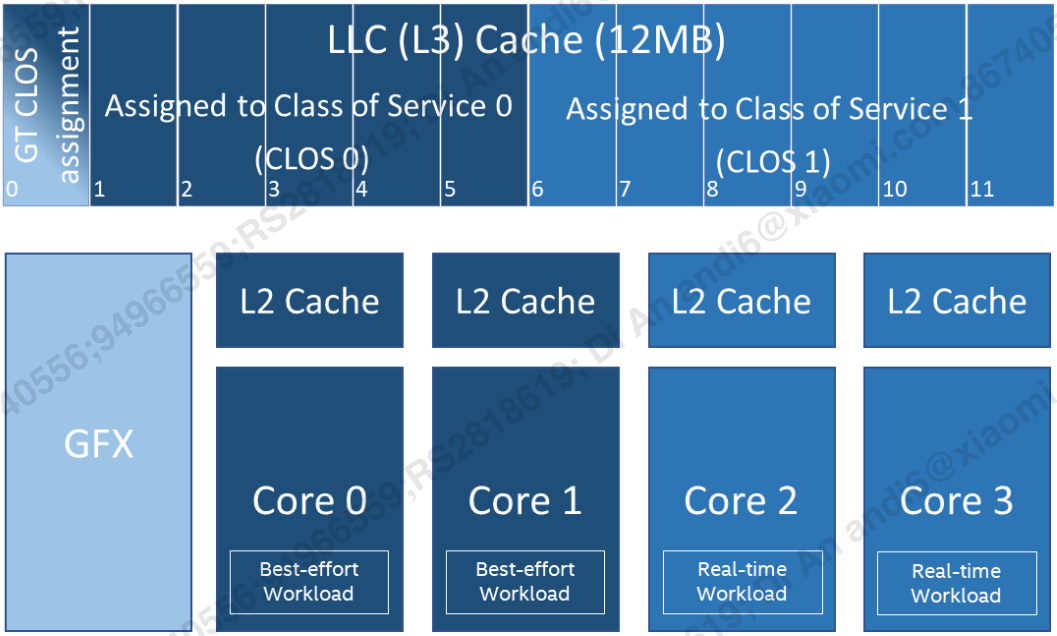


Figure 7: Cache allocation example for 11th Gen Intel® Core™ Processor i7-1185GRE example with GT CLOS enabled.

Table 4: Partitioning the L3 cache in half on the 11th Gen Intel® Core™ Processor i7-1185GRE

Using intel-cmt-cat "pqos" utility	Model Specific Register (MSR) programming	Comments
pqos --iface=msr -e "llc:0=0x3F;llc:1=0xFC0"	wrmsr 0xC90 0x3F wrmsr 0xC91 0xFC0	Assign ½ the cache to CLOS 0 Assign ½ the cache (non-overlapping) to CLOS 1
pqos --iface=msr -a "llc:0=0,1;llc:1=2,3"	wrmsr -p 0 0xC8F 0x000000000 wrmsr -p 1 0xC8F 0x000000000 wrmsr -p 2 0xC8F 0x100000000 wrmsr -p 3 0xC8F 0x100000000	Assign CLOS 0 to Cores 0,1 Assign CLOS 1 to Cores 2,3

A table of capacity bit mask information is provided in Appendix C
Note: More information on Cache Allocation Technology and associated register interfaces can be found in the Intel Software Developers Manual, Volume 3B, Chapter 18.19 "Intel® Resource Directory Technology (Intel® RDT) Allocation Features". The register names used in this section do not contain the "IA32_" prefix as L3 Cache Allocation Technology on the Intel® Core™ Processor i7-1185GRE is non-architectural.

5.2 Using Timed-GPIO

Sometimes it's not enough for software to be told what the current OS/CPU time is "now". For example, when precision time synchronization is an application requirement it can be extremely useful to verify (at least in the lab) the accuracy of the CPU's notion of "now" using a hardware signal to represent ground truth. This is facilitated with a pair of one or more Timed-GPIO (TGPIO) pins that generate a hardware high voltage at precisely the moment the time "ticks" to the next second, followed by a return to low voltage / ground. This aptly named Pulse Per Second (PPS) is commonly used to test synchronization between hardware components. Several examples include:

1. Connect both the TGPIO and the PPS of a PTP-capable hardware component (e.g. an Ethernet NIC such as Intel® Ethernet Controller i226) to an oscilloscope, allowing the test engineer to measure the worst-case time difference between the two signals (which, if synchronized, will both go from low to high simultaneously). This is particularly useful to measure the difference in time accuracy between a NIC and the CPU when PCIe PTM is enabled vs. disabled.
2. Connect the TGPIO to the PPS input of a PTP-capable hardware component, especially for components that do not support PCIe PTM, allowing the time to be synchronized more accurately than with only software. Note that the practicability of this approach may be constrained by the need for a wire to pass from the TGPIO to the NIC.
3. Synchronize time between the CPU and another hardware component, such as a GPS module.

Intel's TGPIO driver triggers a pulse per second (PPS) continuously when installed, allowing engineers to check synchronization or align synchronization to the signal on the TGPIO pin. The TGPIO PPS driver is available in mainline Linux.

5.3 Intel® Speed Shift technology for edge computing to boost real-time performance.

The use of Intel® Speed Shift technology to improve real-time performance was mentioned in Chapter 3.1 as an option. In this chapter we will describe such usage in more detail and walk through a specific configuration example of core frequencies on Intel® Core™ 13th Generation H-series processor for which we also provide a component reliability assessment.

5.3.1 Overview of using Intel® Speed Shift technology for edge computing

Starting with the 12th and 13th Generation Intel® processors Intel® Speed Shift technology, also known as Hardware Controlled Performance States (HWP), was improved by adding per core or module p-state transitions. In contrast to the Enhanced Intel® Speed Step® technology, where the operating system plays a central role in

controlling and monitoring discrete frequency-based operating points, with Intel® Speed Shift technology the processor takes on the responsibility of independently choosing the most suitable performance states based on the workload demand. It does so while considering certain guiding hints programmed by the operating system. These hints encompass factors like setting minimum and maximum performance thresholds, indicating a preference for energy efficiency or performance, and defining a specific time frame for observing the history of workload patterns. The operating system is also equipped with the capability to override HWP's autonomous selection of performance states and assign a desired performance target. However, the actual frequency delivered is still subject to the processor's energy efficiency and performance optimizations. In essence, HWP strikes a dynamic balance between autonomous performance state selection and OS-driven settings.

Setting the frequency of cores that have real-time workloads pinned to them to a level higher than base frequency (HVM) using Intel® Speed Shift technology can boost the real-time performance of those workloads. However, this benefit comes at a cost. Running cores above the HVM frequency impacts reliability and, to stay within the TDP guard bands, may cause more extensive throttling of other cores.

On current Intel platforms the P-state of performance cores, p-cores, can be selected independently per core[1]. Efficiency cores, e-cores, are typically grouped in sets of four cores per module and the P-state can be selected per module.

When set correctly, the real-time cores will constantly run at the set frequency, while other cores will still vary their frequencies as directed by the processor or the OS, including the possibility of throttling as needed. The below figure shows the behavior of various cores. In this example, two cores, labeled RT cores, are set to 3.6Ghz, the rest of the cores are ‘floating’ up to their set max-frequency values, in this example, p-cores up to 2.5GHz, e-cores up to 1.2Ghz, and the integrated GPU up to 1.3GHz.

[1] Future products may group p-cores into modules.

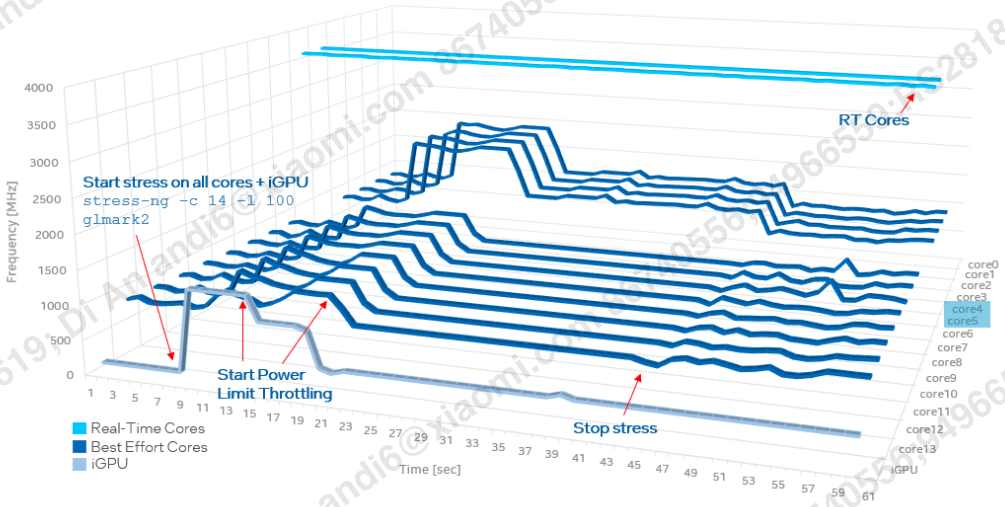


Figure 8: Core behavior when using Intel® Speed Shift technology for edge computing when system is loaded to induce throttling.

Setting some cores to such a higher frequency allows for lower average latencies and reduced jitter for the real-time workloads running on those cores.

5.3.2 Impact of using Intel® Speed Shift technology for edge computing on component reliability and overall system performance.

Setting even just a few cores to a higher, fixed frequency does not come without a cost. Due to higher internal frequency, voltages, and subsequent higher temperature and power, such settings will negatively impact the reliability expectations of the CPU and should be used with careful consideration.

Higher temperatures and power consumption also affects the overall system TDP and depending on the usage may adversely affect the performance of the rest of the cores and the graphics as the processor and OS will automatically throttle those cores and the graphics engine to avoid damage.

To address such concerns, we are describing a specific enveloping configuration on the highest performing SKU of a swim lane that can be leveraged into lower performing SKUs of the same processor family without significant impact on reliability. Such an enveloping configuration example is described in the next section.

5.3.3 Example Configuration using Intel® Speed Shift technology on Intel® Core™ 13th Generation H-series processors.

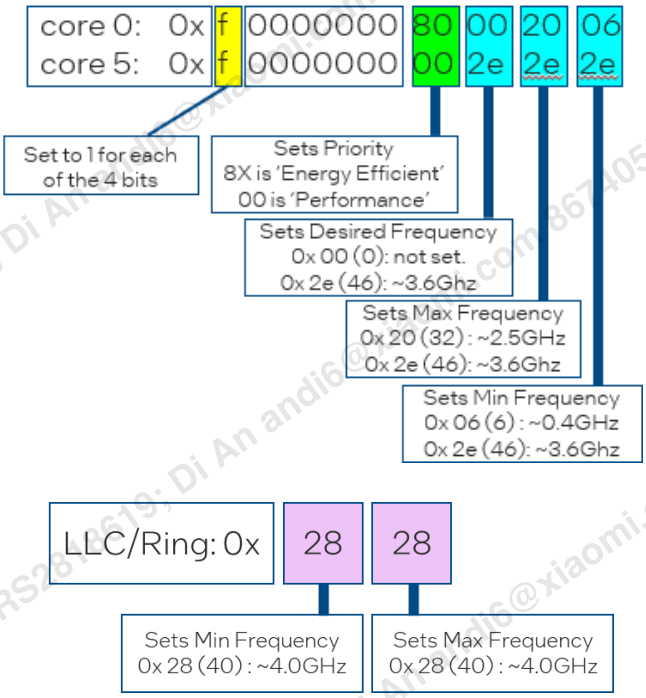
In this example we are using Intel® Speed Shift Technology to set 2 p-cores to a higher frequency and limit the max frequencies of the rest of the P-Cores, all e-cores, the integrated graphics, and the LLC/Ring to their respective HVM frequencies.
To use Intel® Speed Shift Technology for edge computing, it is essential to enable it in the BIOS. The following BIOS settings are recommended:

Ref BIOS menu	BIOS setting	State	Comment
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	Turbo Boost	Enabled	When disabled, turns off Intel® Turbo Boost Technology.
	Intel Speed Shift Technology	Enabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel Speed Step	Enabled	When disabled, turns off Intel Speed Step® technology.
	Energy Efficient Turbo	Disabled	When enabled, turbo frequency is opportunistically lowered to increase efficiency
	HWP Autonomous EPP Grouping	Disabled	When enabled, HWP autonomous requests same p-state for all cores with same EPP value
Intel Advanced Menu > Power &Performance > GT Power Management Control	GT Max Turbo Frequency	300MHz	When set, the GT Max Turbo Frequency is set to the selected value.

Software can detect Intel® Speed Shift technology support using the CPUID instruction. Below are the model-specific registers (MSRs) to be used to configure P-Cores, e-cores, and the LLC/Ring with Intel® Speed Shift technology for this specific example:

MSR details	Setting	Comment
HWP Enable MSR Register: IA32_PM_Enable Address: 0x770	0x1	Switches on Hardware P-States
HWP Request MSR Register: IA32_HWP_REQUEST Address: 0x774	#P-Cores core 0: 0xf000000080002006 core 1: 0xf000000081002006 core 2: 0xf000000082002006 core 3: 0xf000000083002006 core 4: 0xf0000000002e2e2e core 5: 0xf0000000002e2e2e #E-Cores core 6: 0xf000000085001204 core 7: 0xf000000086001204 core 8: 0xf000000087001204 core 9: 0xf000000088001204 core 10: 0xf000000089001204 core 11: 0xf00000008a001204 core 12: 0xf00000008b001204 core 13: 0xf00000008c001204	Set's the frequencies and preferences per core. Used by the OS to provide hints (min, max, desired, energy performance preferences to HWP)
HWP Capabilities MSR Register: IA32_HWP_CAPABILITIES Address: 0x771		Lists HWP performance range
Ring Ratio Limit MSR Register: MSR_RING_RATIO_LIMIT Address: 0x620	0x2828	Sets the minimum and maximum frequency ratio of the LLC/Ring

Figure 9: Intel® Speed Shift technology setting per core frequencies.



Generally, the following formulas should be used to arrive at the right frequency settings:

Performance Cores:

	'Desired Frequency in GHz' * 10 *1.27		= Decimal-	→ Hex- Setting
2.5 GHz example:	2.5	* 10 *1.27	= 32	→ 0x20
3.6 GHz example:	3.6	* 10 *1.27	= 46	→ 0x2e
0.4 GHz example:	0.4	* 10 *1.27	= 6	→ 0x06

Efficiency Cores:

	'Desired Frequency in GHz' * 10 *1.0		= Decimal-	→ Hex-Setting
1.8 GHz example:	1.8	* 10 *1.0	= 18	→ 0x12
0.4 GHz example:	0.4	* 10 *1.0	= 4	→ 0x04

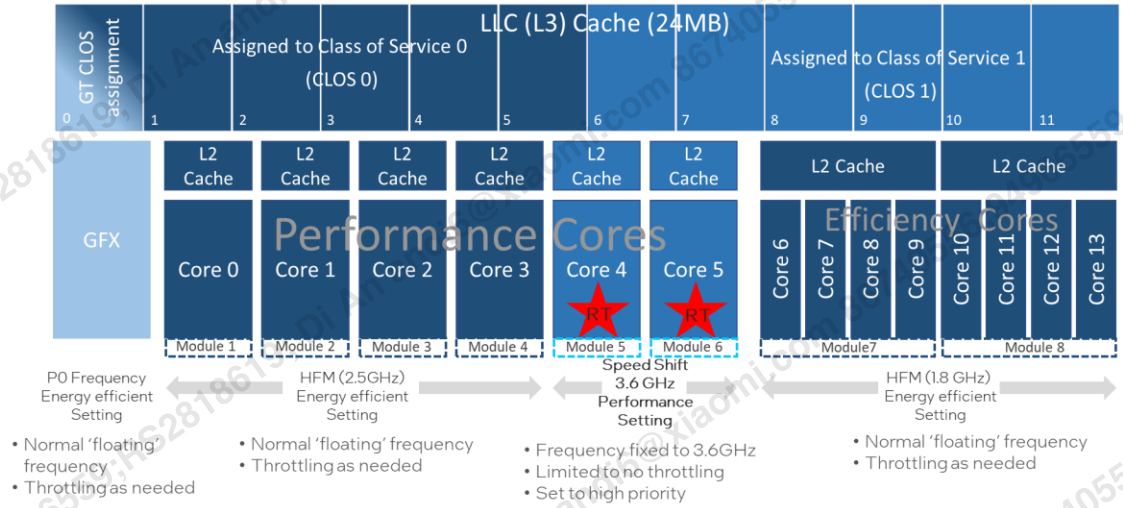
LLC/Ring (Un-core)

	'Desired Frequency in GHz' * 10 *1.0		= Decimal-	→ Hex-Setting
4.0 GHz example:	4.0	* 10 *1.0	= 40	→ 0x28

The amount of throttling occurring on other cores heavily depends on the total load applied by the customer as well as the thermal solution used. If needed customers should evaluate using lower frequency settings than the ones described in this enveloping configuration. Especially for the graphics it may be best to set the frequency to the lowest value that fulfills the workload requirements to reduce throttling of the LLC/Ring.

As mentioned in the previous section, using Intel® Speed Shift technology in that manner may impact reliability and overall system performance. The below described Intel® Speed Shift Technology configuration and associated reliability assessment on Intel® Core™ 13th Generation H-series processors allows customers to confidentially configure their systems to increase the performance of real-time workloads running on specific cores when setting the Max-frequencies at or below the prescribed values, 3.6GHz for up to two cores and HVM on all remaining cores and GFX. While Intel® Turbo Technology is enabled, cores can only reach the prescribed max frequencies, never reaching the much higher turbo frequency of that processor. Depending on the thermal solution used and the workloads running, lower Max-frequencies may be more suitable to avoid throttling of the non-RT cores.

SKU	# of cores	Base Frequency	TDP	Temperature & use condition	Cores w/ higher frequency	Rest of p-cores	E-cores:	GfX
Intel® Core™ i7-13800HRE (RPL H 682)	6 P-cores 8 E-cores	2.5GHz	45W	Extended Temp Industrial use condition	2 of n P-Cores fixed at 3.6GHz	n-2 P-Cores, max frequency at HFM (2.5GHz)	All e-cores, max frequency at HFM (1.8 GHz)	Max frequency at HFM
					Performance Setting (No throttling)	Energy efficiency setting (Will be throttling as needed)		



While this configuration is provided for one specific industrial SKU, Intel® Core™ i7-13800HRE processor, the below reliability assessment for that processor SKU is enveloping other Intel® Core™ 13th Generation H-series processor SKUs when utilizing the same Intel® Speed Shift Technology of edge compute configuration settings:

SKU	# of cores	P-core Base Frequency	Cores w/ higher frequency	Rest of p-cores	E-cores:	GfX
Intel® Core™ i7-13800HE/HRE processors	6 P-cores 8 E-cores	2.5GHz	**1 or 2** of n P-Cores at **≤3.6GHz**	n-2 p-cores at HFM or less (2.5GHz)	All e-cores at HFM or less	At HFM or less
Intel® Core™ i5-13600HE/HRE processors	4 P-cores 8 E-cores	2.7GHz	**1 or 2** of n P-Cores at **≤3.6GHz**	n-2 p-cores at HFM or less (2.7GHz)	All e-cores at HFM or less	At HFM or less
Intel® Core™ i3-13600HE/HRE processors	4 P-cores 4 E-cores	2.1GHz	**1 or 2** of n P-Cores at **≤3.6GHz**	n-2 p-cores at HFM or less (2.1GHz)	All e-cores at HFM or less	At HFM or less

This configuration does not apply to or transfer to other processor generations or swim lanes like for example Intel® Core™ 13th Generation U- Series, P-Series, or S-series processors.

Table 5: Reliability Assessment for enveloping Intel® Speed Shift for edge compute use condition on Intel® Core™ i7-13800HRE processor

Active & Inactive Operation	0-1 Year (8760 hrs)		0-3 Years (26280 hrs)		0-5 Years (43800 hrs)		0-7 Years (61320 hrs)		10 Years (87600 hrs)	
	Cum % Fail	FIT	Cum % Fail	FIT	Cum % Fail	FIT	Cum % Fail	FIT	Cum % Fail	FIT
Goals	0.24%	274	0.72%	274	1.20%	274	NA	NA	2.00%	228
Estimate @ Industrial ET Use Conditions[1]	<0.01%	3	0.01%	3	0.01%	3	0.02%	2	0.02%	2
Estimate @ Industrial ET Intel® Speed Shift for edge compute - Use Conditions[1]	0.01%	12	0.03%	10	0.04%	9	0.05%	8	0.07%	7

Reference Use-condition[2] details for above Reliability assessment.

Category	Parameter	Industrial ET	Industrial ET Intel® Speed Shift for edge compute - Use Conditions
Durations	Operating Time	10 Years 87600 hours	10 Years 87600 hours
Active Operation[3]	Time (%)	100	100
	Junction Temperature, T_j (°C)	83	93
	Time (%)	0	0

[1] Reliability assessments are simulated estimates only.
[2] Reference Use Condition values are intended to represent the integration over time of reliability-related conditions seen over the life of the product in typical use and are not the same as Product Datasheet limits. Sustained exposure to extreme use environments that significantly deviate from the use environment described may affect long-term component reliability.
[3] Active Operation means executing instructions; for multi-core product, equal core usage is assumed. Industrial Extended Temperature reference use conditions do not include the use of turbo within active operation.

Category	Parameter	Industrial ET	Industrial ET Intel® Speed Shift for edge compute - Use Conditions
Inactive Operation[1]	Junction Temperature, T_j (°C)	NA	NA

5.3.4 Advanced use of Intel® Speed Shift technology for edge computing

Intel® Speed Shift technology is not limited to the above shown specific configuration. It could be used to address specific customer needs with other configuration and platforms. Due to the nature of this technology and its impact on component reliability as well as system thermals and overall performance, custom applications are an advanced undertaking and require detailed knowledge of your system and the underlying components and technologies and should only be done with careful consideration.

Intel published a technical paper titled "Empowering Mixed-criticality Industrial Real-time Computing on Performance Hybrid Architecture with Intel's Dynamic Frequency Scaling Evolution". This document offers a more in-depth analysis of the potential impacts and benefits of leveraging Intel's advanced power management features, including Intel® Speed Shift Technology and Intel® Turbo Boost Technology, within real-time computing environments with 12th and 13th Generation Intel® Core™ processors. Additionally, it provides practical guidance on how to effectively implement these capabilities. The technical paper can be found in RDC, document number: 816106.

5.4 Other advanced TCC platform tuning options

The following is a brief description of additional options available in the TCC BIOS menu.

[1] Inactive Operation equates to time spent in idle and/or standby states.

5.4.1 Instruction Fetch Unit

The instruction fetch unit allows the pre-fetchers to be trained on instructions from the application currently running in addition to data accesses from those same applications.
Most workloads do not benefit from this option. Hence it is disabled by default. However, this may help with specific applications such as long linear code found in PLC ladder logic. To evaluate this option, the user should measure the performance both with and without this feature enabled.

5.4.2 AC# on Split Lock and GP# on Lock to UC

Because bus locks, a feature that locks all access to the bus while activated, may adversely affect performance in certain situations. TCC enabled processors may support two features that system software can use to disable bus locking. These are called UC (uncacheable)-lock disable and split-lock disable.

When UC-Lock disable is activated, a locked access using a memory type other than WB (Write back or cacheable) causes a general-protection exception (#GP). The locked access does not occur.
When split-lock disable is activated, a locked access to multiple cache lines causes an alignment-check exception (#AC). The locked access does not occur. For more information about these features see the Intel Software Developer Manual, section 9.1.2.3 “Features to Disable Bus Locks” in volume 3a.
These features can be enabled pre-boot via the options on the TCC options page in BIOS, or post-boot via system software writing to the activation bits, see the Software Developer Manual (SDM) for details on the register.

5.4.3 L2 QoS Enumeration and L2 CAT partitioning

On P-cores, as mentioned previously, L2 cache is per core[1], hence for real-time workloads running on P-cores, L2 CAT is already dedicated to that core. L2 CAT may be beneficial when real-time workloads are running on e-cores, where the L2 cache is shared between 4 E-cores within the same module.

[1] Assumes Hyperthreading is disabled as part of real-time optimizations.

On Hybrid CPUs L2 CAT support is not enumerated and thus not detectable via the standard CPUID leaf enumeration for RDT. In general, Intel does not recommend enabling L2 CAT on hybrid platforms as enumerating L2CAT on hybrid platforms can lead to degraded system performance and errors.

The 'L2 QoS Enumeration' option in TCC BIOS allows this default behavior to be overridden allowing each CPU to enumerate its L2 CAT support, including the number of ways and classes of service supported. In hybrid systems the specific capabilities of each core type could differ, unless the OS enumerates the capabilities of each core the values applied could be incorrect. Potentially resulting in diminished performance as the OS would not use all the available cache ways and or classes of service.

Example on a 12th Generation Intel® Core™ i9-12900E processor

When Resource Control (CONFIG_X86_CPU_RESCTRL) is enabled in the kernel, during the boot sequence the capacity bitmask (CBM) registers for each cache hierarchy that supports Intel® Resource Director Technology (Intel® RDT) Cache Allocation Technology (CAT) are reinitialized. On hybrid systems like the 12th Generation Intel® Core™ processors, the capacity bitmask length for the L2 cache may vary between core types (P-core and E-core). As a result of the differing lengths and depending on which core type was used for initial discovery, programming of one length to all core types can result in undesirable outcomes. Linux utilizes CPUID to discover the capacity bitmask length, however it does not account for different CBM lengths based on core type.

For example, the 12th Generation Intel® Core™ i9-12900E processor consists of 8 P-cores and 8 E-cores. The following table represents the capacity bitmasks out of reset and after reinitialization by Resource Control.

Model Specific Register (MSR) 0xD10 – CBM for L2 Cache

Core Type	Initial value out of reset	Value after Resource Control reinitialization
P-Core	0x3FF	0x3FF
E-Core	0xFFFF	0x3FF

The above values assume the initial probe of CPUID to obtain the capacity bitmask length was issued from a P-core. Reduced performance is a result of changing the E-core L2 CBM from 16-ways (0xFFFF) to only 10 ways (0x3FF), effectively limiting the use of the L2 cache to 62.5% of its total capacity.

It is possible that CPUID may be issued from an E-core, resulting in a CBM length of 0xFFFF. Since it is not possible to program a CBM value of 0xFFFF to a P-core (whose max value is 0x3FF), this will result in an unchecked MSR access error being recorded in the kernel's log messages.

6.0 Terminology

Terminology

Term	Description
API	Application Programming Interface
ASPM	Active State Power Management
BKC	Best Known Configuration
BSP	Board Support Package
C-State	A core power state requested by the Operating System Directed Power Management (OSPM) infrastructure that defines the degree to which the process is “sleeping”.
CAT	Cache Allocation Technology
CBM	Capacity Bit Mask
CMF	Coherent Memory Fabric
COS	Class of Service
CPS	Cyber-physical systems
CRBs	Customer Reference Boards
Deadline	The time when some computation or data must complete or arrive. For some applications, computations or data that arrive late are no longer useful.
E2E	End-to-end
ECC	Error-correcting-code
EDS	External Design Specification
FuSA	Functional Safety
IFWI	Integrated Firmware Image
IHS	Integrated Heat Spreader
Intel® RDT	Intel® Resource Director Technology
TCC	Time Coordinated Computing A modern approach to architecting distributed, synchronized, scalable computing systems that address real-time application requirements for cyber-physical systems (CPS). TCC moves beyond traditional real-time systems based on simple microcontrollers.

Term	Description
IOSF	Input/Output Scalable Fabric
IoT	Internet of Things
Jitter	The difference between the maximum and minimum of some quantity, such as latency measured in units of time. Jitter matters a lot at sensors and actuators, but other mechanisms (such as TSN mechanisms) typically hide software-execution jitter (so long as WCET bounds are satisfied).
KPI	Key Performance Indicator
LCC	Low Core Count
L2	Level 2 cache
L3/LLC	Last level cache
Latency	The duration of time between two events; for example, the time a signal is detected, and a response is received, or the time between an application sending a UDP message until it arrives on the Ethernet wire, or the time required to execute a code segment.
MSR	Model-specific registers are a group of registers available primarily for the operating-system or executive procedures (that is, code running at privilege level 0). These registers control items such as the following: • debug extensions • performance-monitoring counters • machine- check architecture • memory type ranges (MTRRs)
MMIO	Memory Map IO
MVC	Multi Virtual Channel
Noisy neighbor	An application or device, the functioning of which, affects the device or application with temporal requirements (e.g., because of shared resources). Temporal Isolation seeks to reduce the deleterious effect of a noisy neighbor.
OPC UA	A platform-agnostic standard for communication between devices using an “Unified Architecture”, created by the OPC Foundation focusing on the needs of industrial automation.
OSPM	Operating System Directed Power Management
P-State	A power-performance, implantation-dependent state of devices or processors that indicate power and frequency levels.

Term	Description
PCH	Platform Controller Hub
PCS	Physical Coding Sublayer
PCIe*	Peripheral Component Interconnect express*
PM	Power Management
PPS	Pulse Per Second
PTM	Precision Time Measurement, specified by the PCI SIG
PREEMPT_RT	The PREEMPT_RT patch (also the -rt patch or RT patch) makes Linux* into a Real-Time Operating System (RTOS) to a large degree.
RCU	Read-Copy-Update
RDC	Resource & Design Center
Real-time application	An application that requires a complete execution within some WCET with a specified level of reliability. For example, “Has to finish running every millisecond without missing a deadline in 7 days.” Typically, a real-time application contains a sequence of three tasks: sense > compute > actuate and increasingly uses a network to interconnect these. The extent to which a missed deadline impacts the overall system is sometimes described using “soft”, “firm”, and “hard” real-time, but we avoid these terms, preferring to quantify the reliability with number of 9s.
RTCP	Real-Time Compute Performance (Intel developed real-time performance benchmark)
RTOS	Real-Time Operating System
SA	System Agent
SGMII	Serial Gigabit Media-Independent Interface
SKU	Stock Keeping Unit
STA	Station Management
TBI	Ten-Bit Interface
TC	Traffic Classes
TDP	Thermal Design Power

Term	Description
Temporal Isolation	The degree to which a system can meet the time-related requirements of a real-time workload when the workload is running alongside other workloads on the system. In a typical system, concurrent workloads create contention for shared resources that can cause spikes in latency and increased jitter for the real-time workload. TCC capabilities help mitigate concurrent workload interference.
Time-Sensitive Networking (TSN)	A task-group of IEEE 802.1 that creates / amends the Ethernet and other standards, enabling dramatically better worst-case time performance (time-synchronization & latency). Also used to describe the standards / amendments from the TSN task group. https://1.ieee802.org/tsn/
Time synchronization	The degree to which two or more systems or devices agree on what time it is, to within some maximum error. Enables sensors, compute systems, actuators, and network elements to operate on a global schedule. Enables time-coordinated computing devices to time-division multiplex real-time and non-real-time tasks, measure latencies, and detect violation of deadlines. Enables an RTOS to schedule a task at a specific time.
TGPIO	Timed-General Purpose I/O
UDP	User Datagram Protocol
UEFI	Unified Extensible Firmware Interface
VCs	Virtual Channels
Workload	An application that performs some useful computational work, including (perhaps) receiving input, performing computation, and generating an output.
WCET	Worst-case execution time. The maximum measured latency of the compute portion of an application, across multiple iterations. WCET relates to reliability, described by “the number of 9s”. For instance, reliability of two 9s refers to missing the deadline 1 out of 100 times.

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7.0 Reference Documents

In Table 5, documents with a document number are available on Resource and Design Center. Log into the Resource and Design Center to search for and download the document numbers. Contact your Intel field representative for access.

Note: Third-party links are provided as a reference only. Intel does not control or audit third-party benchmark data or the websites referenced in this document. Visit the referenced website and confirm whether the referenced data is accurate.

Table 6: Reverence Documents

Document	Document No./Location
Real-Time Gold Deck	627170 https://cdrdv2.intel.com/v1/dl/getContent/627170
Ethernet Time-Sensitive Networking on Linux* for Intel® Processors & Ethernet Controller i225/i226 – Get Started Guide	616446 https://cdrdv2.intel.com/v1/dl/getContent/616446
Wiki for Intel-cmt-cat on Github	intel/intel-cmt-cat Wiki (github.com)
13th Gen Intel® Core™ Mobile Processors for IoT Edge Page	https://www.intel.com/content/www/us/en/products/details/embedded-processors/core/13thgenmobile.html
14th Gen Intel® Core™ Desktop Processors for IoT Edge Page	https://www.intel.com/content/www/us/en/products/details/embedded-processors/core/14thgen.html
Intel® Ethernet Controller I226 Collection	https://www.intel.com/content/www/us/en/products/details/ethernet/gigabit-controllers/i226-controllers/docs.html?wapkw=i226&grouping=rdc+Content+Types&s=Newest
Intel® Ethernet Controller I225/I226 Product Brief	621753 https://cdrdv2.intel.com/v1/dl/getContent/621753
Intel® 64 and IA-32 Architectures Software Developer's Manual	https://software.intel.com/en-us/articles/intel-sdm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System programming guide, part 2	671427 https://cdrdv2.intel.com/v1/dl/getContent/671427

Document	Document No./Location
Get Started with Linux TSN	https://docs.google.com/document/d/1va_VbXEuVglQR2Xvawd01buUjhs5wifDw0tZ8xI56yE/edit?usp=sharing This User Guide describes the Time-Sensitive Networking (TSN) Reference Software for Linux*. It includes three demos and walks users through running them as well as understanding the features and capabilities of this reference software.
Yocto Project* Linux Kernel Development Manual	https://www.yoctoproject.org/docs/1.6.1/kernel-dev/kernel-dev.html
PCI-SIG, PCI Express Base Specification Revision 2.1 (subscription based)	http://pcisig.com/specifications/pciexpress/base
Linux kernel command-line parameters	https://www.kernel.org/doc/html/latest/admin-guide/kernel-parameters.html
Event Histograms	https://git.kernel.org/pub/scm/linux/kernel/git/rt/linux-stable-rt.git/tree/Documentation/trace/histogram.rst?h=v5.15-rt
PREEMPT_RT patches	https://wiki.linuxfoundation.org/realtime/start
Technical Paper: Empowering Mixed-criticality Industrial Real-time Computing on Performance Hybrid Architecture with Intel's Dynamic Frequency Scaling Evolution	816106 Empowering Mixed-criticality Industrial Real-time Computing on Performance Hybrid Architecture with Intel's Dynamic Frequency Scaling Evolution

Appendix A - Intel processors with Time Coordinated Compute support

A.1 Intel® Xeon™ Processors with Intel® TCC support

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: Intel® Xeon™ Processors

A.1.1 Intel® Xeon™ D-2700 and D-1700 Processors

The following SKUs provide support for Time Coordinated Compute (check intel.com for the most up-to-date product information).

Intel® Xeon™ D-2700 and D-1700 processors with Intel® TCC support.

	D-2752TER	D-1746TER	D-1735TR	D-1715TER	D-1712TR
Use Condition	Embedded	Embedded	Embedded	Embedded	Embedded
Cores	12	10	8	4	4
TDP	77W	67W	59W	50W	40W
TCC	Yes	Yes	Yes	Yes	Yes

A.1.2 Intel® Xeon™ W-11000E Series Processors

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

Intel® Xeon™ W-11000E Series processors with Intel® TCC support

	W-11865MRE	W11865MLE
Use Condition	Industrial	Industrial
Cores	8	8
TDP	45W	25W
TCC	Yes	Yes

	W-11555MRE	W-11555MLE	W-11155MRE	W-11155MLE
Use Condition	Industrial	Industrial	Industrial	Industrial

	W-11555MRE	W-11555MLE	W-11155MRE	W-11155MLE
Cores	6	4	4	6
TDP	45W	25W	35W	25W
TCC	Yes	Yes	Yes	Yes

A.2 Intel® Core™ Processors with Intel® TCC support

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: Intel® Core™ Processors

A.2.1 14th Generation Intel® Core™ Processors (S Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

14th Generation Intel® Core™ S-series Processors with Intel® TCC support (Corporate/Mainstream)

	i9-14900/ 14900T	i7-14700/ 14700T	i5-14500/ 14500T	i5-14400/ 14400T	i3-14100/ 14100T
Use Condition	PC Client	PC Client	PC Client	PC Client	PC Client
Cores[1]	24 (8 + 16)	20 (8 + 12)	14 (6 + 8)	10 (6 + 4)	8 (4 + 0)
TCC	Yes	Yes	Yes	Yes	Yes

14th Generation Intel® Core™ S-series Processors with Intel TCC support (Low Power)

	I9-13900T	i7-14700T	i5-14500T	i5-14400T	i3-14100T
Use Condition	PC Client	PC Client	PC Client	PC Client	PC Client
Cores[1]	24 (8 + 16)	20 (8 + 12)	14 (6 + 8)	10 (6 + 4)	8 (4 + 0)
TCC	Yes	Yes	Yes	Yes	Yes

A.2.2 13th Generation Intel® Core™ Processors (U/P/H Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

13th Generation Intel® Core™ U-Series Processors (15W) with Intel® TCC support

	i7-1365UE	i5-1345UE	I5-1335UE	i3-1315UE
Use Condition	Gen Embedded	Gen Embedded	Gen Embedded	Gen Embedded

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

	i7-1365UE	i5-1345UE	I5-1335UE	i3-1315UE
Cores[1]	10 (2 + 8)	10 (2 + 8)	10 (2 + 8)	6 (2 + 4)
TCC	Yes	Yes	Yes	Yes

	i7-1365URE	i5-1345URE	i3-1315URE	I7-1366URE (Fusa)
Use Condition	Industrial	Industrial	Industrial	Industrial
Cores[1]	10 (2 + 8)	10 (2 + 8)	6 (2 + 4)	10 (2 + 8)
TCC	Yes	Yes	Yes	Yes

13th Generation Intel® Core™ P-Series Processors (28W) with Intel® TCC support

	i7-1370PE	i5-1350PE	i5-1340PE	i3-1320PE
Use Condition	Gen Embedded	Gen Embedded	Gen Embedded	Gen Embedded
Cores[1]	14 (6 + 8)	12 (4 + 8)	12 (4 + 8)	8 (4 + 4)
TCC	Yes	Yes	Yes	Yes

	i7-1370PRE	i5-1350PRE	i3-1320PRE	I7-1375PRE (Fusa)
Use Condition	Industrial	Industrial	Industrial	Industrial
Cores[1]	14 (6 + 8)	12 (4 + 8)	8 (4 + 4)	14 (6 + 8)
TCC	Yes	Yes	Yes	Yes

13th Generation Intel® Core™ H-Series Processors (45W) with Intel® TCC support

	i7-13800HE	i5-13600HE	i3-13300HE
Use Condition	Gen Embedded	Gen Embedded	Gen Embedded
Cores[1]	14 (6 + 8)	12 (4 + 8)	8 (4 + 4)
TCC	Yes	Yes	Yes

	i7-13800HRE	i5-13600HRE	i3-13300HRE
Use Condition	Industrial	Industrial	Industrial
Cores[1]	14 (6 + 8)	12 (4 + 8)	8 (4 + 4)
TCC	Yes	Yes	Yes

A.2.3 13th Generation Intel® Core™ Processors (S Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

13th Generation Intel® Core™ S-series Processors with Intel® TCC support (Corporate/Mainstream)

	i9-13900	i7-13700	i5-13500	i5-13400	i3-13100
Use Condition	PC Client	PC Client	PC Client	PC Client	PC Client
Cores[1]	24 (8 + 16)	16 (8 + 8)	14 (6 + 8)	10 (6 + 4)	4 (4 + 0)
TCC	yes	Yes	Yes	Yes	Yes

	i9-13900E	i7-13700E	i5-13500E	i5-13400E	i3-13100E
Use Condition	Embedded	Embedded	Embedded	Embedded	Embedded
Cores[2]	24 (8 + 16)	16 (8 + 8)	14 (6 + 8)	10 (6 + 4)	4 (4 + 0)
TCC	Yes	Yes	Yes	Yes	Yes

13th Generation Intel® Core™ S-series Processors with Intel® TCC support (Low Power)

	i7-13700T	i5-13500T	i3-13100T
Use Condition	PC Client	PC Client	PC Client
Cores[1]	16 (8 + 8)	14 (6 + 8)	4 (4 + 0)
TCC	Yes	Yes	Yes

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.
[2] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

	i9-13900TE	i7-13700TE	i5-13500TE	i3-13100TE
Use Condition	Embedded	Embedded	Embedded	Embedded
Cores[1]	24 (8 + 16)	16 (8 + 8)	14 (6 + 8)	4 (4 + 0)
TCC		Yes	Yes	Yes

A.2.4 12th Generation Intel® Core™ Processors (S-Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

12th Generation Intel® Core™ S-series Processors with Intel® TCC support

	i9-12900E	i7-12700E	i5-12500E	i3-12100E
Use Condition	Embedded	Embedded	Embedded	Embedded
Cores[1]	16 (8 + 8)	12 (8 + 4)	6 (6 + 0)	4 (4 + 0)
TDP	65W	65W	65W	65W
TCC	Yes	Yes	Yes	Yes

A.2.5 11th Generation Intel® Core™ Processors (UP3 Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

11th Generation Intel® Core™ UP3-Series Processors with Intel® TCC support

	i7-1185GRE	I5-1145GRE	I3-1115GRE
Use Condition	Industrial	Industrial	Industrial
Cores	4	4	2
TDP	28W	28W	28W
TCC	Yes	Yes	Yes

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

A.3 Intel Atom® Processors with Intel® TCC support

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: Intel Atom® Series Processors

A.3.1 Intel Atom® x7000E, x7000RE, and x7000C Series Processors

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

Intel Atom® x7000RE Series Processors with Intel® TCC support (Industrial)

	X7211RE	X7213RE	X7433RE	X7835RE
Use Condition	Embedded, Industrial, and Communication			
Cores	2	2	4	8
TDP	6W	9W	9W	12W
TCC	Yes	Yes	Yes	Yes
FuSa	No	No	No	No

Intel Atom® x7000C Series Processors with Intel® TCC support (Communication)

	X7203C	X7405C	X7809C
Use Condition	Embedded and Communication		
Cores	2	4	8
TDP	9W	12W	25W
TCC	Yes	Yes	Yes
FuSa	No	No	No

Intel Atom® x7000E Series Processors with Intel® TCC support

	X7211E	X7425E	X7213E
Use Condition	Embedded		
Cores	2	4	2
TDP	6W	12W	10W
TCC	Yes	Yes	Yes

	X7211E	X7425E	X7213E
FuSa	No	No	No

A.3.2 Intel Atom® x6000E Series Processors

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

Intel Atom® x6000E Series Processors with Intel® TCC support

	x6212RE	X6414RE	X6425RE	X6200FE	X6427FE
Use Condition	Industrial	Industrial	Industrial	Industrial	Industrial
Cores	2	4	4	2	4
TDP	6W	9W	12W	4.5W	12W
TCC	Yes	Yes	Yes	Yes	Yes
FuSa	No	No	No	Yes	Yes

Intel Atom® x6000E Series Performance Upgrade Processors with Intel® TCC support

	X6214RE	X6416RE
Use Condition	Industrial	Industrial
Cores	2	4
TDP	6W	9W
TCC	Yes	Yes
FuSa	No	No

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Appendix B Platform Specific Firmware Configurations (included in TCC Mode)

B.1 Intel® Xeon® Processors Firmware Configuration

B.1.1 Intel® Xeon® D-2700 and D-1700 Series Processors (Ice Lake D)

The following table lists the individual BIOS menu items set by TCC BIOS mode automatically. Specific menu path reflects locations in Intel's reference BIOS. Your BIOS vendor may use different naming convention. If needed ask your BIOS vendor for more information.

Menu	Option	TCC Mode Setting	Description
EDKII Menu\ Socket Configuration\ Advanced Power Management Configuration\ CPU P State Control	HW P-states	Disabled	When disabled, prohibits the core from entering low-power states.
	Intel Speed Step	Disabled	When disabled, turns off Intel Speed Step® technology.
EDKII Menu\ Socket Configuration\ Advanced Power Management Configuration\ CPU C State Control\	Enable Monitor MWAIT	Disabled	Allows Monitor and MWAIT instructions and disables C-States
EDKII Menu\ Socket Configuration\ Advanced Power Management Configuration\ Hardware PM State Control	Hardware P-States	Disabled	Disable: Hardware chooses a P-state based on OS
EDKII Menu\ Socket Configuration\ Processor Configuration	Hyper-Threading	Disabled	Disable Hyper-Threading Technology.
EDKII Menu\ Socket Configuration\ Memory Configuration	Page Policy	Adaptive	Select Page Policy
EDKII Menu\ Platform Configuration\ PCH-IO Configuration	Legacy IO Low Latency	Enabled	When enabled, turns off PCH clock gating.

Menu	Option	TCC Mode Setting	Description
EDKII Menu\ Socket Configuration\ Advanced Power Management Configuration\ Memory Power & Thermal Configuration\ DRAM RAPL Configuration	DRAM RAPL	Disabled	Disable DRAM Rapl
	DRAM RAPL Extended Range	Disabled	Disable DRAM Rapl Extended Range
EDKII Menu\ Socket Configuration\ Advanced Power Management Configuration\ Memory Power & Thermal Configuration\ Memory Power Savings Advanced Options	CKE Throttling	Manual	Configures CKE Throttling
EDKII Menu\ Socket Configuration\ Advanced Power Management Configuration\ Memory Power & Thermal Configuration\ Memory Power Savings Advanced Options\ CKE Feature	APD	Disabled	APD Off
	PPD	Disabled	PPD Off
EDKII Menu\ Platform Configuration\ PCH-IO Configuration\ Debug Settings	Rlink ASPM Enable	Disabled	Disable L1 ASPM for Rlink
EDKII Menu\ Platform Configuration\ PCH-IO Configuration\ PCI Express Configuration\ PCI Express Root Port #	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.
	Multi-VC	Enabled	Enables Multi Virtual Channels

B.1.2 Intel® Xeon® W-11000E Series Processors (Tiger Lake H)

See chapter 3.3.1.2.3 for details of FW configuration.

B.2 Intel® Core™ Processors Firmware Configuration

B.2.1 13th & 14th Generation Intel® Core™ Processors (Raptor Lake & Raptor Lake Refresh)

The following table lists the individual BIOS menu items set by TCC BIOS mode automatically. Specific menu path reflects locations in Intel's reference BIOS. Your BIOS vendor may use different naming convention. If needed ask your BIOS vendor for more information.

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	C states	Disabled	When disabled, prohibits the core from entering low-power states.
	Intel Speed Shift Technology	Enabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel Speed Step	Enabled	When disabled, turns off Intel Speed Step® technology.
Intel Advanced > ACPI D3Cold settings	ACPI D3Cold Support	Disabled	When disabled, prohibits some device power management states.
Intel Advanced > ACPI Settings	Low Power S0 Idle Capability	Disabled	When disabled, prohibits S0ix states. S0ix states shut off parts of the SoC when they are not in use.
Intel Advanced Menu\CPU Configuration	Hyper-Threading	Disabled	Disable Hyper-Threading Technology.
Intel Advanced > Memory Configuration	Page Close Idle Timeout	Disabled	When disabled, turns off memory power management.
	Power Down Mode	No Power Down	When disabled, turns off memory power management.
	SA GV	Disabled	When disabled, turns off SA GV. SA GV dynamically scales the work point (V/F), by applying DVFS (Dynamic Voltage Frequency Scaling)
Intel Advanced > Power & Performance > GT – Power Management Control	RC6(Render Standby)	Disabled	When disabled, prohibits the GPU from entering low-power state (RC6).
Intel Advanced > PCH-IO Configuration	Legacy IO Low Latency	Enabled	When enabled, turns off PCH clock gating.

Menu	Option	TCC Mode Setting	Description
Intel Advanced > PCH-IO Configuration > PCI Express Configuration	DMI Link ASPM Control	Disabled	When disabled, turns off Active State Power Management (ASPM) control for the DMI link.
Intel Advanced > PCH-IO Configuration > TSN GBE Configuration	PCH TSN Multi-VC	Enabled	Enables PCH Multi Virtual Channels for integrated 2.5Gb Ethernet MAC with TSN support
Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.
	Multi-VC	Enabled	Enables Multi Virtual Channels
	PCI Express Clock Gating	Disabled	When enabled, provides support for PCIe virtual channel capability.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

The following options are part of TCC BIOS mode but are only available in BIOS versions that include TCC enhancements:

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Intel® Time Coordinated Computing	GT CLOS	Enabled	Integrated GPU only has access to small portion of the last level cache

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Intel® Time Coordinated Computing	IO Fabric Low Latency	Enabled	When enabled, turns off some power management in the PCH IO fabrics. This option provides the most aggressive IO fabric performance setting. S3 state is not supported.

B.2.2 12th Generation Intel® Core™ Processors (Alder Lake)

The following table lists the individual BIOS menu items set by TCC BIOS mode automatically. Specific menu path reflects locations in Intel's reference BIOS. Your BIOS vendor may use different naming convention. If needed ask your BIOS vendor for more information.

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	C states	Disabled	When disabled, prohibits the core from entering low-power states.
	Intel Speed Shift Technology	Enabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel Speed Step	Enabled	When disabled, turns off Intel Speed Step® technology.
Intel Advanced > ACPI D3Cold settings	ACPI D3Cold Support	Disabled	When disabled, prohibits some device power management states.
Intel Advanced > ACPI Settings	Low Power S0 Idle Capability	Disabled	When disabled, prohibits S0ix states. S0ix states shut off parts of the SoC when they are not in use.
Intel Advanced Menu\CPU Configuration	Hyper-Threading	Disabled	Disable Hyper-Threading Technology.
Intel Advanced > Memory Configuration	Page Close Idle Timeout	Disabled	When disabled, turns off memory power management.
	Power Down Mode	No Power Down	When disabled, turns off memory power management.
	SA GV	Disabled	When disabled, turns off SA GV. SA GV dynamically scales the work point (V/F), by applying DVFS (Dynamic Voltage Frequency Scaling)

Menu	Option	TCC Mode Setting	Description
Intel Advanced > Power & Performance > GT – Power Management Control	RC6(Render Standby)	Disabled	When disabled, prohibits the GPU from entering low-power state (RC6).
Intel Advanced > PCH-IO Configuration	Legacy IO Low Latency	Enabled	When enabled, turns off PCH clock gating.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration	DMI Link ASPM Control	Disabled	When disabled, turns off Active State Power Management (ASPM) control for the DMI link.
Intel Advanced > PCH-IO Configuration > TSN GBE Configuration	PCH TSN Multi-VC	Enabled	Enables PCH Multi Virtual Channels for integrated 2.5Gb Ethernet MAC with TSN support
Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.
	Multi-VC	Enabled	Enables Multi Virtual Channels
	PCI Express Clock Gating	Disabled	When enabled, provides support for PCIe virtual channel capability.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

The following options are part of TCC BIOS mode but are only available in BIOS versions that include TCC enhancements:

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Intel® Time Coordinated Computing	GT CLOS	Enabled	Integrated GPU only has access to small portion of the last level cache
Intel Advanced Menu > Intel® Time Coordinated Computing	IO Fabric Low Latency	Enabled	When enabled, turns off some power management in the PCH IO fabrics. This option provides the most aggressive IO fabric performance setting. S3 state is not supported.

B.2.3 11th Generation Intel® Core™ Processors (Tiger Lake)

The following table lists the individual BIOS menu items set by TCC BIOS mode automatically. Specific menu path reflects locations in Intel's reference BIOS. Your BIOS vendor may use different naming convention. If needed ask your BIOS vendor for more information.

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	C states	Disabled	When disabled, prohibits the core from entering low-power states.
	Intel Speed Shift Technology	Disabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel Speed Step	Disabled	When disabled, turns off Intel Speed Step® technology.
Intel Advanced > ACPI D3Cold settings	ACPI D3Cold Support	Disabled	When disabled, prohibits some device power management states.
Intel Advanced > ACPI Settings	Low Power S0 Idle Capability	Disabled	When disabled, prohibits S0ix states. S0ix states shut off parts of the SoC when they are not in use.
Intel Advanced Menu > CPU Configuration	Hyper-Threading	Disabled	Disable Hyper-Threading Technology.
Intel Advanced > Memory Configuration	Page Close Idle Timeout	Disabled	When disabled, turns off memory power management.
	Power Down Mode	No Power Down	When disabled, turns off memory power management.
	SA GV	Disabled	When disabled, turns off SA GV. SA GV dynamically scales the

Menu	Option	TCC Mode Setting	Description
			work point (V/F), by applying DVFS (Dynamic Voltage Frequency Scaling)
Intel Advanced > Power & Performance > GT – Power Management Control	RC6(Render Standby)	Disabled	When disabled, prohibits the GPU from entering low-power state (RC6).
Intel Advanced > PCH-IO Configuration	Legacy IO Low Latency	Enabled	When enabled, turns off PCH clock gating.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration	DMI Link ASPM Control	Disabled	When disabled, turns off Active State Power Management (ASPM) control for the DMI link.
Intel Advanced > PCH-IO Configuration > TSN GBE Configuration	PCH TSN Multi-VC	Enabled	Enables PCH Multi Virtual Channels for integrated 2.5Gb Ethernet MAC with TSN support
Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.
	Multi-VC	Enabled	Enables Multi Virtual Channels
	PCI Express Clock Gating	Disabled	When enabled, provides support for PCIe virtual channel capability.
Intel Advanced > System Agent (SA) Configuration	WRC	Enabled	When enabled, turns on Intel® Data Direct I/O Technology (Intel® DDIO).
Intel Advanced > PCH-IO Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

The following options are part of TCC BIOS mode but are only available in BIOS versions that include TCC enhancements:

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Intel® Time Coordinated Computing	GT CLOS	Enabled	Integrated GPU only has access to small portion of the last level cache
Intel Advanced Menu > Intel® Time Coordinated Computing	IO Fabric Low Latency	Enabled	When enabled, turns off some power management in the PCH IO fabrics. This option provides the most aggressive IO fabric performance setting. S3 state is not supported.
Intel Advanced > Intel® Time Coordinated Computing	OPIO Recentering	Disabled	Disable OPIO Recentering to improve PCIe latency.

B.3 Intel Atom® Processors Firmware Configuration

B.3.1 Intel Atom® x7000E/x7000C/x7000RE Series Processors (Alder Lake-N & Amston Lake)

The following table lists the individual BIOS menu items set by TCC BIOS mode automatically. Specific menu path reflects locations in intel's reference BIOS. Your BIOS vendor may use different naming convention. If needed ask your BIOS vendor for more information.

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	C states	Disabled	When disabled, prohibits the core from entering low-power states.
	Intel Speed Shift Technology	Enabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel Speed Step	Enabled	When disabled, turns off Intel Speed Step® technology.
Intel Advanced > ACPI D3Cold settings	ACPI D3Cold Support	Disabled	When disabled, prohibits some device power management states.
Intel Advanced > ACPI Settings	Low Power S0 Idle Capability	Disabled	When disabled, prohibits S0ix states. S0ix states shut off parts

Menu	Option	TCC Mode Setting	Description
			of the SoC when they are not in use.
Intel Advanced > Memory Configuration	Page Close Idle Timeout	Disabled	When disabled, turns off memory power management.
	Power Down Mode	No Power Down	When disabled, turns off memory power management.
	SA GV	Disabled	When disabled, turns off SA GV. SA GV dynamically scales the work point (V/F), by applying DVFS (Dynamic Voltage Frequency Scaling)
Intel Advanced > Power & Performance > GT – Power Management Control	RC6(Render Standby)	Disabled	When disabled, prohibits the GPU from entering low-power state (RC6).
Intel Advanced > PCH-IO Configuration	Legacy IO Low Latency	Enabled	When enabled, turns off PCH clock gating.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration	DMI Link ASPM Control	Disabled	When disabled, turns off Active State Power Management (ASPM) control for the DMI link.
Intel Advanced > PCH-IO Configuration > TSN GBE Configuration	PCH TSN Multi-VC	Enabled	Enables PCH Multi Virtual Channels for integrated 2.5Gb Ethernet MAC with TSN support
Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	N/A	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	N/A	When disabled, turns off PCIe L1 substates.
	PTM	N/A	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.
	Multi-VC	N/A	Enables Multi Virtual Channels
	PCI Express Clock Gating	N/A	When enabled, provides support for PCIe virtual channel capability.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).

Menu	Option	TCC Mode Setting	Description
Repeat the same for all available PCI Express Root Port's	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

The following options are part of TCC BIOS mode but are only available in BIOS versions that include TCC enhancements:

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Intel® Time Coordinated Computing	GT CLOS	Enabled	Integrated GPU only has access to small portion of the last level cache
Intel Advanced Menu > Intel® Time Coordinated Computing	IO Fabric Low Latency	Enabled	When enabled, turns off some power management in the PCH IO fabrics. This option provides the most aggressive IO fabric performance setting. S3 state is not supported.

B.3.2 Intel Atom® x6000E Series Processors (Elkhart Lake)

The following table lists the individual BIOS menu items set by TCC BIOS mode automatically. Specific menu path reflects locations in intel's reference BIOS. Your BIOS vendor may use different naming convention. If needed ask your BIOS vendor for more information.

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	C states	Disabled	When disabled, prohibits the core from entering low-power states.
	Intel Speed Shift Technology	Disabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel SpeedStep	Disabled	When disabled, turns off Intel SpeedStep® technology.

Menu	Option	TCC Mode Setting	Description
Intel Advanced > ACPI D3Cold settings	ACPI D3Cold Support	Disabled	When disabled, prohibits some device power management states.
Intel Advanced > ACPI Settings	Low Power S0 Idle Capability	Disabled	When disabled, prohibits S0ix states. S0ix states shut off parts of the SoC when they are not in use.
Intel Advanced > Memory Configuration	Page Close Idle Timeout	Disabled	When disabled, turns off memory power management.
	Power Down Mode	No Power Down	When disabled, turns off memory power management.
	SA GV	Disabled	When disabled, turns off SA GV. SA GV dynamically scales the work point (V/F), by applying DVFS (Dynamic Voltage Frequency Scaling)
Intel Advanced > Power & Performance > GT – Power Management Control	RC6(Render Standby)	Disabled	When disabled, prohibits the GPU from entering low-power state (RC6).
Intel Advanced > PCH-IO Configuration	Legacy IO Low Latency	Enabled	When enabled, turns off PCH clock gating.
Intel Advanced > PCH-IO Configuration > PCI Express Configuration	DMI Link ASPM Control	Disabled	When disabled, turns off Active State Power Management (ASPM) control for the DMI link.
Intel Advanced > PCH-IO Configuration > TSN GBE Configuration	PCH TSN Multi-VC	Enabled	Enables PCH Multi Virtual Channels for integrated 2.5Gb Ethernet MAC with TSN support
Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration Repeat the same for all available PCI Express Root Port's	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.
	Multi-VC	Enabled	Enable Multi Virtual Channels

Menu	Option	TCC Mode Setting	Description
Intel Advanced > PCH-IO Configuration > PCI Express Configuration **Repeat the same for all available PCI Express Root Port's**	ASPM	Disabled	When disabled, turns off Active State Power Management (ASPM).
	L1 Substates	Disabled	When disabled, turns off PCIe L1 substates.
	PTM	Enabled	When enabled, provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

The following options are part of TCC BIOS mode but are only available in BIOS versions that include TCC enhancements:

Menu	Option	TCC Mode Setting	Description
Intel Advanced Menu > Intel® Time Coordinated Computing	GT CLOS	Enabled	Integrated GPU only has access to small portion of the last level cache
Intel Advanced Menu > Intel® Time Coordinated Computing	IO Fabric Low Latency	Enabled	When enabled, turns off some power management in the PCH IO fabrics. This option provides the most aggressive IO fabric performance setting. S3 state is not supported.

Appendix C Timed GPIO (TGPIO) Pin information

In the following tables list the Time GPIO Pin information as labeled on intel reference boards. PMC stands for Power Management Controller.

C.1 Intel® Xeon® Processors

C.1.1 Intel® Xeon® W-11000E Series Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPP_H_23_TIME_SYNC_0
	Pin 1: GPP_B_1_GSPI1_CS1B_TIME_SYNC_1

C.1.2 Additional Xeon platforms with TGPIO support

Platform	Component	Timed GPIO Pins	Ball Name
Eagle Stream	PCH	GPPC_S_0_TIME_SYNC_0	BB18
Eagle Stream	PCH	GPPC_S_1_TIME_SYNC_1	AU16
Birch Stream	Granite Rapids-AP	TIMED_GPIO_0	F6
Birch Stream	Granite Rapids-AP	TIMED_GPIO_1	E7
Birch Stream	Granite Rapids-SP	TIMED_GPIO_0	BM65
Birch Stream	Granite Rapids-SP	TIMED_GPIO_1	BM63

C.2 Intel® Core™ Processors

C.2.1 14th Generation Intel® Core™ S-Series Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPPC_B_14_SPKR_TIME_SYNC_1_SATA_LEDB_ISH_GP_6
	Pin 1: GPPC_B_15_TIME_SYNC_0_ISH_GP_7

C.2.2 13th Generation Intel® Core™ S-Series Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPP_H23 TIME_SYNC_0
	Pin 1: GPP_I10 TIME_SYNC_1

C.2.3 13th Generation Intel® Core™ P-Series Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPPC_B14 TIME_SYNC_0
	Pin 1: GPPC_B15 TIME_SYNC_1

C.2.4 12th Generation Intel® Core™ S-Series Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPP_H_23_TIME_SYNC_0
	Pin 1: GPP_I_10_GSPI1_CS1B_TIME_SYNC_1

C.2.5 11th Generation Intel® Core™ Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPPC_H19_TIME_SYNC_0
	Pin 1: GPPC_B14_SPKR_TIME_SYNC_1_GSPI0_CS1_N

C.3 Intel Atom® Processors

C.3.1 Intel Atom® x7000E/x7000C/x7000RE Series Processors

Scenario	Reference Board SoC Pin Name
TGPIO	Pin 0: GPPC_B_15_TIME_SYNC_0_ISH_GP_7
	Pin 1: GPPC_B_14_SPKR_TIME_SYNC_1_SATA_LEDB_ISH_GP_6

C.3.2 Intel Atom® x6000E Series Processors

Scenario	Reference Board SoC Pin Name
PMC TGPIO	Pin 0: GPPC_H_19_DDP1_CTRLDATA_TIME_SYNC_0_OSE_TGPIO20
	Pin 1: GPPC_B_14_SPKR_TIME_SYNC_1_GSPI0_CS1B_OSE_SPI2_CS B1
PSE TGPIO	Pin 17: GPPC_B_4_CPU_GP_3_ESPI_ALERTB_1_OSE_TGPIO27
	Pin 18: GPPC_B_23_PCHHOTB_GSPI1_CS1B_OSE_SPI3_CSB1_OSE_TGPIO28

There are 40 TGPIO pin options available on the Intel Atom® x6000E Series Processor PSE. For more information, please refer to chapter 22 of the Intel Atom® x6000E Series Processor External Design Specification (RDC#601458)

Appendix D Capacity Bit Masks for LLC Cache

Table 7: Capacity bit masks for LLC Cache

Processor	Brand String	# L3 Classes of Service (CLOS)	Capacity Bitmask Length (CBM)
Intel Atom® Processors X6000 Series	Intel Atom® x6427FE Processor	4	16 (0xFFFF)
	Intel Atom® x6425RE Processor		16 (0xFFFF)
	Intel Atom® x6414RE Processor		16 (0xFFFF)
	Intel Atom® x6212RE Processor		16 (0xFFFF)
	Intel Atom® x6200FE Processor		8 (0xFF)
	Intel Atom® X6416RE Processor		16 (0xFFFF)
	Intel Atom® X6214RE Processor		16 (0xFFFF)
Intel Atom® Processors X7000 Series	Intel Atom® x7211E Processor	16	12 (0xFFF)
	Intel Atom® x7425E Processor		12 (0xFFF)
	Intel Atom® x7213E Processor		12 (0xFFF)
	Intel Atom® x7211RE Processor		12 (0xFFF)
	Intel Atom® x7213RE Processor		12 (0xFFF)
	Intel Atom® x7433RE Processor		12 (0xFFF)
	Intel Atom® x7835RE Processor		12 (0xFFF)
	Intel Atom® x7203C Processor		12 (0xFFF)
	Intel Atom® x7405C Processor		12 (0xFFF)
	Intel Atom® x7809C Processor		12 (0xFFF)
11 Gen Intel® Core™ Processors (UP3-Series)	Intel® Core™ i7-1185GRE Processor	4	12 (0xFFF)
	Intel® Core™ i5-1145GRE Processor		8 (0xFF)
	Intel® Core™ i3-1115GRE Processor		12 (0xFFF)
Intel® Xeon® W Processors (TGL-H)	Intel® Xeon® W-11865MRE Processor	4	12 (0xFFF)
	Intel® Xeon® W-11865MLE Processor		12 (0xFFF)
	Intel® Xeon® W-11555MRE Processor		8 (0xFF)
	Intel® Xeon® W-11555MLE Processor		8 (0xFF)
	Intel® Xeon® W-11155MRE Processor		8 (0xFF)
	Intel® Xeon® W-11155MLE Processor		8 (0xFF)
12 Gen Intel® Core™ Processors (S-Series)	Intel® Core™ i9-12900E Processor	16	12 (0xFFF)
	Intel® Core™ i7-12700E Processor		10 (0x3FF)
	Intel® Core™ i5-12500E Processor		12 (0xFFF)
	Intel® Core™ i3-12100E Processor		12 (0xFFF)
13 Gen Intel® Core™ Processors (P-Series)	Intel® Core™ i7-1365UE Processor	16	12 (0xFFF)
	Intel® Core™ i7-1365URE Processor		12 (0xFFF)
	Intel® Core™ i5-1345UE Processor		12 (0xFFF)
	Intel® Core™ i5-1345URE Processor		12 (0xFFF)
	Intel® Core™ i3-1335UE Processor		12 (0xFFF)
	Intel® Core™ i3-1315UE Processor		10 (0x3FF)
	Intel® Core™ i3-1315URE Processor		10 (0x3FF)
	Intel® Core™ i7-1370PE Processor		12 (0xFFF)
	Intel® Core™ i7-1370PRE Processor		12 (0xFFF)
	Intel® Core™ i5-1350PE Processor		8 (0xFF)
	Intel® Core™ i5-1350PRE Processor		8 (0xFF)
	Intel® Core™ i3-1340PE Processor		8 (0xFF)
	Intel® Core™ i3-1320PE Processor		8 (0xFF)
	Intel® Core™ i3-1320PRE Processor		8 (0xFF)
	Intel® Core™ i7-13800HE Processor		12 (0xFFF)
	Intel® Core™ i7-13800HRE Processor		12 (0xFFF)
	Intel® Core™ i5-13600HE Processor		12 (0xFFF)

Processor	Brand String	# L3 Classes of Service (CLOS)	Capacity Bitmask Length (CBM)
	Intel® Core™ i5-13600HRE Processor		12 (0xFFF)
	Intel® Core™ i3-13300HE Processor		8 (0xFF)
	Intel® Core™ i3-13300HRE Processor		8 (0xFF)
13 Gen Intel® Core™ Processors (S-Series)	Intel® Core™ i9-13900E Processor	16	12 (0xFFF)
	Intel® Core™ i9-13900TE Processor		12 (0xFFF)
	Intel® Core™ i7-13700E Processor		12 (0xFFF)
	Intel® Core™ i7-13700TE Processor		12 (0xFFF)
	Intel® Core™ i5-13500E Processor		12 (0xFFF)
	Intel® Core™ i5-13500TE Processor		12 (0xFFF)
	Intel® Core™ i5-13400E Processor		10 (0x3FF)
	Intel® Core™ i3-13100E Processor		12 (0xFFF)
	Intel® Core™ i3-13100TE Processor		12 (0xFFF)
14 Gen Intel® Core™ Processors (S-Series)	Intel® Core™ i9-14900 Processor	16	12 (0xFFF)
	Intel® Core™ i9-14900T Processor		12 (0xFFF)
	Intel® Core™ i7-14700 Processor		11 (0x7FF)
	Intel® Core™ i7-14700T Processor		11 (0x7FF)
	Intel® Core™ i5-14500 Processor		12 (0xFFF)
	Intel® Core™ i5-14500T Processor		12 (0xFFF)
	Intel® Core™ i5-14400 Processor		10 (0x3FF)
	Intel® Core™ i5-14400T Processor		10 (0x3FF)
	Intel® Core™ i3-14100 Processor		12 (0xFFF)
	Intel® Core™ i3-14100T Processor		12 (0xFFF)

Note: This table does not cover Intel® Xeon® Processors (except Intel® Xeon® W Processors - TGL-H), as Cache Allocation Technology on those processors is architectural and the equivalent specifications can be obtained via the CPUID instruction. Consult the Intel Software Developer's Manual for complete details.

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