Synaptics®

CX11880 Ultra Low-Power HD Audio CODEC Datasheet

505-000838-01 Rev B

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Revision History

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A	Convert to Synaptics branding. Updated DAC/ADC performance specifications and power consumption.	12/05/17	John Howley
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Table of Contents

Revision History **2**
Introduction **7**
General Description **7**
System Compatibility **8**
CX11880 Audio CODEC Features **8**
Hardware Interface **11**
General **11**
Host Interface 11
Audio Ports 11
Block Diagram **12**
Pin Information **13**
Pin Configuration 13
Pin Assignments 14
Absolute Maximum Ratings **16**
DC Specifications **16**
Device Performance Specifications **17**
Power Consumption **17**
Package Dimensions **19**
HD Audio Interface **20**
Overview **20**
Intel ECR HDA048A Support **21**
Verbs **21**
Node ID 00: Root Node 22
Node ID 01: Audio Function Group (AFG) 23
Nodes 10, 11: DAC 1, 2 Widgets 25
Node 12: PC Beep Generator Widget 26
Node ID 13: ADC1 Widget 27
Node ID 14: ADC2 Widget 29
Node ID 15: Mixer Widget 30
Node ID 16: Port A/Vendor Widget 31
Node ID 17: Port G BTL Pin Widget 32
Node ID 18: Port B Widget 33
Node ID 19: Port D Widget 35

Node ID 1A: Port C Widget 36
Node ID 20: DAC 3—Sony/Philips Digital Interface Format (S/PDIF) Output Widget 37
Node ID 21: Port I S/PDIF Output Widget 38
Node 1B: Vendor-Specific Widget 38
Node 1C: Vendor-Specific Widget 38

Ordering Information 39

List of Figures

Figure 1: CX11880 Block Diagram 12
Figure 2: CX11880 Pin Configuration 13
Figure 3: Package Diagram 19

List of Tables

Table 1: Pin Assignments 14
Table 2: Absolute Maximum Ratings 16
Table 3: DC Specifications 16
Table 4: Analog Performance 17
Table 5: D3 Power Consumption 17
Table 6: 1mW Headphone into 32Ω 17
Table 7: Full Scale Class-D Power—0dB Sine Wave 18
Table 8: Port B Recording (24dB Boost) 18
Table 9: Node 0 Responses 22
Table 10: Node 01 Responses 23
Table 11: Node 10 and 11 Responses 25
Table 12: PC Beep Generator Responses 26
Table 13: Node ID 13 Responses 27
Table 14: Node ID 14 Responses 29
Table 15: Node ID 15 Responses 30
Table 16: Node ID 16 Responses 31
Table 17: Node ID 17 Responses 32
Table 18: Node ID 18 Responses 33
Table 19: Node ID 19 Responses 35
Table 20: Node ID 1A Responses 36
Table 21: Node ID 20 Responses 37
Table 22: Node ID 21 Responses 38
Table 23: Ordering Information 39

Introduction

General Description

The Synaptics CX11880 is a low-power HD audio CODEC that supports ECR HDA048A mobile extensions, and is primarily targeted for desktop and notebook PCs, tablets, and battery-operated speakers. The CX11880 is fully compliant with all industry specifications, including UAA and the latest WHCK. Host interface signaling levels of 1.5V, 1.8V, and 3.3V are selectable.

The CX11880 has audio fidelity that exceeds Microsoft desktop and notebook premium logo requirements. With two 24-bit stereo DACs and two 24-bit stereo ADCs operating up to 192kHz, the CODEC supports multi-streaming and RTC applications. By combining these hardware features with Synaptics' playback and voice and speech pre-processing algorithms, this CODEC is the ideal solution for Enterprise platforms that require Skype certification, general consumer applications, and gaming/multi-media enthusiasts.

The integrated stereo AudioSmart class-D 1.0 provides intelligent power delivery and dynamic signal loudness optimization that is capable of driving up to 2.8WRMS per channel into 4Ω loads. The Class-D amplifier can be powered directly from the battery supply, which reduces the external power management component cost. SpeakerShield technology provides industry-leading, load-based speaker protection in real-time that includes DC detection, short-circuit, near-short, high temperature, and over-temperature. Integrated 14-band hardware EQ and DRC optimizes speaker response and loudness without distortion to enable a high-quality audio experience on integrated speakers that are independent of a driver and an OS. The EQ can also be applied to the headphone path. Additional unlimited bands of EQ and DRC are available in software.

Low-power Class G capless headphone driver produces a full-range frequency response, and eliminates AC coupling capacitors. Integrated headset support with auto-detect and auto-switch between Apple and Nokia-style headsets eliminates all external BOM. Synaptics supports four-button, in-line headset detection, as well as headset impedance low and high threshold detection for ear safety as required for Chromebooks. A single universal jack supports headsets, headphones, external microphones, and line-in devices. The CODEC prevents hum noise from external powered speakers connected to a global headset jack (CTIA/OMTP) while the system is off—it does not require a standby power supply to operate.

Mono or stereo digital or analog internal microphones can be connected with integrated boost and DC offset removal. Together with Synaptics' AudioSmart voice and speech input processing technologies, this device supports all convertible, detachable, and tablet microphone configurations. The digital microphone clock is programmable and supports low frequency modes to minimize power consumption. Multiple GPIOs and an S/PDIF output are available. The D3-Live mode enables external audio devices to play through an input or a universal jack to the internal speakers with full speaker EQ/DRC while in system is in connected standby, low power, and sleep modes.

Synaptics' PopShield technology eliminates pops and clicks during all transition states. This technology includes active DC offset removal ground calibration and innovative Vref ramping schemes to avoid pops on AC-coupled paths. The CX11880 has D-Flex power management that exceeds industry power requirements, and consumes minimum power during a connected standby and all low-power system states without pops or clicks. In its non-active lowest power state, the CODEC consumes less than 300µW. 26mW headphone playback power consumption into 32Ω loads ensures maximum system battery life.

Synaptics' offers comprehensive audio software driver support, with both in-house and third-party software APOs, including Dolby, DTS, Sound Research, Waves, and more. Synaptics' AudioSmart voice and speech processing algorithm suite ensures clear voice communication and speech command and control in noisy environments. The Smart Source Pickup (SSP) does not rely on beam-forming techniques, and provides an easy to use powerful solution that requires few or no user controls. The SSP passes all of the latest speech recognition certifications such as Cortana in portrait and landscape modes with just two microphones, and is available for Windows, Linux, and Android. AudioSmart also offers keystroke, screen tapping, and fan noise suppression.

System Compatibility

- HD Audio Specification, Revision 1.0a including ECR
- HDA048A mobile extensions
- All Windows versions
- Microsoft Premium Logo
- Linux, Android, and Chrome

CX11880 Audio CODEC Features

- Two pairs of independent DACs and ADCs have independent sampling rates of up to 192kHz:
  - DACs provide over 103dB SNR at –90dBFS dB THD+N
  - ADCs provide 100dB SNR at –93dBFS THD+N
- 2.8W_{RMS} per channel SMART stereo class-D with spread spectrum and common mode scrambling to reduce EMI
- AudioSmart™ class-D intelligent power delivery and dynamic signal loudness optimization maximizes even small speaker SPL and ensures no speaker damage
- Class-D amplifier can be powered directly from the battery supply, reducing external power management component cost
- EQ and DRC:
  - Integrated 14-band hardware programmable EQ ensures optimal speaker frequency response
  - DRC maximizes loudness while preventing distortion
  - EQ can be applied to a headphone path
  - Additional unlimited bands of EQ and DRC are available in the software
- SpeakerShield technology provides real-time, load-based class-D speaker protection that is independent of driver and application—programmable by BIOS and includes:
  - Programmable High-Pass Filter (HPF) protects speakers against damage from high energy, low frequency content
  - DC protection detects DC voltage across the speakers and prevents damage by immediately shutting down the class-D amplifier
  - Short circuit protects against straight shorts to ground that can happen during manufacturing
  - When near-shorts are detected, the amplifier gain adjusts to auto recover and shuts it down if the problem persists
  - Very high temperature conditions immediately shut off the amplifier
  - High temperature throttles down the class-D gain to auto recover, or shuts it down if the problem persists
  - Class-D voltage supplies, presence, and accuracy of DAC and class-D clocks are carefully monitored
- A low-power Class G stereo capless headphone driver directly drives 16Ω and 32Ω loads with no pops, and eliminates the BOM cost and space of external headphone amplifiers and DC-blocking capacitors
- Built-in, four-conductor headset jack supports headphone/headset auto-detection, as well as auto-switching between Apple and Nokia-style headsets without any external components
- Four-button, in-line headset detection, wake, and low/high speaker impedance level detection

- Prevents hum noise from powered speakers that are connected to a global headset jack (CTIA/OMTP) while the system is off—does not require standby power supply to operate
- Universal audio jack supports all headsets, headphones, external microphones, and external line-in devices on one jack
- Analog and digital stereo microphone inputs with DC offset removal and programmable boost supports a stereo microphone array. Programmable clock outputs are available (768kHz/1.536MHz/3.072MHz), including low frequency modes for low-power operation of DMIC modules. The DMIC interface signaling can run at 1.8V or 3.3V.
- S/PDIF output
- Record security prevents unwanted recordings from all or selected input ports
- Integrated headphone limiter supports GS Mark EN50332-2 without an external BOM—selectable through BIOS or a driver/GUI
- Supports analog and digital PC Beep—Wake-on-Beep never misses a beep, even when in low-power mode
- Multiple GPIOs are available for custom applications, and can be selected for 1.8V or 3.3V signaling levels
- Bi-directional EAPD supports external amplifier control for power savings as well as integrated headphone and class-D amplifier shutdown/mute on a single pin—avoids external BOM cost and design complexity
- Integrated Low Drop-Outs (LDOs) provide on-chip clean rails and clean Microphone Bias (micbias)
- Supports 1.5V, 1.8V, and 3.3V host interface signaling levels
- Pop Shield II enhanced pop and click suppression on all ports
- Jack sense detects jack plug events
- An integrated digital mixer is used to record what is playing pre-EQ, so recorded audio sounds great on all devices and peripherals
- D3 Live allows external audio devices to play to the internal speakers, with full hardware EQ and DRC while the system is asleep or in low power modes—use your notebook as a speaker dock
- CODEC consumes less than 300µW in it lowest power state
- Supports ultra-low power headphone playback of 1mW into 32Ω of 26mW
- Compliant with Intel's *High Definition Audio Specification, Revision 1.0a*, including ECR HDA048A mobile extensions
- Available in a 42-pin, thermally-enhanced QFN package
- AudioSmart speech/voice pre-processing algorithms are available from Synaptics:
  - End-to-end noise reduction
  - True stereo AEC
  - SSP solves common, real-world problems, and works much better than traditional beam-forming noise reduction approaches—works in all orientations (portrait, landscape, LCD panel flat on a table) with stereo microphone only and without user control changes
  - Best-in-class keystroke suppression, tap suppression, and fan noise suppression solutions
  - SSP optimizes hit rates for speech recognition applications like Cortana—solution ensures near flawless hit rates while other processing like keystroke suppression and VOIP enhancements remain enabled simultaneously
  - Far Field Pickup enables far field speakerphone and group conference call applications
- 10-band graphic EQ:
  - Provides additional, user-controlled, enhancements and pre-sets
  - Night mode boosts vocal clarity while maintaining background sound quality

- Multi-band dynamic EQ (multi-band DRC) improves the sound quality of low-cost speakers and prevents speaker rattle and distortion—allows different threshold tuning on different frequency bands
- Phantom bass psycho-acoustic technology creates virtual bass content on mainstream speakers
- 3D:
  - Expander widens the audio stage for a fuller and richer sound
  - Headphones recreates a surround sound, speaker-like environment in headphones so users can enjoy a richer and fuller music listening experience
- SmartAudio GUI—advanced audio control panel
- Audio director for classic and multi-stream selections
- Third-party software support includes, but is not limited to:
  - Creative Labs
  - Dolby
  - DTS, Inc.
  - Sound Research Corporation
  - Waves

Hardware Interface

General

Host Interface

The host interface supports HD audio and mobile extensions in ECR HDA048A and uses the following common set of signals:

- Bit clock (BIT_CLK), input
- Frame sync (SYNC), input
- Serial data output (SDATA_OUT), input
- Serial data input (SDATA_IN), input/output
- Bus reset (RESET#)/Master clock (MCLK), input

Audio Ports

The following lists the supported audio interface signals:

- Port A (PORTA_L and PORTA_R), capless headphone output/line output, headset
- Port B (PORTB_L and PORTB_R), microphone input/line input with micbias
- Port C, stereo analog microphone, Line, or digital microphone input
- Port D (PortD_A, PortD_B), analog headset mono microphone input (supports Apple/Nokia-style headset auto-detection and auto-switching with no BOM)
- Port G (Left+ and Right+), class-D speaker amplifier output, stereo/mono selectable
- Port I, S/PDIF output
- PC speaker beep pass-through (PC_BEEP), input

Block Diagram

The following figure shows the CX11880 block diagram.

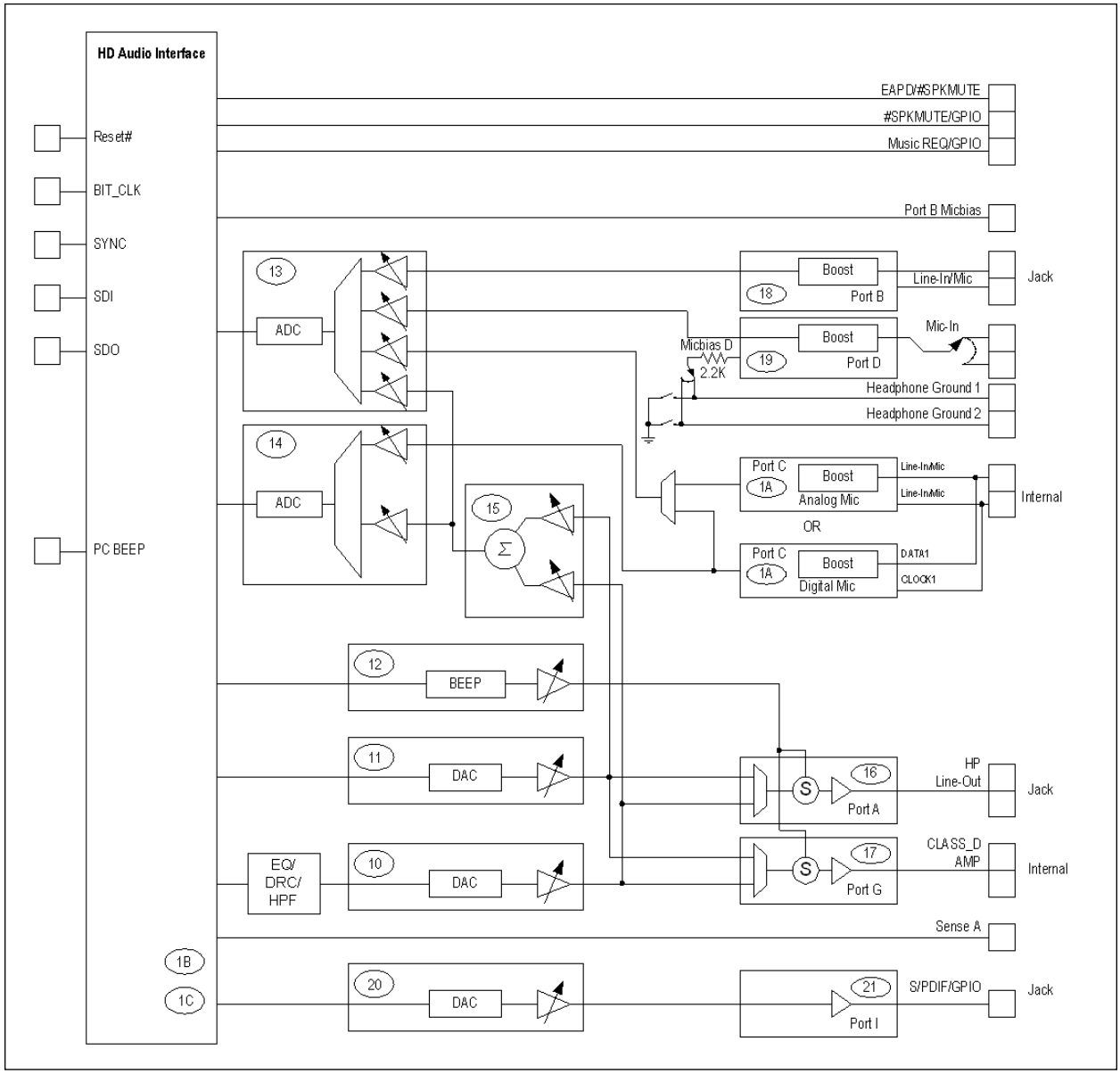

Figure 1: CX11880 Block Diagram

Pin Information

Pin Configuration

The following figure shows the CX11880 pin configuration.

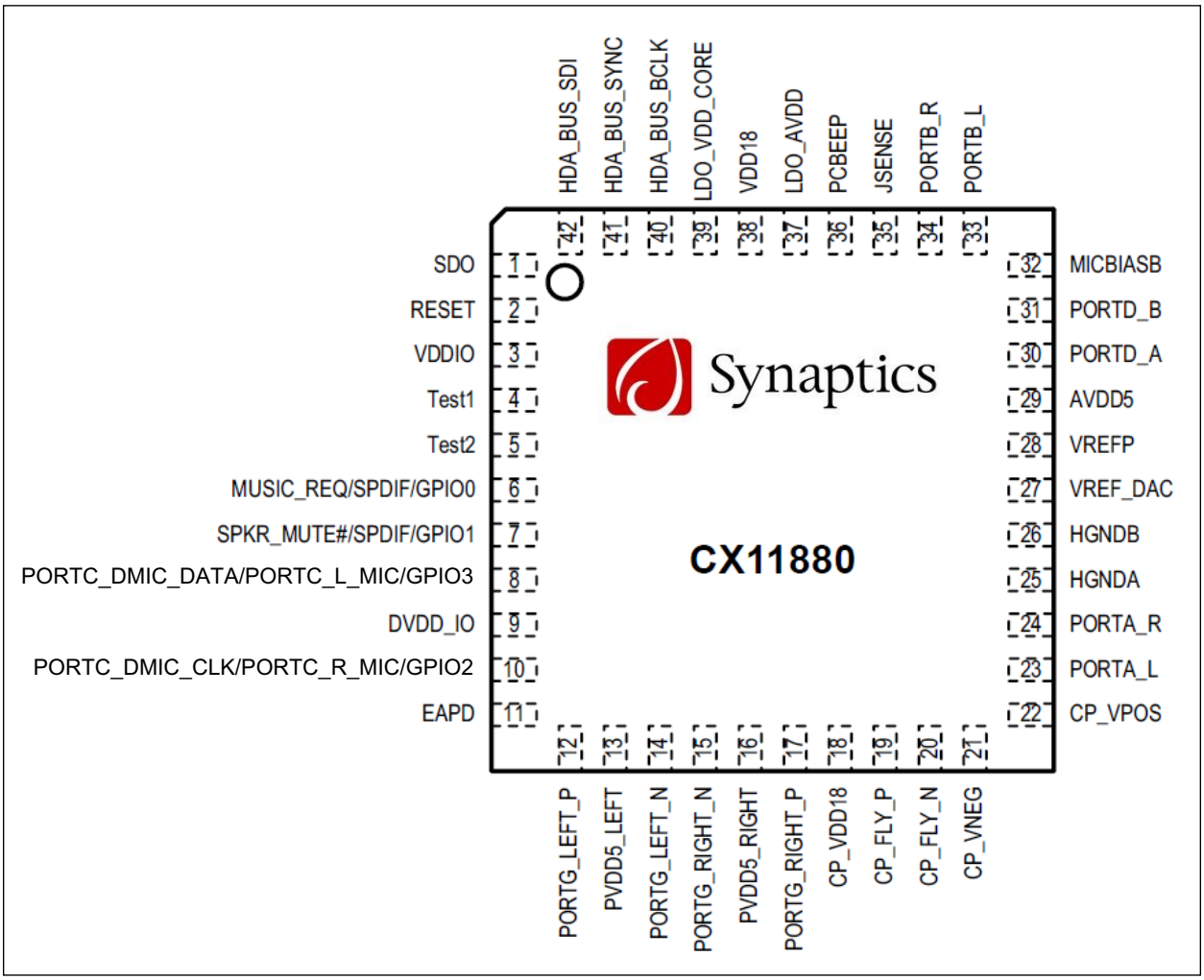

Figure 2: CX11880 Pin Configuration

Pin Assignments

The following table lists the CX11880 pin assignments.

Table 1: Pin Assignments

Pad Number	Signal Name
1	**SDO.** HD audio bus serial data input to the CODEC.
2	**RESET#.** HD audio bus master hardware reset.
3	**HDA_VDDIO—1.5V/1.8V/3.3V, ±5%.** Sets the host interface signaling level. Connect to the same power supply as the host bus controller.
4	**TEST1.** Test mode pin. All designs must pull this pin high. Refer to the reference schematic for details.
5	**TEST2.** Test mode pin. All designs must pull this pin high. Refer to the reference schematic for details.
6	**MUSIC_REQ/SPDIF/GPIO0.** Multi-function pin. **MUSIC_REQ.** Pull high by the external controller to enable D3 Live Mode. **SPDIF.** S/PDIF output. **GPIO0.** GPIO.
7	**SPKR_MUTE#/SPDIF/GPIO1.** Multi-function pin. **SPKR_MUTE#.** When pulled low, holds class-D on mute. Instead, Synaptics recommends using a bi-directional EAPD pin. **SPDIF.** S/PDIF output. **GPIO1.** GPIO.
8	**PORTC_DMIC_DATA/PORTC_L_MIC/ GPIO3.** Multi-function pin. **DMIC_DATA.** An input to the CODEC—the digital MIC data from one or two DMICs. **PORTC_L_MIC.** Left analog microphone or Line input. **GPIO3.** GPIO.
9	**DVDD_IO.** Sets the: • Digital I/O level. Connect to 1.8V/3.3V, ±5%. • Signaling level for the DMIC, S/PDIF, EAPD, and GPIO.
22	**CP_VPOS.** Charge pump positive rail output—connect to the digital ground through a 2.2µF capacitor.
23	**PORTA_L.** Capless headphone output, left channel.
24	**PORTA_RIGHT.** Capless headphone output, right channel.
25	**HGNDA.** Microphone: • Ground terminal for CTIA-style headsets. • Bias for OMTP-style headsets.
26	**HGNDB.** Microphone: • Ground terminal for Open Mobile Terminal Platform (OMTP) style headsets. • Bias for CTIA-style headsets.
27	**VREF_DAC.** Analog Ground (AGND) reference—connect directly to AGND.
28	**VREFP (Analog Reference).** AGND reference—connect to AGND through a capacitor (typically 1µF).
29	**AVDD5. 5V ±10%.** LDO voltage supply input to the CODEC.
30	**PORTD_A.** • Headset microphone input. • Mono microphone input for CTIA-style headsets.

Pad Number	Signal Name
10	**PORTC_DMIC_CLK/PORTC_R_MIC/ GPIO2.** Multi-function pin. **DMIC_CLK.** Output from the CODEC—the digital MIC clock. **PORTC_R_MIC.** Right analog microphone or Line input. **GPIO2.** GPIO.
11	**Bi-directional EAPD.** Bi-directional pin, Refer to the reference schematics for details. **Output.** Controls the external amplifiers' power up/down per the *HD Audio Specification*. **Input.** Can be driven by EC or such to mute class-D and headphones.
12	**PORTG, Class D LEFT +.** Class-D amplifier output, left channel, positive.
13	**PVDD5 LEFT.** Class-D left power supply voltage. Connect to PVDD5 RIGHT, and connect both to system 5V or battery.
14	**PORTG, Class D LEFT –.** Class-D amplifier output, left channel, negative.
15	**PORTG, Class D RIGHT –.** Class-D amplifier output, right channel, negative.
16	**PVDD5 RIGHT.** Connect to PVDD5 LEFT, and connect both to system 5V or battery.
17	**PORTG, Class D RIGHT +.** Class-D amplifier output, right channel, positive.
18	**CP_AVDD18, 1.8V, ±5%.** Charge pump supply input.
19	**FLY_P, Flying Capacitor.** Charge pump positive transfer charge—connect to FLY_N through a 2.2µF capacitor.
20	**FLY_N, Flying Capacitor.** Charge pump negative transfer charge—connect to FLY_P through a 2.2µF capacitor.
21	**CP_VNEG.** Charge pump negative rail output—connect to digital ground through a 2.2µF capacitor.

Pad Number	Signal Name
31	**PORTD_B.** • Headset microphone input. • Mono microphone input for OMTP-style headsets.
32	**MICBIAS_B.** Programmable micbias output for port B.
33	**PORTB_L.** Microphone/line-in port, left channel.
34	**PORTB_R.** Microphone/line-in port, right channel.
35	**JSENSE.** Jack sense input. Connect to the resistor network per the *HD Audio Specification*. Refer to the reference schematic for details.
36	**PC BEEP.** PC speaker beep input. Needs to be AC-coupled using a 0.1µF capacitor. Maximum input level is 1.8V. Use external attenuator if using a 3.3V signal to drive this pin.
37	**LDO_AVDD.** 1.8V to 1.6V LDO output. Connect to AGND through a capacitor.
38	**VDD18. 1.8V ±5%.** Analog supply voltage input to the CODEC.
39	**LDO_VDD_CORE.** 1.2V LDO output. Connect to digital GND through a capacitor.
40	**BCLK.** HD audio bus bit clock input to the CODEC.
41	**SYNC.** HD Audio Bus SYNC input to the CODEC.
42	**SDI.** HD audio bus serial data output from the CODEC.

Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	AVDD5	–0.5 to 6.0	V
	PVDD5_LEFT/PVDD5_RIGHT	–0.5 to 6.0	V
	CP_AVDD18	–0.5 to 2.5	V
	VDD18	–0.5 to 2.5	V
	VDDIO	–0.5 to 4.6	V
	DVDD_IO	–0.5 to 4.6	V
Digital Input Voltage	V_{ind}	–0.5 to VDDIO/DVDD_IO + 0.5 (Not to Exceed 4.6)	V
DC Clamp Current			
Input	I_{ik}	20	mA
Output	Io_k	20	mA
Storage Temperature	T_{stg}	–55 to 125	°C
Operating Temperature	T_{op}	0 to +70	°C

DC Specifications

The following table summarizes the DC specifications of the 3.3V/1.8V/1.5V digital signals.

Table 3: DC Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Units	Notes
V_{cc}	Supply Voltage	3.3V Mode	3.135	3.465	V	-
		1.8V Mode	1.70	1.90	V	-
		1.5V Mode	1.418	1.583	V	-
V_{ih}	Input High Voltage	3.3V Mode	0.65xVcc	-	V	-
		1.8V Mode	0.65xVcc	-	V	-
		1.5V Mode	0.60xVcc	-	V	-
V_{il}	Input Low Voltage	3.3V Mode	-	0.35xVcc	V	-
		1.8V Mode	-	0.35xVcc	V	-
		1.5V Mode	-	0.40xVcc	V	-
V_{oh}	Output High Voltage	Iout =-500µA	0.9xVcc	-	V	-
V_{ol}	Output Low Voltage	Iout =1500µA	-	0.10xVcc	V	-
I_{il}	Input Leakage Current	0<Vin<Vcc	-	±10	µA	1
C_{in}	Input Pin Capacitance	-	-	7. 5	pF	-
L_{pin}	Pin Inductance	-	-	20	nH	-

Note: For any bi-directional buffer with tri-state output, the input leakage current also includes hi-Z output leakage.

Device Performance Specifications

The following table details the analog performance. The PSRR >85dB for all analog inputs and outputs.

Table 4: Analog Performance

Device Type	Requirement	Minimum	Typical	Maximum	Frequency Range at 48kHz and Above
Class-D Speaker Amplifier	THD+N @ –3dBFS (1W 4Ω)	-	–84dBFS	-	[20Hz, 20kHz]
	Dynamic Range	-	100dBFS Awt	-	[20Hz, 20kHz]
	Crosstalk	-	86dB	-	[20Hz, 15kHz]
Analog Headphone Out Jack	THD+N @ –3dBFS/32Ω	-	–90dBFS	-	[100Hz, 20kHz]
	DNR	-	100dBFS Awt	-	[100Hz, 20kHz]
	Crosstalk	-	86dB	-	[100Hz, 15kHz]
	Full-scale Output Voltage, 10kΩ Load	-	$1V_{RMS}$	-	-
	Full-scale Output Voltage, 32Ω Load	-	$820mV_{RMS}$	-	-
Analog Line/ Microphone-in	THD+N @ –3dBFS	-	–93dBFS	-	[20Hz, 20kHz]
	DNR	-	97dBFS Awt	-	[20Hz, 20kHz]
	Full-scale Input Voltage	$0.707V_{RMS}$	-	-	-

Power Consumption

The tables in this section provide the power consumption parameters. Test conditions are for a nominal device.

Table 5: D3 Power Consumption

Power Rail	Voltage (V)	Current (µA)	Power (µW)
AVDD5	5	10.94	54.68
PVDD5	5	2.27	11.35
VDD18	1.8	113.75	204.75
CP_VDD18	1.8	0.32	0.57
HDA_VDDIO	3.3	3.38	11.15
DVDD_IO	3.3	1.05	3.45
Total Power (µW)			**285.95**

Table 6: 1mW Headphone into 32Ω

Power Rail	Voltage (V)	Current (mA)	Power (mW)
AVDD5	5	0.06	0.29
PVDD5	5	0	0
VDD18	1.8	7.43	13.37
CP_VDD18	1.8	6.76	12.17
HDA_VDDIO	3.3	0	0
DVDD_IO	3.3	0	0
Total Power (mW)			**25.84**

Table 7: Full Scale Class-D Power—0dB Sine Wave

Power Rail	Voltage (V)	Current (mA)	Power (mW)
AVDD5	5	0.06	0.30
PVDD5	5	909	4545
VDD18	1.8	7.02	12.64
CP_VDD18	1.8	1.76	3.17
HDA_VDDIO	3.3	0	0
DVDD_IO	3.3	0	0
Total Power (mW)			**4561.11**

Table 8: Port B Recording (24dB Boost)

Power Rail	Voltage (V)	Current (mA)	Power (mW)
AVDD5	5	0.06	0.29
PVDD5	5	0	0
VDD18	1.8	5.71	10.28
CP_VDD18	1.8	0	0
HDA_VDDIO	3.3	0	0
DVDD_IO	3.3	0	0
Total Power (mW)			**10.57**

Package Dimensions

The following figure provides the CX11880 package diagram.

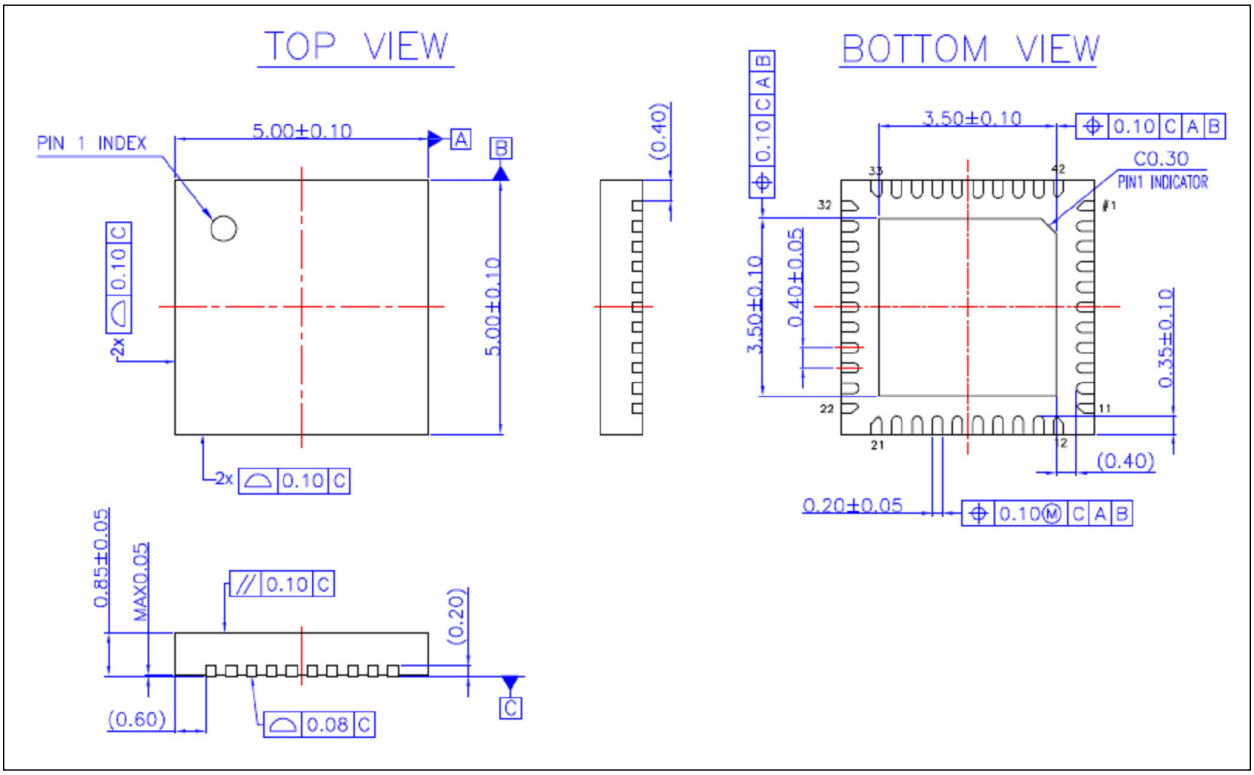

Figure 3: Package Diagram

HD Audio Interface

Overview

The CX11880 host interface supports Intel's *High Definition Audio Specification, Revision 1.0a*. The HD audio interface is a five-pin interface:

- Clock (BIT_CLK)
- Serial data in (SDATA_IN)
- Serial data out (SDATA_OUT)
- SYNC
- RESET#

The clock is provided by the controller at a frequency of 24MHz. Because the SDATA_OUT signal is provided by the controller and contains data for every edge of the 24MHz clock, the CX11880 must sample data on both rising and falling edges of SDATA_OUT.

The SYNC signal not only signals the beginning of the 500 clock frame, it designates the beginning of the data for each stream and indicates which stream of data is to be on SDATA_OUT next (streams do not need to appear in order; the controller may do as it likes). Channels are another way of organizing the serial data. Each stream has at least one channel. Each stream must start with channel 0 and proceed without interruption until all the assigned channels are exhausted. Because a stereo pair takes two adjacent channels, if:

- DAC1 is in stereo mode and assigned to channel 0, then the left data will be on channel 0 and the right on channel 1
- DAC2 is in stereo mode and assigned to channel 2 (and the same stream as DAC1), then the left data will be on channel 2 and the right on channel 3

The SDATA_IN signal contains the CX11880 data headed towards the controller, and is only generated on rising edges. This includes information read from the HD audio registers, ADC, and incoming modem data. The stream and channel are indicated before the data is transmitted on SDATA_IN (refer to Intel's *HD Audio Specification 1.0a* for the format). The SDATA_IN signal is responsible for knowing the device number, which is the CODEC Address (CAd) in Intel's *HD Audio Specification 1.0a*. During the last clock of the first sync after a Power-on Reset (PoR), the SDATA_IN is driven high by the CX11880 for one clock cycle. This indicates to the controller the need for a CAd. The CX11880 then stops driving the SDATA_IN signal, and the controller begins to drive it. The controller drives SDATA_IN high through the next sync, and the CAd is assigned by the number of clocks after the fall of sync that it takes for the SDATA_IN to fall. The interface then turns around again, and SDATA_IN is an output from the CX11880 until reset.

Intel's *HD Audio Specification 1.0a* also contains one other concept of an unsolicited message. Unsolicited messages can occur for a number of reasons, such as timers, ringing phones, answers from the device to a register read, etc. Because the bus has no interrupt, these reasons are taken care of in unsolicited messages. If the controller was not addressing the CAd assigned to the CX11880 during the previous frame and if one of these unsolicited messages is needed (and enabled), the CX11880 uses the first cycles after the sync on SDATA_IN to alert the controller to the event. Only one event can be signaled in a frame. The CX11880 only sends the message once, and does not expect any sort of acknowledgment from the controller.

Refer to Intel's *High Definition Audio Specification, Revision 1.0a* for details on link interface signaling and protocols.

Intel ECR HDA048A Support

The CX11880 CODEC also supports Intel's HD audio mobile extensions in ECR HDA048A. These new power savings extensions to Intel's *High Definition Audio Specification* are fully backward-compatible with HD audio 1.0a. The CODECs that only support the *HD Audio Specification 1.0a* work with host chipsets that support ECR HDA048A. Similarly, the CODECs that support ECR HDA048A work with the host chipsets that only support the *HD Audio Specification 1.0a*.

Under ECR HDA048A the HD audio architecture is designed to support static clock frequency switching. This is an optional feature that helps to save power when the audio subsystem is configured for lower bandwidth operations when it is feasible to run a slower BCLK. In addition to supporting the mandatory default 24MHz BCLK, HD audio controllers and CODECs may optionally support a set of lower operating frequencies (i.e., 6MHz and 12MHz). The CX11880 supports these rates.

Verbs

This section describes how this device interacts with the verbs defined in Intel's *HD Audio Specification 1.0a*. Each of the following subsections describe the verb IDs, parameters/payload, and corresponding responses that apply to that node.

Verbs are commands and queries that are passed from the HD audio controller to the CODECs on the HD audio bus. Responses are data passed from the HD audio CODEC to the HD audio controller. All controller verbs must be followed by a CODEC response. Unsolicited responses from the CODEC are data transmitted without a controller verb request.

A *1* in the:

- Valid bit position indicates the Response field contains a valid response.
- UnSol bit position is meaningful only when the Valid bit is set, and indicates that the response is unsolicited rather than in reply to a verb.

The 32 actual response bits vary in format and are each documented in Intel's *HD Audio Specification 1.0a*.

> ***Note:*** For more information regarding the verbs, controller, CODEC commands, and control protocol, refer to Intel's *HD Audio Specification 1.0a* document.

Each node in the CODEC is addressed using a CAd that is assigned to the CODEC during initialization, and the Node's ID (NID). The concatenation of the CAd and NID provide a unique address that allows commands to reference a specific node within the audio subsystem.

The entire verb is formed by pre-pending the CAd and the NID to the verb ID and parameter/payload. In this section's tables and descriptions, the CAd and NID are not listed as part of the verb.

Register values may have up to five letters included with their default value. These letters indicate which of the possible reset events force the register to its default value. The five letters are as follows:

- P = POR
- R = HD audio reset pin assertion
- V = Single verb reset
- W = Double verb reset
- D = D-state change reset

Only the letters in the list force the register to its default value.

Node ID 00: Root Node

The following table defines a root note that has one Audio Function Group (AFG).

Table 9: Node 0 Responses

Description	Verb ID	Parameter	Response	Default Value	Comments
Vendor an Device ID	F00h	00h	14F1xxxxh	-	• Vendor ID = 14F1h • Device ID = 1F86h
Revision ID	F00h	02h		-	Revision. ***Note:*** This field increments with silicon stepping.
Subordinate Node Count	F00h	04h	0x00010001	-	AFG.
Bit Clock Capabilities	F00h	16h	0x00000007	-	Supports 6MHz, 12MHz, and 24MHz.
Interface Capabilities	F00h	17h	0x00000000	-	Default.
Get Current BCLK Frequency	F37	00h	0x0000000a	0x00000004	24MHz.

Node ID 01: Audio Function Group (AFG)

Table 10 describes an AFG. made up of 19 nodes, and indicates the default supported sample rates and bit widths for the entire device. Nodes that have differing capabilities also respond to verb queries. The configuration default register in the AFG is not a standard feature

Table 10: Node 01 Responses

Description	Verb ID	Parameter	Response	Default Value	Comments
Subordinate Node Count	0xF00	0x04	0x00100013	-	• Starting node = 10 • Node count = 19
Function Group	0xF00	0x05	0x00000101	-	• AFG • Unsolicited capable
AFG Capabilities	0xF00	0x08	0x00010F0F	-	Sample delay in and out is 16—PC Beep generator.
PCM Size and Rate	0xF00	0x0A	0x000A0140	-	• 16-bit and 24-bit • 48kHz and 96kHz
PCM Format	0xF00	0x0B	0x00000001	-	PCM only.
Supported Power States	0xF00	0x0F	0xE000001F	-	EPSS, clock stop, D0, D1, D2, D3, and D4.
GPIO Count	0xF00	0x11	0xC0000007	-	Seven GPIOs unsolicited message and wake.
Get Power State	0xF05	0x00	0x00000abc	0x00000633 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Unsolicited	0xF08	0x00	0x000000aa	0x00000000 (P, W)	aa = Unsolicited enable and tag.
Set Unsolicited	0x708	0xaa	0x00000000	-	aa = Unsolicited enable and tag.
Get GPIO Data	0xF15	0x00	0x000000aa	0x00000000 (P, W)	aa = GPIO data.
Set GPIO Data	0x715	0xaa	0x00000000	-	aa = GPIO data.
Get GPIO Enable	0xF16	0x00	0x000000aa	0x00000000 (P, W)	aa = GPIO enable.
Set GPIO Enable	0x716	0xaa	0x00000000	-	aa = GPIO enable.
Get GPIO Direction	0xF17	0x00	0x000000aa	0x00000000 (P, W)	aa = GPIO direction.
Set GPIO Direction	0x717	0xaa	0x00000000	-	aa = GPIO direction.
Get GPIO Wake	0xF18	0x00	0x000000aa	0x00000000 (P, W)	aa = GPIO wake.
Set GPIO Wake	0x718	0xaa	0x00000000	-	aa = GPIO wake.
Get GPIO UM Enable	0xF19	0x00	0x000000aa		aa = Unsolicited message enable.
Set GPIO UM Enable	0x719	0xaa	0x00000000		aa = Unsolicited message enable.
Get GPIO Sticky Mask	0xF1A	0x00	0x000000aa	0x00000000 (P, W)	aa = Sticky mask.
Set GPIO Sticky Mask	0x71A	0xaa	0x00000000		aa = Sticky mask.
Get Default Config	0xF1C-0xF1F	0x00	0xaabbccdd	0x00000000 (P)	• aa = Config 4 • bb = Config 3 • cc = Config 2 • dd = Config 1
Set Config Default 1	0x71C	0xaa	0x00000000	-	aa = Config 1.
Set Config Default 2	0x71D	0xaa	0x00000000	-	aa = Config 2.

Table 10: Node 01 Responses (Continued)

Description	Verb ID	Parameter	Response	Default Value	Comments
Set Config Default 3	0x71E	0xaa	0x00000000	-	aa = Config 3.
Set Config Default 4	0x71F	0xaa	0x00000000	-	aa = Config 4.
Get Subsystem ID	0xF20-0xF23	0x00	0xaaaabbcc	0x14F10101 (P)	• aaaa = Subsystem ID • bb = SKU ID • cc = Assembly ID
Set Subsystem ID 1	0x720	0xaa	0x00000000	-	aa = Assembly ID.
Set Subsystem ID 2	0x721	0xaa	0x00000000	-	aa = SKU ID.
Set Subsystem ID 3	0x722	0xaa	0x00000000	-	aa = Subsystem ID low byte.
Set Subsystem ID 4	0x723	0xaa	0x00000000	-	aa = Subsystem ID high byte.
Soft Reset	0x7FF	0x00	0x00000000	-	Soft reset.

Nodes 10, 11: DAC 1, 2 Widgets

The following table describes a stereo DAC.

Table 11: Node 10 and 11 Responses

Description	Verb ID	Parameter	Response	Default Value	Comments
Get Converter Format	0xA	0x0000	0x0000aaaa	0x00000031 (P, W)	aaaa = Converter format.
Set Converter Format	0x2	0xaaaa	0x00000000	-	aaaa = Converter format.
Get Amplifier Gain	0xB80 0xBA0	0x00 0x00	0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Set Amplifier Gain	0x390 0x3A0 0x3B0	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Right and left gain
Audio Widget DAC	0xF00	0x09	0x00000C1D	-	DAC—analog.
PCM Size and Rate	0xF00	0x0A	0x000A0540	-	• 16-bit and 24-bit • 44.1kHz, 96kHz, and 192kHz
PCM Format	0xF00	0x0B	0x00000001	-	PCM only.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Output Amplifier Capabilities	0xF00	0x12	0x80034A4A	-	• Mute, 1dB step • Step 74 is 0dB • 74 of 80 steps are exposed
Get Power State	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Converter Stream and Channel	0xF06	0x00	0x000000ab	0x00000000 (P, R, V, W, D)	• a = Stream • b = Channel position
Set Converter Stream and Channel	0x706	0xab	0x00000000	-	• a = Stream • b = Channel position
Get EAPD	0xF0C	0x00	0x0000000a	0x00000000 (P, W)	a = Left/right swap.
Set EAPD	0x70C	0x0a	0x00000000	-	a = Left/right swap.

Node 12: PC Beep Generator Widget

The following table describes a beep generator.

Table 12: PC Beep Generator Responses

Description	Verb ID	Parameter	Response	Default Value	Comments
Get Amplifier Gain	0xBA0	0x00	0x0000000a	0x00000003 (P, W)	aa = Left gain –24dB
Set Amplifier Gain	0x3A0 0x3B0	0xaa	0x00000000	-	• aa = Left gain • aa = Left gain
Audio Widget PC Beep	0xF00	0x09	0x0070000C	-	PC Beep generator with an output amplifier.
Get Output Amplifier Capabilities	0xF00	0x12	0x000F0707	-	4dB step, eight steps, and step 8 is –4dB.
Get Beep Generation Control	0xF0A	0x00	0x000000aa	0x00000000 (P, W)	aa = Divider.
Set Beep Generation Control	0x70A	0xaa	0x00000000	-	aa = Divider.

Node ID 13: ADC1 Widget

The following table describes a stereo ADC.

Table 13: Node ID 13 Responses

Description	Verb ID	Parameter	Response	Default Value	Comments
Get Converter Format	0xA	0x0000	0x0000aaaa	0x00000031 (P, W)	aaaa = Converter format.
Set Converter Format	0x2	0xaaaa	0x00000000	-	aaaa = Converter format.
Get Index 0 Amp Gain	0xB00 0xB20	0x00	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 1 Amp Gain	0xB00 0xB20	0x01	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 2 Amp Gain	0xB00 0xB20	0x02	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 3 Amp Gain	0xB00 0xB20	0x03	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 4 Amp Gain	0xB00 0xB20	0x04	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 5 Amp Gain	0xB00 0xB20	0x05	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 6 Amp Gain	0xB00 0xB20	0x06	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Set Index 0 Amp Gain	0x350 0x360 0x370	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 1 Amp Gain	0x351 0x361 0x371	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 2 Amp Gain	0x352 0x362 0x372	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 3 Amp Gain	0x353 0x363 0x373	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 4 Amp Gain	0x354 0x364 0x374	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 5 Amp Gain	0x355 0x365 0x375	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 6 Amp Gain	0x356 0x366 0x376	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Audio Widget Capabilities	0xF00	0x09	0x00100D1B	-	ADC—Analog.
PCM Size and Rate	0xF00	0x0A	0x000A0140	-	• 16-bit and 24-bit • 48kHz and 96kHz

*Table 13: **Node ID 13 Responses (Continued)***

Description	Verb ID	Parameter	Response	Default Value	Comments
PCM Format	0xF00	0x0B	0x00000001	-	PCM only.
Input Amplifier Capabilities	0xF00	0x0D	0x8003504A	-	Mute, 1db step, 80 steps, and step 74 is 0db.
Connection Length	0xF00	0x0E	0x00000004	-	-
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Connection Select	0xF01	0x00	0x0000000a	0x00000000 (P, W)	a = Connection index.
Set Connection Select	0x701	0x0a	0x00000000	-	a = Connection index.
Get Connection List	0xF02	0x00	0x151A1918	-	• 18 = Port B input 19 = Headset microphone • 1A = Digital mic1 input 15 = DAC mix
Get Connection List	0xF02	0x04	0x001F1E1D	-	• 1D = Port E input 1E = Port F input 1F = Digital mic2 input
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state • The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	• a = Requested state.
Get Converter Stream/ Channel	0xF06	0x00	0x000000ab	0x00000000 (P, R, V, W, D)	• a = Stream • b = Channel position
Set Converter Stream/ Channel	0x706	0xab	0x00000000	-	• a = Stream • b = Channel position
Get EAPD	0xF0C	0x00	0x0000000a	0x00000000 (P, W)	a = Left/right swap.
Set EAPD	0x70C	0x0a	0x00000000	-	a = Left/right swap.

Node ID 14: ADC2 Widget

The following table describes a stereo ADC.

Table 14: Node ID 14 Responses

Description	Verb ID	Parameter	Response	Default Value	Comments
Get Converter Format	0xA	0x0000	0x0000aaaa	0x00000031 (P, W)	aaaa = Converter format.
Set Converter Format	0x2	0xaaaa	0x00000000	-	aaaa = Converter format.
Get Index 0 Amp Gain	0xB00 0xB20	0x00	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 1 Amp Gain	0xB00 0xB20	0x01	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Get Index 2 Amp Gain	0xB00 0xB20	0x02	0x000000aa 0x000000aa	0x0000004A (P, W)	• aa = Right gain • aa = Left gain
Set Index 0 Amp Gain	0x350 0x360 0x370	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 1 Amp Gain	0x351 0x361 0x371	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Set Index 2 Amp Gain	0x352 0x362 0x372	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Audio Widget Capabilities	0xF00	0x09	0x00100D1B	-	ADC—Analog.
PCM Size and Rate	0xF00	0x0A	0x000A0140	-	• 16-bit and 24-bit • 48kHz and 96kHz
PCM Format	0xF00	0x0B	0x00000001	-	PCM only.
Input Amplifier Capabilities	0xF00	0x0D	0x8003504A	-	Mute, 1db step, 80 steps, and step 74 is 0db.
Connection Length	0xF00	0x0E	0x00000002	-	-
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Connection Select	0xF01	0x00	0x0000000a	0x00000000 (P, W)	a = Connection index.
Set Connection Select	0x701	0x0a	0x00000000	-	a = Connection index.
Get Connection List	0xF02	0x00	0x0000151A	-	-
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state • The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	• a = Requested state.
Get Converter Stream/ Channel	0xF06	0x00	0x000000ab	0x00000000 (P, R, V, W, D)	• a = Stream • b = Channel position
Set Converter Stream/ Channel	0x706	0xab	0x00000000	-	• a = Stream • b = Channel position
Get EAPD	0xF0C	0x00	0x0000000a	0x00000000 (P, W)	a = Left/right swap.
Set EAPD	0x70C	0x0a	0x00000000	-	a = Left/right swap.

Node ID 15: Mixer Widget

The following table describes a mixer widget.

Table 15: Node ID 15 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Index 0 Amp Gain	0xB00 0xB20	0x00	0x000000aa 0x000000aa	0x00000000 (P, W)	• a = Right gain • a = Left gain
Get Index 1 Amp Gain	0xB00 0xB20	0x01	0x000000aa 0x000000aa	0x00000000 (P, W)	• a = Right gain • a = Left gain
Set Index 0 Amp Gain	0x350 0x360 0x370	0xaa	0x00000000	-	• a = Right gain • a = Left gain • a = Left & Right gain
Set Index 1 Amp Gain	0x351 0x361 0x371	0xaa	0x00000000	-	• a = Right gain • a = Left gain • a = Left & Right gain
Audio Widget Mixer	0xF00	0x09	0x0020050B	-	Mixer with input amplifier.
Input Amplifier Capabilities	0xF00	0x0D	0x80034A4A	-	Mute, 1dB steps, 74 steps, step 74 is 0dB.
Connection Length	0xF00	0x0E	0x00000002	-	Connected to two widgets.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Connection List	0xF02	0x00	0x00001110	-	Connected to DAC1, DAC2.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.

Node ID 16: Port A/Vendor Widget

The following table describes a pin widget that has selectable headphone or line drive and supports jack sensing.

Table 16: Node ID 16 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Audio Widget Pin	0xF00	0x09	0x00400581 0x00F00000	-	• Pin—Analog • Vendor widget in UAJ mode
Get Pin Capabilities	0xF00	0x0C	0x0001001C	-	Output, HP, sense, EAPD.
Connection Length	0xF00	0x0E	0x00000002	-	Connected to 2.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, D3.
Get Connection	0xF01	0x00	0x0000000a	0x00000000 (P, W)	DAC1 is selected.
Set Connection	0x701	0x0a	0x00000000	-	• 0 = DAC1 • 1 = DAC2
Get Connection List	0xF02	0x00	0x00001110	-	DAC1, DAC2.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Pin Control	0xF07	0x00	0x000000a0	0x000000C0 (P, W)	a = Headphone and output enable.
Set Pin Control	0x707	0xa0	0x00000000	-	a = Headphone and output enable.
Get Unsolicited Response	0xF08	0x00	0x000000aa	0x00000000 (P, W)	aa = Unsolicited enable and tag.
Set Unsolicited Response	0x708	0xaa	0x00000000	-	aa = Unsolicited enable and tag.
Get Pin Sense	0xF09	0x00	0xa0000000	-	• a = Presence detect • 8 = Present • 0 = Missing
Get EAPD	0xF0C	0x00	0x0000000a	0x00000000 (P, W)	a = EAPD.
Set EAPD	0x70C	0x0a	0x00000000	-	a = EAPD.
Get Default Config	0xF1C-0xF1F	0x00	0xaabbccdd	0x0421401F (P)	• aa = Config 4 • bb = Config 3 • cc = Config 2 • dd = Config 1
Set Default Config 1	0x71C	0xaa	0x00000000	-	aa = Config 1.
Set Default Config 2	0x71D	0xaa	0x00000000	-	aa = Config 2.
Set Default Config 3	0x71E	0xaa	0x00000000	-	aa = Config 3.
Set Default Config 4	0x71F	0xaa	0x00000000	-	aa = Config 4.

Node ID 17: Port G BTL Pin Widget

The following table describes a pin that accepts a stereo signal and drives stereo speakers.

Table 17: Node ID 17 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Audio Widget Pin	0xF00	0x09	0x00400501	-	Pin—Analog.
Get Pin Capabilities	0xF00	0x0C	0x00010010	-	Output, EAPD.
Connection Length	0xF00	0x0E	0x00000002	-	Connected to 2.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, D3.
Get Connection	0xF01	0x00	0x0000000a	0x00000000 (P, W)	DAC1 is selected.
Set Connection	0x701	0x0a	0x00000000	-	• 0 = DAC1 • 1 = DAC2
Get Connection List	0xF02	0x00	0x00001110	-	Connected to DAC1, DAC2.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Pin Control	0xF07	0x00	0x000000a0	0x00000040 (P, W)	a = Output enable.
Set Pin Control	0x707	0xa0	0x00000000	-	a = Output enable.
Get EAPD	0xF0C	0x00	0x0000000a	0x00000000 (P, W)	a = EAPD.
Set EAPD	0x70C	0x0a	0x00000000	-	a = EAPD.
Get Default Config	0xF1C-0xF1F	0x00	0xaabbccdd	0x90170010 (P)	• aa = Config 4 • bb = Config 3 • cc = Config 2 • dd = Config 1
Set Default Config 1	0x71C	0xaa	0x00000000	-	aa = Config 1.
Set Default Config 2	0x71D	0xaa	0x00000000	-	aa = Config 2.
Set Default Config 3	0x71E	0xaa	0x00000000	-	aa = Config 3.
Set Default Config 4	0x71F	0xaa	0x00000000	-	aa = Config 4.

Node ID 18: Port B Widget

Table 18 describes a stereo pin widget that can be configured to be a line input or microphone input. There is a microphone boost control and micbias.

Table 18: Node ID 18 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amp Gain	0xB00 0xB20	0x00	0x000000aa 0x000000aa	0x00000000 (P, W)	• aa = Right gain • aa = Left gain
Set Amp Gain	0x350 0x360 0x370	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Audio Widget Pin	0xF00	0x09	0x0040048B 0x0040058B	Default UAJ Mode	• Pin—Analog • Add connection list
Get Pin Capabilities	0xF00	0x0C	0x00001324 0x0001133C	-	Vref, input, jack sense.
Input Amp Capabilities	0xF00	0x0D	0x002F0300	-	12db step, four steps, and step 0 is 0db.
Connection Length	0xF00	0x0E	0x00000002	-	Connected to 2.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Connection	0xF01	0x00	0x0000000a	0x00000000 (P, W)	DAC 1 is selected.
Set Connection	0x701	0x0a	0x00000000	-	• 0 = DAC 1 • 1 = DAC 2
Get Connection List	0xF02	0x00	0x00001110	-	DAC 1, 2.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Pin Control	0xF07	0x00	0x000000aa	0x00000000 (P, W)	aa = Vref, input enable, output, HP.
Set Pin Control	0x707	0xaa	0x00000000	-	aa = Vref, input enable, output, HP.
Get Unsolicited Response	0xF08	0x00	0xaa	0x00000000 (P, W)	aa = Unsolicited enable and tag.
Set Unsolicited Response	0x708	0xaa	0x00000000	-	aa = Unsolicited enable and tag.
Get Pin Sense	0xF09	0x00	0xa0000000	-	• a = Presence detect • 8 = Present • 0 = Missing
Get EAPD	0xF0C	0x00	0x0000000a	0x00000000 (P, W)	a = EAPD.
Set EAPD	0x70C	0x0a	0x00000000	-	a = EAPD.
Get Default Config	0xF1C- 0xF1F	0x00	0xaabbccdd	0x048130F0 (P)	• aa = Config4 • bb = Config3 • cc = Config2 • dd = Config1

Table 18: ***Node ID 18 Responses (Continued)***

Description	Verb ID	Parameter	Response	Default Value	Comment
Set Default Config 1	0x71C	0xaa	0x00000000	-	aa = Config1.
Set Default Config 2	0x71D	0xaa	0x00000000	-	aa = Config2.
Set Default Config 3	0x71E	0xaa	0x00000000	-	aa = Config3.
Set Default Config 4	0x71F	0xaa	0x00000000	-	aa = Config4.

Node ID 19: Port D Widget

Table 19 describes a stereo pin widget that is a microphone input. There is a microphone boost control and micbias.

Table 19: Node ID 19 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amp Gain	0xB00 0xB20	0x00	0x000000aa 0x000000aa	0x00000000 (P, W)	• aa = Right gain • aa = Left gain
Set Amp Gain	0x350 0x360 0x370	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Audio Widget Pin	0xF00	0x09	0x0040048B 0x0040040B	Headset enabled	Pin—Analog.
Get Pin Capabilities	0xF00	0x0C	0x00001324 0x00001320	Headset enabled	• Vref-in, jack sense • Vref-in
Input Amp Capabilities	0xF00	0x0D	0x002F0300	-	12db step, four steps, and step 0 is 0db.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Pin Control	0xF07	0x00	0x000000aa	0x00000000 (P, W)	aa = Vref, input enable.
Set Pin Control	0x707	0xaa	0x00000000	-	aa = Vref, input enable.
Get Unsolicited Response	0xF08	0x00	0xaa	0x00000000 (P, W)	aa = Unsolicited enable and tag.
Set Unsolicited Response	0x708	0xaa	0x00000000	-	aa = Unsolicited enable and tag.
Get Pin Sense	0xF09	0x00	0xa0000000	-	• a = Presence detect • 8 = Present • 0 = Missing
Get Default Config	0xF1C- 0xF1F	0x00	0xaabbccdd	0x04A190F0 (P)	• aa = Config4 • bb = Config3 • cc = Config2 • dd = Config1
Set Default Config 1	0x71C	0xaa	0x00000000	-	aa = Config1.
Set Default Config 2	0x71D	0xaa	0x00000000	-	aa = Config2.
Set Default Config 3	0x71E	0xaa	0x00000000	-	aa = Config3.
Set Default Config 4	0x71F	0xaa	0x00000000	-	aa = Config4.

Node ID 1A: Port C Widget

Port C is a stereo microphone.

Table 20: Node ID 1A Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amp Gain	0xB00 0xB20	0x00	0x000000aa 0x000000aa	0x00000000 (P, W)	• aa = Right gain • aa = Left gain
Set Amp Gain	0x350 0x360 0x370	0xaa	0x00000000	-	• aa = Right gain • aa = Left gain • aa = Left and right gain
Audio Widget Pin	0xF00	0x09	0x0040040B	Headset enabled	Pin—Analog.
Get Pin Capabilities	0xF00	0x0C	0x00000020	Headset enabled	Input only.
Input Amp Capabilities	0xF00	0x0D	0x002F0300	-	12db step, four steps, and step 0 is 0db.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Pin Control	0xF07	0x00	0x000000aa	0x00000000 (P, W)	a = Input enable.
Set Pin Control	0x707	0xaa	0x00000000	-	a = Input enable.
Get Default Config	0xF1C- 0xF1F	0x00	0xaabbccdd	0x90A700F0 (P)	• aa = Config4 • bb = Config3 • cc = Config2 • dd = Config1
Set Default Config 1	0x71C	0xaa	0x00000000	-	aa = Config1.
Set Default Config 2	0x71D	0xaa	0x00000000	-	aa = Config2.
Set Default Config 3	0x71E	0xaa	0x00000000	-	aa = Config3.
Set Default Config 4	0x71F	0xaa	0x00000000	-	aa = Config4.

Node ID 20: DAC 3—Sony/Philips Digital Interface Format (S/PDIF) Output Widget

The following table describes an S/PDIF DAC that supports 16-bit and 24-bit widths, and a 96kHz sample rate.

Table 21: Node ID 20 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Converter Format	0xA	0x0000	0x0000aaaa	0x00000031 (P, W)	aaaa = Converter format.
Set Converter Format	0x2	0xaaaa	0x00000000	-	aaaa = Converter format.
Audio Widget S/PDIF	0xF00	0x09	0x00000611	-	DAC—Digital stereo.
PCM Size and Rate	0xF00	0x0A	0x000E05E0	-	• 16-bit and 24-bit • 48K, 96K, and 192K sample rates
PCM Format	0xF00	0x0B	0x00000005	-	PCM and AC-3.
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Power State	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Converter Stream/ Channel	0xF06	0x00	0x000000ab	0x00000000 (P, R, V, W, D)	• a = Stream • b = Channel
Set Converter Stream/ Channel	0x706	0xab	0x00000000	-	• a = Stream • b = Channel
Get Digital Converter Control	0xF0D 0xF0E	0x00	0xaabbccdd	0x00000000 (P, W)	• aa = Reserved • bb = Coding mode • cc = Category code • dd = Header information
Set Digital Control 1	0x70D	0xaa	0x00000000	-	aa = Header information.
Set Digital Control 2	0x70E	0xaa	0x00000000	-	aa = Category code.
Set Digital Control 3	0x73E	0xaa	0x00000000	-	aa = IEC coding type and keep alive enable.
Set Digital Control 4	0x73F	0x00	0x00000000	-	Reserved, read as 0.

Node ID 21: Port I S/PDIF Output Widget

The following table describes a digital output pin.

Table 22: Node ID 21 Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Audio Widget Pin	0xF00	0x09	0x00400701	-	Pin—Digital.
Get Pin Capabilities	0xF00	0x0C	0x00000010	-	Output.
Connection Length	0xF00	0x0E	0x00000001	-	-
Supported Power States	0xF00	0x0F	0x8000000F	-	EPSS, D0, D1, D2, and D3.
Get Connection	0xF01	0x00	0x0000000a	0x00000000 (P, W)	S/PDIF DAC is selected.
Set Connection	0x701	0x0a	0x00000000	-	0 = S/PDIF DAC.
Get Connection List	0xF02	0x00	0x00000020	-	Connects to S/PDIF DAC.
Get Power Sate	0xF05	0x00	0x00000abc	0x00000433 (P, W)	• a = Settings reset • b = Actual state • c = Requested state The settings reset is cleared by this verb or any write to this node.
Set Power State	0x705	0x0a	0x00000000	-	a = Requested state.
Get Pin Control	0xF07	0x00	0x000000a0	0x00000000 (P, W)	a = Output enable.
Set Pin Control	0x707	0xa0	0x00000000	-	a = Output enable.
Get Default Config	0xF1C- 0xF1F	0x00	0xaabbccdd	0x044510F0 (P)	• aa = Config4 • bb = Config3 • cc = Config2 • dd = Config1
Set Default Config 1	0x71C	0xaa	0x00000000	-	aa = Config1.
Set Default Config 2	0x71D	0xaa	0x00000000	-	aa = Config2.
Set Default Config 3	0x71E	0xaa	0x00000000	-	aa = Config3.
Set Default Config 4	0x71F	0xaa	0x00000000	-	aa = Config4.

Node 1B: Vendor-Specific Widget

This node describes the EQ, DRC, and other registers that are available in this device. Refer to the *BIOS Guide* document for details.

Node 1C: Vendor-Specific Widget

This node describes the vendor-specific registers. Refer to the *BIOS Guide* document for details.

Ordering Information

Table 23: ***Ordering Information***

Model/Order/Part Numbers				AudioSmart Class-D 1.0	Operating Temperature
Device Order Number	Audio CODEC Part Number	Revision	Audio CODEC Package Type		
CX11880-11Z	CX11880	-11Z	42-QFN, 5x5	Yes	0 to 70°C

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