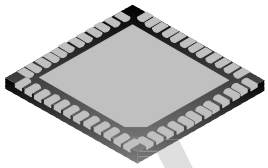
Audio Processing SoC With High-Performance DSP

INTRODUCTION

The SC5864D is a highly-integrated audio system-on-chip (SoC) integrated with Cortex-M0 processor for low power management, and a high performance audio dedicated DSP for sound effect processing. Furthermore, it is also integrated with SAR-ADC, USB, SD/MMC controllers, and audio CODEC.



QFN-48-7X7X0.75-0.5

APPLICATIONS

- Audio processing
- Sound effect processing

FEATURES

Architecture

- DSP
  - 5-level pipelines, maximum operating frequency: 160MHz;
  - 32bit/16bit multiplication: MAC16, MUL16, MUL32;
  - 32bit integer division;
  - Single-precision floating-point operation;
  - Dedicated hardware audio acceleration engine;
  - 32KB instruction/data Cache, WB/WT supported;
  - Local SRAM;
- MCU
  - High performance Cortex-M0 core, maximum operating frequency: 80MHz;
  - Embedded 8KB Cache, four address areas, independently configure;
  - Supports frequency reduction, a quarter of maximum bus frequency;

Clock & Power Manager

- External 12MHz oscillators;
- Built-in RCL and RCH;
- Built-in System PLL, Audio PLL and USB PLL;
- Built-in double 1.2V LDO;
- Multi low-power operating modes supported, such as frequency reduction, STOP mode.

Memory Controller

- SPI flash controller
  - Supports SPI Flash 1/2/4-wire modes;
  - Core runs directly in SPI Flash;
  - Packaged with 16Mbit SPI NorFlash;
- SRAM

- Embedded 240KB SRAM, system 32KB+16KB, DSP 192KB;
- Supports Byte, Half-word, Word access;

Peripherals

- Audio CODEC
  - Built-in stereo Audio ADCs; SNR 100db (A-weight, Line in);
  - Supports stereo analog MIC input and ALC;
  - Built-in stereo Audio DAC, SNR 100db(A-weight);
- USB_HS
  - Built-in USB2.0 high-speed PHY;
  - Compliance with USB2.0 standard;
  - Supports control, bulk, interrupt, and synchronous transfer;
  - Built-in 2KB SRAM;
  - Built-in Normal and Scatter-Gatter DMA transfer;
- SD/MMC
  - Compliance with SD2.0, MMC4.3 standards;
  - Supports 4-bit mode;
  - Built-in Normal and chained DMA transfer;
- UARTx3
  - 3 UART modules provided;
  - High-speed UART1 integrated with 64-byte FIFO, UART2 with 8-byte FIFO, while UART3 with 16-byte FIFO;
  - Programmable data bits and stop bit;
  - Parity check supported or no check;
  - Supports receiving/sending FIFO interrupt;
  - PDMA mode supported by UART1/3;
- I^2C
  - Supports standard speed, fast speed, and high speed modes;
  - Supports Master and Slave modes;
- SPI
  - Supports SPI standard 4-wire protocol;
  - Embedded independent 8x32 receive and send buffers;
  - Supports PDMA mode;
- PWM
  - Supports preset frequency division;
  - 16-bit counting accuracy;
- ADC
  - 6-channel analog inputs, 10bit accuracy;
- GPIO
  - Two GPIO controllers, GPIOs;
  - Independent pull-up resistor enable;
  - Selectable drive strength (2/4/8/24mA)；

- Supports configurable interrupt of each IO, edge or level triggered;

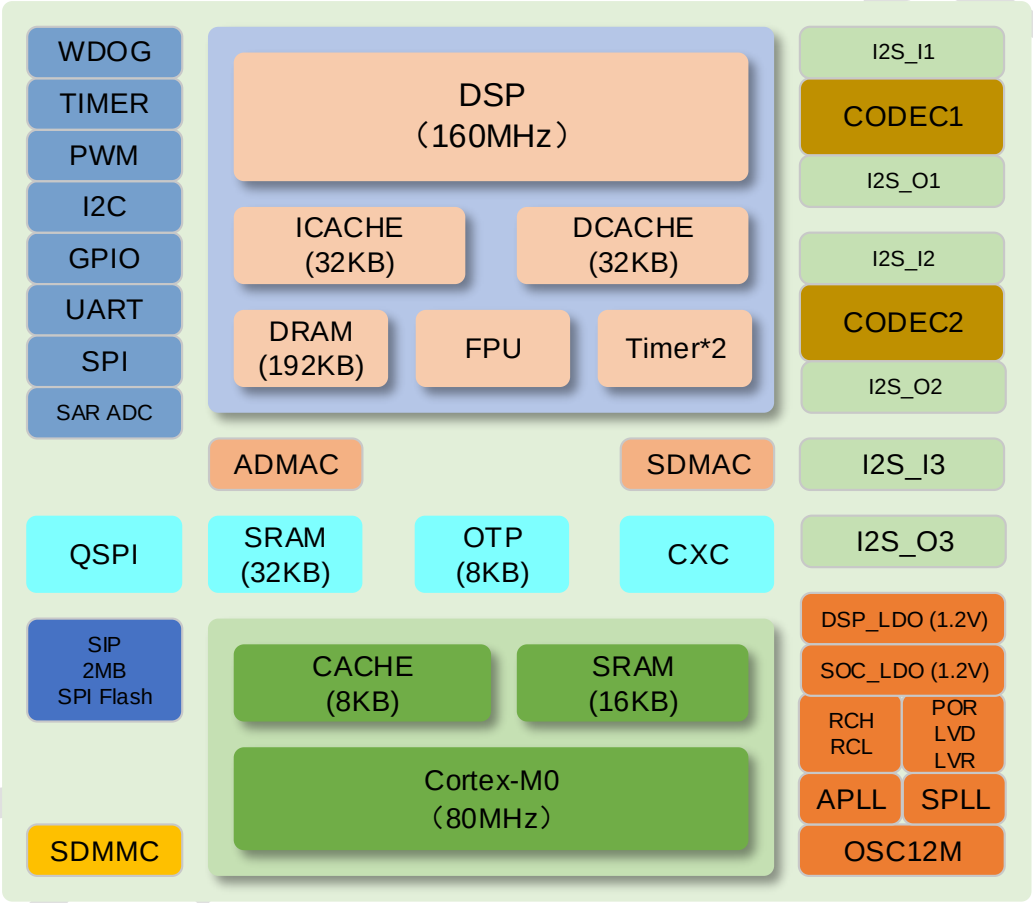
Applications

- Audio processing

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SC5864D	QFN-48-7X7X0.75-0.5	SC5864D	Halogen free	Tray

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Unit
Core voltage	V_{CCINT}	1.08 ~ 1.32	V
Port voltage	V_{CCIO}	2.97 ~ 3.63	V
Pin input voltage	V_{IN}	2.97 ~ 3.63	V
Operating Temperature Range	T_{amb}	-40 ~ 85	°C
Storage Temperature Range	T_{STG}	-40 ~ 150	°C

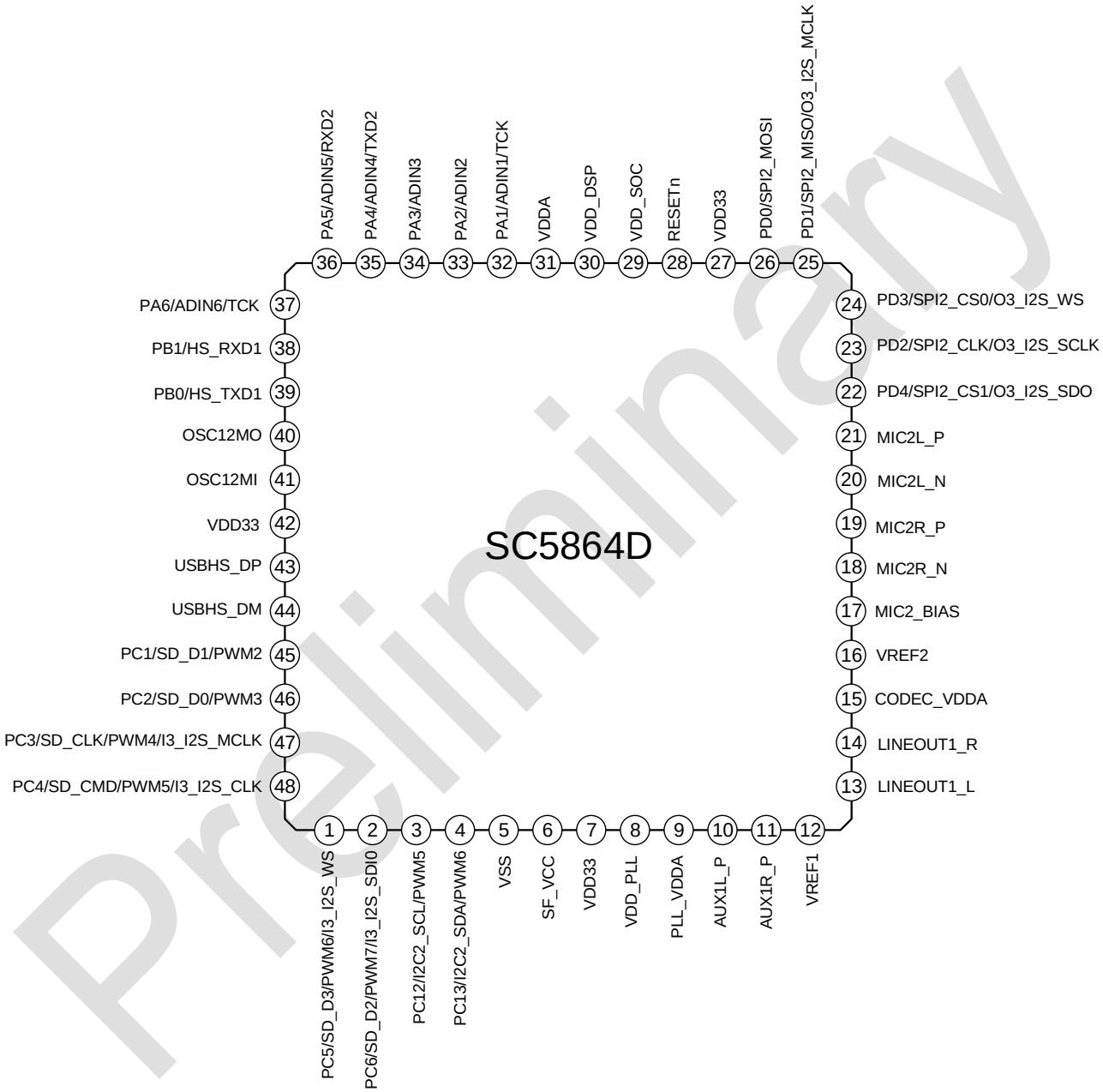
ELECTRICAL PARAMETERS

(V_{CCINT}=1.20V, V_{CCIO}=3.3V, T_{amb}=25°C, f=120MHz)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Core operating voltage	V_{CCINT}	Normal operation	1.08	1.20	1.32	V
Port operating voltage	V_{CCIO}	Normal operation	2.97	3.3	3.63	V
VDD33 operating current in main oscillation mode	I_{CCIO}	Power supply current at Core V_{DD33} (SYSCLK=120M)	144	160	176	mA
VDD33 operating current in low frequency mode	I_{CCIO}	Power supply current at Core V_{DD33}(M0 runs with low frequency@4MHz)	1	2	2.5	mA
VDD33 operating current in circuit IDLE mode	I_{CCIO}	Power supply current at Core V_{DD33}(IDLE mode)	/	650	/	uA
Pull-up resistance	R_{PU}		30	/	90	KΩ
Crystal oscillation feedback resistance (internal)	R_{OSC}	--	/	1	/	MΩ
High Input level	V_{IH}	--	1.6	3.3	4.5	V
Low Input level	V_{IL}	V_{IN}=V_{DD}	/	0	1.4	V
High Input Current	I_{IH}	V_{IN}=V_{DD}	/	0	/	μA
Low Input Current	I_{IL}	V_{IN}=V_{SS}	/	0	/	μA
High Output Current	I_{OH}	V_{OH}=2.4V, I_{OH}=8mA	/	14	/	mA
Low Output Current	I_{OL}	V_{OL}=0.4V, I_{OH}=8mA	/	8	/	mA
DAC Line Out (10KΩ load)						
Full amplitude output level	V_{FS}	0dB gain		0.88		Vrms
Sampling rate	Fs		8		192	KHz
Signal-to noise ratio (A-Weighted)	SNR	1KHz	95	100		dB
Dynamic range (A-Weighted)	DR	1kHz, -60dBr	95	100		dB
Total harmonic distortion	THD+N	-1dBr		-85	-80	dB
Programmable gain step	DA_PGA	128 step, -72dB~+23.5dB		0.75		dB
Channel isolation		1KHz, -20dB/-100dB	80	100		dB
Frequency response		Passband	0.02	0.416*FS	20	KHz
		Passband Ripple		0.2		dB
Power Supply Rejection Ratio	PSRR	1KHz, 100mVpp	42	53		dB
		20Hz~20KHz, 100mVpp	37.5	45	55	dB
ADC AUX/Line Input (differential input)						
Sampling rate	Fs		8		96	KHz
Signal-to noise ratio (A-Weighted)	SNR	1KHz, AD_PGA=0dB	90	100		dB
Dynamic range (A-Weighted)	DR	1KHz, -60dBr	90	100		dB
Total harmonic distortion	THD+N	1KHz, -1dBr		-84	-75	dB
Differential full amplitude output level	V_{FS}	0dB gain		1.5		Vrms

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Channel isolation		1KHz, L/R	80	98		dB
		1KHz, AUX/FM/LINEIN/MIC	100	110		dB
Frequency response		Passband	0.02	0.416*FS	20	KHz
		Passband Ripple		0.25	0.38	dB
Power Supply Rejection Ratio	PSRR	1KHz, 100mVpp		65		dB
		20Hz~20kHz, 100mVpp	50		70	dB
Programmable gain (analog) step	AUX_PGA	-12dB~+12dB		0.75		dB
Programmable gain (digital) step	AD_PGA	0dB~23dB		1		dB
ADC MIC Input (differential input)						
Sampling rate	Fs		8		96	kHz
Signal-to noise ratio (A-Weighted)	SNR	Input:1KHz MIC_Boost=20dB	80	84		dB
Dynamic range (A-Weighted)	DR	Input:1KHz, -60dBr MIC_Boost=20dB	80	84		dB
Total harmonic distortion	THD+N	Input: 1KHz, -1dBr, 0dB Gain		-77	-70	dB
		Input: 1kHz, -1dBr, 20dB Gain		-74	-70	dB
Differential full amplitude output level	V_{FS}	MIC_PGA=20dB		0.15		Vrms
Channel isolation		1KHz, L/R, 0dB	80	98	105	dB
		1KHz, L/R, 20dB	80	94	96	dB
MIC Bias voltage	$V_{MICBIAS}$		1.6		2.5	V
MIC Bias current	$I_{MICBIAS}$				4.7	mA
MIC Boost	MIC_BOOST		0		20	dB
Programmable gain step	MIC_PGA	0dB ~ +34.5dB		1.5		dB

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Description
0	**VSS**	**G**	**Digital GND**
1	PC5	I/O	SD_D3/I3_I2S_WS/PWM6/GPIO1_14
2	PC6	I/O	SD_D2/I3_I2S_SDI0/PWM7/GPIO1_15
3	PC12	I/O	I2C2_SCL/ PWM5/GPIO1_21
4	PC13	I/O	I2C2_SDA/ PWM6/GPIO1_22
5	VSS	I/O	Digital GND
6	SF_VCC	O	Internal SPI NorFlash power supply, connected to 1uF filter capacitor
7	**VDD33**	**P3**	**IO power supply 3.3V**
8	**VDD_PLL**	**PA**	**AUDIO PLL1.2V dedicated power supply**
9	**PLL_VDDA**	**PA**	**AUDIO PLL3.3V dedicated power supply**
10	AUX1L_P	AI	CODEC1_FM left channel differential input channel P
11	AUX1R_P	AI	CODEC1_FM right channel differential input channel P
12	VREF1	AO	CODEC1 reference voltage
13	LINEOUT1_L	AO	CODEC1 DAC left channel output
14	LINEOUT1_R	AO	CODEC1 DAC right channel output
15	**CODEC_VDDA**	**PA**	**CODEC analog power supply 3.3V**
16	VREF2	AO	CODEC2 reference voltage
17	MIC2_BIAS	AI	CODEC2_MIC bias voltage
18	MIC2R_N	AI	CODEC2_MIC right channel differential input channel N
19	MIC2R_P	AI	CODEC2_MIC right channel differential input channel P
20	MIC2L_N	AI	CODEC2_MIC left channel differential input channel N
21	MIC2L_P	AI	CODEC2_MIC left channel differential input channel P
22	PD4	I/O	SPI2_CS1/O3_I2S_SDO/DSP_JTRST/PWM3/TCK/GPIO2_4
23	PD2	I/O	SSP_CLK/SPI2_CLK/TXD3/O3_I2S_SCLK/DSP_JTDO/RISC_SWCLK/PWM1/GPIO2_2
24	PD3	I/O	SSP_FSS/SPI2_CS0/RXD3/O3_I2S_WS/DSP_JTMS/RISC_SWD/PWM2/GPIO2_3
25	PD1	I/O	SSP_MISO/SPI2_MISO/RXD2/O3_I2S_MCLK/DSP_JTDI/MCU_SWD/PWM0/GPIO2_1
26	PD0	I/O	SSP_MOSI/SPI2_MOSI/TXD2/DSP_JTCK/MCU_SWCLK/PWM7/GPIO2_0
27	**VDD33**	**P3**	**IO power supply 3.3V**
28	RESETn	I	Reset pin, active low
29	**VDD_SOC**	**P0**	**SOC core power supply 1.2V**
30	**VDD_DSP**	**P1**	**DSP core power supply 1.2V**
31	**VDDA**	**PA**	**LDO power supply input**
32	PA1	I/O	ADIN1/PWM1/TCK/GPIO2_12/ key wake-up
33	PA2	I/O	ADIN2/PWM2/GPIO2_13/ key wake-up

Pin No.	Pin Name	I/O	Pin Description
34	PA3	I/O	ADIN3/PWM3/GPIO2_14/ key wake-up
35	PA4	I/O	ADIN4/TXD2/PWM4/GPIO2_15/ key wake-up
36	PA5	I/O	ADIN5/RXD2/PWM5/GPIO2_16/ key wake-up
37	PA6	I/O	ADIN6/PWM6/TCK/GPIO2_17/ key wake-up
38	PB1	I/O	HS_RXD1/PWM1/GPIO1_1
39	PB0	I/O	HS_TXD1/PWM0/GPIO1_0
40	OSC12MO	AO	12M crystal oscillator pin
41	OSC12MI	A1	12M crystal oscillator pin
42	**VDD33**	**P3**	**IO power supply 3.3V**
43	USBHS_DP	AIO	DP of High-speed USB
44	USBHS_DM	AIO	DM of High-speed USB
45	PC1	I/O	SD_D1/PWM4/GPIO1_12
46	PC2	I/O	SD_D0/PWM5/GPIO1_13
47	PC3	I/O	SD_CLK/I3_I2S_MCLK/PWM4/GPIO1_12
48	PC4	I/O	SD_CMD/I3_I2S_SCLK/PWM5/GPIO1_13

Note:

1) Introduction to I/O:

I –Input pin

O – Output pin

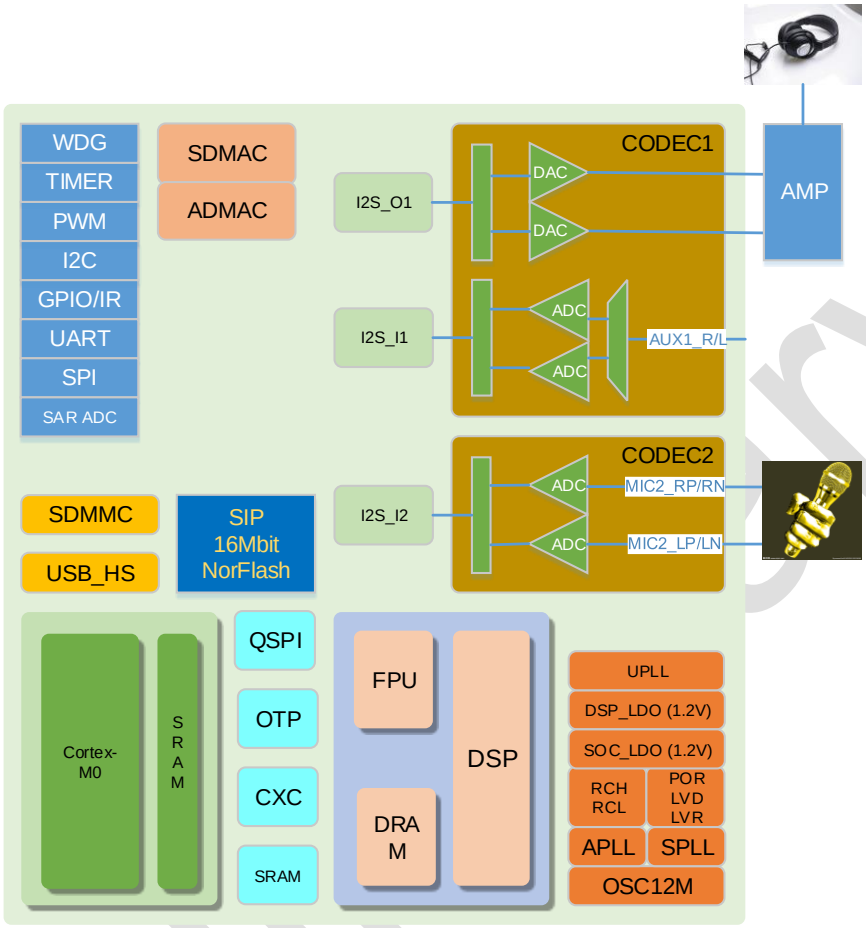
I/O– Input/output pin

A – Analog pin, AI—analog input, AO—analog output

P – Power supply, P3--3.3V IO power supply, PA—analog 3.3V power supply, PA1—analog 1.2V power supply

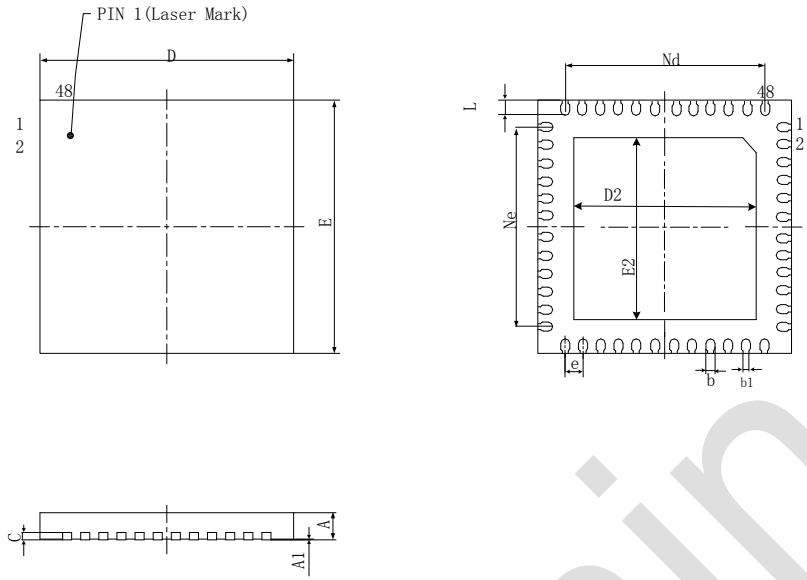
G – Ground, GA—analog ground

TYPICAL APPLICATION



PACKAGE OUTLINES

QFN-48-7x7x0.75-0.5 **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1		0.16REF	
c	0.18	0.20	0.23
D	6.80	7.00	7.20
D2	—	—	5.80
e		0.50BSC	
Ne		5.50BSC	
Nd		5.50BSC	
E	6.80	7.00	7.20
E2	—	—	5.80
L	0.35	0.40	0.45

注:D2、E2由载体规格决定，以实际测量尺寸为准

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Disclaimer :

- **Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
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Rev.: 0.2

Revision History:

1. Modify title

Rev.: 0.1

Revision History:

1. Preliminary