

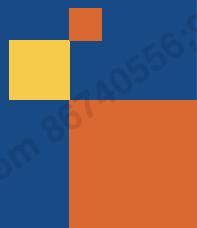
Raptor Lake Platform Turbo and Thermal Power Management Guide for Intel® Core™ - based Processors

User Guide

Revision 1.0

January 2023

Document Number: 721867



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Revision History

Revision Number	Description	Revision Date
0.5	▪ Initial Release	February 2022
0.7	▪ Added Intel Performance Hybrid Architecture	May 2022
1.0	▪ Updated Slide 150	January 2023

Terminology

Old Name	New Name
TDP	Processor Base Power (TDP)
cTDP Down Power	Minimum Assured Power (cTDP Down Power) [W]
cTDP Down Frequency	Minimum Assured Frequency (cTDP Down Frequency) [MHz]
cTDP Up Power	Maximum Assured Power (cTDP Up Power) [W]
cTDP Up Frequency	Maximum Assured Frequency (cTDP Up Frequency)[MHz]
P1 Freq	Processor P-Core Base Frequency (P1) [MHz]
Small core , Big Core	Small core -> E-Core Big core -> P-Core

Contents

- Introduction and Turbo Configuration Options
- Turbo Concepts
- Introduction to Power Limits
- Thermal Management
- Power Delivery
- Turbo Control Interface Reference
- cTDP Design Considerations
- Software Tools
- Checklist
- Reference

1.0 Introduction and Turbo Configuration Options

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1.1 Document Scope

- This guide provides details on the growing number for controls exposed by the SoC. It also supplies a starting point for the usage and settings of those controls for power/thermal management.
- The target audience for this document includes board design engineers, thermal engineers, power delivery engineers, BIOS/FW engineers and validation engineers.
- Guidance in this document is not necessarily SKU specific, although examples utilizing a specific SKU may be used. Refer appropriate specifications for details.

Note: Where any discrepancy exists between this document and any referenced specification, the most current version of the referenced specification takes precedence.

1.2 Introduction

- System design and power management capabilities have grown more complex over the past few processor generations. This guide provides details on the growing number for controls exposed by the SoC. It also supplies a starting point for the usage and settings of those controls for power/thermal management.
- To maximize performance, Intel strongly recommends the use of active feedback and dynamic control of the SoC thermal/power controls. This can best be done via the use of skin temperature sensors for systems that are primarily limited by skin temperature. This document provides details on Turbo related hardware power management features.
- Intel® Dynamic Tuning provides means to easily add active feedback and dynamic control of the Turbo power settings using skin sensor in the systems. Intel strongly recommends using Intel® Dynamic Tuning to manage many of the turbo related parameters dynamically. (Refer the collateral list for Intel® Dynamic Tuning related material.)
- When you use Intel® Dynamic Tuning you control some parameters with the framework. However, this document guides you in setting all parameters in the absence of Intel® Dynamic Tuning.

Intel® Turbo Boost Technology 2.0 is intended to provide designers with the ability to utilize available thermal capacitance in a system for additional performance

Proper implementation is a multi-disciplinary effort, requiring coordination between thermal, power delivery, BIOS/FW and embedded/system controller disciplines

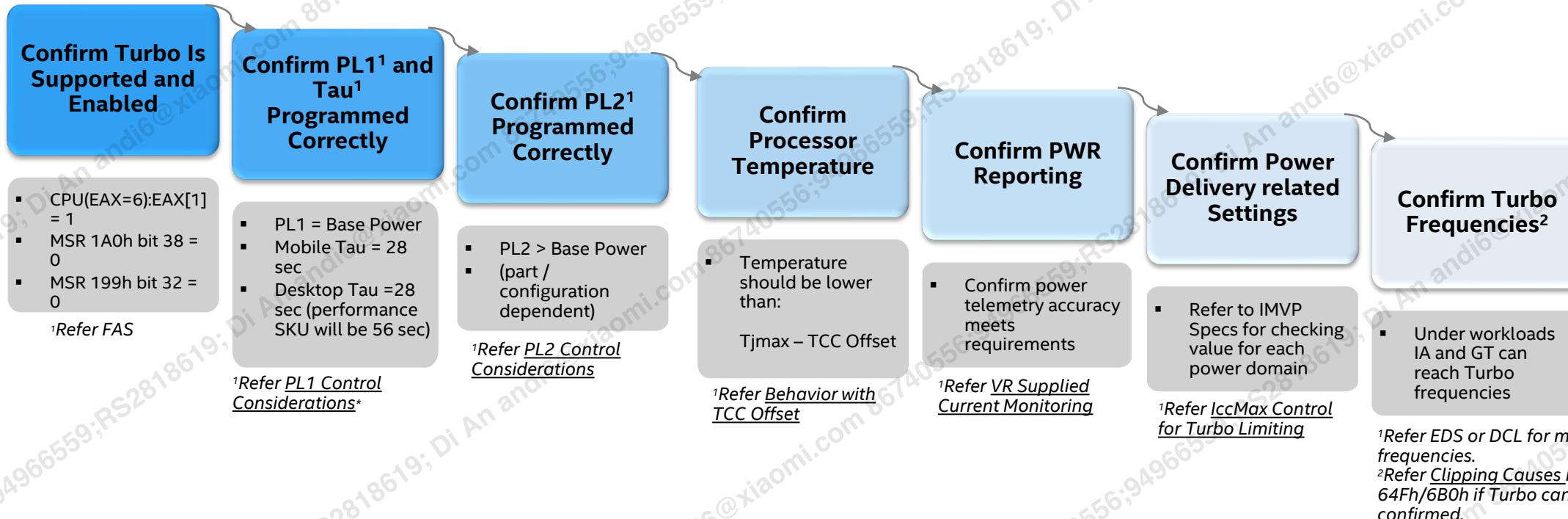
1.3 Objective

- This document provides system development teams a quick start to understanding Intel® Turbo Boost Technology 2.0 for Intel® Core™ based processors.
- This document also provides the system development team deep-level guidance on how to implement Turbo to achieve the best end-user experience.

1.4 Turbo Features

Feature	Description
<u>Intel Speed Shift Technology</u>	Also known as Hardware Controlled P-states. Provides improved performance and battery Life Savings
<u>Psys</u> <u>PsysPL1</u> <u>PsysPL2</u> <u>PsysPL3</u>	Total System Power Based SoC Control Options
<u>VR_TDC/Tau</u>	Per-VR Average Current Limiting Requirement
<u>PL4</u>	SoC Package Level Preemptive Peak Power Limiting Option
<u>VR_Imax</u>	Per-VR Peak Preemptive Current Limiting Option
<u>TCC_Offset</u> <u>Tj_Avg reporting</u>	Peak SoC Temperature Averaging Options
<u>PL4 Platform offset</u>	Additional PL4 Control for external device plug-in events, controlled by EC
<u>PROCHOT# protection for battery system</u>	SoC Package Level Reactive Peak Power Limiting Option

1.5 Turbo Setting Verification Guide



Values shown above are recommended levels; some designs may choose to use other values;

¹Refer to MSR 610h, MMIO 59A0, and PECL Index 26 and Index 27

²Other areas to focus if referring less than expected performance include: PsysPL1, PsysPL2, (Psys)PL3, PL4, VR_TDC

1.6 Turbo Related Parameters

Parameter	Reqd.	Limit Type	Potential Usage
TCC_Offset / Tau	Yes ¹	CPU Average Temperature Limit	Better support for using CPU temperature as proxy for crude skin temperature protection. These parameters may be required for power compliance on certain SKUs (see EDS v1.0)
Tj_Avg/Tau	No	CPU Average Temperature Reporting	Software such as Intel® Dynamic Tuning can base interrupts on Tj_Avg instead of instantaneous Tj
PL1 / Tau	Yes ¹	CPU Average Power Limit (Can be sustained infinitely)	Set to SoC influenced thermal capability (CPU or skin)
PL2	Yes ¹	CPU High Power Limit (Sustained for ~10s of seconds)	Set as high as power delivery and heat pipes can handle
PL3	No	CPU Peak Power Occurrences Limit (duty cycle allowed above PWR threshold)	Set to PL3 = PL2 + 2W ³
PL4/ PL4 platform offset	No	A Preemptive ² CPU Package Peak Power Limit (It will not be exceeded, sustain <10ms)	Set lower as battery drains to prevent going lower than battery min voltage
VR_TDC / Tau	Yes	VR Average per-rail Current Limit (Can be sustained infinitely)	Set to VR sustainable Icc level (TDC) to prevent VR thermal events

¹Only required to be set in MSR.

²A Preemptive limit is a limit that is assured in advance based on estimates of activity, not real-time current measurements. (Ex. A max frequency limit regardless of power/current level consumed).

³Refer to [Slide 5](#) for details.

Threshold Terminology
Average = Long Term (Ex. PL1)
High = Short Term (Ex. PL2)
Peak (Ex. VR_Imax)

1.6 Turbo Related Parameters (Cont.)

Parameter	Reqd.	Limit Type	Potential Usage
VR_Imax	Yes ¹	A Preemptive ² CPU Per-Rail Peak Current Limit (It will not be exceeded)	Set statically to VR rail peak limit; any reduction could limit max frequency
PsysPL1 / Tau *Psys supported charger required.	No	System level Average Power Limit (Can be sustained infinitely)	Set to long term system total thermal capability (for example: Fanless)
PsysPL2 *Psys supported charger required.	No	System level High Power Limit (Sustained for ~10's of seconds)	Set as high as power delivery can sustain such as brick or battery max rating
PsysPL3 *Psys supported charger required.	No	System Peak Power Occurrences Limit (duty cycle allowed above PWR threshold)	Set to PsysPL3 = PsysPL2 + 2W ³

¹ Only required to be set in MSR.

² A Preemptive limit is a limit that is assured in advance based on estimates of activity, not real-time current measurements.

(Example, a max frequency limit regardless of power/current level consumed).

³ Refer to [Slide 5](#) for details.

Threshold Terminology
 Average = Long Term (Ex. PL1)
 High = Short Term (Ex. PL2)
 Peak (Ex. VR_Imax)

1.7 Turbo Related Interfaces

Parameter	Run Time Configurable?	Interfaces ²	BIOS Default ³ / Recommendation
TCC_Offset / Tau	Yes ¹	MSR	0 (Tjmax)
Tj_Avg/Tau	Yes (for Tau only)	PECI, MMIO/MMIO	Tj_Avg is read only, Tau default is 0.
PL1 / Tau	Yes ¹	MSR/(MMIO/PECI for both)	Base Power / 28 seconds (For Mobile and Halo), 8 seconds (For Desktop)
PL2	Yes ¹	MSR/MMIO/PECI	Refer to Platform Design Guide(PDG) for PL2 settings / Consider disabling or setting higher if using PsysPL2, or set to level needed to prevent heat pipe dry-out
PL3	Yes	MSR/PECI	Disable / PL3 = PL2 + 2W ⁵
PL4	Yes	MSR/PECI	Refer to Platform Design Guide(PDG) for PL4 settings/control with Intel® Dynamic Tuning power boss
PL4 platform offset	Yes	PECI	Refer to Slide PL4 platform offset slide
VR_TDC / Tau	No – set at boot	BIOS Mailbox for both	Set to IPL2 or Irsm (Refer to power delivery in PDG chapter for more data)
VR_Imax	No – set at boot	BIOS Mailbox	PCU reads VR IccMax from VR register/VR IccMax capability should meet IccMax spec
PsysPL1 / Tau	Yes	MSR/PECI for both	Disable/Design Dependent
PsysPL2	Yes	MSR/PECI	Disable/AC Brick Rating or Battery Dependent
PsysPL3	Yes	MSR/PECI	Disable/AC Brick and Battery Dependent

¹Only required to be set in MSR

²Subject to change

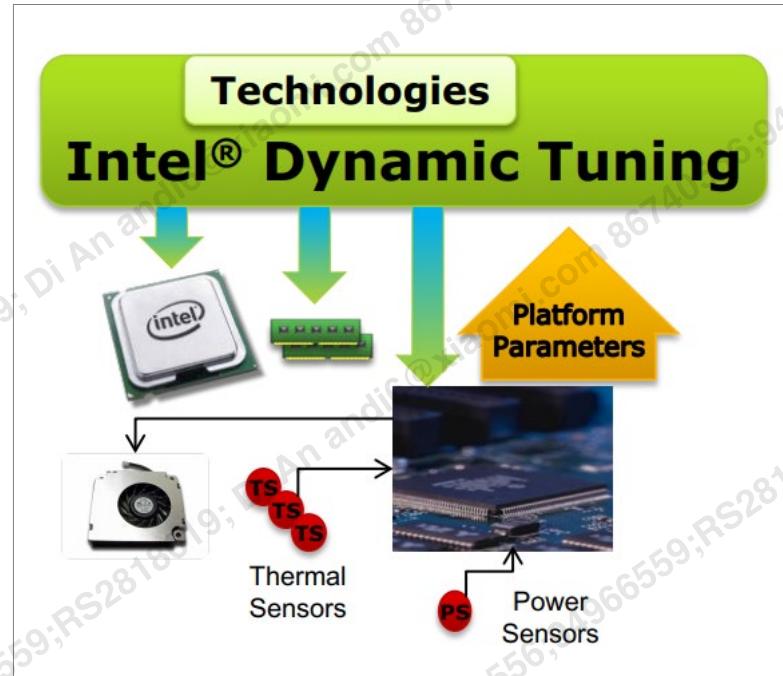
³BIOS default refers to settings in Intel's BIOS reference code

⁴All Tau are different for its associated turbo parameter

⁵See section 5 for details

1.8 Intel® Dynamic Tuning

- Intel® Dynamic Tuning is a software solution for advanced thermal and power management
 - Cross Segment (Ultrabook™, Tablets, and so on) and cross OS (Windows*, Chrome*, Android*)
 - Built on standardized Intel-defined ACPI compliant Dynamic Tuning specification; can also allow OS/App awareness of platform power/thermal conditions
- Intel® Dynamic Tuning Enables Robust Platform Capabilities
 - Highly scalable and configurable solution for optimal power and thermal management
 - More comprehensive platform-level control, based on skin temperature and other inputs
 - Intel® Dynamic Tuning on Raptor Lake extends to cover many of the new control parameters included in this presentation.



Contact Intel® Thermal AE for the latest training material on Intel® Dynamic Tuning

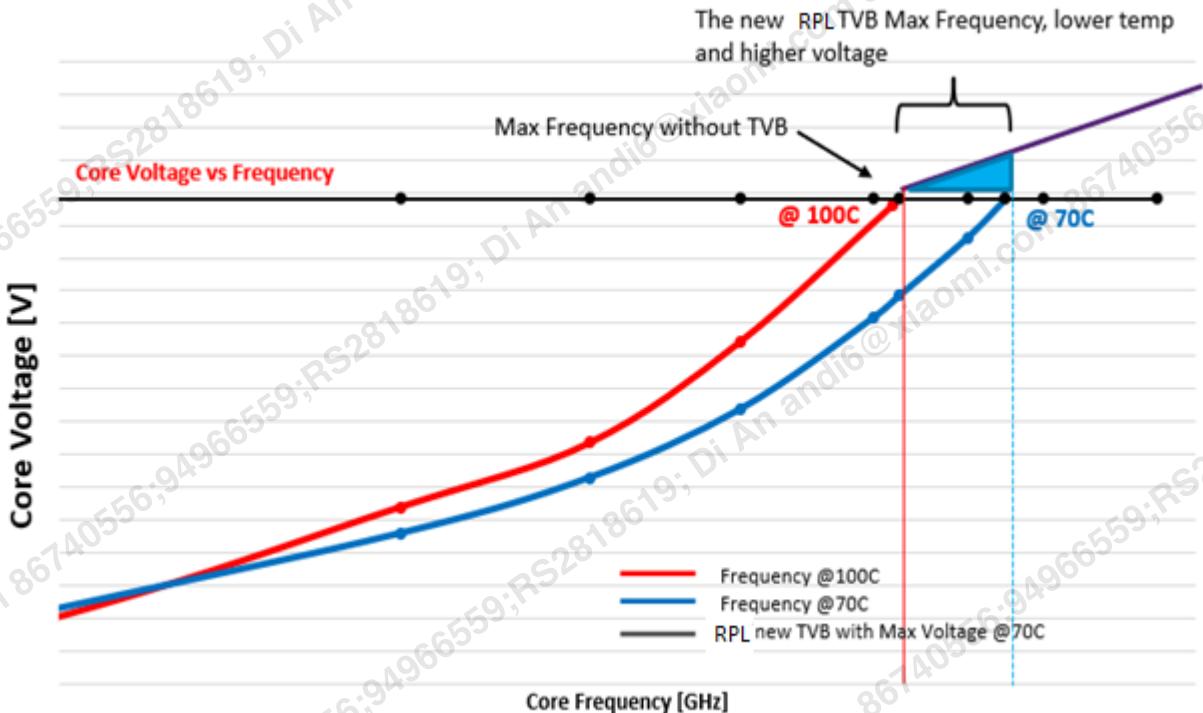
Intel® Dynamic Tuning 8.x BIOS Specification
([541817](#))

Intel® Strongly Recommends Intel® Dynamic Tuning for Adaptive Thermal Management

1.9 Intel® Thermal Velocity Boost (TVB)

Intel® Thermal Velocity Boost (TVB)

- It opportunistically and automatically increases clock frequency above Single-core and Multi-core Intel® Turbo Boost 2.0 Technology frequencies based on how much the processor is operating below its maximum temperature.
- The frequency gain and duration is dependent on the workload, capabilities of the processor and the processor cooling solution.
- For processors that have Intel® Thermal Velocity Boost enabled, the maximum Core Frequency is achieved while the processor is at a temperature of 70°C or lower and turbo power budget is available. Frequencies may reduce over time as processor temperature increases.



NOTE

- Intel® Thermal Velocity Boost (TVB) may not be available on all SKUs.
- TVB opportunistically have higher frequencies than ITMBT3 only for the parts supporting ITMBT3.0 (Intel Turbo Max Boost Technology 3.0)

1.10 Dual Tau – S Sku - Channel Desktop Systems

- Dual Tau is a CML-S and beyond BIOS feature, with the goal to boost performance in Channel Desktop Systems.
- The target audience is the Channel motherboard vendors that :
 - Build the MB for S systems
 - Own the system BIOS for the MB(mother board)
- Dual Tau is being offered as an alternative Performance Boost Option in BIOS for Systems that do not use Intel DTT (DPTF).
 - Intel® DTT (DPTF) is not available to our Channel MB Vendors due to the tuning required in a chassis system.
- Performance Boost 6-7% CineBench20 (MT) on a 125W CML-S RVP System.

1.10.1 Intel® DTT Features - Relevant to Desktops

- The Table below are some features available with DTT relevant to Desktops.
- Use of DTT driver requires system tuning for the various policies.
- Dual Tau provides a conservative Performance Boost, without any additional SW and Tuning

Features (Policies)	RPL-S	Comments
Active 2.0	✓	
Passive 2.0	✓	Performance Boost based on Thermal Sensors on board
Adaptive Performance	✓	OS Game Mode Condition, potential performance boost
Processor (Temperature, power control ⁽¹⁾)	✓	SOC TJ based Performance Boost
Fan (fan speed)	✓	Fan Speed Control
NVMe Storage (Temperature, P-State control)	✓	Under Temperature Threshold support with NVMe 1.3 SPEC.

1.10.2 Dual Tau – Feature Enabling

- The Dual Tau Performance Boost option will be available in BIOS , Disabled by Default.
- When Enabled, MSR & MMIO registers will be initialized with Dual Tau Intel Recommended Values.(examples below)

125W Sku	PL1(W)	PL2(W)	Tau(Secs)
MSR	125	250	224
MMIO	165	250	28

65W Sku	PL1(W)	PL2(W)	Tau(Secs)
MSR	65	224	224
MMIO	85	224	28

35W Sku	PL1(W)	PL2(W)	Tau(Secs)
MSR	35	70	224
MMIO	45	70	28

- Values will depend on the CML-S sku being used and the associated PL values.
 - MMIO PL1 == 1.3 MSR PL1.
 - PL2 (Turbo) Values will not change, same as the default MSR PL2 values
 - MMIO Tau = Default MSR Tau
 - MSR Tau = 224
- When Dual Tau is **Disabled**, the MSR and MMIO registers have the same values (System Default).

125W Sku	PL1(W)	PL2(W)	Tau(Secs)
MSR	125	250	28
MMIO	125	250	28

65W Sku	PL1(W)	PL2(W)	Tau(Secs)
MSR	65	224	28
MMIO	65	224	28

35W Sku	PL1(W)	PL2(W)	Tau(Secs)
MSR	35	70	28
MMIO	35	70	28

Note :Values based on CML S ,maybe changed for RPL-S

1.10.3 Dual Tau : Package Power Details

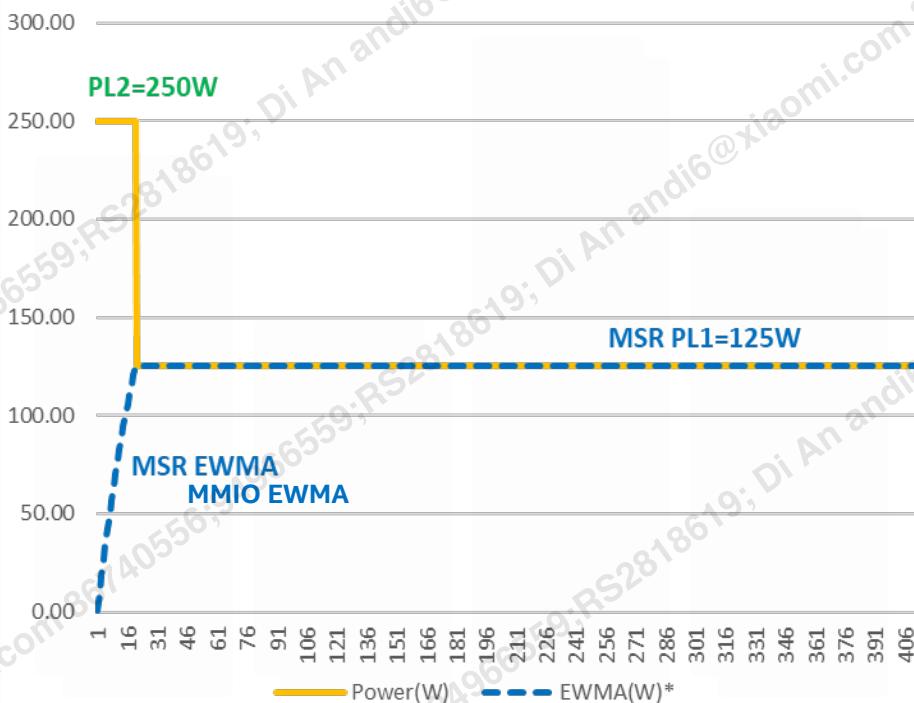
Baseline

125W Sku	PL1	PL2	Tau (secs)
MSR Registers	125W	250W	28
MMIO Registers	125W	250W	28

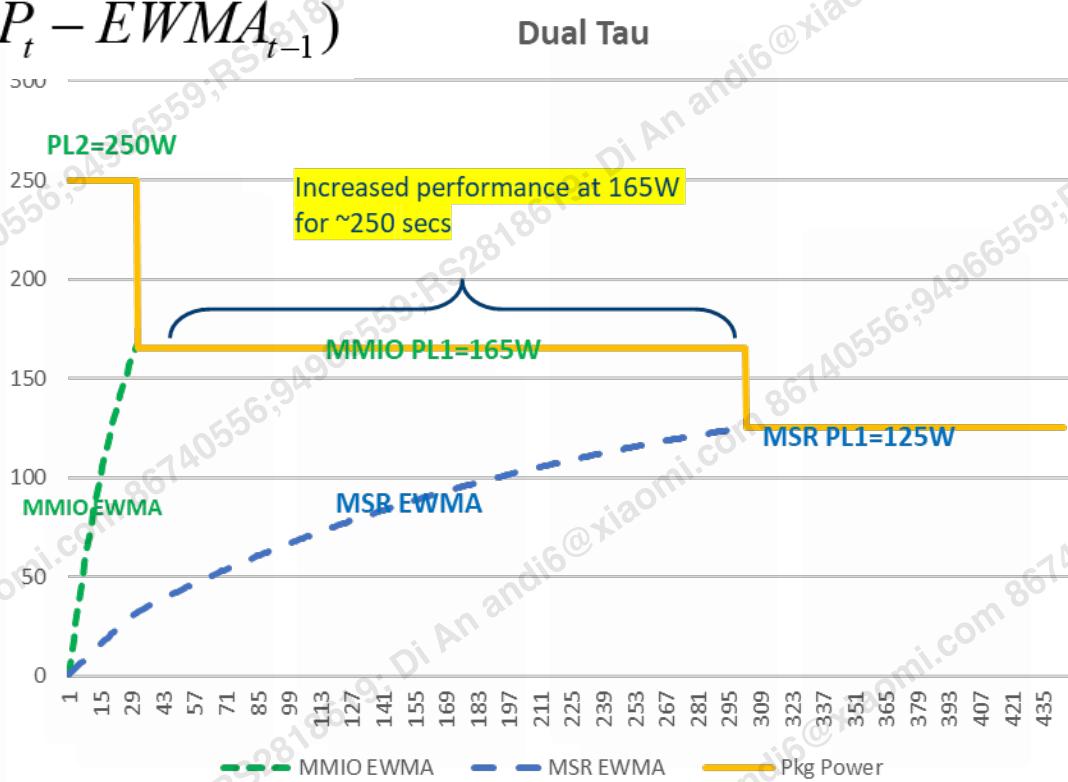
Dual Tau

125W Sku	PL1	PL2	Tau(Secs)
MSR	125W	250W	224
MMIO	165W	250W	28

$$EWMA_t = EWMA_{t-1} + \frac{\Delta t}{\tau} \cdot (P_t - EWMA_{t-1})$$



Note :Values based on CML S.



1.10.4 Dual Tau CML-S 125W Benchmark Gains

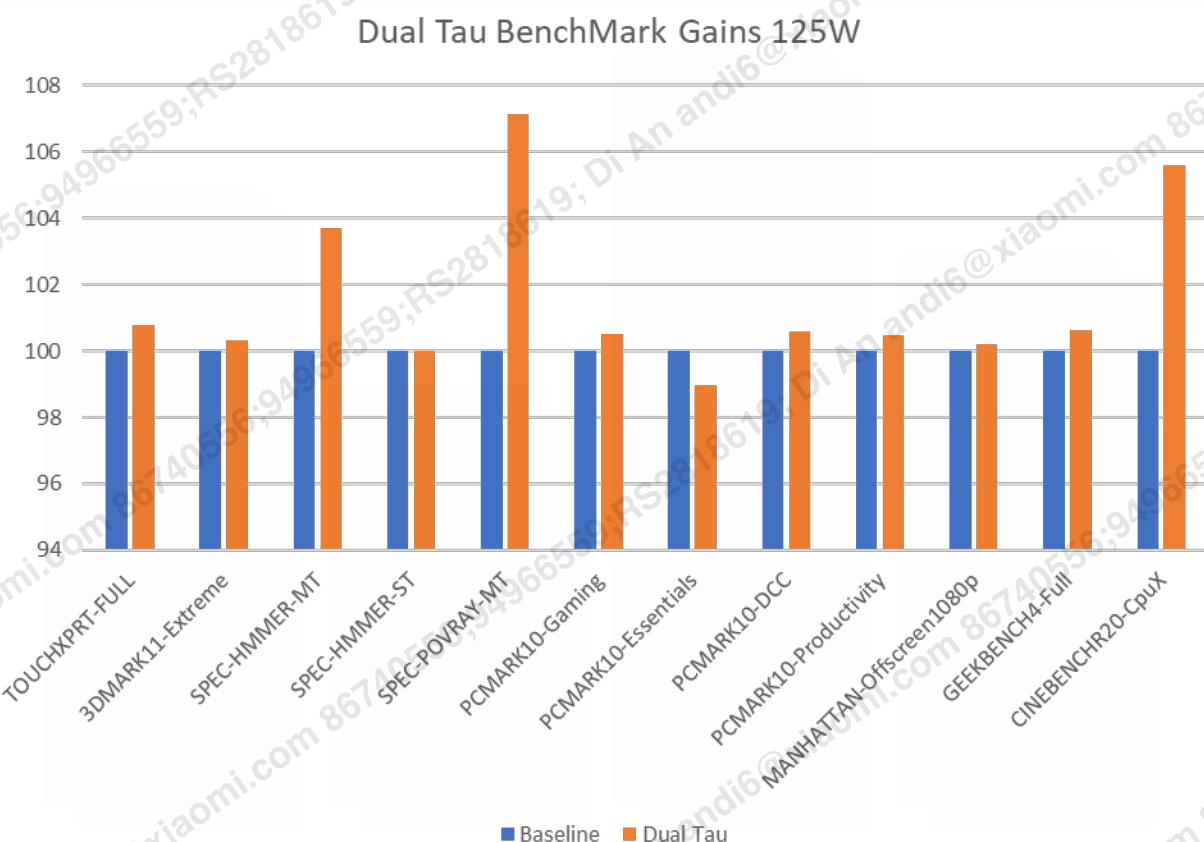
System Configuration:
Intel RVP: CML-S 125W

Baseline

125W Sku	PL1	PL2	Tau (secs)
MSR Registers	125W	250W	28
MMIO Registers	125W	250W	28

Dual Tau

125W Sku	PL1 (W)	PL2(W)	Tau(Secs)
MSR	125W	250W	224
MMIO	165W	250W	28



Notes:

1. Performance benchmarks are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary.
2. Values based on CML S.

1.10.5 Dual Tau CML-S 65W Benchmark Gains

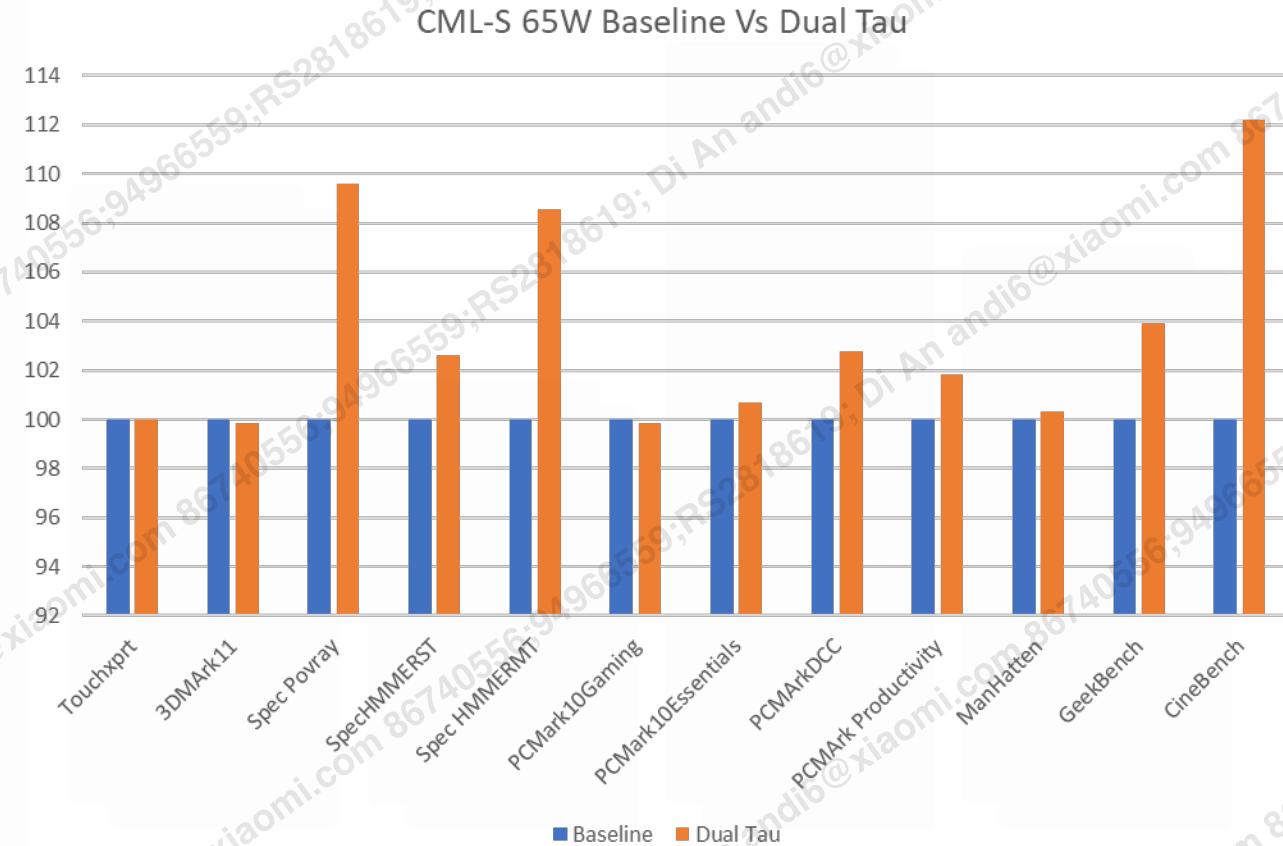
System Configuration:
Intel RVP: CML-S 65W

Baseline

65W Sku	PL1	PL2	Tau (sec)
MSR Registers	65W	224W	28
MMIO Registers	65W	224W	28

Dual Tau

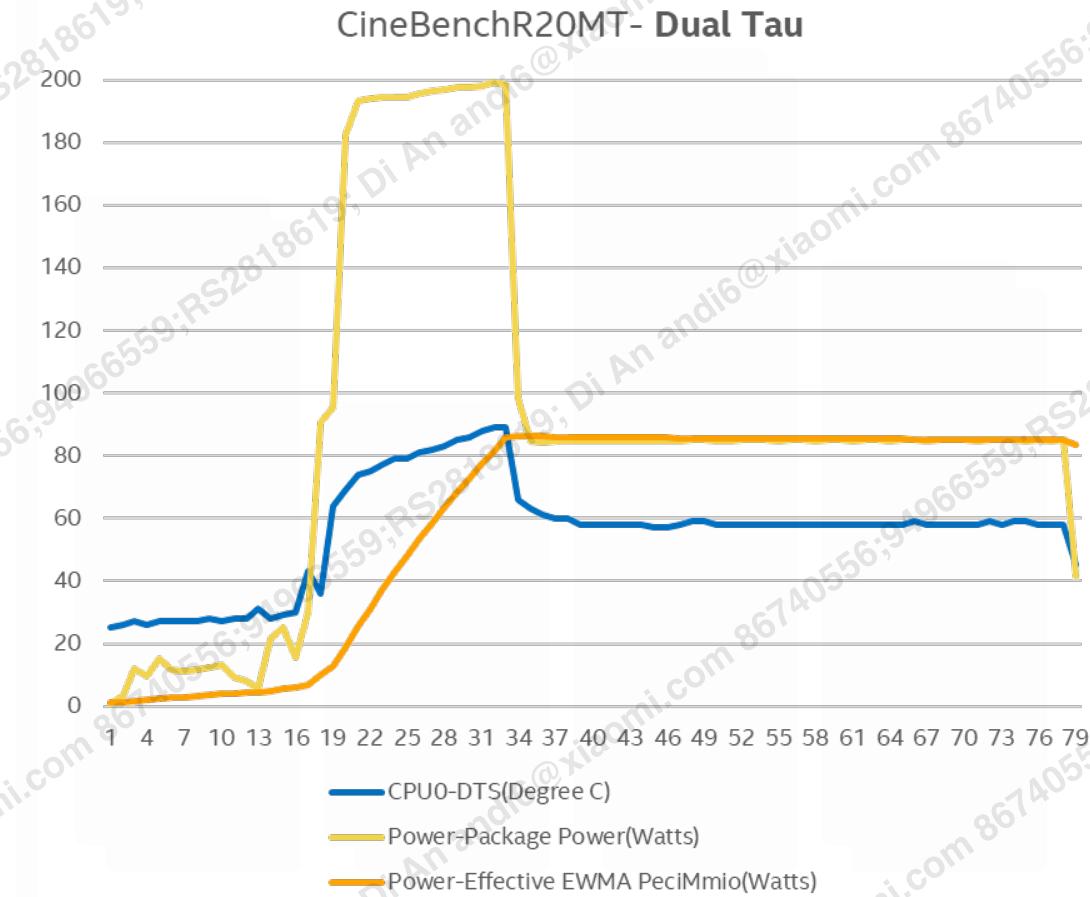
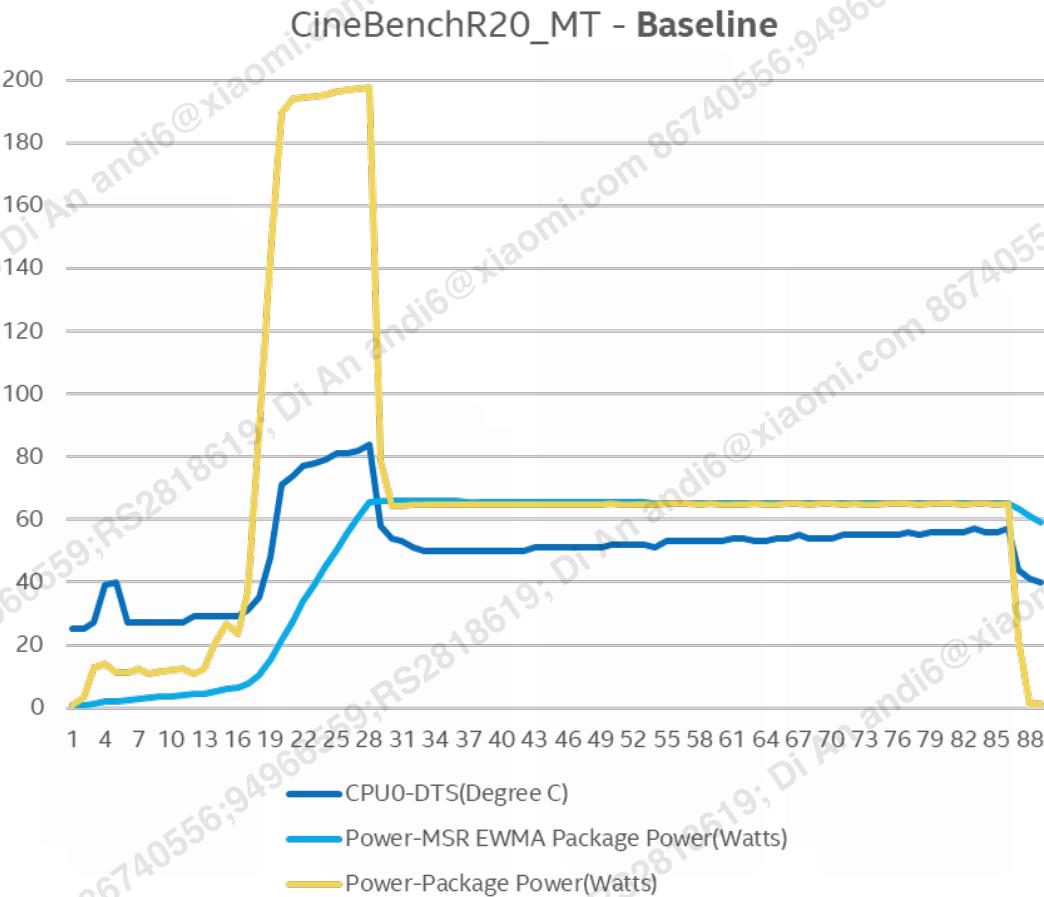
65 W Sku	PL1 (W)	PL2(W)	Tau(Secs)
MSR	65W	224W	224
MMIO	85W	224W	28



Notes:

1. Performance benchmarks are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary.
2. Values based on CML S.

1.1.6 CinebenchR20-MT – 65W Sku Baseline VS Dual Tau



Note: Values based on CML S.

1.11 Intel® Turbo Boost Maximum Technology 3.0

- Intel® Turbo Boost Maximum Technology 3.0, also known as ITBMT 3.0, allows the Operating System (Windows* 10 RS1 or newer) to take advantage of the maximum turbo frequency of each individual core of the processor. In this state, a specific processor core running a workload runs at a higher frequency than the marked maximum turbo frequency of the processor package.
- Individual asymmetric core maximum frequency information is exposed to the operating system via ACPI 5.1 (or newer) Collaborative Processor Performance Control (CPPC2) interface.
- The general value proposition for ITBMT 3.0 is the performance benefit delivered by exposing all cores' native frequency capability instead of limiting the top-end performance of all cores to that of the lowest performance core.
- ITBMT 3.0 performance benefit is most visible in low (1-2) thread count workloads. Highly threaded workloads do not benefit from ITBMT 3.0.

Notes:

- The Logical Core IDs of the faster cores are sample specific.
- All samples within a SKU (SSPEC/QDF) have the same per-core frequencies (in different Cores).
- This document does not list performance numbers.

1.11.1 Power and Thermal Validation

- ITBMT 3.0 enables 1-2 cores to run at higher frequency than other cores. The higher frequency is achievable only if the other cores are not in active (Core C6 state).
- The faster cores are chosen during manufacturing so that they do not require more voltage or power than the slower cores while operating at higher frequency.
- In other words, ITBMT 3.0 does not require any changes to power delivery, cooling solution, etc.,
- No additional checks are required with respect to power and thermal validation.

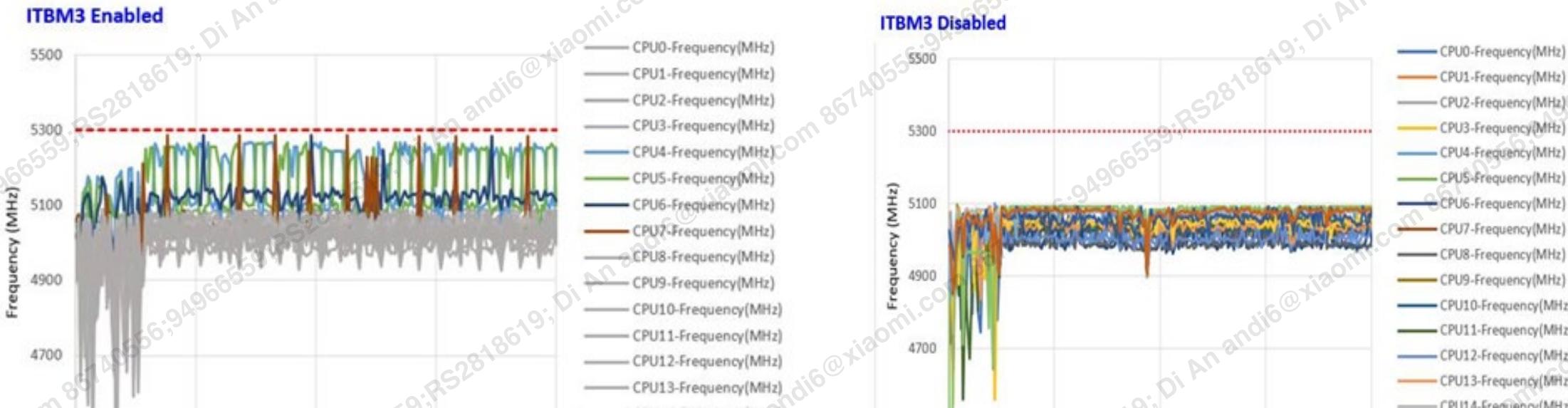
Note: The Core ID of the faster cores is not fixed within a SKU. The faster cores' IDs are sample specific. Refer to Comet Lake Platform Intel® Turbo Boost Max Technology 3.0 Technical Advisory ([621487](#)) for more information.

1.11.2 Intel® Turbo Boost Maximum Validation Guidance

To capture ITBM 3.0 higher frequencies, run one of the options:

- Run Thermal Analysis Tool (TAT) with log capture.
- Run Cinebench R15/R20 single threaded or any other single threaded workload like SPEC (ST).
- View the log generated by TAT as shown below:

CML-S RVP with Core i9-10900K Example:



Note: For more ITBMT 3.0 information, refer to Comet Lake Platform Intel® Turbo Boost Max Technology 3.0 Technical Advisory ([621487](#)).

1.12 Intel® Performance Hybrid Architecture

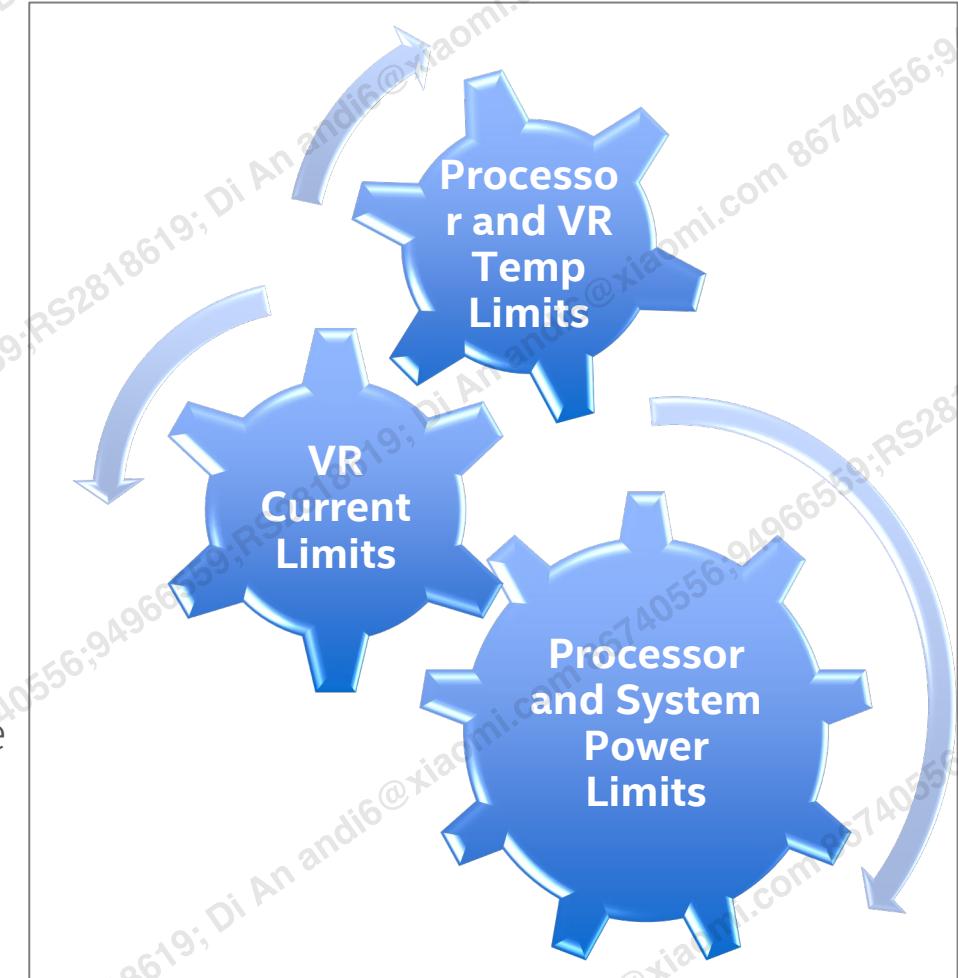
- The processor contains two types of cores, denoted as P-Cores and E-Cores (P core is a Performance core and E core is efficient core).
- The P-Cores and E-Cores share the same instruction set and model specific registers (MSRs).
- The available instruction sets, when hybrid computing is enabled, is limited compared to the instruction sets available to P-Cores.
- P core and E core frequency's will be determined by the processor algorithmic, to maximize performance and power optimization.
- Hybrid Computing may not be available on all SKUs.
- For more details, refer to: <https://www.intel.com/content/www/us/en/developer/articles/technical/hybrid-architecture.html>

2.0 Turbo Concepts

- 2.1 Intel® Turbo Boost Technology 2.0 Parameters
- 2.2 Turbo Power Budget Concept
- 2.3 Key Turbo Power Limits
- 2.4 Turbo Thermal Capacitance Model
- 2.5 Simplistic Heavy Power Scenario with Turbo
- 2.6 SoC Manages to Most Restrictive Constraint
- 2.7 Control Parameter Design Choices Examples
- 2.8 Turbo Parameters
- 2.9 Tau Effect on 'Time Above PL1'
- 2.10 Starting Condition Effect on 'Time Above PL1'
- 2.11 PL2 Effect on 'Time Above PL1'
- 2.12 Real Turbo Example Logged from Heavy Workload
- 2.13 Intel® Speed Shift Technology

2.1 Intel® Turbo Boost Technology 2.0 Parameters

- The Intel® Turbo Boost Technology provides sophisticated configuration to maximize Turbo performance within platform limitations.
- Turbo utilizes inherent thermal capacitance by running at higher power until power or thermal limits are reached, thereby maximizing performance.
- System designers have multiple ways to specify limits for temperature, current, and power for the system, processor, or VR.
- Some turbo parameters can be dynamically tuned during runtime to account for cooling requirements.
- Additionally, there are sophisticated controls available via multiple HW and SW interfaces.



Turbo automatically manages temperature and power constraints.

2.2 Turbo Power Budget Concept

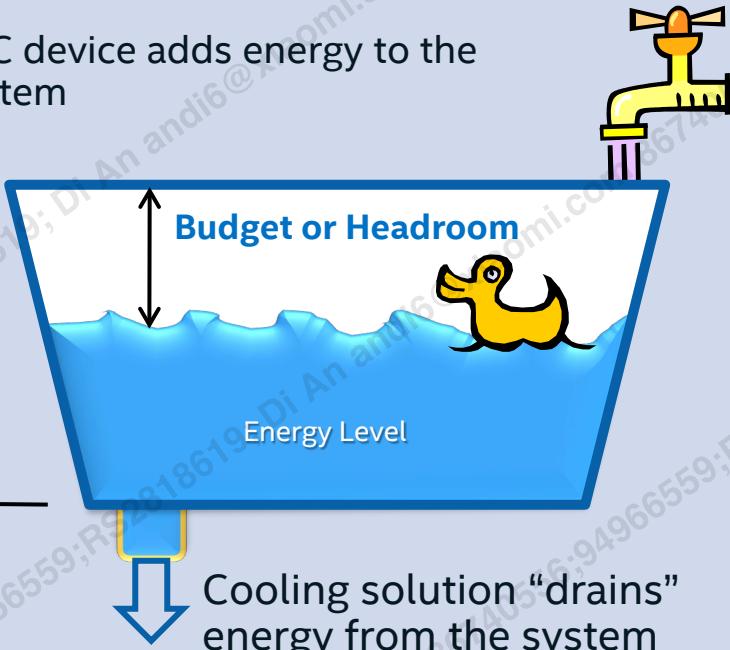
Bathtub Model

- Flow from the faucet (SoC power) can exceed drain flow (Thermal solution capability) if the bathtub (Energy or Temperature) is not full (At energy capacity limits) for a short time (Depending on capacity, level and flow)

Implications

- Processor can safely operate > Base Power for short periods without exceeding package thermal specifications
- There is more power headroom for Turbo when system has been at low power for a while (tub level is low)
- There is Less power headroom for Turbo if system has been running at high power without a rest (tub level is high)
- Better cooling solutions help provide turbo head room quicker (bigger drain in tub)

SoC device adds energy to the system



Power Budget Management and the Turbo Algorithm allow for bursts of power above the Processor Base Power (TDP) level for maximum performance when thermal headroom exists

2.3 Key Turbo Power Limits

- Power Limit 1 (PL1)

A threshold that average power will not exceed - recommend to set equal to Base Power. PL1 must not be set higher than thermal solution cooling limits

- Power Limit 2 (PL2)

A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2

- PL1 Tau

A weighting constant used in the EWMA (exponentially weighted moving average) power averaging calculations to support PL1 limit checking described above

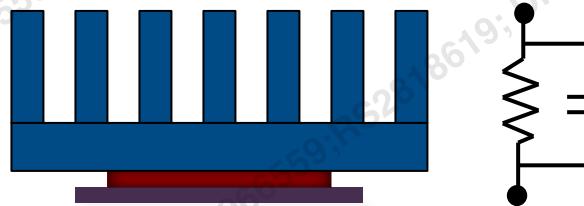
$$Budget_t = PL1 - EWMA_t$$

$$EWMA_t = EWMA_{t-1} + \frac{\Delta t}{\tau} \cdot (P_t - EWMA_{t-1})$$

Number shown in gauge is an arbitrary counter for concept explanation. Power can exceed PL2 for a short amount of time no greater than 10 ms, within which PL2 could reach power level corresponding to IccMax. EWMA formula shown for average power is a simplistic representation of the actual formula used that closely approximates the expected behavior.



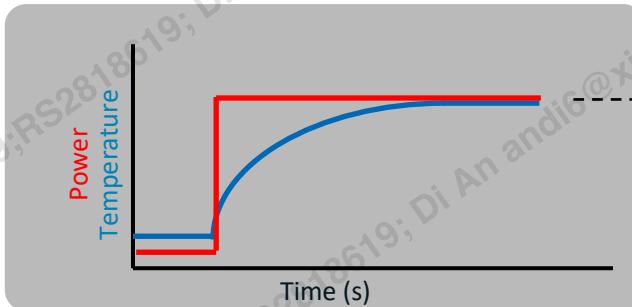
2.4 Turbo Thermal Capacitance Model



Temperature rises as energy is stored in the thermal solution

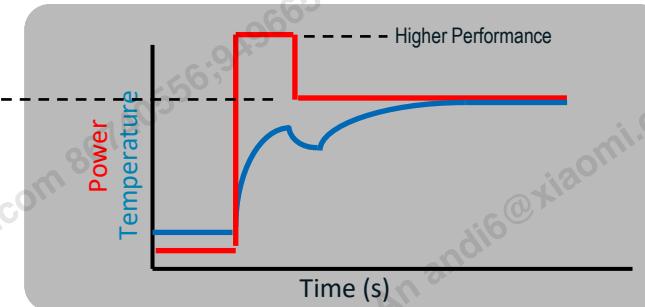
Classic Thermal Design Model

Assumes Constant base power



Turbo Design Model

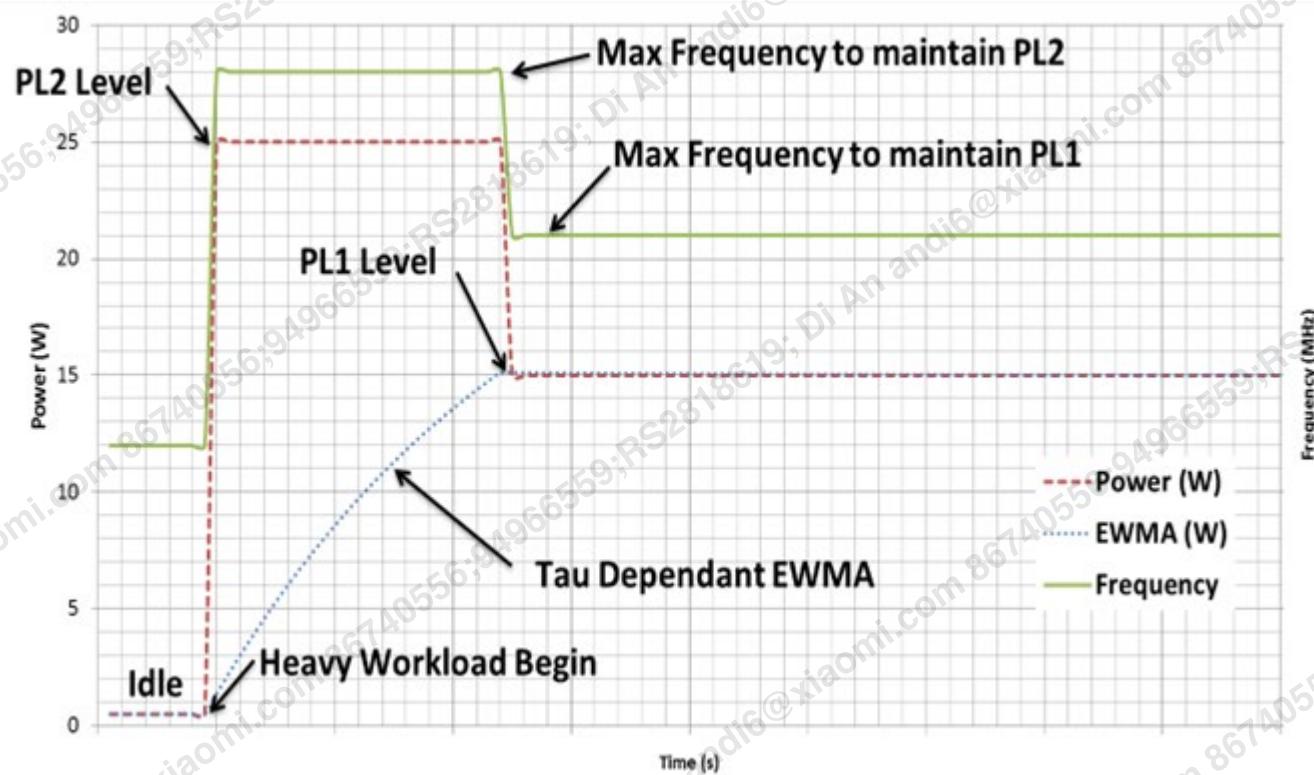
Utilizes Thermal Latency for Improved Performance



Turbo utilizes available thermal capacitance without the need to increase base power

2.5 Simplistic Heavy Power Scenario with Turbo

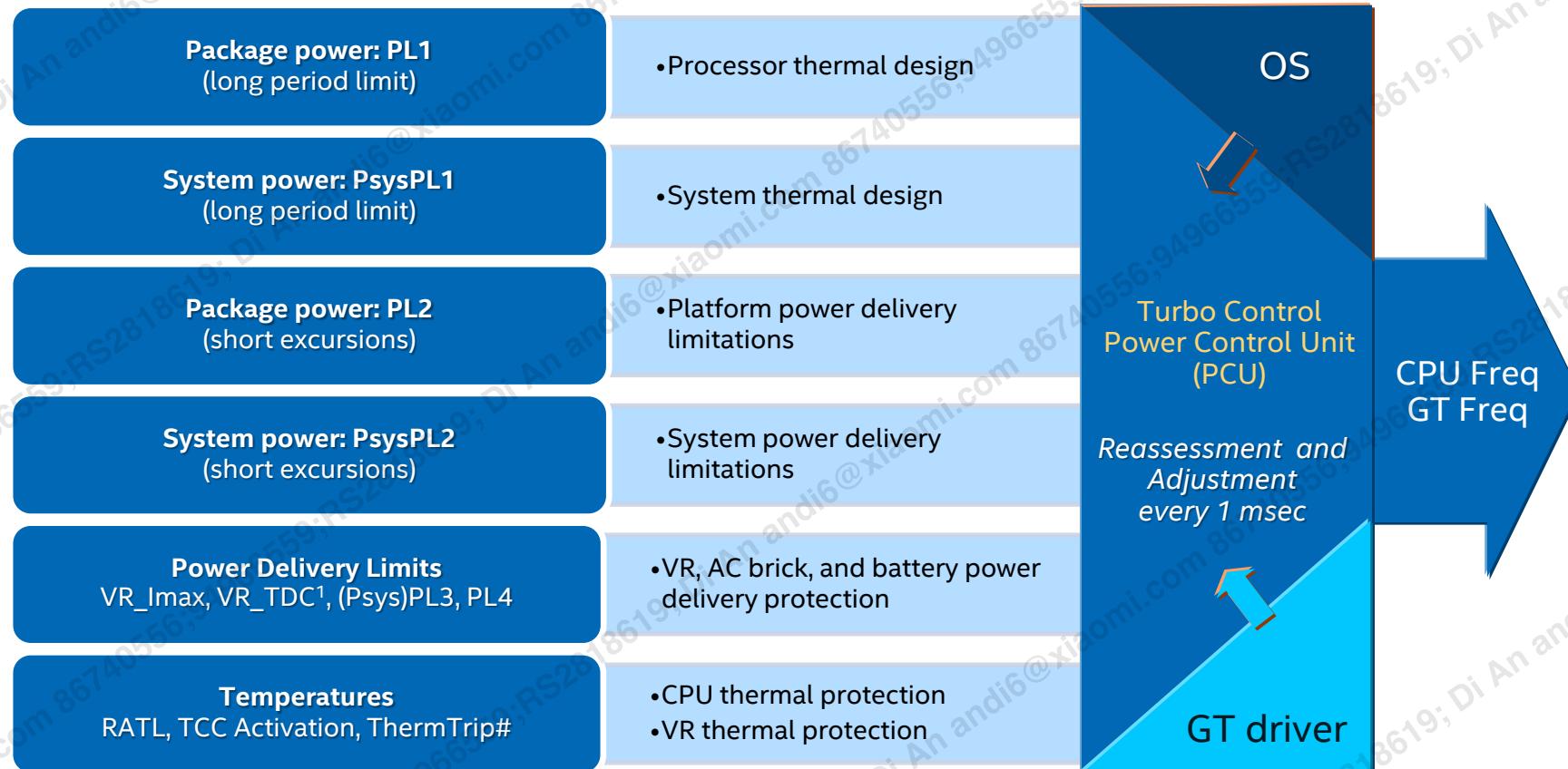
- Maximum operating frequency can be limited by application power consumption:
 - At ~10 seconds a heavy workload begins.
 - Since the system has been idling for a long time, EWMA is approximately equal to idle power, indicating that the available turbo budget is at maximum; so “turbo” adjusts the SoC frequencies to those that will not exceed PL2.
 - EWMA rises while SoC operates at the PL2 power. (Refer the blue dotted line).
 - When EWMA eventually reaches the PL1 level, the turbo “budget” is exhausted so the frequency is turned down to a level that will run at a PL1 power level.



When EWMA reaches PL1, frequency, and power reduced to maintain limit.

2.6 SoC Manages to Most Restrictive Constraint

Intel® Core Processors provide sophisticated control and input parameters to maximize Turbo performance within platform limitations.



¹: Refer to Power Delivery chapter in Alder Lake S Platform Design Guide ([619508](#)) for more data

2.7 Control Parameter Design Choices Examples

'Out of Box'
Simplistic Settings

Simplistic Design Choice

PL1 – Set at Default¹

PL2 – Set at Default¹

PL4 – Set at Default¹

VR_Imax – Set at Default⁴

Risk: Assumes system and component design supports specified thermal and power design specifications



System Limitation Aware
Settings

Optimized Design² Choice

PL1 – Set as high as PL2 level

PsysPL1 – Set for system thermal limit

TCC_Offset – Tcc_offset /Tau optional³

PL2 – Set for heat pipe limit

VR_TDC – Set for VR thermal limit

PsysPL2 – Set for brick and battery rating limit

VR_Imax – Set at Defaults¹ or design limit

PsysPL3 – Set for battery or brick limit

PL4 – Set for battery or brick limit

PL4 offset – Set for ROP power changes

Intel® Dynamic Tuning – Tuned for system design

System Designer has Full Flexibility in Design Choices

¹ Silicon or BIOS reference code defaults.

² Optimized and preferred thermal management design uses Intel® Dynamic Tuning or dynamic modulation of many of these settings.

³ For performance optimized systems, Intel recommends usage of skin thermal sensors instead of using Tj temperature.

⁴ VR controller IccMax capability default.

2.8 Turbo Parameters

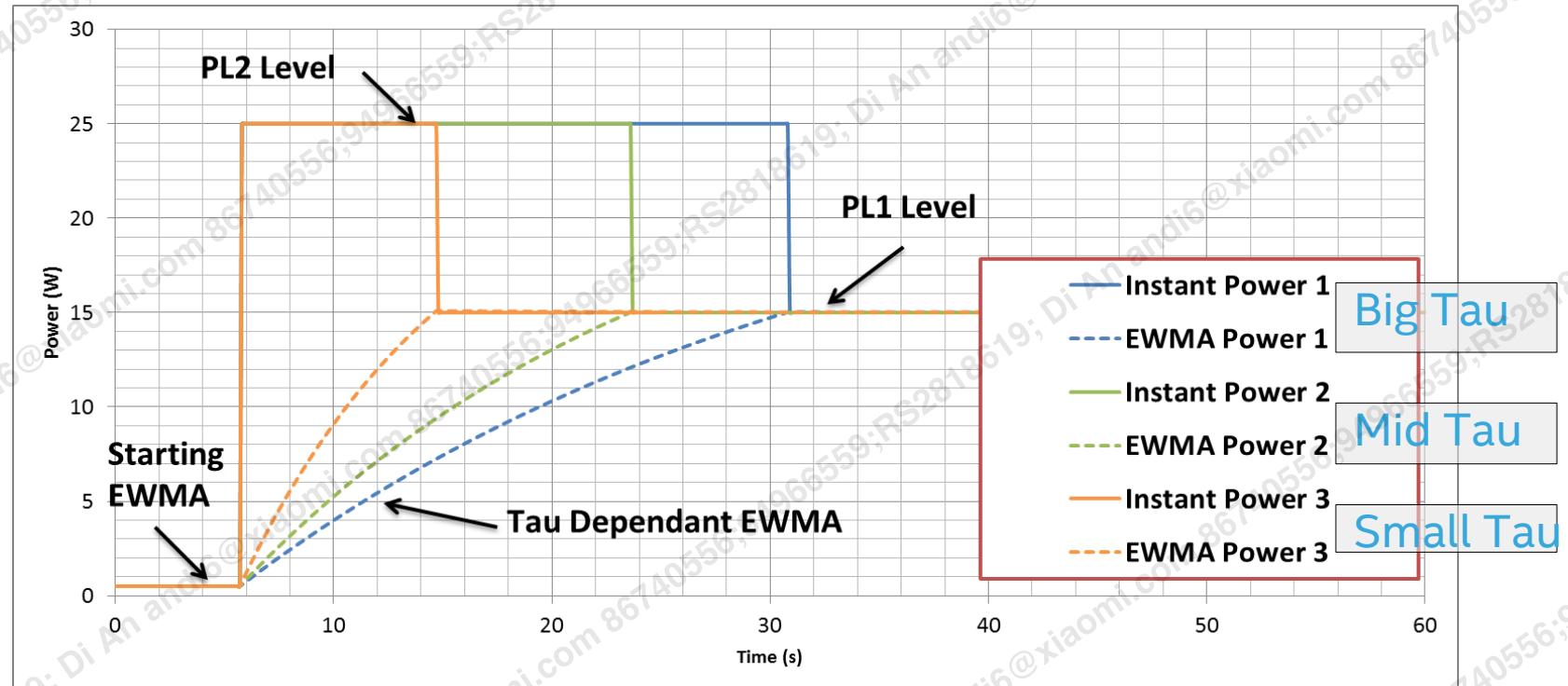
- Many factors influence maximum Time Above PL1:

- Tau parameter
- Energy state at start of workload
- PL1 and PL2 thresholds
- Workload duration and characteristics
- Temperature

Tau is not the only parameter limiting time above PL1

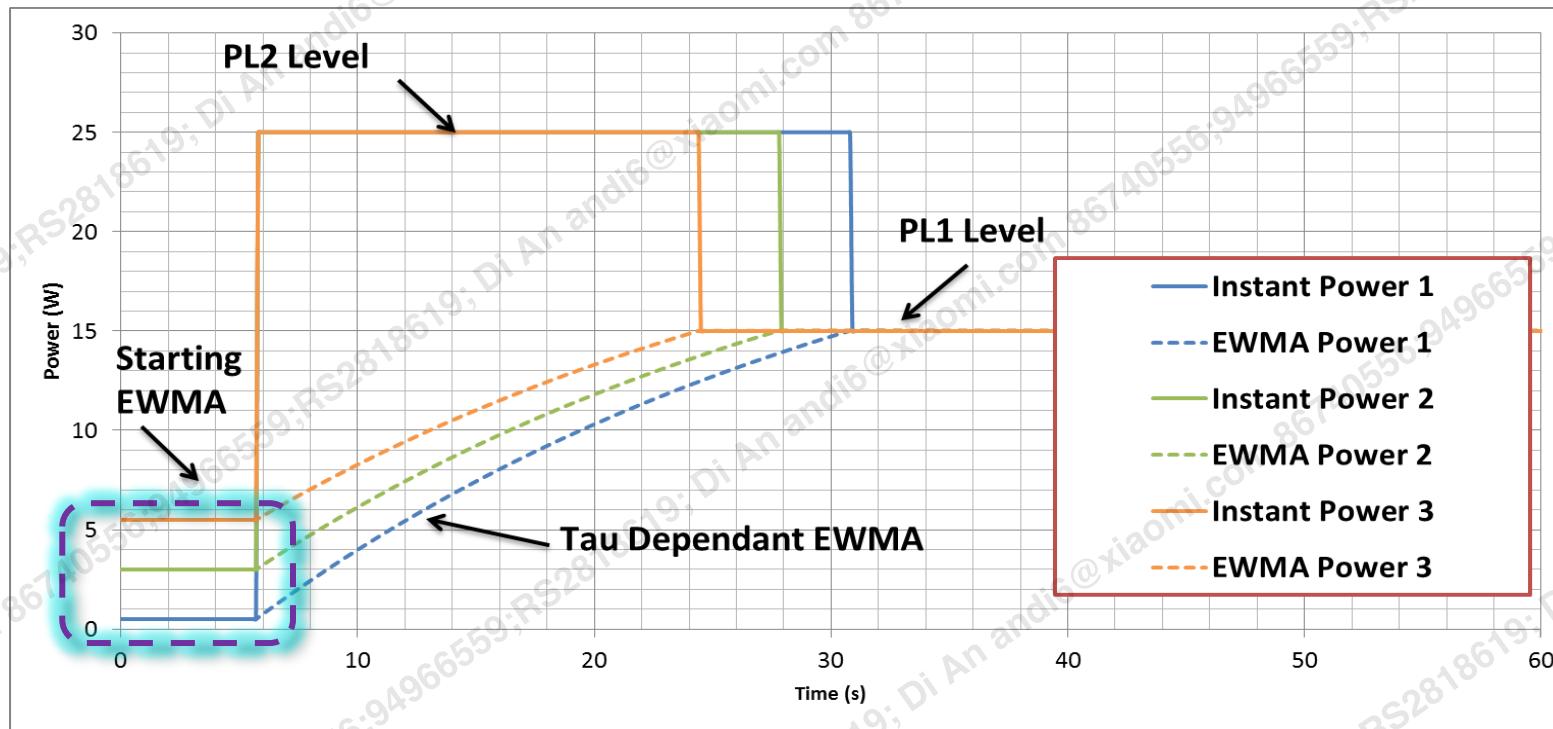
2.9 Tau Effect on ‘Time Above PL1’

- Time above PL1- Tau Dependency:
 - Tau parameter is used as constant in EWMA power calculation.
 - As soon as EWMA power approaches PL1, Turbo is reduced.
 - Shorter Tau parameter will cause EWMA power to ramp faster.
 - Larger Tau parameter will cause EWMA power to ramp slower.



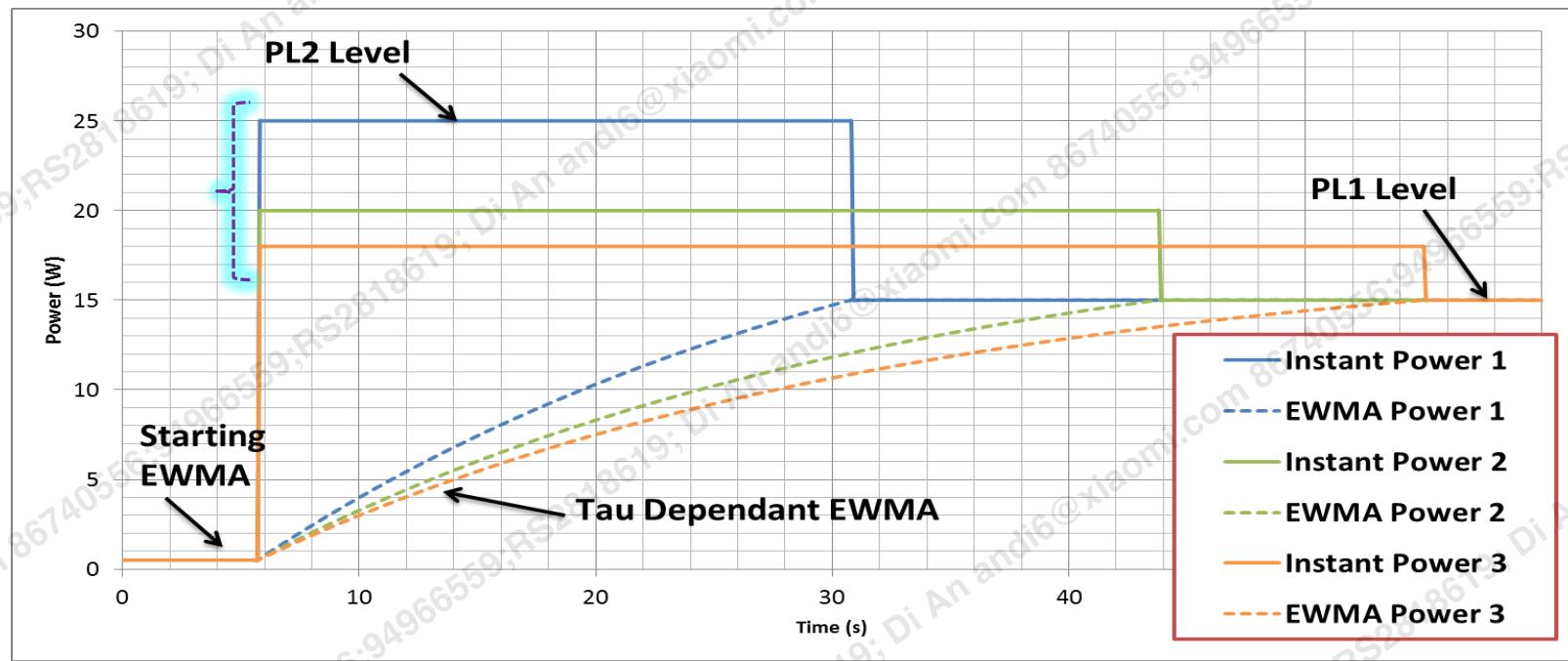
2.10 Starting Condition Effect on 'Time Above PL1'

- Time Above PL1- Start Condition Dependency:
 - Average power before workload begins will affect the max time above base power.
 - As soon as EWMA power reaches PL1, Turbo is reduced.

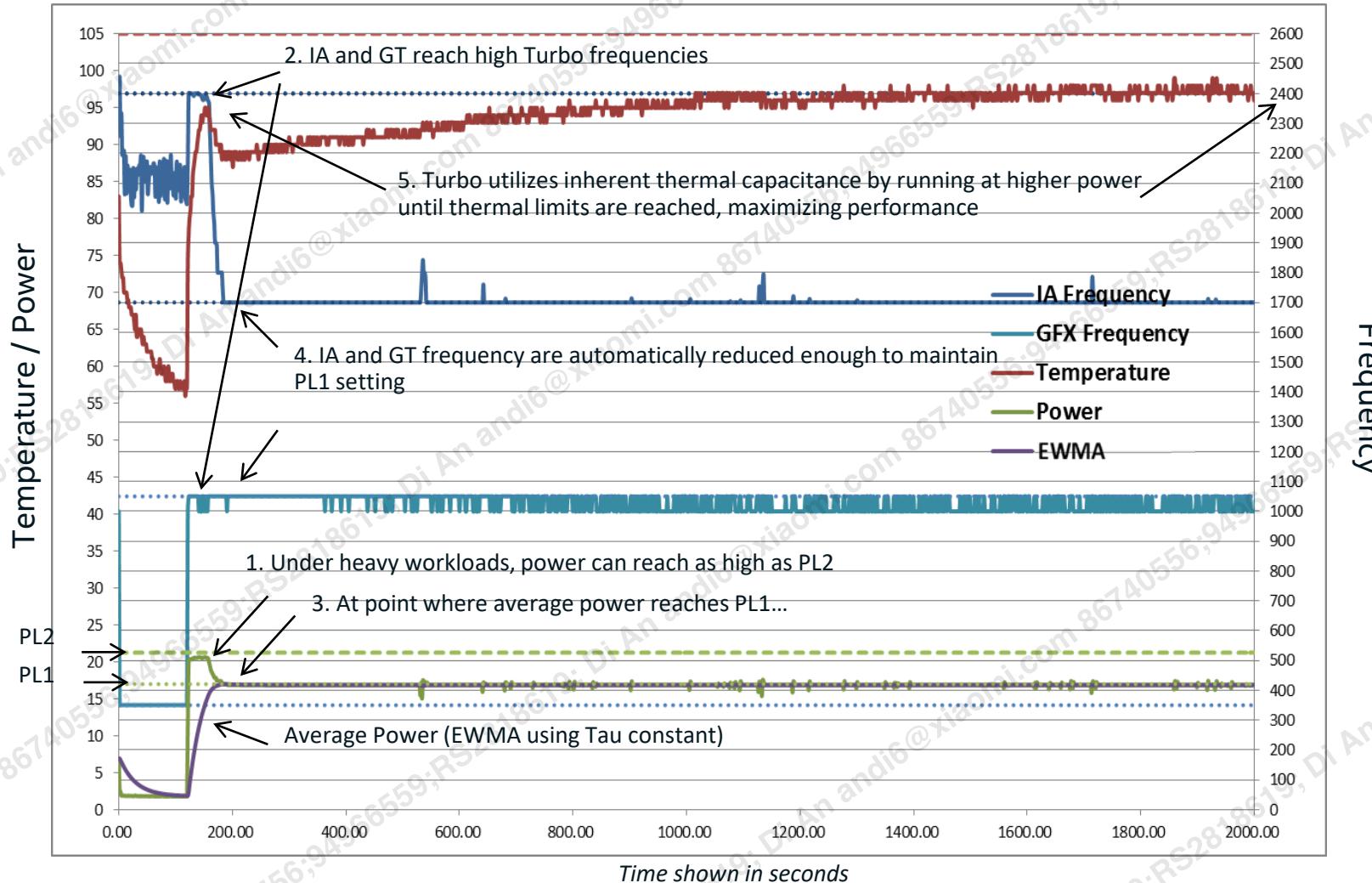


2.11 PL2 Effect on 'Time Above PL1'

- Time Above PL1- PL2 Dependency
- PL2 acts as a cap to maximize power level. As soon as power reaches PL2, Turbo is reduced (explanation in future foils).
- Lower PL2 or lighter workload can allow system to stay above base power for longer.



2.12 Real Turbo Example Logged from Heavy Workload



2.13 Intel® Speed Shift Technology

- What is Intel® Speed Shift Technology?
 - Also known as Hardware-controlled P-states (HWP), these are energy efficient methods of frequency control done by the SoC rather than by relying on OS control.
 - HWP is a hardware implementation of the ACPI defined Collaborative Processor Performance Control (CPPC2).
- What does Intel® Speed Shift Technology do?
 - Improves energy efficiency and performance, increases battery life.
- What is required to use Intel® Speed Shift Technology?
 - Windows* 10 will support natively.
 - Windows* 7-based systems only support legacy P-state control.

3.0 Introduction to Power Limits

3.1	Introduction	3.5	Power Limit 4 (PL4)
3.2	Power Limit 1 (PL1) <ul style="list-style-type: none">3.2.1 Processor Power Budget Management (PBM) Energy Tracking3.2.2 Calculating Budget at Each Time Step3.2.3 Estimated EWMA Calculation Example3.2.4 Turbo Budget Consumption Example3.2.5 Tau Considerations for PL1 and PsysPL13.2.6 PL1-Resulting Frequency Considerations	3.5.1 PL4-Terminology	
3.3	Power Limit 2 (PL2) <ul style="list-style-type: none">3.3.1 PL2 in Action	3.5.2 PL4 Control – SoC Peak Power Limiter	
3.4	Power Limit 3 (PL3) <ul style="list-style-type: none">3.4.1 PL3 Recommendations3.4.2 PL3/PsysPL3-Programming	3.5.3 PL4-Limitations	
		3.6	Power of system <ul style="list-style-type: none">3.6.1 PsysPL1 and PsysPL2 Introduction (Optional – Requires Psys Support)3.6.2 PL2 vs. PsysPL2 Usage Benefit Example3.6.3 PsysPL3
		3.7	Skin Temperature <ul style="list-style-type: none">3.7.1 Skin Temperature Based PL1/PsysPL1 Control3.7.2 Skin Thermal Sensor Options3.7.3 Skin Temperature Monitor and Control via PL1

3.1 Introduction

- Intel® Core processors provide sophisticated controls and input parameters to maximize Turbo performance within platform limitations.
- The following slides will cover:
 - Power limit controls
 - Thermally relevant controls
 - Power-delivery relevant controls

3.2 Power Limit 1 (PL1)

- Power limit 1 can be described as a threshold above which the average power will not exceed.
- Recommended to set to equal base power.
- PL1 must not be set higher than thermal solution cooling limits.

3.2.1 Processor Power Budget Management (PBM) Energy Tracking

Basics:

- Power must be managed to a limit set in PL1 or PsysPL1 (Processor Base Power (TDP), for example).
- Power = Energy/Time
- Energy is measured by using Iout and architectural counters and checked every 1 ms for both the SoC and platform.

Solution:

- PBM calculates average power using an “Exponentially Weighted Moving Average” (EWMA) algorithm.
- Adds energy accumulated to EWMA calculation every 1 ms.
- Time constant can be reduced/increased as necessary for OEMs to match chassis design characteristics and performance tradeoffs.

3.2.2 Calculating Budget at Each Time Step

- For each time step, the Budget can be calculated based on the following equation:

$$\text{Budget}_t = PL1 - EWMA_t$$

- Where the exponentially weighted moving average (EMWA) is:

$$EWMA_t = EWMA_{t-1} + \frac{\Delta t}{\tau} \cdot (P_t - EWMA_{t-1})$$

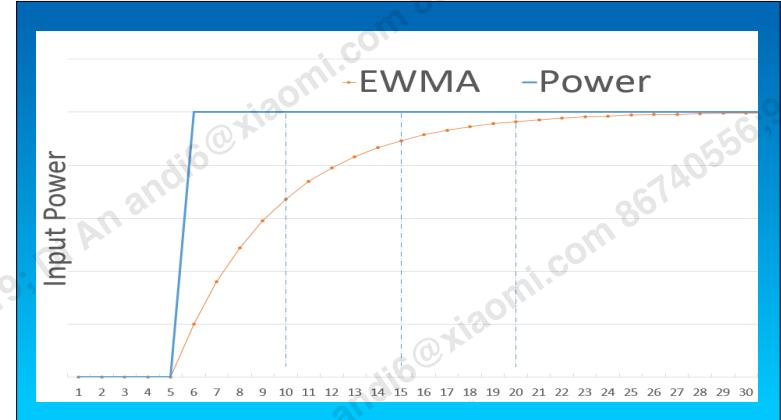
- P_t is the power consumed at that time step, Δt is the time step (can vary in a TAT data file), and Tau is the input to the Turbo algorithm (default is 28 seconds for mobile and 8 seconds for desktop).

- The initial value of EWMA is the idle power consumed by the package once thermal equilibrium is reached:

$$EWMA_0 = P_{idle}$$

- In TAT, the appropriate power to use is the total package power, "Thermal-Info-Package Power(Watts)". Idle power should be recorded after a thermal equilibrium, after a soak of up to 30 minutes.

Note: EWMA formula shown for average power is a simplistic representation of the actual formula used that closely approximates the expected behavior



Example of how EWMA changes relative to a step input in power

3.2.3 Estimated EWMA Calculation Example

- Log power from TAT and use formula from previous slide for calculating an EWMA.

Example

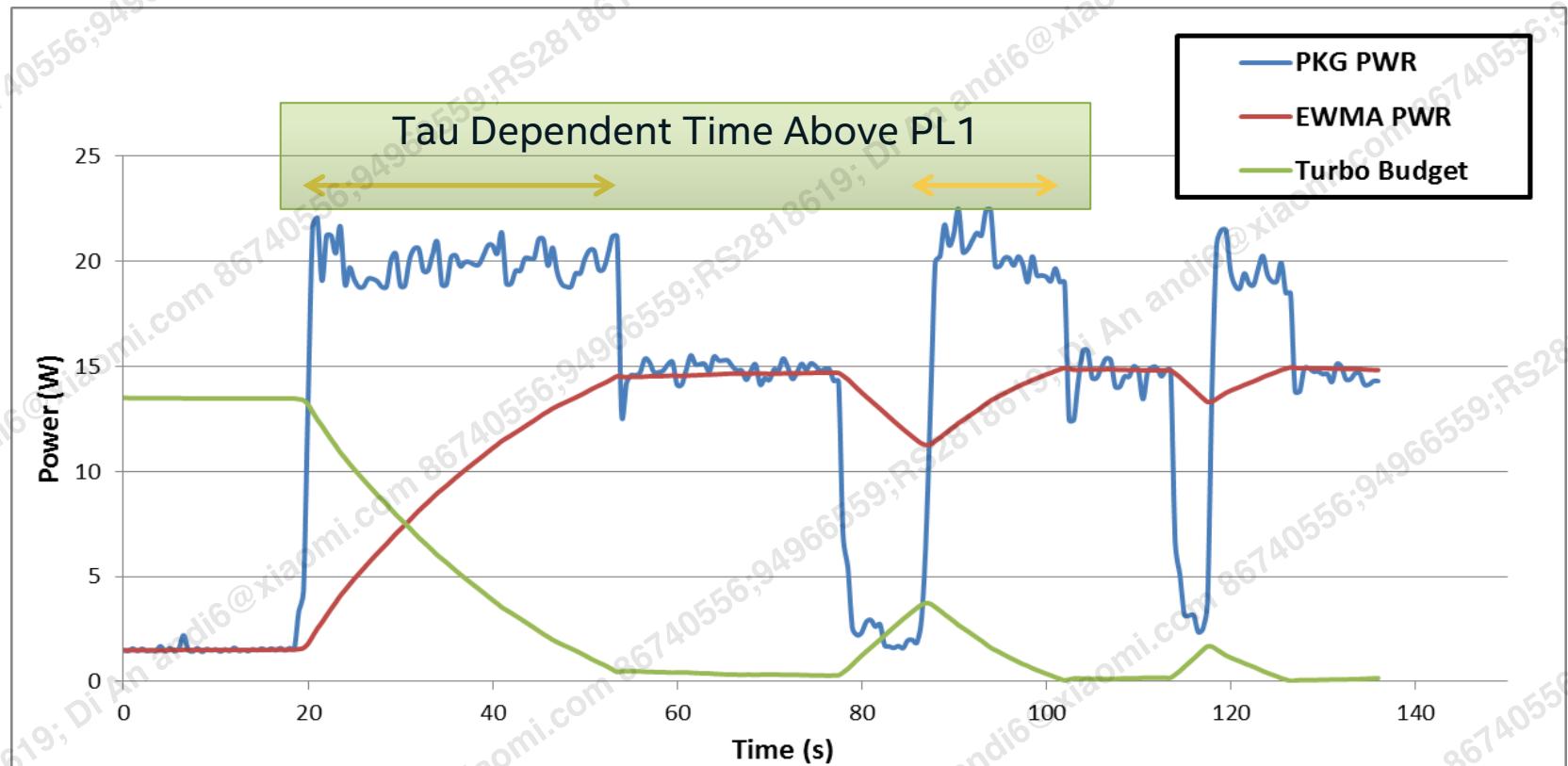
	P_t (Instant Power)	Δt Sample Period (1 sec shown - default TAT value may be different)	τ (28 seconds)	$EWMA_t = EWMA_{t-1} + \frac{\Delta t}{\tau} \cdot (P_t - EWMA_{t-1})$
C3		=C2+(1/28)*(B3-C2)		
A	Time (sec)	Thermal-Info- Package Power(Watts)	C	
1	0	9.81	EWMA	
2	1	13.76	9.81	
3	2	35.43	9.95	
4	3	39.62	10.86	
5	4	40.55	11.89	
6	5	40.79	12.91	
7	6	40.55	13.91	
8	7	39.26	14.86	
9	8	39.6	15.73	
10		16.58		

Note: EWMA calculated from logged power will only approximate the EWMA power calculated by the processor due to sample rate limitations, the EWMA formula shown for average power is a simplistic representation of the actual formula used that closely approximates the expected behavior.

Calculating EWMA is useful for Turbo validation when comparing with frequency, temperature, and power curves.

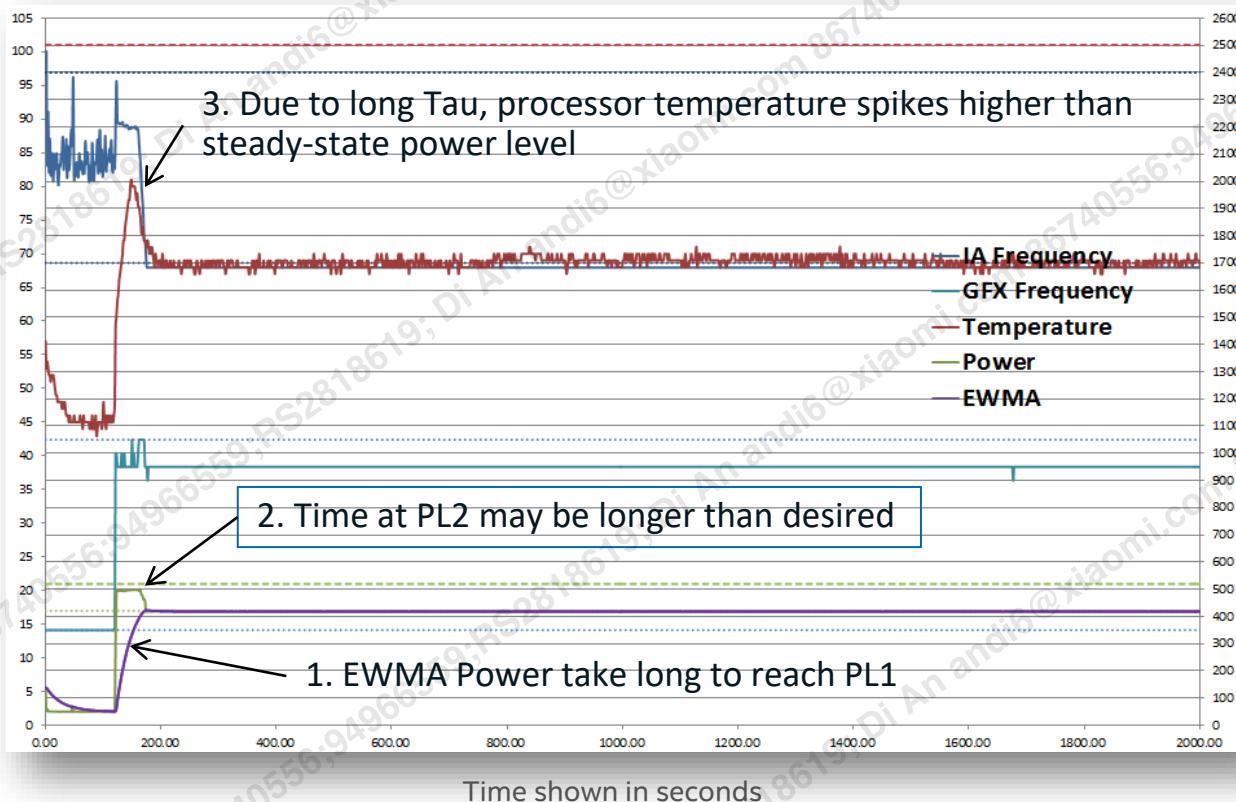
3.2.4 Turbo Budget Consumption Example

- Example Power Limits:
- PL1 = 15 W
- PL2 = 25 W
- TAT IA + .GT workload run in cycles.



3.2.5 Tau Considerations for PL1 and PsysPL1

- Tau is an averaging constant used in PL1 exponential weighted moving average (EWMA) power calculation.
- Tau roughly relates to the amount of thermal capacitance in package thermal solution.
- Unless testing indicates otherwise, Intel recommends setting PL1 Tau to 28 seconds for mobile, eight seconds for desktop.



$$Budget_t = PL1 - EWMA_t$$

$$EWMA_t = EWMA_{t-1} + \Delta t / \tau \cdot (P_t - EWMA_{t-1})$$

3.2.6 PL1 - Resulting Frequency Considerations

- Customers may observe IA frequency running below the Maximum Assured Frequency when the processor is running at sustained base power levels and the PL1 limit is set to Base Power.
- While still meeting Base Power (TDP) specification, to maximize overall platform performance, the processor may reduce the IA frequency lower than the Base frequency in order to provide additional power budget to the graphics domain.
 - This behavior is required for the PL1 based duty cycle function to manage powers to PL1 requests below base power.
 - The noted behavior is enabled by the PL1 'PKG_CLMP_LIM_1' feature set in MSR¹ and MMIO.
 - Customers can choose to disable this feature, but it may result in reduced performance and will also hinder the ability to manage powers to PL1 requests below base power (for example, PL1 set at SDP on Y processors).

¹Refer to Alder Lake and Raptor Lake Processor Family Core and Uncore BIOS Specification ([627270](#)) for more information.

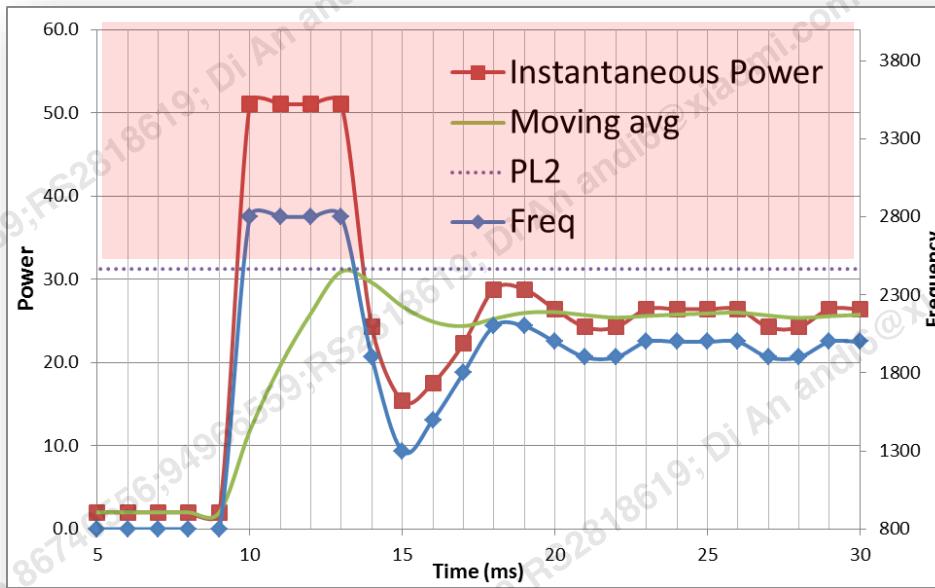
3.3 Power Limit 2 (PL2)

- A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2.
- It is a short duration thermal and power-delivery power limit.
- It can be a thermal issue if set for too long, and a power-delivery issue related to brick and battery if set too high.

3.3.1 PL2 in Action

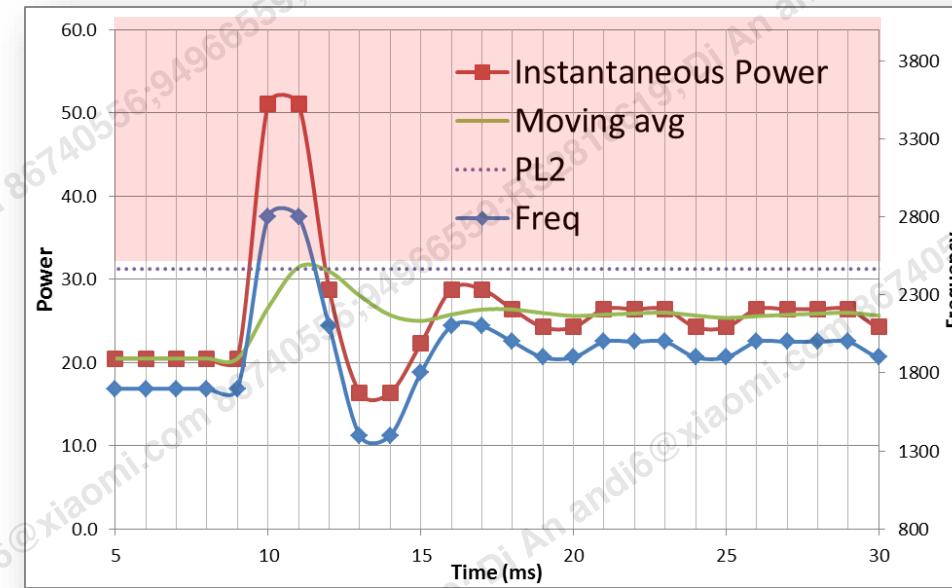
- Raptor Lake still controls PL2 limit to < 10 ms:
 - Time above PL2 would be longest when starting from an idle condition.

31W PL2 Example



Longer time above PL2 when starting from idle

Above PL2



Shorter time above PL2 when starting from other workload

3.4 Power Limit 3 (PL3)

- A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency.
- This is an optional setting.
- PL3 can help mitigate some degradation risks over the lifetime of the batteries.
- Also, it provides a way to limit the maximum duty cycle of peaks above a desired power level.
- PL3 duty cycle control may not be assured within any single time window.

3.4.1 PL3 Recommendations

- Program PL3 slightly higher than PL2 (1 W to 2 W).
- Program PL3 duty cycle reaction time as low as 2 ms.
 - Having a shorter reaction time on PL3 can help reduce the noise on the PL2 control.
 - This would give a more stable frequency, for example, $2 \text{ ms} = \text{Time Window} * \text{Duty Cycle}$.
- The peak power excursions above PL2 are managed within 10 ms by the PL2 response time.

Refer to Raptor Lake Platform Design Guide for additional guidance.

3.4.2 PL3/PsysPL3 - Programming

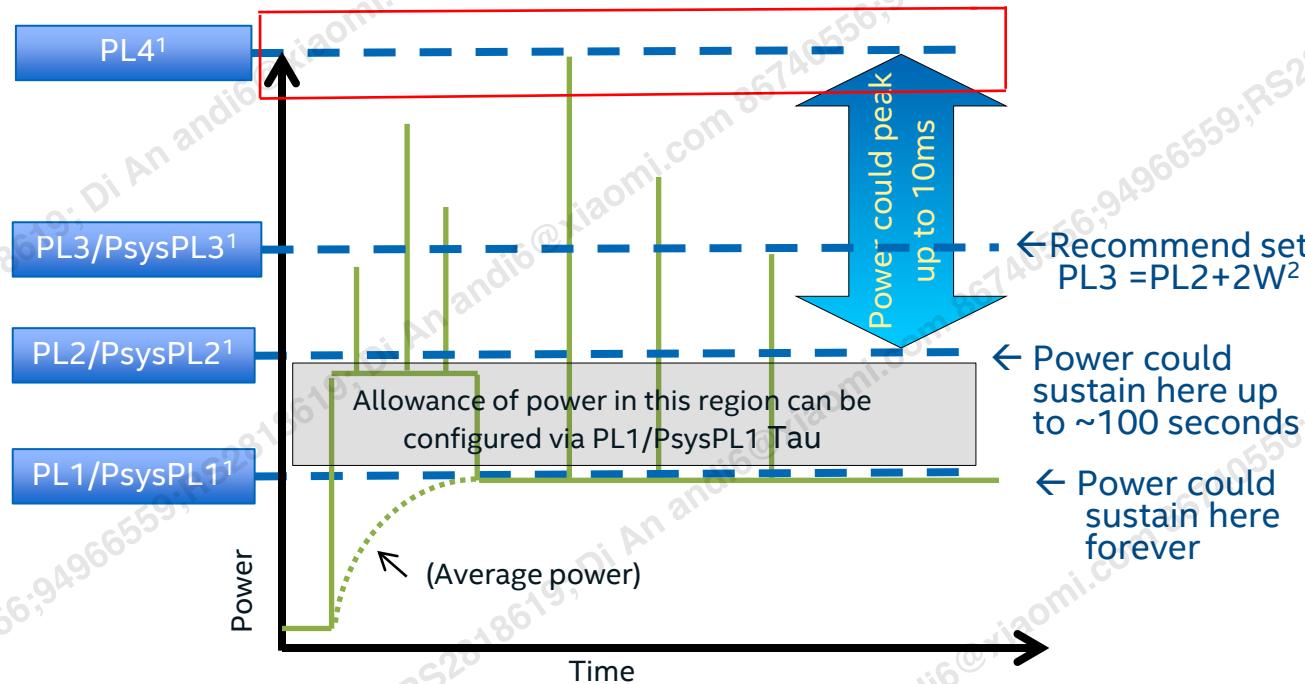
- MSR and PECI Interfaces available (PLATFORM_POWER_CONTROL)
- MSR Details: MSR 0x615
- PECI Details: PECI Index 57
 - Same Interfaces¹ used for both PL3 and PsysPL3²

Bits	Field Name	Description	Time Window Decoder			
			xx	YYYYY	ms	Min Allowed Duty Cycle
[14:0]	Power_Limit	'PL3', a power reading above this will be interpreted as a violation (in increments of 1/8 th Watt)	10	00001	3	67%
11			11	00001	3.5	58%
00			00	00010	4	50%
01			01	00010	5	40%
10			10	00010	6	34%
11			11	00010	7	29%
00			00	00011	8	25%
01			01	00011	10	20%
10			10	00011	12	17%
11			11	00011	14	15%
00			00	00100	16	13%
01			01	00100	20	10%
10			10	00100	24	9%
11			11	00100	28	8%
00			00	00101	32	7%
01			01	00101	40	5%
10			10	00101	48	5%
11			11	00101	56	4%
00			00	00110	64	4%

Example: 0xA4A8140 → 40 W PL3, 40 ms Time, 10% duty

3.5 Power Limit 4 (PL4)

- PL4 establishes a power limit that preemptively limits *potential* SoC power to prevent brief power spikes from tripping the power adapter and battery over-current protection mechanisms.



¹Optional Feature, default is disabled.

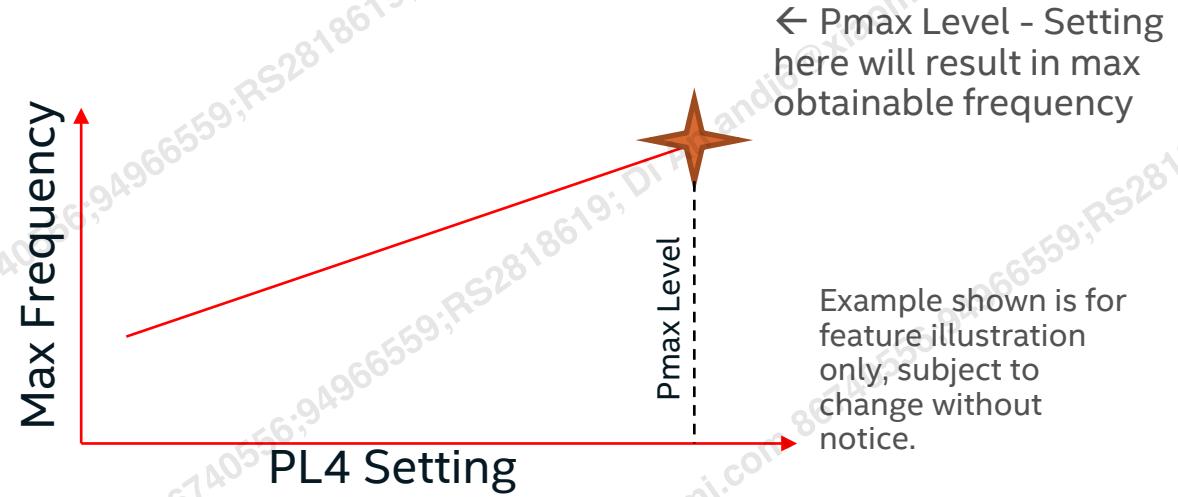
Note 1: Optional Feature, default is disabled.
Note 2: See slide 11.6 for details.

3.5.1 PL4 - Terminology

- Potential Peak Power (PPP)
 - PPP is an expected worst-case power level calculated by the Power Control Unit based on the component characteristics and the present operating frequency (IA, GT, Ring domains).
 - PPP is calculated:
 - Prior to any frequency transition (normally on 1 ms boundaries), or
 - Anytime when AVX instructions enter the pipeline, or
 - A core C-state transition is about to occur.
 - PPP assumes a scenario across the domains that represents the most intensive application known.
- PL4
 - PL4 is the limit that PPP is compared against.
 - If $\text{PPP} > \text{PL4}$ at the frequency transition, then a lower frequency is selected to prevent PPP from exceeding PL4.
 - If frequency is reduced due to PL4 limits, then the PL4 Clipping Cause bit (MSR 0x64F, bit 8) is set.

3.5.2 PL4 Control – SoC Peak Power Limiter

- Designs can limit SoC from exceeding a design peak power limit:
 - May allow new options for battery protection (Refer following slides on BPO).
 - Limits can be set dynamically via MSR or PECI.
- Expect some max frequency reduction based on the setting:
 - Preemptive limit; could limit performance to prevent exceeding.
 - PL4 setting will result in a loss in max obtainable frequency (Fmax).
 - Low PL4 setting is not expected to cause functional failure.
 - Performance impact will depend on workload.

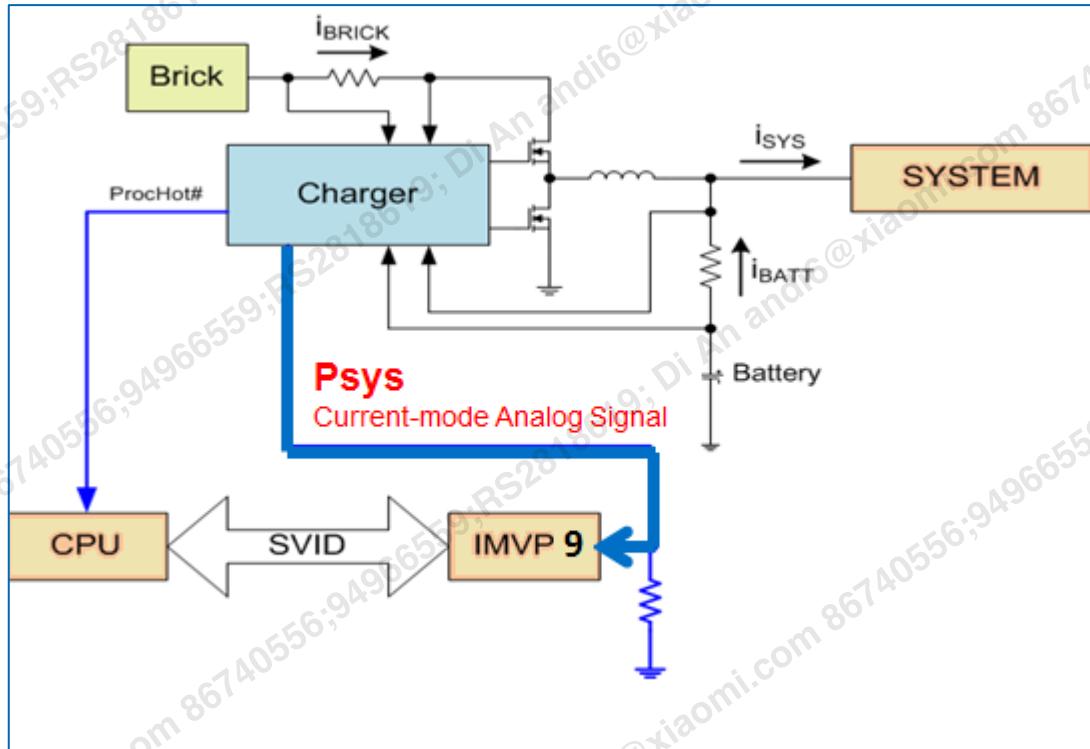


3.5.3 PL4 - Limitations

- PPP is a projection and NOT based on the power telemetry of the current workload.
- PPP projection is not exposed via any software interface. It is only used within the PCU.
- If PL4 is set too low, performance may be reduced excessively due to more aggressive power protection and resulting frequency reduction.
- Workload characteristics used in the PPP calculation are based on workload and “power virus” research and are not easily duplicated on a real system for testing.

3.6 Power of System

- Psys (Power of System)
 - Total Platform Power monitor.
 - Provided to the CPU.
- H/W Implementation
 - Enabled via battery charger.
 - Low impact solution.
 - Not required if not using Psys.
- Advantages
 - SOC-Platform Power Sharing via PsysPL1.
 - Power Delivery Protection (Battery/Brick Protection) via PsysPL2 and PsysPL3.



Psys allows the SoC to track and control SoC power based on the total platform power consumption.

3.6.1 PsysPL1 and PsysPL2 Introduction (Optional – Requires Psys Support)

What are PsysPL1 and PsysPL2?

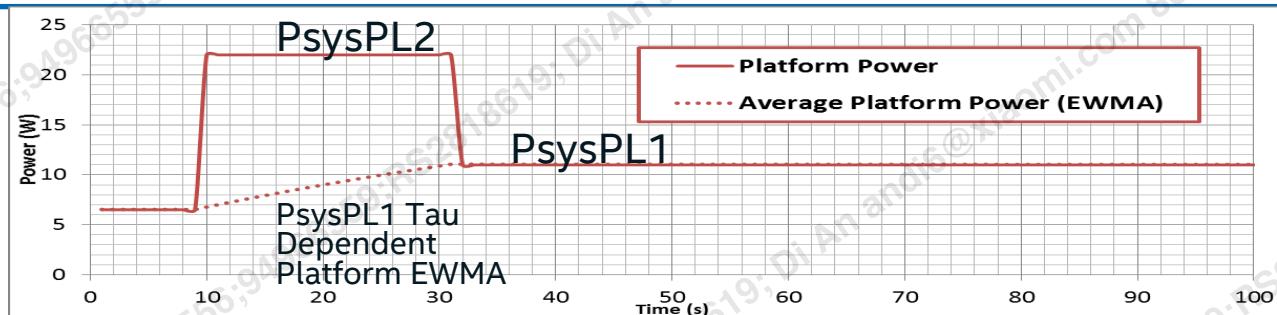
- Allows SoC power to be controlled to within monitored platform power limits, analogous to SoC power management (PL1/PL2).

How can PsysPL1 and PsysPL2 help my design?

- PsysPL1/tau is configurable at runtime and typically set to total system cooling level.
- PsysPL2 is configurable at runtime and typically set to platform power source limits (AC/Battery).
- PL1 and PL2 power algorithms run concurrent with PsysPL1 and PsysPL2, each can be used for different objectives.

What are the limitations of PsysPL1 and PsysPL2?

- Both limits when reached can only limit SoC power.
- Limits may over compensate if power consumption is from a USB device, for example, USB HDD.



3.6.2 PL2 versus PsysPL2 Usage Benefit Example

How can PsysPL2 help my design?

- AC brick ratings are driven by total platform power, not just SoC power
- Instead of setting PL2 to a level with some assumption of 'rest of platform' power, designers can set PsysPL2 to a known level where AC brick or batteries can sustain for 100s of seconds
- Some designers may choose to use both PL2 and PsysPL2 for different motives (for example, PL2 for heat pipe max power capability)

Refer to RPL
Platform design
guide for PL2
default values

Important considerations regarding PL2 and PsysPL2

- Hybrid Power Boost or NVDC are also recommended in order to assist if PsysPL2 (or PL2+ROP) excursion exceeds the AC adaptor limit
- Caution also advised when only powered by AC (no battery). PL2 and PsysPL2 may be too slow to react to short bursts above adaptor rating (Refer 'Short Term' Power Delivery Protection)

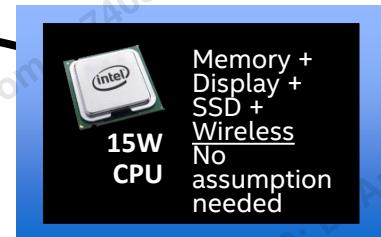
System A – PL2 Approach



$$\text{PL2} = 45\text{W} - 25\text{W(ROP)} = 20\text{W}$$

SoC could have run higher if assumption was not made!

System B – PsysPL2 Approach



$$\text{PsysPL2} = 45\text{W}$$

SoC enjoys more Turbo when other components use less power

3.6.3 PsysPL3

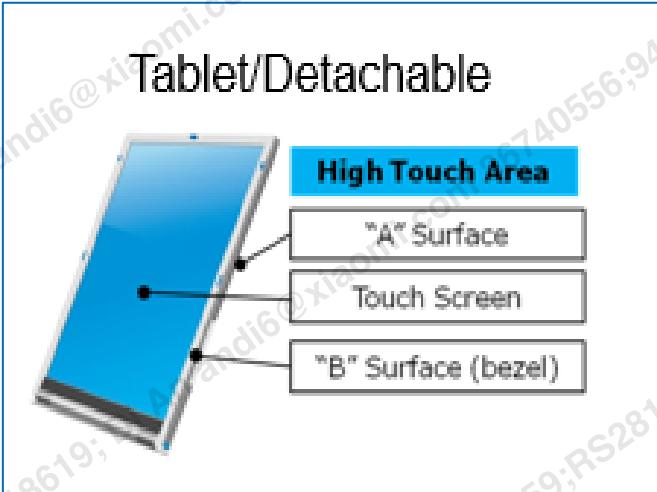
- A threshold that if exceeded, the PsysPL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PsysPL3 by reactively limiting frequency.
- PsysPL3 allows for the elimination of static ROP assumptions that are required for standard PL3 protection.
- PL3/PsysPL3 can be set dynamically during run-time based on system events like power source changes.
- Specifics to PL3 functionalities subject to change

Note: Refer to Raptor Lake Platform Design Guide on guidance for PL3 recommendations

3.7 Skin Temperature

- Multiple skin temperature measurement solutions exist:
 - Non-contact solutions (for example, IR sensors, motherboard sensor).
 - Direct contact solutions (for example, thermistors).
- Intel® Dynamic Tuning software allows the most robust system power/thermal management solution:
 - Maximizing customer experience, perceived performance, and ergonomic impact.
 - Thermal policies under Dynamic Tuning can support multiple skin temperature monitoring solutions and can provide an alternate control over just limiting PL1 based on skin sensor.
 - Embedded Controller (EC) solutions also possible for non-Dynamic Tuning adopters that can implement skin temperature based dynamic PL1 control via the PECL bus but they will not be able to take advantage of additional power control knobs at the platform level that Intel® Dynamic Tuning offers.

Note: Refer to Technologies, Research and Initiatives Skin Temperature Jury Study Technical White Paper ([419899](#)) for more information on Intel's skin temperature.



3.7.1 Skin Temperature Based PL1/PsysPL1 Control

- Small form factor systems like tablets and convertibles are most likely to be skin temperature limited.
 - Systems limited by maximum CPU temperature are less likely.
- Customers are strongly encouraged to implement hardware skin temperature monitoring and thermal management.
 - A closed loop, skin temperature based solution, using modulation of PL1 based on temperature excursions, is Intel's recommended thermal management approach one.

Note: Intel® also strongly recommends use of Intel® Dynamic Tuning for thermal management.

3.7.2 Skin Thermal Sensor Options

Motherboard Sensors (Thermistor/Diode)

Pros

- Low cost
- Easy to implement
- No wires required inside chassis

Cons

- May be difficult to place due to physical routing limitations
- Good signal grounding required to reduce signal noise
- Requires characterization to identify offset to actual skin temperature
- Temperature rise/fall may not correlate accurately with skin changes

Infrared Sensor

Pros

- Provide real time surface temp
- Does not require extensive system thermal characterization to establish correlations to skin
- No wires required inside chassis

Cons

- Higher cost
- Need line of sight
- Requires keep out on MB
- Layout / routing capabilities will need additional MB real estate

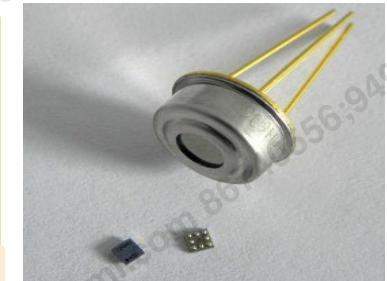
Direct Contact Thermistor

Pros

- Relatively Low cost
- Provide real time surface temp
- Multiple routing options including direct surface attach to skin

Cons

- Reliability for direct attach to inside skin surface
- Must consider z-height and potential interference issue along sensor/wire
- Connector requires, additional BOM cost
- Need to calibrate and may need additional EC code
- Wires can conduct heat and affect measurement
- Complex assembly process with wires

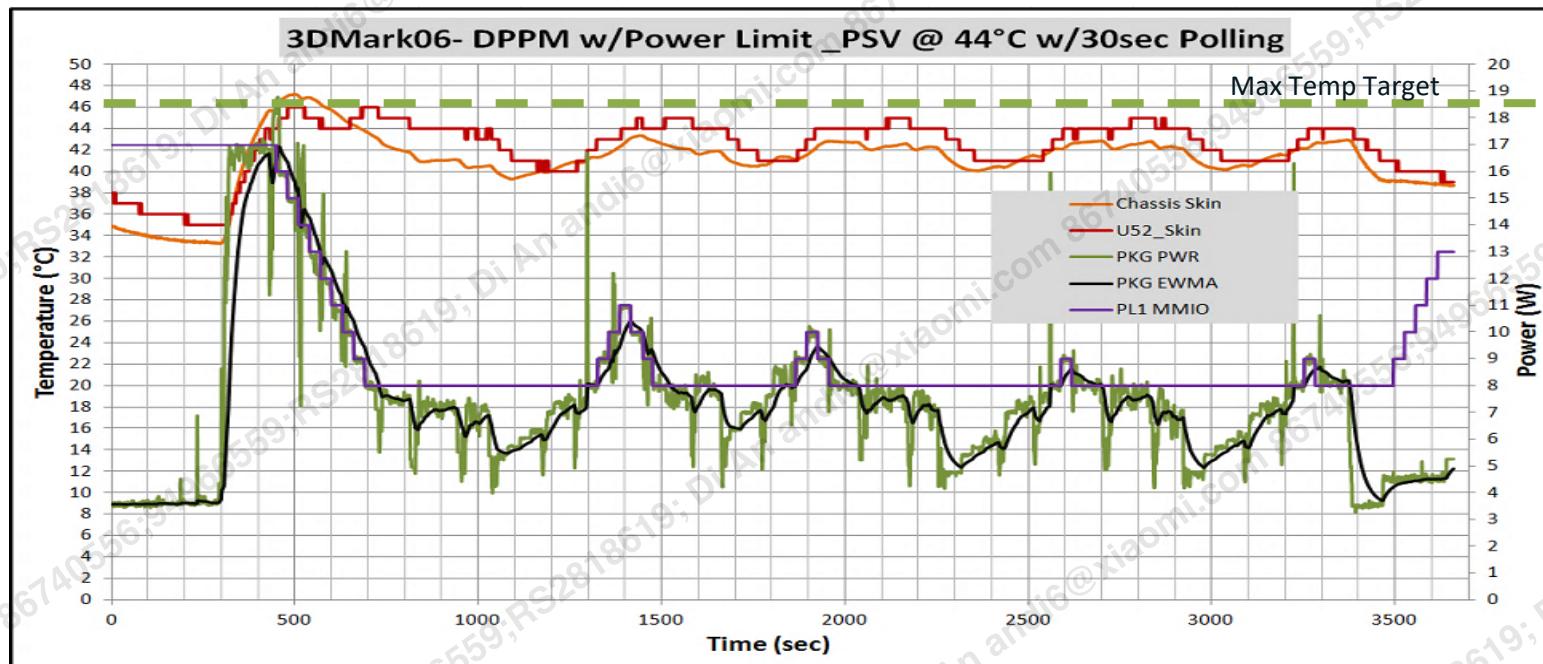


(TI Sensor Pictured)

All solutions require some characterization based on the customer-defined workload scenarios.

3.7.3 Skin Temperature Monitor and Control via PL1

- Reduce PL1 as T_{skin} gets closer to T_{skin_max} .
- Example Algorithm: Set PL1 in 1 W increments at 44 C threshold with 30 second polling.



Intel® Dynamic Tuning provides the easiest solution for automatic PL1 control in addition to platform 'smarter' power reduction mechanisms

4.0 Thermal Management

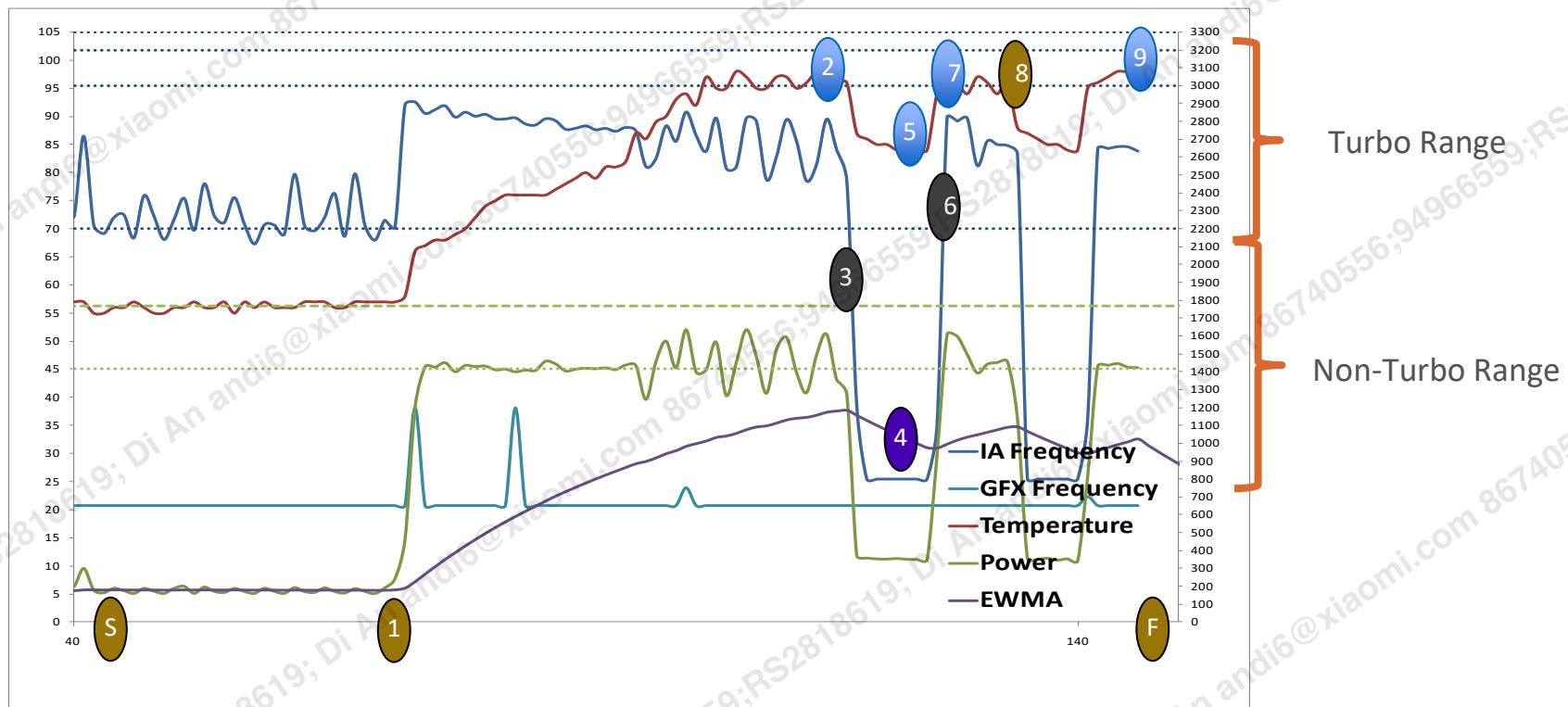
- 4.1 Under-Designed Thermal Solution Risk
- 4.2 Turbo Thermal Control
- 4.3 System Thermally Constrained Options
- 4.4 Running Average Temperature Limiting (RATL)
- 4.5 RATL – Usage Example
- 4.6 VR_TDC Introduction - VR Thermal Management

4.1 Under-Designed Thermal Solution Risk

- If ACPI (_PSV) or (_CRT) trip points are enabled, customers must set Tcc Activation Offset to a temperature below the ACPI (_PSV) or (_CRT) value. Otherwise ACPI (_PSV) (Passive throttling states) when triggered will cause the operating system to request a P-state below P0, thus disabling Turbo.
- Tau, if set longer than system design, can thermally handle (under-protection); can also contribute to performance loss.

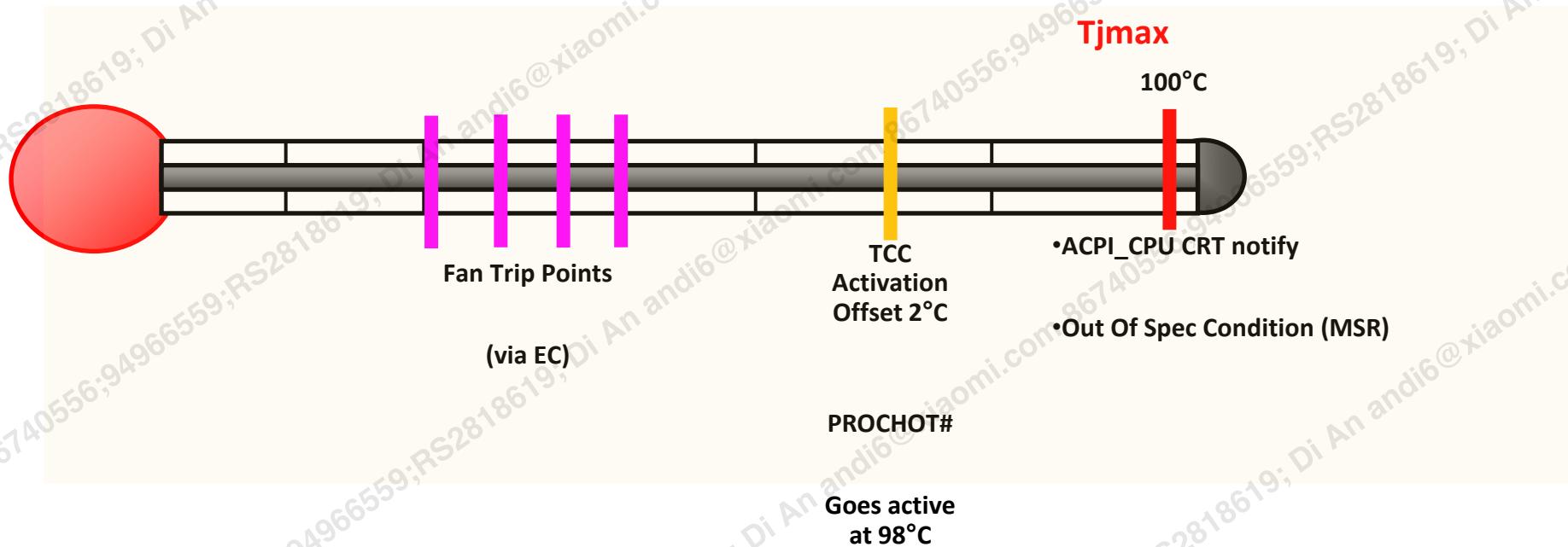
Example of impact

- S. System in idle
- 1. Workload Begins
- 2. _PSV Reached
- 3. System Throttles
- 4. Turbo Budget Up
- 5. _PSV Relieved
- 6. Turbo returns
- 7. Temp spikes
- 8. Cycle repeats
- 9. _CRT Reached
- F. OS shutdown



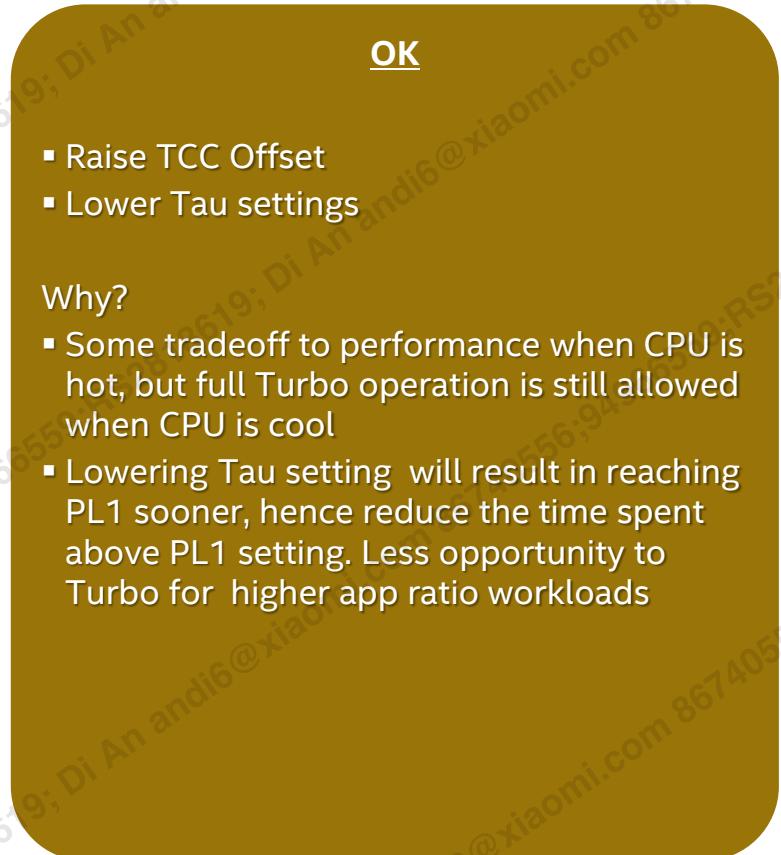
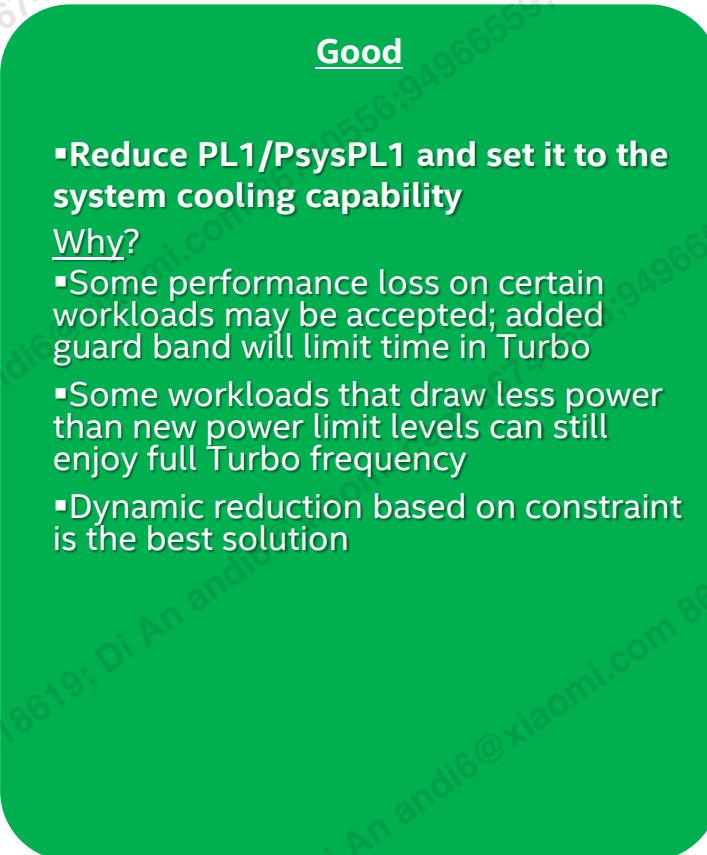
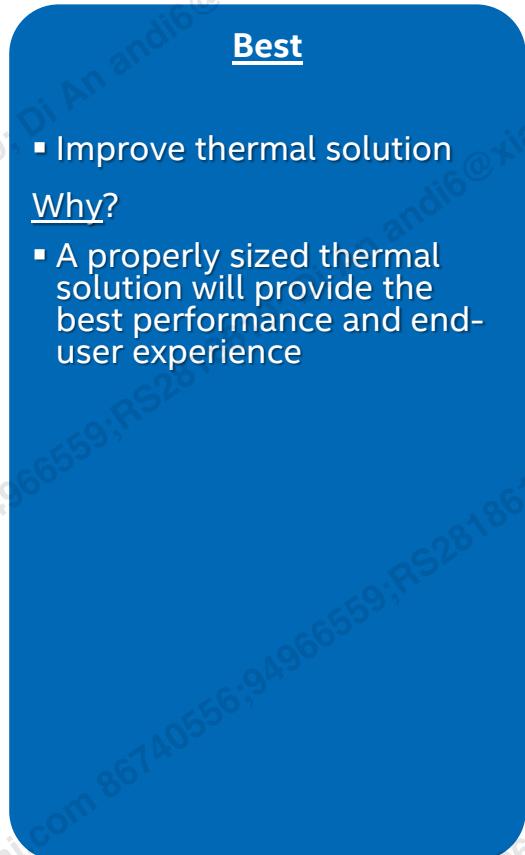
4.2 Turbo Thermal Control

- Hardware-based Turbo control offers the best performance.
 - Handles both IA and GT thermal issues
 - Ensures IA/GT are fully throttled at T_{jmax}



4.3 System Thermally Constrained Options

- Thermally under-designed systems may have big impact on performance.



4.4 Running Average Temperature Limiting (RATL)

CPU Temperature Limiting Background

- Intel's CPU offers a robust way of doing fast HW-level power control in order to meet a temperature limit (Thermal Control Circuit or TCC).
- Until now, lowered TCC activation via programming TCC_Offset was setting an instantaneous limit.
- From Skylake, the same Tcc_Offset interface now includes an averaging constant (Tau).
- The SoC manages power/frequencies to keep the average temperature at or below the target temperature (Tjmax limit still invokes instant throttling).
- The averaged temperature used for TCC activation can now be read via PECL.

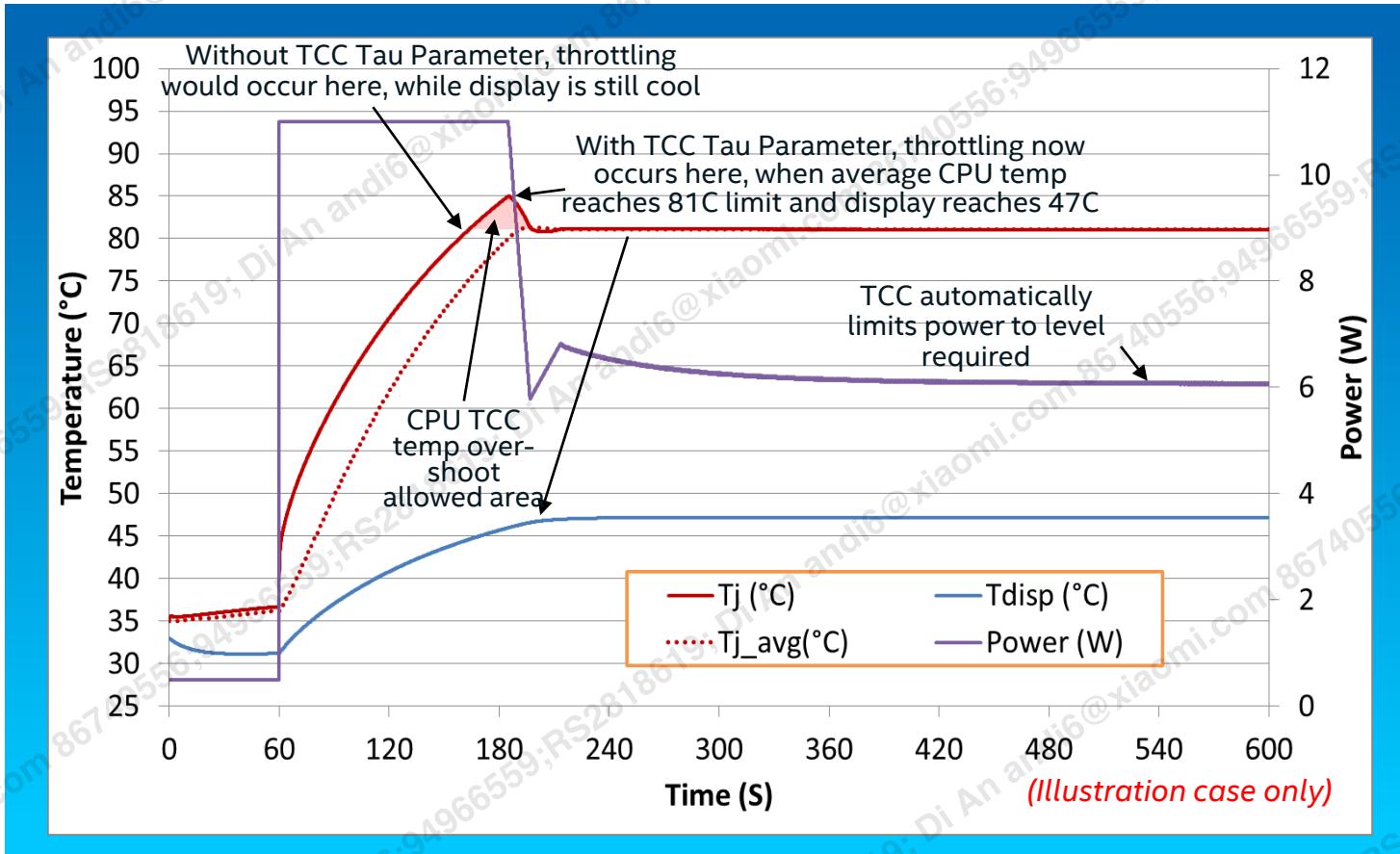
Why use an Average SoC Temp Limit?

- In the absence of a more robust skin sensor monitoring solution and Intel® Dynamic Tuning, the CPU temperature might be used as a crude proxy for skin temperature. The problem here is that SoC junction temperature increases much faster than skin temperature.
- Having an average SoC temperature limit will allow some short duration excursions above the SoC target temperature, increasing performance while retaining intended protection.
- Intel® Dynamic Tuning still provides a much better approach to skin temperature thermal management.

4.5 RATL– Usage Example

- Design Assumptions:

- In steady state, when CPU is at 81°C the skins are at 47°C (display temperature target).
- The TCC_Offset Tau was tuned to limit skin from exceeding target.



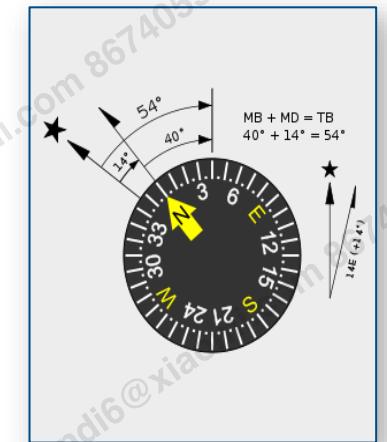
Note: System assumed not to reach PL1 or PsysPL1 setting in this example

4.6 VR_TDC Introduction - VR Thermal Management

- IMVP Spec historically has provided a good way to do VR thermal management, but the actions have significant performance reduction¹.
 - Stage 1 – Disable Turbo from hot VR (SVID ALERT Signal).
 - Stage 2 – Limit all domains to min frequency (PROCHOT#).
- VR_TDC Setting
 - Designers can set VR_TDC for each power rail to a thermally sustainable current level.
 - Depending on the setting, current reduction action is more graceful than removing Turbo or asserting PROCHOT#
 - VR_TDC is a moving average current limiting algorithm with a Tau time constant (1 s default).
 - Intel recommends setting VR_TDC to be set to the Thermal Design Current (Icc_TDC) level; setting lower could result in performance loss.



“Big Hammer”



¹Refer to Power Delivery Design Guidance section for additional information.

¹Refer to Power Delivery chapter in Raptor Lake U P H Platform Design Guide ([686872](#)) for more data.

5.0 PD Controls

5.1 Introduction

5.1.1 Soc Key Terms

5.1.2 Platform Key Terms

5.2. SoC PD Controls

5.3. PD Power Management

5.1 Introduction

- This section provides a brief overview of the platform-level power delivery protection mechanisms and considerations.
- Power Delivery Protection Mechanisms include:
 - PL3
 - PsysPL2
 - PsysPL3
 - PL4
 - PL4 platform offset
 - VR_Imax
 - VR_TDC¹
 - Vmin protection for 2S battery
 - PROCHOT# protection for 1S-3S battery
 - VR Alert

¹ Refer to Power Delivery chapter in PDG (TBD) for more details.

5.1.1 SoC Key Terms

IccMax: VR Max Current

- Applies to each power plane; should support electrically
- Drives regulator electrical design
- More decoupling required to prevent voltage overshoot on load release

Icc_TDC: VR Thermal Design Current

- To be supported electrically and thermally, indefinitely
- Drives regulator thermal design (either inductor, board or FET limited)
- Expect more workloads to reach TDC limits often with Turbo

Iout: VR Current Monitor

- Allows each VR to inform processor of current consumption (also known as IMON)

Pmax: Max 'Virus' Processor Instantaneous Power

- Not a specification but guidance for expected worst case total SoC power
- Drives power supply electrical design
- Lower than sum of reach VR rail IccMax x Vcc

Pmax.app: Max 'Realistic' Instantaneous Power

- Not a specification but guidance for expected real world application's total SoC peak power

SVID ALERT and VR_HOT#: VR Thermal Protection Mechanisms

- Thermal protection at VR as hardware protection against thermal events
- Allows VR to limit Turbo via SVID bus (ALERT) and also pull bi-directional PROCHOT# for temperature protection

5.1.1 SoC Key Terms (Cont.)

PL3 (Optional Setting)

- A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency.
- If the brick and battery does not support up to 10 ms peak power protection, implementing PL4 and/or a peak current monitor that can trigger PROCHOT# may be required.

PL4 (Use with caution)

- It can be set lower as battery drains to prevent going lower than battery min voltage (Power Boss).
- Preemptive limit; could limit performance to prevent exceeding.

PL4 Platform Offset (also known as EC/PECI PL4 offset)

- The EC can be used to detect when a USB device is connected to the system and communicate the PL4 Platform Offset via PECL.

VR_Imax (Use with caution)

- It can be set to a lower level if under-design VR for BOM reduction .
- Preemptive limit; could limit performance to prevent exceeding.

5.1.2 Platform Key Terms

PsysPL2 (Refer PL2/PsysPL2 section)

- Can be set to max sustainable power level for AC brick or battery.
- Reactive limit; will not limit performance unless triggered.

PsysPL3

- Can be used to limit occurrence of large power spikes.
- Reactive limit; will not limit performance unless triggered.

PROCHOT# protection for 1S-3S battery

- Can be used to indicate to the SoC that peak power is too high and must be dropped.
- SoC will drop the peak power by ~33% in 10 μ s, and even further in 100 μ s.
- For “Fast” PROCHOT#, peak power will drop by $\geq 30\%$ in $\leq 10 \mu$ s.

Vth: set value for Vsys for PROCHOT# assertion, threshold voltage

- Asserted by the charger if the system voltage drops below it.
- The Vth can be set in the charger by the EC or Intel® Dynamic Tuning.
- When crossed, the charger will assert.

Vmin Active Protection: Allows the charger to supplement the battery

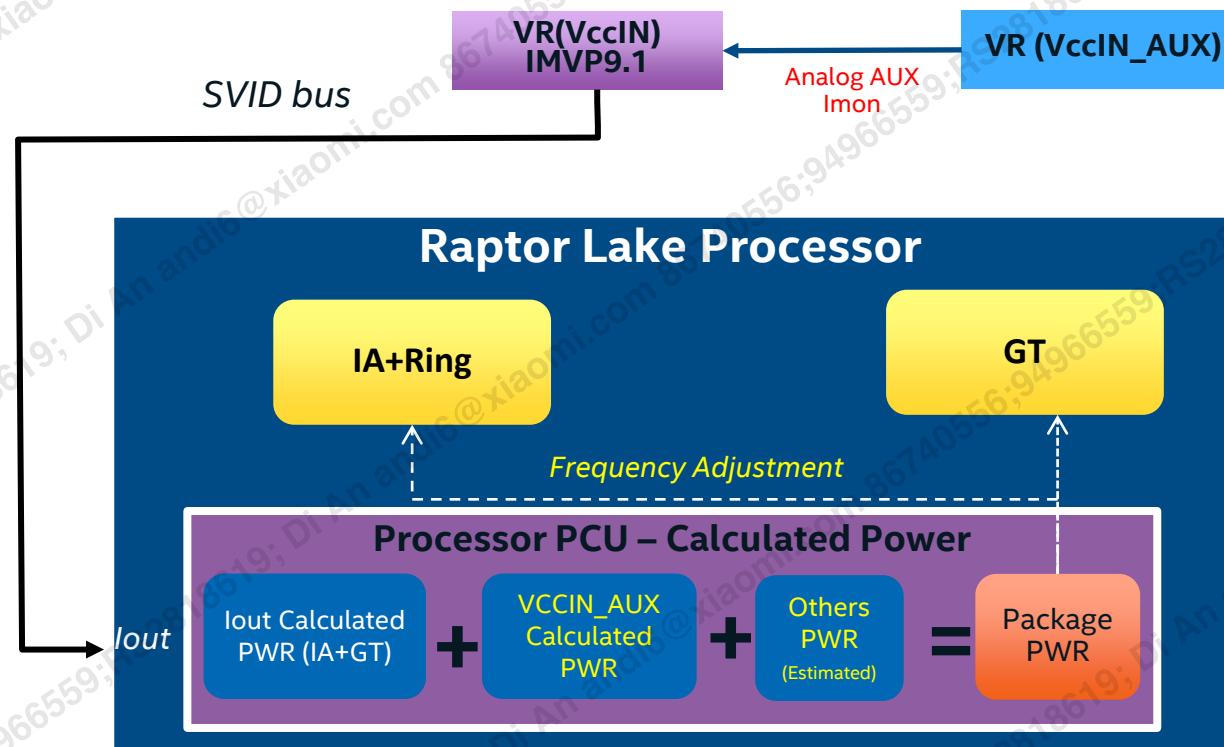
- Active Vmin protection allows the charger to store energy in the input coupling.
- When system voltage drops below Vth, the charger will use this energy to supplement the battery and give extra time for the SoC and ROP to drop their power.

5.2 SoC PD Controls

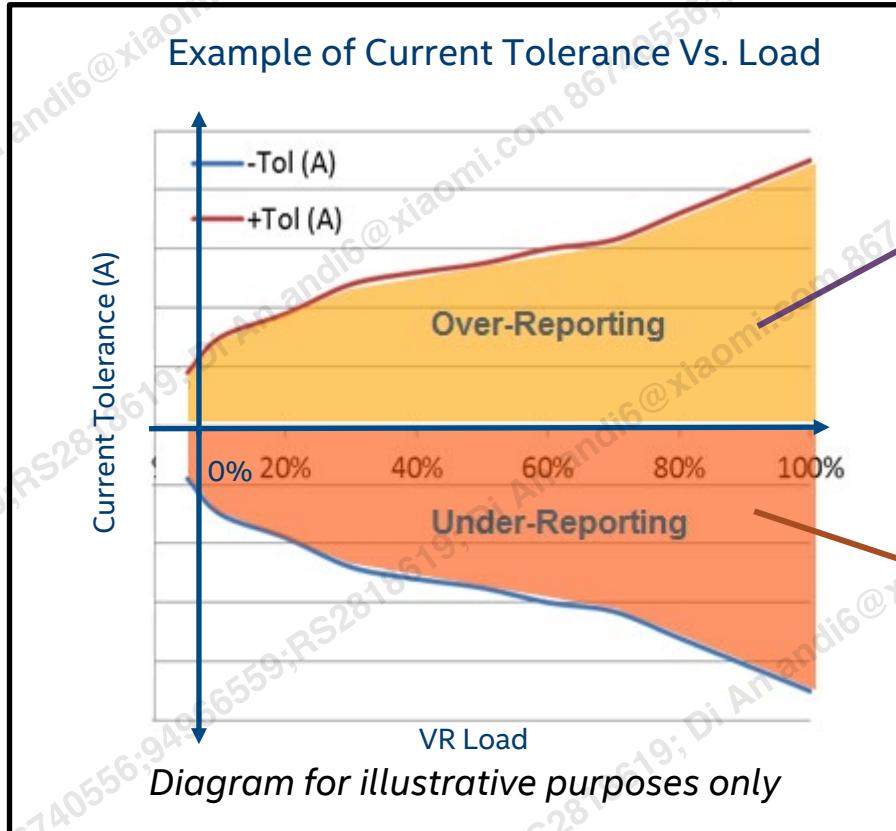
- 5.2.1 Power Reporting Telemetry in Raptor Lake(RPL)
- 5.2.2 Iout Over-Reporting vs Under-Reporting
- 5.2.3 PL2 Alone Cannot Prevent P(max) Spikes
- 5.2.4 PL2 Alone Cannot Prevent Regular P(max) Occurrence.
- 5.2.5 VR_Imax Control Intro (VR Peak Limiter)
- 5.2.6 IccMax Programming

5.2.1 Power Reporting Telemetry in Raptor Lake(RPL)

- SVID specification includes digital communication of “Iout” over SVID bus.
 - Analog to digital conversion done in the Voltage Regulator (VR), CPU converts current to power.
 - Each VR (VccIN) reports out digital Iout over SVID bus to the processor.
 - Analog VccIN_AUX Imon is read by IMVP9.2 VR and digital value is sent via SVID bus



5.2.2 Iout Over-Reporting versus Under-Reporting



Over-Reporting

- Potentially lower system performance
 - VR reports higher current on Iout than the actual CPU loading
 - CPU/VR consumes less current than expected.

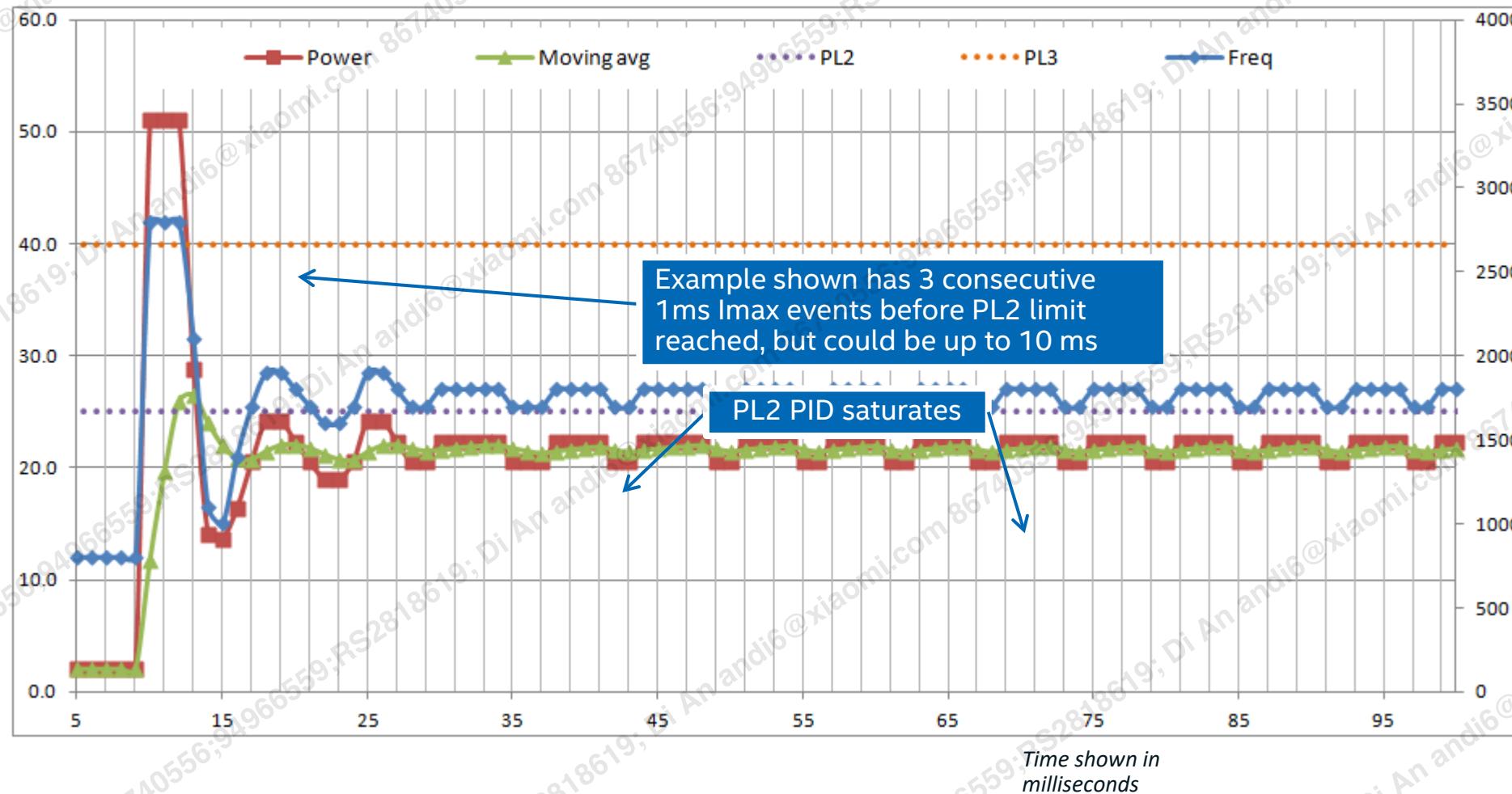
Under-Reporting

- Potentially higher system performance
 - VR reports lower current on Iout than the actual CPU loading.
 - CPU/VR run hotter than programmed power limits.
 - Can cause temperature triggered throttling mechanism to kick in first.

For more information, refer to IMVP9.2 Pulse Width Modulation VR Vendor Enabling Specification
[\(637348\)](#)

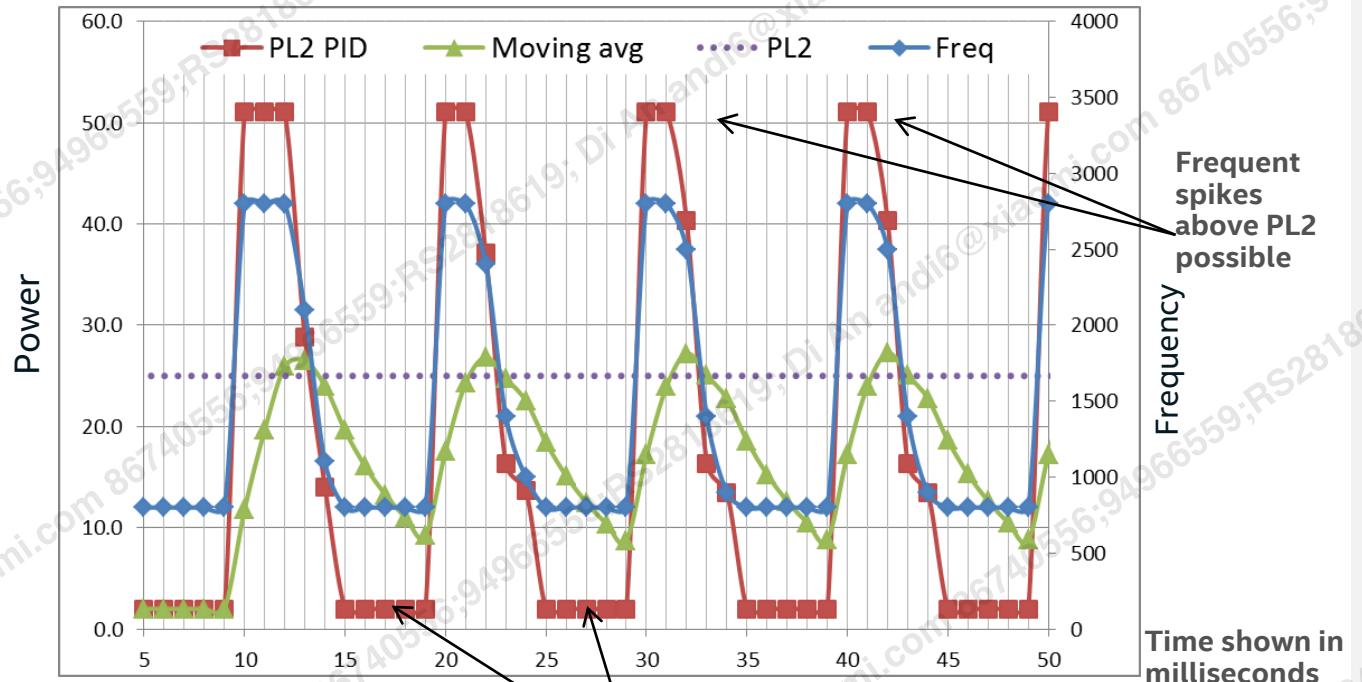
5.2.3 PL2 Alone Cannot Prevent Pmax Spikes

- Pmax is defined as the worst case maximum SoC power behavior.
- PL2 PID algorithm takes time to catch power spike as high as Pmax. During that time, power can spike up to Pmax for up to 10ms.



5.2.4 PL2 Alone Cannot Prevent Regular Pmax Occurrence

- PL2 algorithm ensures power excursion above PL2 level does not last > 10ms.
- PL2 algorithm does not manage duty cycle of back-to-back excursion above PL2 (Refer example below).
- A cyclical workload could potentially spike up to Pmax very often, reducing battery longevity.
- PL3 algorithm can be used to reactively control the duty cycle of these events when they occur

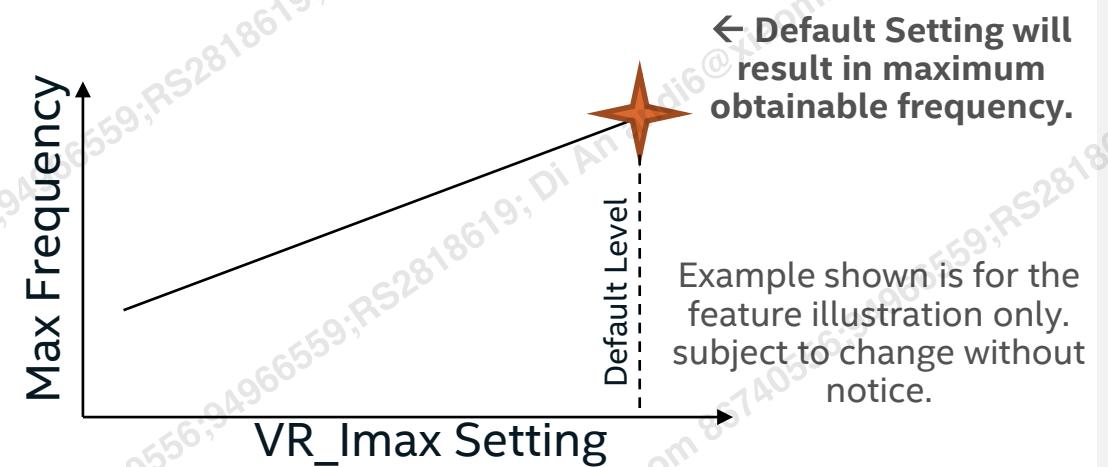


PL2 alone may not be sufficient protection for battery or AC bricks.

Example:
5 ms power virus
followed by 5 ms idle
periods simulated for
illustration purpose

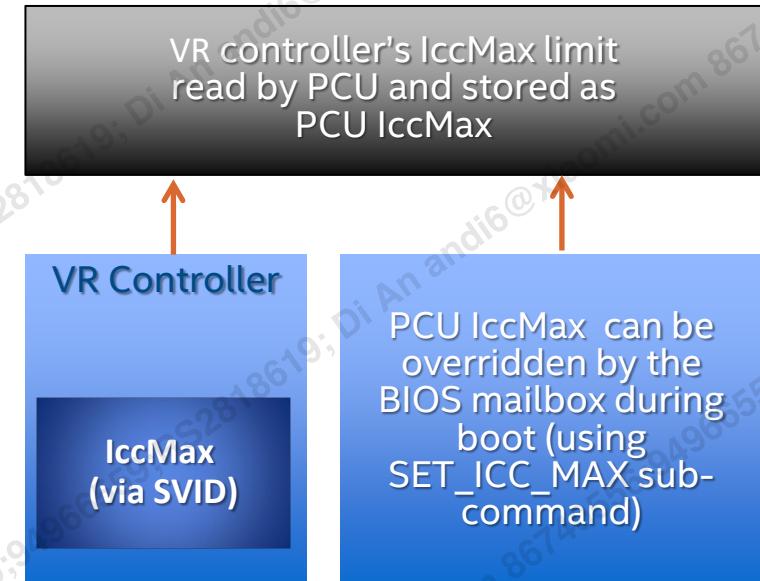
5.2.5 VR_Imax Control Introduction (VR Peak Limiter)

- Designs can limit SoC from exceeding EDS specified VR Icc limits
 - May allow the new options if designing VR below Intel's specification.
 - Limits need to be set via mailbox commands at boot.
- Expect some max frequency reduction based on the setting.
 - Preemptive limit could limit performance to prevent exceeding.
 - VR_Imax setting will result in a loss of maximum obtainable frequency (Fmax).
 - Performance impact will depend on workload.



5.2.6 IccMax Programming

- Reading IccMax
 - RPL does not have the customer readable domain registers for IccMax. IccMAX for VCCin is only available.
- Writing IccMax
 - In RPL, program IccMax through BIOS mailbox
 - MSR 0x601 is only used for PL4.
- IccMax specification applies to VR (VccIN). VR's maximum current capabilities must be provided to the processor via SVID.
- The processor could limit the maximum Turbo frequency to prevent exceeding IccMax in real time.



5.3 PD Power Management

- 5.3.1 Platform Design Choices for Battery Mode
- 5.3.2 Optimizing Power Delivery Controls for Best Performance
- 5.3.3 Intel® Battery Performance Optimizer (BPO) [new]
- 5.3.4 Intel® Battery Performance Optimizer (BPO)
- 5.3.5 Intel® Battery Performance Optimizer (BPO)
- 5.3.6 Setting PLx Power Levels with Intel® Battery Performance Optimizer (BPO)
- 5.3.7 Intel® Dynamic Tuning Introduction
- 5.3.8 Power Boss Policy Introduction (merged)
- 5.3.9 Simple Example: Power Boss Policy In Action
- 5.3.10 PL4 Platform (EC/PECI) Offset Background
- 5.3.11 Windows* PMAX Driver: Maximize Performance when Platform Component is Idle
- 5.3.12 Windows* PMAX architecture
- 5.3.13 Fast V-Mode Technology
- 5.3.14 Reactive PL4

5.3.1 Platform Design Choices for Battery Mode

- Design for Battery Mode
- In battery mode the power available for turbo is limited. As battery is being discharged the available peak power is reduced
- Design choices need to be made to optimize power limits in battery mode for turbo performance
- If power is not sufficient, power limits need to be reduced to avoid system instability

- To optimize PL2/PL4 in battery mode
- Use 3S battery configuration:
 - May need to optimize voltage regulator conversion efficiency
- For 2S battery configuration, increase the battery peak power capability:
 - Minimum System Voltage Reduction
 - Minimize battery path impedance

5.3.2 Optimizing Power Delivery Controls for Best Performance

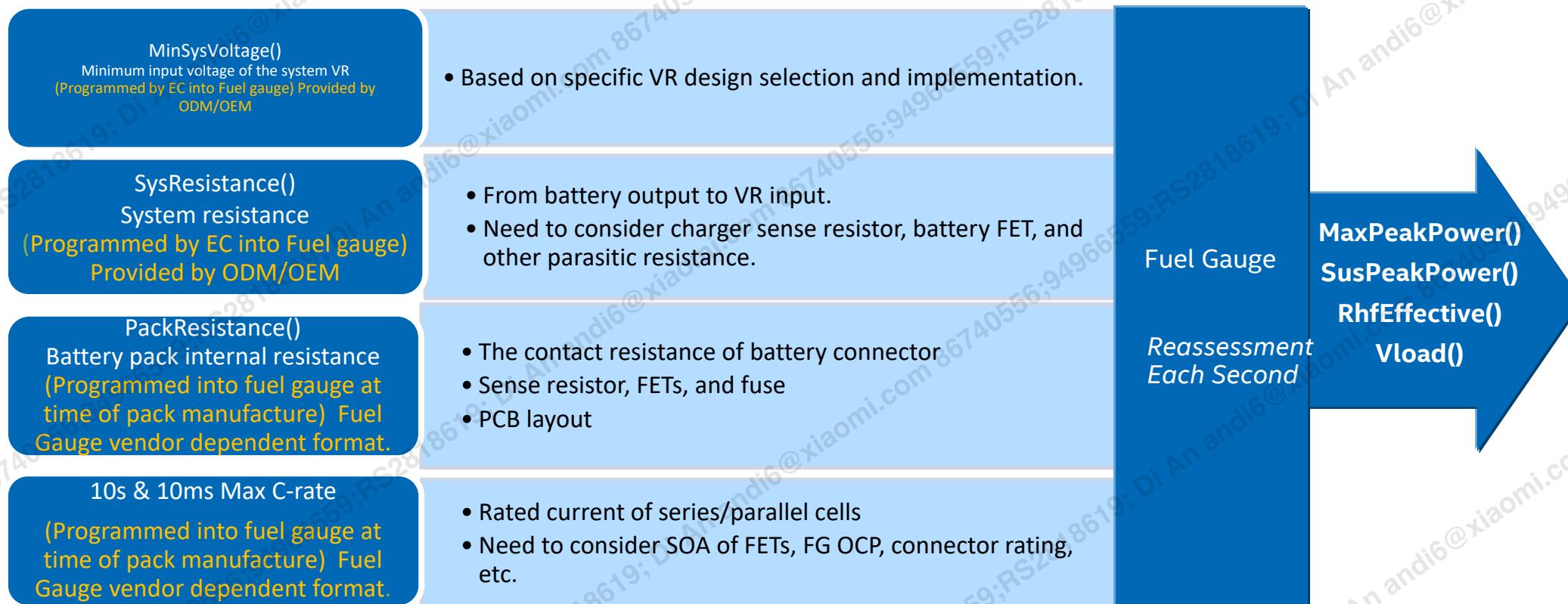
- Power Supply Selection:
 - Select appropriate battery and AC brick configuration to maximize performance within the form factor.
 - Smaller input supplies will require lower power limit settings, resulting in reduced performance.
- Implement Platform Power Protection:
 - Set PsysPL2 according to power supply limitations to allow the SoC to operate at higher power when platform power is low.
 - Use Vmin Active Protection and PROCHOT# to protect power supplies while allowing for recommended PL4 settings.
- Set SoC Power Limits:
 - With additional protection provided in step 2, set PL4 and PL2 to recommended values for best performance.
- Dynamically Adjust Power Limits:
 - Use Intel® Dynamic Tuning Power Boss to dynamically adjust power limits according to battery state of charge or other policy events.
 - Dynamic Battery Power Technology (BPO)
 - Use PL4 Platform Offset to account for USB-C connection events
 - Windows PMAX Driver to account for device activity based on device power states

5.3.3 Intel® Battery Performance Optimizer (BPO) [new]

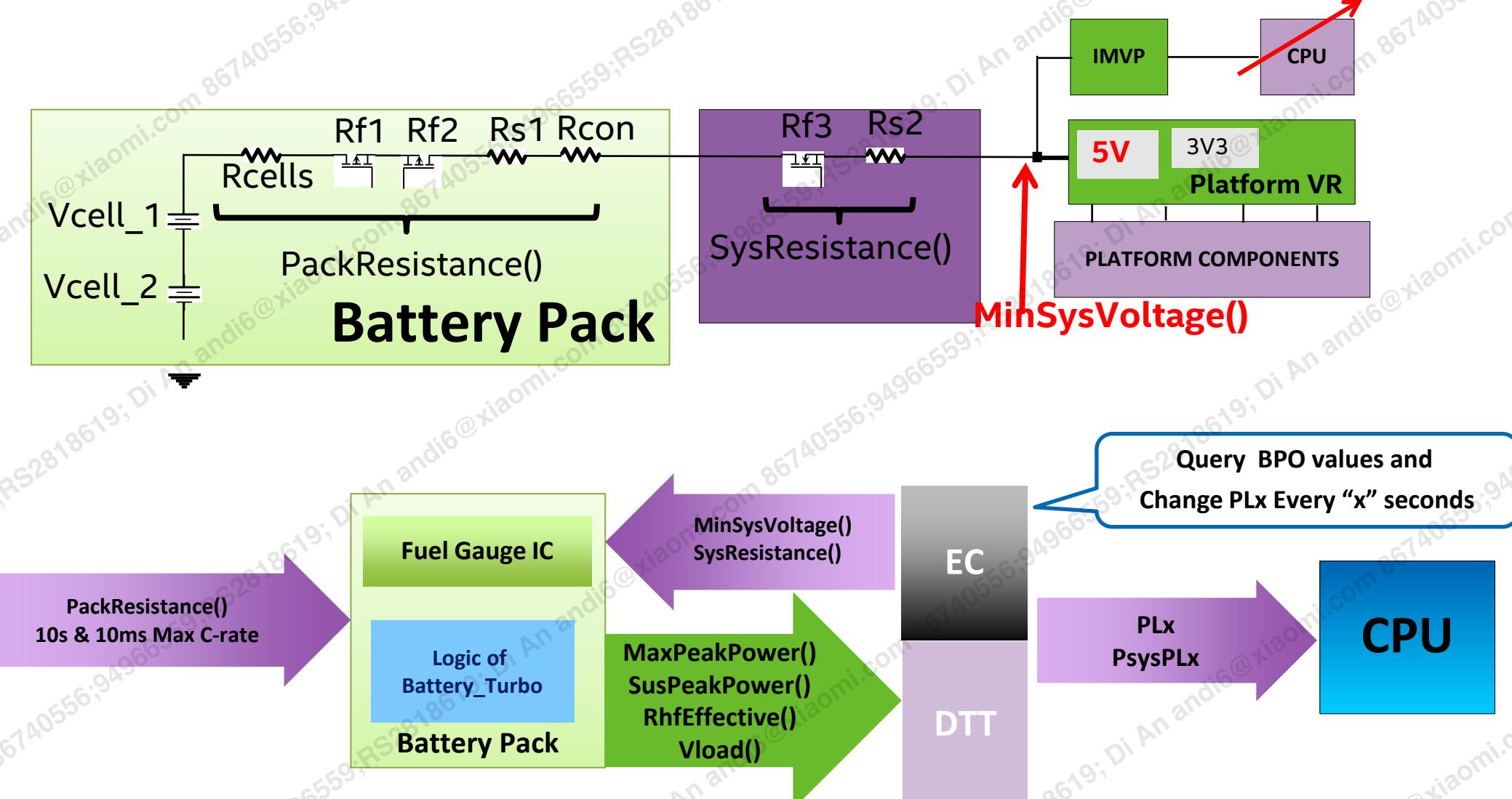
- Embedded smart battery fuel gauges that support BPO provide real time information on the maximum battery output power that can be delivered to the system without violating the minimum system input voltage
- Read by EC through SMBus
- Highly recommended to be used alongside Power Boss to help the CPU to set / regulate its power limits based on the battery of maximum power and Rest of System Power (ROP):
- BPO facilitates and enables the following features and capabilities:
 - Turbo on Battery Mode and related Vdroop concerns:
 - Preventing a premature system shutdown
 - Allowing longer Turbo goodness on battery
 - Allows for Processor performance (PL levels) to be dynamically changed as the battery power capability changes, resulting in higher performance on battery.
 - Usage of batteries of different power capability within the same system

5.3.4 Intel® Battery Performance Optimizer (BPO)

- Intel® BPO is based on a complex estimation algorithm implemented within the fuel gauge to allow greater performance flexibility on portable devices with battery
- Calculates the following:
 - MaxPeakPower() for PL4 determination
 - SusPeakPower() for PL2 determination
 - Vbnl() and Rbhf() for Under Voltage Protection (UVTH) and Fast PROCHOT#



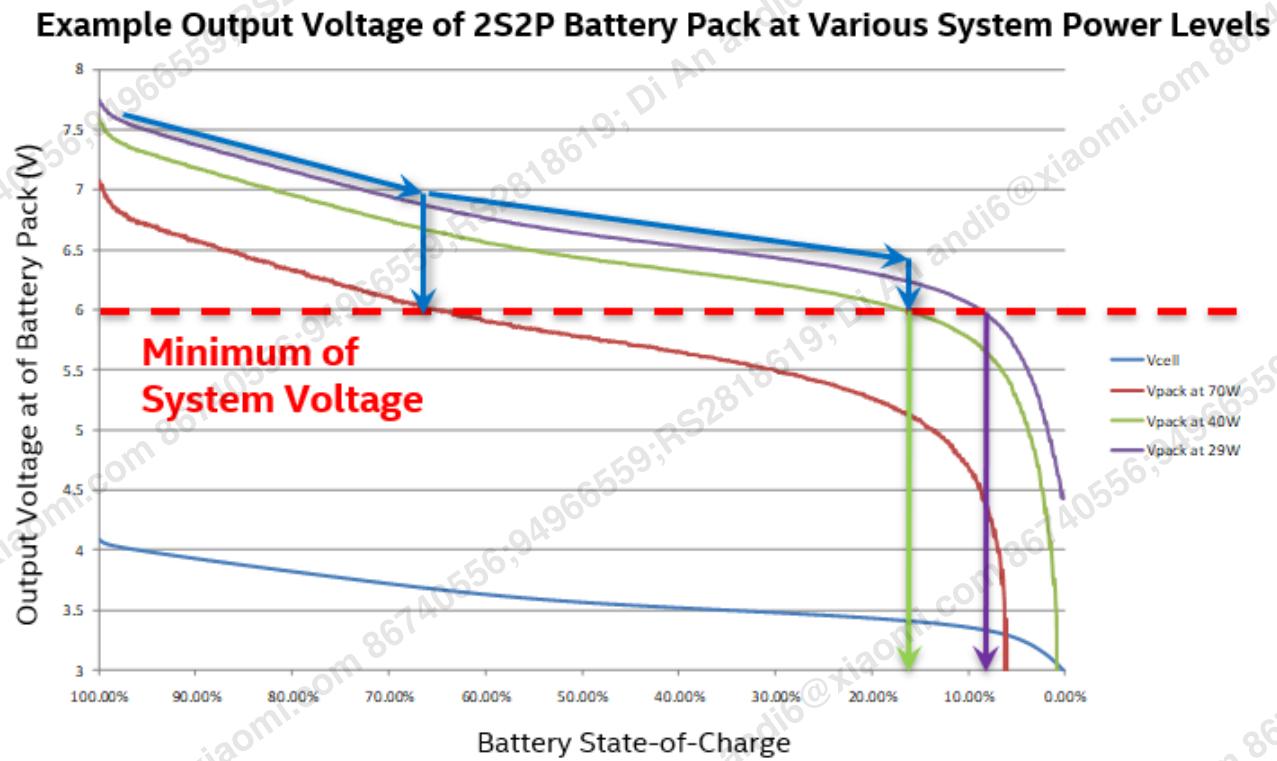
5.3.5 Intel® Battery Performance Optimizer (BPO) (Cont.)



- To extend Turbo in battery mode significantly, cell and pack resistance have to be kept as low as possible. `PackResistance()` is a complex function of frequency, state of charge, battery wear-out and cell temperature.

5.3.6 Setting PLx Power Levels with Intel® Battery Performance Optimizer (BPO)

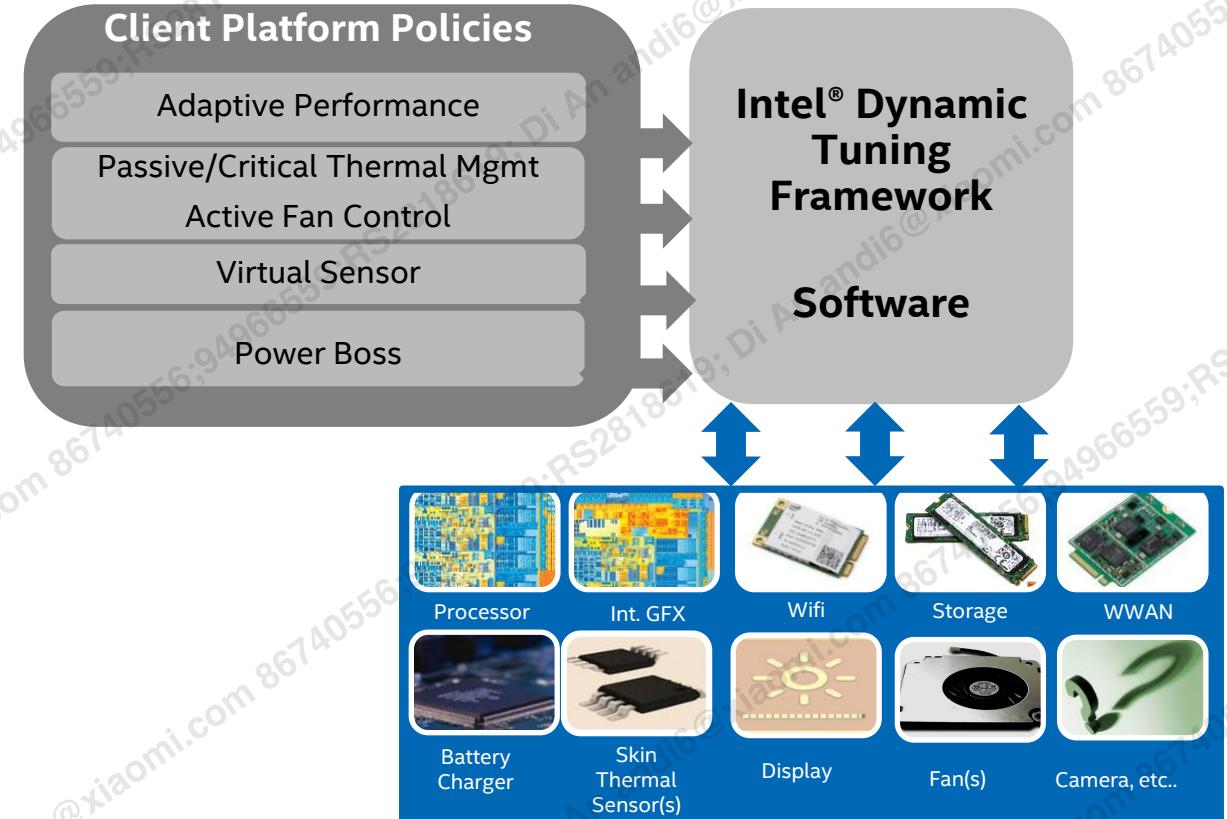
- Monitor battery pack power capability
- Use Fuel Gauge that supports BPO to account for time
- System needs to modulate the PLx parameters dynamically without compromising the system stability
- Enabled via Embedded Controller (EC) custom code



Fuel Gauge / System Controller will determine when/how to modulate CPU PLx on platform

5.3.7 Intel® Dynamic Tuning Introduction

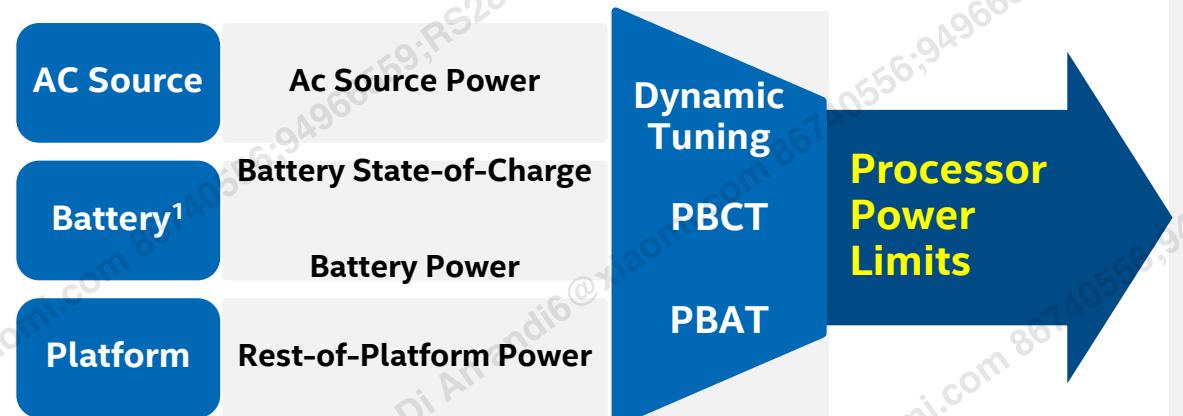
- Intel® Dynamic Tuning is a software solution for advanced thermal and power management.
- Cross Segment and cross OS.
- Built on standardized Intel-defined ACPI compliant Dynamic Tuning specification, it can also allow OS/App awareness of platform power/thermal conditions.
- Intel® Dynamic Tuning Enables Robust Platform Capabilities.
- Highly scalable and configurable solution for optimal power and thermal management.
- More comprehensive platform-level control based on skin temperature and other inputs.



5.3.8 Power Boss Policy Introduction

- IF **CONDITIONS**
 TRUE Then Calculate **MATH**
 Power Boss Conditions
 Table (PBCT) Power Boss
 Math Table
 (PBMT or VTMT) Then Do These **ACTIONS**
 Power Boss Actions
 Table (PBAT)
- Power Boss Policy is a condition-driven policy that adjusts the peak and steady state power draw of the platform components as a power delivery capability for the platform changes.
 - Power Boss Condition Table (PBCT) defines various system states or conditions to detect and act on.
 - Power Boss Action Table (PBAT) describes in detail the actions to perform.

Note: Refer to Intel® Dynamic Tuning Configuration Guide for OS/feature support matrix ([575150](#))



¹ Battery info provided by BPO

5.3.9 Simple Example: Power Boss Policy In Action

1

Condition Change
Event:

Evaluate each line in the PBCT following the ActionID sequence. The evaluation stops at the first TRUE line

2

PB Condition Table (PBCT)

ActionID	Minterm0	Operation0	Minterm1	Description
1	Power Source == AC	AND	Battery Percentage >= 5	AC present, battery > 5% charge
2	Power Source == DC	AND	Battery Percentage >= 10	On battery, battery > 10% charge
3	Power Source == DC	AND	Battery Percentage >= 5	On battery, battery 5% - 10% charge
4	Power Source == DC	AND	Battery Percentage >= 0	Fail safe condition

3

Perform all Actions for the first TRUE line in PBCT.

PB Action Table (PBAT)				Description
ActionID	Participant	Code	Argument	
1	TCPU	PL2PowerLimit	15000	P2 and PL4 are set to the default values when AC present
1	TCPU	PL4PowerLimit	30000	
2	TCPU	PL2PowerLimit	15000	P2 and PL4 are set to the default values when battery > 10% charge
2	TCPU	PL4PowerLimit	30000	
3	TCPU	PL2PowerLimit	10000	PL2 is reduced to 10 W whereas PL4 is reduced to 20 W when battery 5% - 10% charge
3	TCPU	PL4PowerLimit	20000	
4	TCPU	PL2PowerLimit	8000	None of the conditions in the PBCT are met, PL2 and PL4 are set to fail safe values
4	TCPU	PL4PowerLimit	8000	

Refer to Intel® Dynamic Tuning Technology (Intel® DTT) Feature Enabling User Guide ([572349](#)) for additional information.

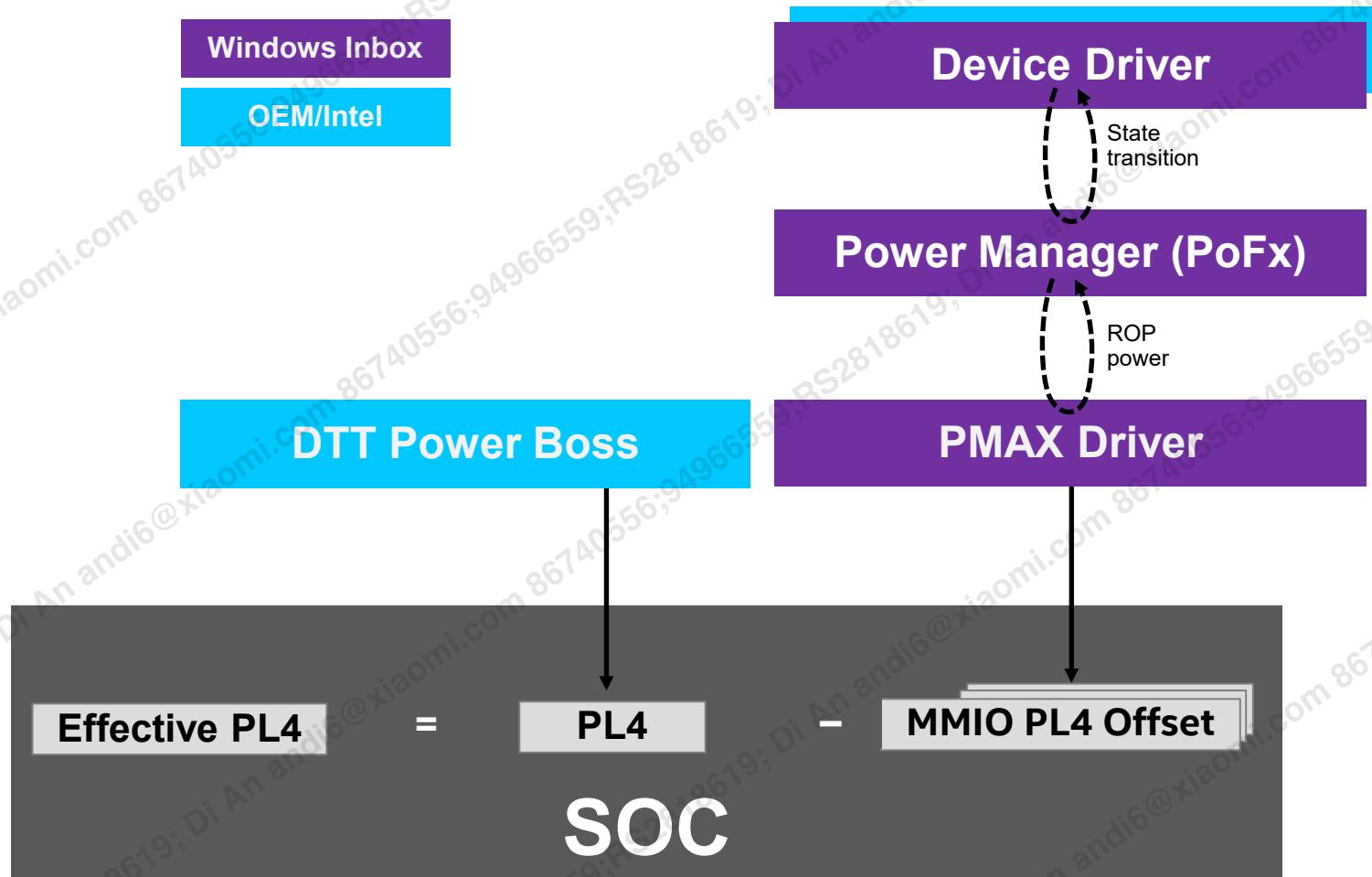
5.3.10 PL4 Platform (EC/PECI) Offset Background

- When a USB device is plugged into a system, it introduces additional power loading on the platform.
- This additional load may require reducing the SoC PL4 Power Limit to accommodate the load.
 - For example, a USB-C Thunderbolt connection could require up to 15W of power. In this scenario, the PL4 may need to be reduced by the amount of the USB-C TBT power draw.
- In order to provide dynamic PL4 control within the specific window, a PL4 Offset is provided in RPL, which is set by the embedded controller.
- The EC can be used to detect when an USB device is connected to the system and communicate the PL4 Platform Offset via PECL.

Command	Service Name	Index	Format	Default Value
Write through WrPkgConfig()	PL4 Platform Offset	72 (decimal)	Same as PL4_LIMIT (Index 60 decimal) : Only lower 13 bits are used, same power unit as others (1/8W as given in Package Power SKU Unit)	0

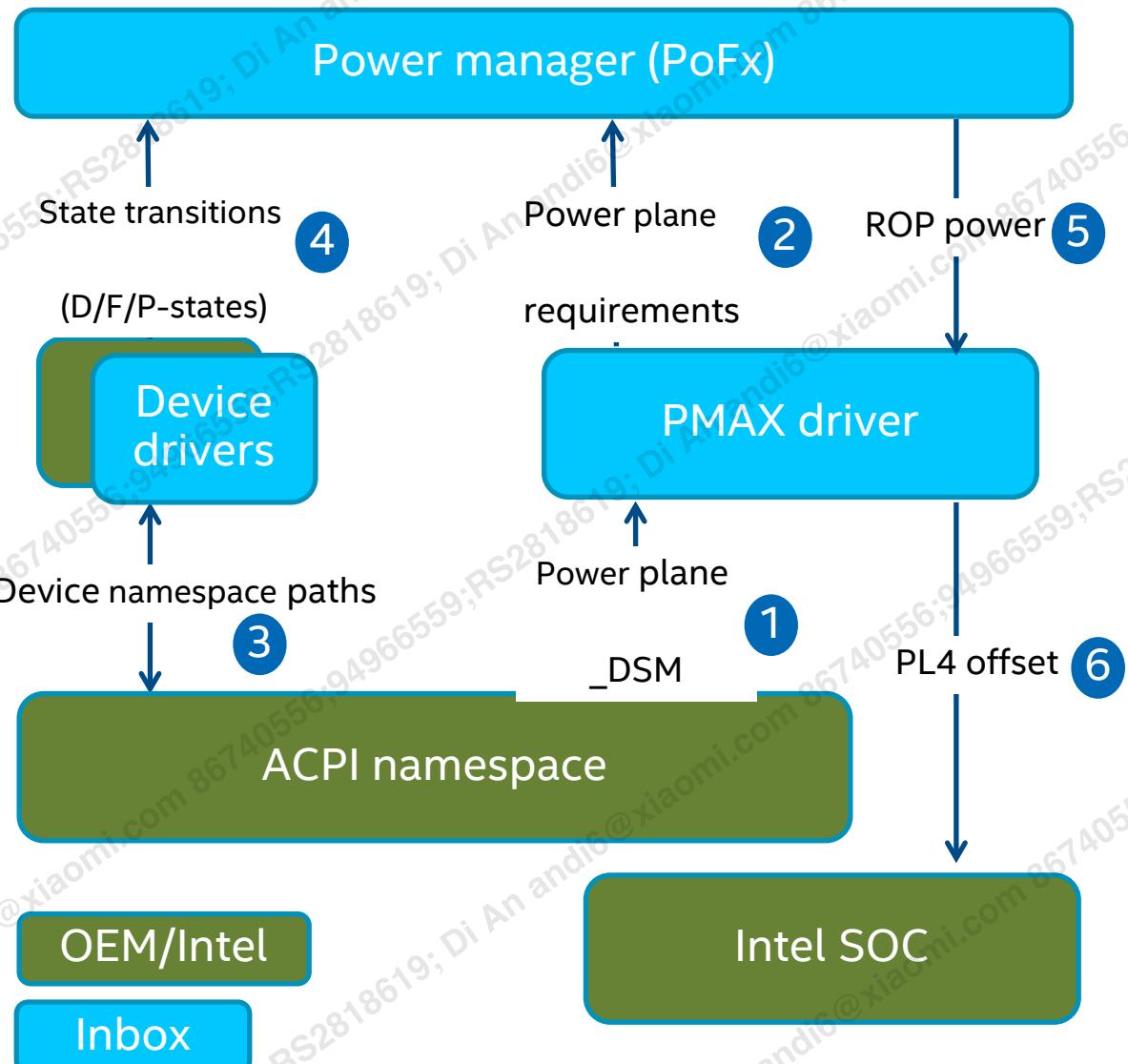
5.3.11 Windows* PMAX Driver: Maximize Performance when Platform Component is Idle

- **Windows* PMAX Driver** opportunistically maximizes the CPU Turbo performance when peripheral devices are in idle state
- Why two SW solutions?
 - **Windows* PMAX Driver** allows quick PL4 Offset adjustment (based on device power states) minimizing impact to QoS
 - **DTT Power Boss** allows quick deployment of Intel new control algorithms and OEM defined solutions



5.3.12 Windows* PMAX architecture

- Starting Windows* 10, 19H1, PoFx supports a new power plane concept for ROP computations
- PMAX driver is an inbox driver that owns PL4 offset register programming
- Platforms that need to opt-in to PMAX have to report power plane information through ACPI _DSM
- Device drivers need to opt into PoFx (Most drivers already do this)

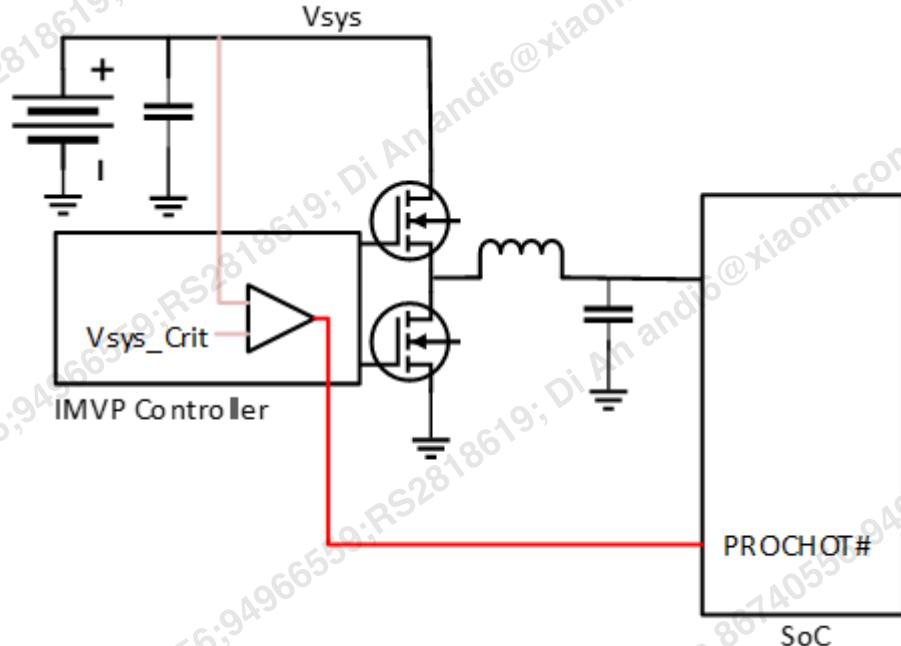
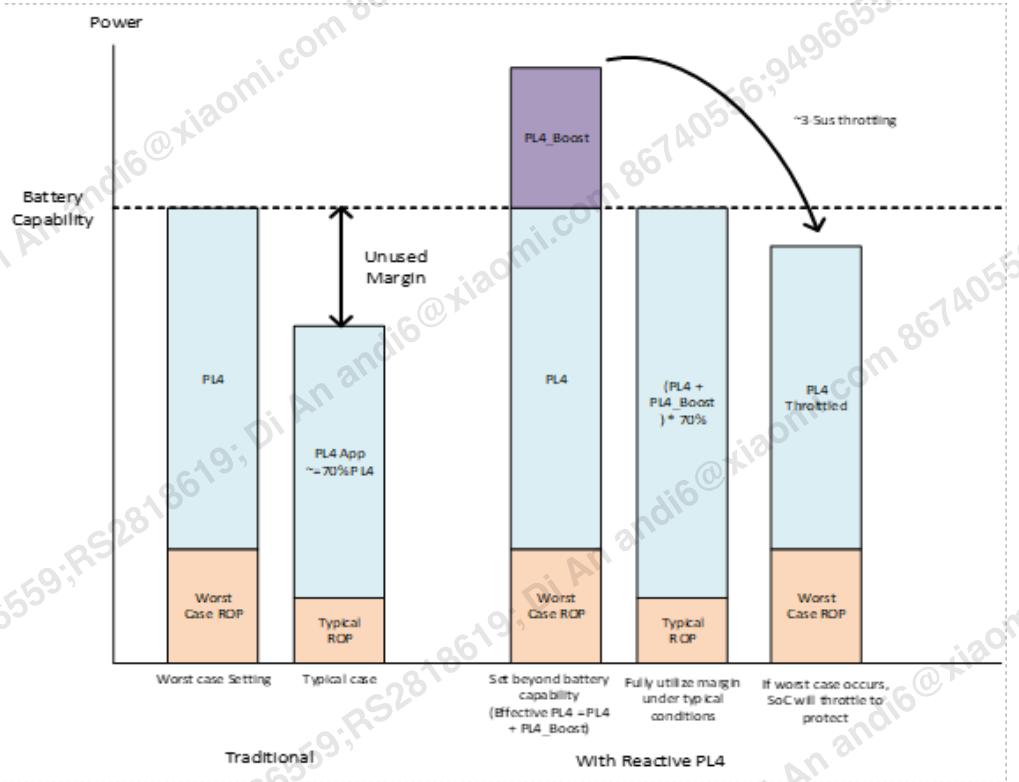


5.3.13 Fast V-Mode Technology

- Present IMVP VR Design Paradigm: IMVP VR FETs, inductors, & decoupling designed to support I_{CCMAX}
 - Required to ensure proper electrical performance for the target SoC performance
 - Results in large power components & power sources to support “rare” high current events that are atypical of realistic workloads
 - Majority of “real-life” workloads do not reach I_{CCMAX}
- What is Fast V-mode (FMV) and why implement it?
 - Fast reaction mechanism used to detect load currents that exceed a specified current threshold
 - Combines VR cycle by cycle current limiting AND SoC based voltage droop detection (CEP) to throttle the SoC during rare instances where SoC current exceeds $I_{CCMAX.APP}$
 - IMVP (FET & Inductors) and upstream power delivery infrastructure components can be sized for real life workload ($I_{CCMAX.APP}$)
 - Protects IMVP VR (FET & Inductors) and upstream power delivery infrastructure (battery & brick) from rare SoC high current events
 - **Customer Benefit: SoC performance of a system designed to full I_{CCMAX} using components sized for $I_{CCMAX.APP}$**
- A New IMVP VR Design Paradigm: VRs designed to $I_{CCMAX.APP}$ via support for Fast V-mode
 - Decoupling sized for traditional I_{CCMAX} to ensure proper electrical performance for the target performance
 - VR Power stage components and upstream power sources sized for realistic workloads ($I_{CCMAX.APP}$)

Fast V-mode allows SoC & upstream power delivery components sized for realistic workloads with minimal impact to realistic workload performance

5.3.14 Reactive PL4



- PL4 is budgeted considering worst case events
- Actual peak SoC power events are typically ~70-80% of PL4. Rest of Platform (ROP) is usually lower than worst case as well. This leaves room for power margin.
- Extra performance can be achieved with a higher effective PL4 (PL4 + PL4_Boost)

- The fast PROCHOT# mechanism protects the system from dropping below Vmin if worst case event occurs.

6.0 Turbo Control References

- 6.1 Turbo Control Parameter Setting Locations
- 6.2. Clipping Cause Encoding
- 6.3. Turbo Control Summary (Processor Level)
- 6.4. Turbo Control Summary (Platform Level)
- 6.5. Intel® Turbo Boost Technology 2.0 Control Summary
- 6.6. Turbo Control: Package Power
- 6.7. Turbo Control: Units Conversion
- 6.8. Turbo Control: Power/Energy Units
- 6.9. Turbo Control: Time Unit Example (Tau Time Unit Calculation)
- 6.10. Turbo Control: Time Unit Example (Tau Time Constant Calculation)
- 6.11. PECI Over eSPI
 - 6.11.1 PECI over eSPI Flows and Encapsulation Format

6.1 Turbo Control Parameter Setting Locations

- Unique Turbo Power Limits can be set independently in multiple programmatic interfaces and are non-mirrored
- Customers have full flexibility of how they want to set each limit
- The most limiting parameter in power/current limits will take precedence.
- **Example:** A system might have multiple unique settings in each interface (Refer to section 15 for details on parameters set up with MSR, MMIO and PECI)

- **MSR - BIOS** ideally initializes **static PL1, PsysPL1, PL3, PL4** to the highest levels that a system will ever want to support (using a lock bit to prevent exceeding).
- **PECI - EC** may **dynamically** update **PL2, PsysPL2, PL3, PL4** to a level that corresponds to power source capability (Example: scale setting with AC brick size).
- **MMIO - SW Drivers¹** may **dynamically** set **PL1 or PsysPL1** according to temperature sensors or advanced thermal management triggers (Example: scale PL1 with skin temperature).

Refer to Intel® Dynamic Tuning Technology Feature Enabling User Guide ([572349](#)) for additional information.

6.2. Clipping Cause Encoding

- MSR 0x64F IA_PERF_LIMIT_REASON

Bit	Name	Description
14	TVB	TVB(Turbo Velocity Boost) Status ,When set by PCODE indicates that TVB has caused reasons IA frequency Clipping
13	Turbo attenuation	Turbo attenuation (multi core turbo) Status, RO: when set by PCODE indicates that Turbo attenuation (multi core turbo) has caused IA frequency clipping.
12	Max Turbo Limit	Maximum turbo limit Status, RO: when set by PCODE indicates that Max turbo limit has caused IA frequency clipping
11	PBM PL2	PBM PL2, PL3 (pkg, platform) Status, RO: when set by PCODE indicates that PBM PL2 or PL3 (package or platform PL2 or PL3) has caused IA frequency clipping
10	PBM PL1	PBM PL1 (pkg, platform), RO: when set by PCODE indicates that PBM PL1 (package or platform PL1) has caused IA frequency clipping
9	FIVR TDC	
8	Other Limit such as VR_Imax or PL4	Other (IccMax, PL4, etc) Status, RO: when set by PCODE indicates that other has caused IA frequency clipping
7	VR_TDC Limit	VR TDC (Thermal design current) Status, RO: when set by PCODE indicates that VR TDC has caused IA frequency clipping
6	VR Thermal Alert	Hot VR (any processor VR) Status, RO: when set by PCODE indicates that Hot VR (any processor VR) has caused IA frequency clipping
5	RATL	Running average thermal limit Status, RO: when set by PCODE indicates that Running average thermal limit has caused IA frequency clipping
4	RSR LIMIT	Reliability stress Restrictor Status, RO: when set by PCODE indicates that Reliability stress restrictor has caused IA frequency clipping
3	Reserved	Reserved
2	Reserved	Reserved
1	Thermal Event	Thermal Status, RO: when set by PCODE indicates that Thermal event has caused IA frequency clipping
0	External PROCHOT#	PROCHOT# Status, RO: when set by PCODE indicates that PROCHOT# has caused IA frequency clipping

- The “Clipping Cause register” provides a method to report when and why a frequency is being limited (clipped).
- Intel’s TAT utility includes the ability to log clipping cause registers to help with debugging.
- These tables show the current bit encodings for Raptor Lake .

Status Bit Decoder

0 = Limit not reached
1 = Limit is currently reached

Log bits also exist. Refer FAS for more info

6.2 Clipping Cause Encoding (Cont.)

MSR 0x6B0 GT_PERF_LIMIT_REASONS

Bit	Name	Description
13	Reserved	Reserved
12	Inefficient operation	Inefficient operation, has caused GT frequency clipping
11	PBM_PL2	PBM PL2, PL3 (pkg, platform) Status, RO: when set by PCODE indicates that PBM PL2 or PL3 (package or platform PL2 or PL3) has caused GT frequency clipping
10	PBM_PL1	PBM PL1 (pkg, platform), RO: when set by PCODE indicates that PBM PL1 (package or platform PL1) has caused GT frequency clipping
8	Other Limit such as VR_Imax or PL4	Other (IccMax, PL4, etc) Status, RO: when set by PCODE indicates that other has caused GT frequency clipping
7	VR_TDC Limit	VR TDC (Thermal design current) Status, RO: when set by PCODE indicates that VR TDC (Thermal design current has caused GT frequency clipping
6	VR Thermal Alert	Hot VR (any processor VR) Status, RO: when set by PCODE indicates that Hot VR (any processor VR) has caused GT frequency clipping
5	RATL	Running average thermal limit Status, RO: when set by PCODE indicates that Running average thermal limit has caused GT frequency clipping
4	Reserved	Reserved
3	Reserved	Reserved
2	Reserved	Reserved
1	Thermal Event	Thermal Status, RO: when set by PCODE indicates that Thermal event has caused GT frequency clipping
0	External PROCHOT#	PROCHOT# Status, RO: when set by PCODE indicates that PROCHOT# has caused GT frequency clipping

MSR 0x19C (IA32_THERM_STATUS)

Bit	Name
14	Cross-domain Limit (for example: GFX driver)
12	Current Limit

Status Bit Decoder

0 = Limit not reached
1 = Limit is currently reached

Log bits also exist. Refer FAS for more info

6.3 Turbo Control Summary (Processor Level)

ReadWrite Parameters



- Customizable Turbo Power Limits (Only if PLATFORM_INFO MSR (0CEh) Bit 29 is set to 1)

	Description	MSR (for initialization)	PECI (for real time control)	Comment
Set based on platform characteristics	Processor Power Limit 1 (PL1)	TURBO_POWER_LIMIT (0x610) Default: Enabled (1 s Time Constant)	Index 26 (R/W) Default: Disabled	Use default or set to thermal solution limit
	Processor Power Limit 1 Time Constant (Tau)			Runtime changes not recommended
	Processor Power Limit 2 (PL2)	TURBO_POWER_LIMIT (0x610) Default: Enabled	Index 27 (R/W) Default: Disabled	Must enable Power Limit 2 (Enabled by default in PPMRC)
	Processor Power Limit 3 (PL3)	PLATFORM_POWER_CONTROL (0x615) Default: Disabled	Index 57 (R/W) Default: Disabled	Refer Power Delivery Section for more details on this protection mechanism
	Processor Instantaneous Power Limit (PL4)	VR_CURRENT_CONFIG (0x601)	Index 60 (R/W) Default: Disabled	PL4 Limit
	VR Peak Current Limit (ICC_Max)	N/A - BIOS Mailbox	None	Can be set lower for under-designed power delivery (expect some performance reduction)
	VR TDC Current Limit (VR_TDC)	N/A - BIOS Mailbox	None	Set to VR thermal design limits sustainable for 1s of seconds
	Processor Temperature Limit_Offset (TCC_Offset)	TEMPERATURE_TARGET (0x1A2) Default: 0	Index 16 (TCC Settings)	If using CPU as a proxy for skin temperature, should use appropriate Tau. Tcc_Offset Tau is not Tj_Avg Tau.
	Processor Avg Temp Reporting (Tj_Avg_)		Index 47	Also can be read through MMIO: Tj_Avg: MCHBAR+0x7200 [22:16] Tj_Avg Tau: MCHBAR+0x5820 [31:25]

Refer to Quick Reference to the EDS, FAS and PECI Implementation Guides

6.4 Turbo Control Summary (Platform Level)

Read/Write Parameters



- All of these features require the implementation of a Psys capable charging controller

	Description	MSR (for initialization)	PECI (for real time control)	Comment
Set based on platform characteristics	Platform Power Limit 1 (PsysPL1)	PLATFORM_POWER_LIMIT (0x65C) Default: Disabled (1s Time Constant)	Index 58 Default: Disabled Read/Write	Use default or set to system total power dissipation limit
	Platform Power Limit 1 Time Constant (Tau)			Runtime changes not recommended
	Platform Power Limit 2 (PsysPL2)	PLATFORM_POWER_LIMIT (0x65C) Default: Disabled	Index 59 Default: Disabled Read/Write	Set to the AC brick power rating
	Platform Power Limit 3 (PsysPL3)			See Power Delivery Section for more details on this protection mechanism *Note, same interface as PL3, PsysPL3 will be used if Psys is enabled

Refer to Quick Reference to the EDS, FAS and PECI Implementation Guides

6.5 Intel® Turbo Boost Technology 2.0 Control Summary

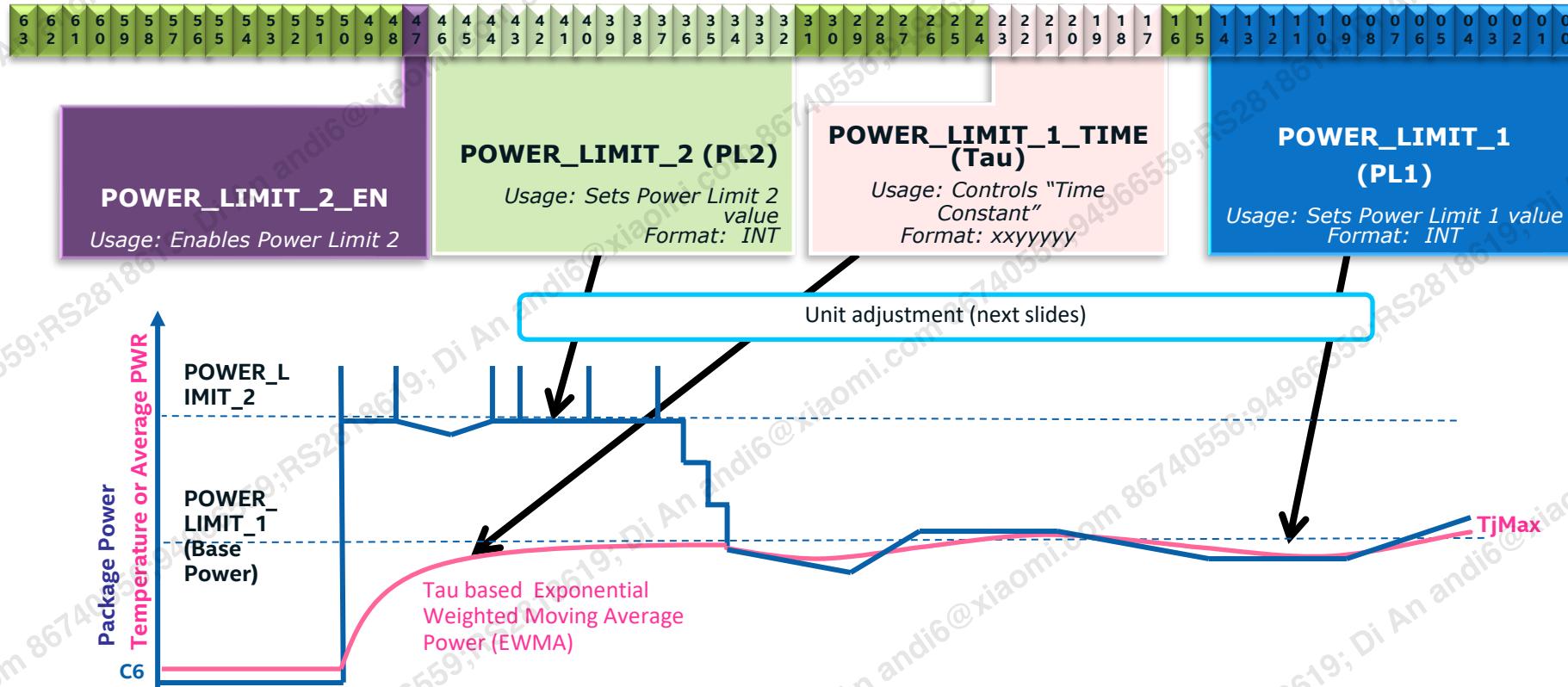
Read Only Parameters

	Description	MSR	PECI	Comment
No action required	Power and time units	PACKAGE_POWER_SKU_UNIT (0x606h)	Index 03 Read Only	Read only
	Processor Energy Counters	PACKAGE_ENERGY_COUNTER (0x611h, 0x639h, 0x641h)	Index 03 Parameters 0xFF, 0x00, 0x01 Read Only	Read only
	System Energy Counter	PLATFORM_ENERGY_COUNTER (0x64D)	Index 03 Parameter 0xFE Read Only	Read only, requires Psys supported charging controller
	SKU Specific Limits	PACKAGE_POWER_SKU (0614h)	Index 28 Index 29 Read Only	Read only

Refer to Quick Reference to the EDS, FAS and PECI Implementation Guides

6.6 Turbo Control: Package Power

MSR 0x610: TURBO_POWER_LIMIT (RW/L)
PECI: PKG_TURBO_POWER_LIMIT ([WrPkgCfg/RdPkgCfg\[27:26\]](#))



Package PBM Controls Contained in a Single Register

6.7 Turbo Control: Units Conversion

MSR 0x610: TURBO_POWER_LIMIT (RW/L)

PECI: PKG_TURBO_POWER_LIMIT (WrPkgCfg/RdPkgCfg[27:26])



POWER_LIMIT_2

Usage: Sets Power Limit 2 value
Format: INT * POWER_UNIT

POWER_LIMIT_1_TIME

Usage: Controls "Time Constant"
Format: xxYYYYYY

POWER_LIMIT_1

Usage: Sets Power Limit 1 value
Format: INT * POWER_UNIT

Power and time values are scaled by values in the "SKU_UNIT" register to convert to physical values

$$\text{LIMIT} * \text{UNIT} = \\ \text{Values in "real" units}$$

Power, Watts
(1/8 W units)

"Time Constant"
(0.976 ms units)

Power, Watts
(1/8 W units)

MSR 0x606: PACKAGE_POWER_SKU_UNIT (RO)

PECI: PKG_POWER_SKU_UNIT (RdPkgCfg[30])



Read only
Register

6.8 Turbo Control: Power/Energy Units

MSR 0x606: PACKAGE_POWER_SKU_UNIT (RO)
PECI: PKG_POWER_SKU_UNIT ([RdPkgCfg\[30\]](#))



- Unit of Energy is the increment in energy used by controls

Unit of Energy = $1/(2^{\text{ENERGY_UNIT}})$ Joules

Example: Default = 0x0Eh = 14_{10} , Unit of Energy = $1/2^{14} = 61 \mu\text{Joules}$

- Unit of Power is the increment in power used by controls

Unit of Power = $1/(2^{\text{POWER_UNIT}})$ Watts

Example: Default = 0x3h = 3_{10} , Unit of Power = $1/2^3 = 1/8 \text{ W}$

6.9 Turbo Control: Time Unit Example (Tau Time Unit Calculation)

MSR 0x606: PACKAGE_POWER_SKU_UNIT (RO)
PECI: PKG_POWER_SKU_UNIT ([RdPkgCfg\[30\]](#))



- Unit of Time is the increment in time used by controls
 - Unit of Time = $1/(2^{\text{TIME_UNIT}})$ Seconds
- **Example**
 - The default value is 0xAh (1010b)
 - 0xAh = 10 Decimal
 - Unit of Time = $1/2^{10} = 1/1024 = 0.000976 \text{ s} = 0.976 \text{ ms}$
- **Results**
 - 0.976 ms will be multiplied by all other time parameters to resolve time in "ms"

Continued...

6.10 Turbo Control: Time Unit Example (Tau Time Constant Calculation)

MSR 0x610: TURBO_POWER_LIMIT (RW/L)

PECI: PKG_TURBO_POWER_LIMIT ([WrPkgCfg/RdPkgCfg\[27:26\]](#))



$$\text{Time Constant} = (1 + (0.25 * X)) * 2^y * \text{"Unit of Time"}$$

Example of possible values

- Assume POWER_LIMIT_1_TIME (MSR 0x610[23:17]) = 0xAh
 - 0xAh = 001010b, so x = 00 and y = 1010b = 10 decimal
- From the previous example, where the time unit = 0.976 ms
- Time Constant = $1.0 * 2^{10} * 0.976 \text{ ms} = 1 \text{ second}$

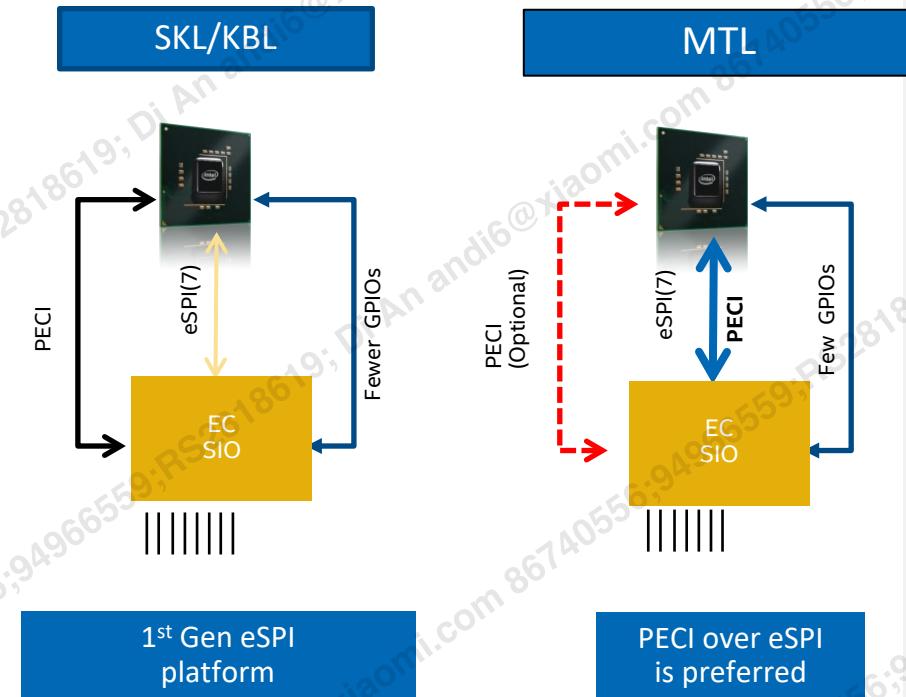
Package and VR time constants will differ but utilize same "Unit of Time"

X	Y	(Sec)
11	00110	0.11
00	01010	1
01	01010	1.25
10	01010	1.5
11	01010	1.75
00	01011	2
01	01011	2.5
10	01011	3
11	01011	3.5
00	01100	4
01	01100	5
10	01100	6
11	01100	7
00	01101	8
01	01101	10
10	01101	12
11	01101	14
00	01110	16
01	01110	20
10	01110	24
11	01110	28
00	01111	32
01	01111	40
10	01111	48
11	01111	56
00	10000	64

XX	YYYY	seconds
00	00000	0.001
00	00001	0.002
10	00001	0.003
00	00010	0.004
01	00010	0.005
10	00010	0.006
11	00010	0.007
00	00011	0.008
01	00011	0.01

6.11 PECL Over eSPI

- RPL has hardware changes to save the package pins
- Background: PECL is a slow bus; due to limited BW and latency issues, customers/design engineer mainly use it for thermal data and a bit of dynamic processor control.
- Benefits:
- Responsiveness: Extremely fast access to PECL functionality for better use
- Legacy removal: Paves the way for removal of PECL pin in ICL and beyond
- Convergence:
 - Better architectural alignment with Intel segments
 - Fast PECL access for server/workstations
- Efficiency:
 - Resource savings: PECL platform validation, debug, sightings

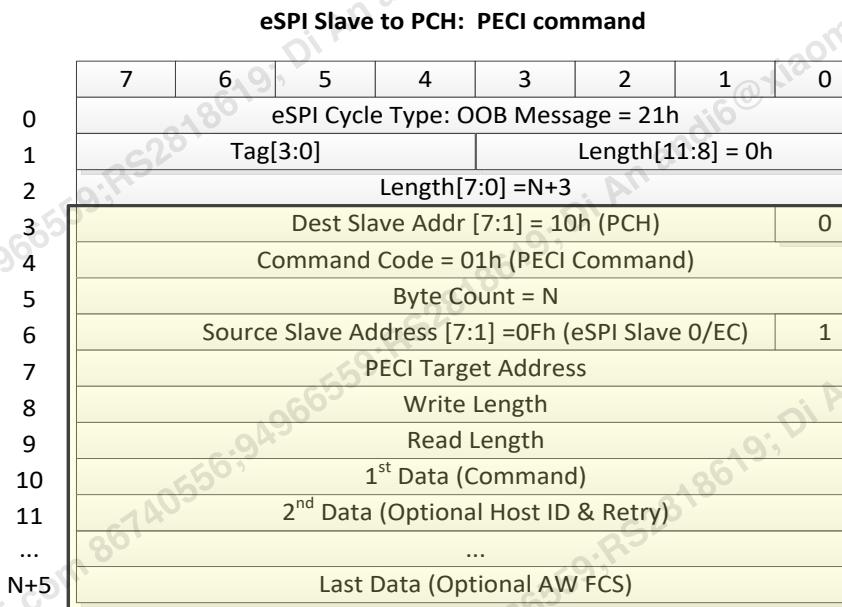


Note: Refer to Raptor Lake S Platform Controller Hub External Design Specification Volume 1 of 2 ([619362](#)) for more information

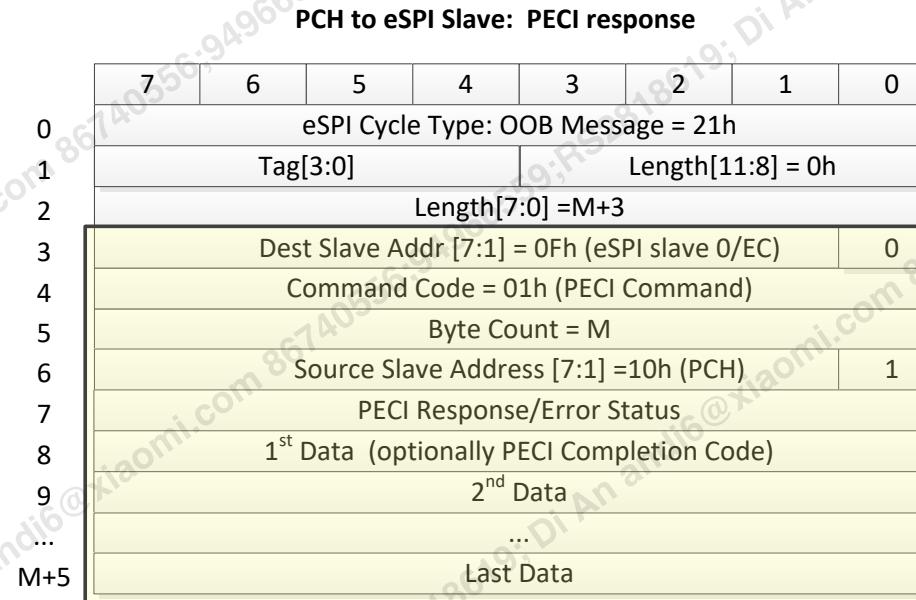
6.11.1 PECl over eSPI Flows and Encapsulation Format

PECl over eSPI Flow

1. EC encapsulates the PECl command as shown below in an eSPI OOB upstream packet and indicates an eSPI_OOB_avail to PCH.
2. PCH fetches the OOB packet from EC.
3. PCH processes the received PECl OOB command.
4. PCH generates the PECl responses and returns it using eSPIOOB PUT_OOB cycle.



header
PECl Command



header
PECl Command

MTL Supported Commands

PECl Command	Client
Ping()	Yes
GetDIB()	Yes
GetTemp ()	Yes
RdPkgConfig()	Yes
WrPkgConfig()	Yes
RdIAMS(R)	Yes

Note: Refer MTL PCH EDS and MTL PDG Doc #TBD for more information

7.0 cTDP Design Considerations

- 7.1 Configurable Processor Base Power (TDP) (cTDP) Introduction
 - 7.1.1 High-Level Flow of cTDP Operation
 - 7.1.2 Intel Speed Shift Enabled
 - 7.1.3 Designing to Intermediary cTDP Points
 - 7.1.4 Processor Base Power (TDP) CTC/ Power Limiting Relationship
 - 7.1.5 cTDP P-State/ TAR Relationship
- 7.2 High-Level Flow of cTDP Operation and Implementation Options
 - 7.2.1 EC Control Implementation Option
 - 7.2.2 BIOS Control Required Settings
- 7.3 cTDP Registers Summary

7.1 Configurable Processor Base Power (TDP) (cTDP) Introduction

- Config TDP (cTDP) provides an option to modify the Base frequency and Base Power (TDP) of the CPU within the specific values posted on the product specification page, <https://ark.intel.com>.
- Config TDP should be based on platform power, thermal and chassis capabilities. The computer manufacturer may increase or decrease Base Frequency and Base Power.
- Maximum/Minimum Assured Power has a frequency and corresponding Base Power that is higher/lower than the processor IA core Base Frequency and SKU Segment Base Power.
- Config TDP is an optional feature that may be added depending on product and SKU.
- Intel® Dynamic Tuning Technology (Intel® DTT) does not support cTDP starting CML and beyond.

Only valid for systems running windows with speed shift disabled

7.1.1 High-Level Flow of cTDP Operation

System triggers new mode of operation

- Examples: Power scheme change, HW button, docking situation change, BIOS setting update and so on.

Platform selects **CONFIG_TDP_CONTROL**

- Sets the cTDP point (Level 0, Level 1, Level 2)

Platform reconfigures **PL1/PL2**

- Sets the turbo power limits to the cTDP point

Setup **TURBO_ACTIVATION_RATIO**

- Selects the ratio above which CPU can activate turbo

Platform notifies OS of new frequency limit via **_PPC**

- Sets the OS controlled frequency range

Explanation

Configuration where turbo ends

- PL1 and PL2 define HW power limits that will reduce turbo frequency
- CTC¹ redefines the lowest frequency the processor can clamp down to when a PL1/PL2 limit is reached

Configuration where turbo starts

- PPC tells the OS the max P-state it can request
- TAR² redefines the lowest frequency that the processor PCU can initiate turbo that corresponds with the _PPC setting

¹CTC is CONFIG_TDP_CONTROL

²TAR is TURBO_ACTIVATION_RATIO

Only valid for systems running windows with speed shift disabled

7.1.2 Intel® Speed Shift Enabled

- If Intel® Speed Shift technology is enabled, the OS handles a notification on the change and re-enumerates the current Base Power ratio level.
- PL1 levels can only be changed.
- Changing TAR, CTC, PPC will not have any impact when Intel Speed Shift technology is enabled.

¹CTC is CONFIG_TDP_CONTROL

²TAR is TURBO_ACTIVATION_RATIO

7.1.3 Designing Intermediary Base Power Points

Specified Base Power Points
12 W/15 W/28 W

Example Base Power level 1

- PL1 = 15 W
- CTC = 0
- TAR = 15
- PPC = P6

Desired Base Power Point
20 W



Example Unique Point

- PL1 = 20 W
- CTC = 0
- TAR = 15
- PPC = P6

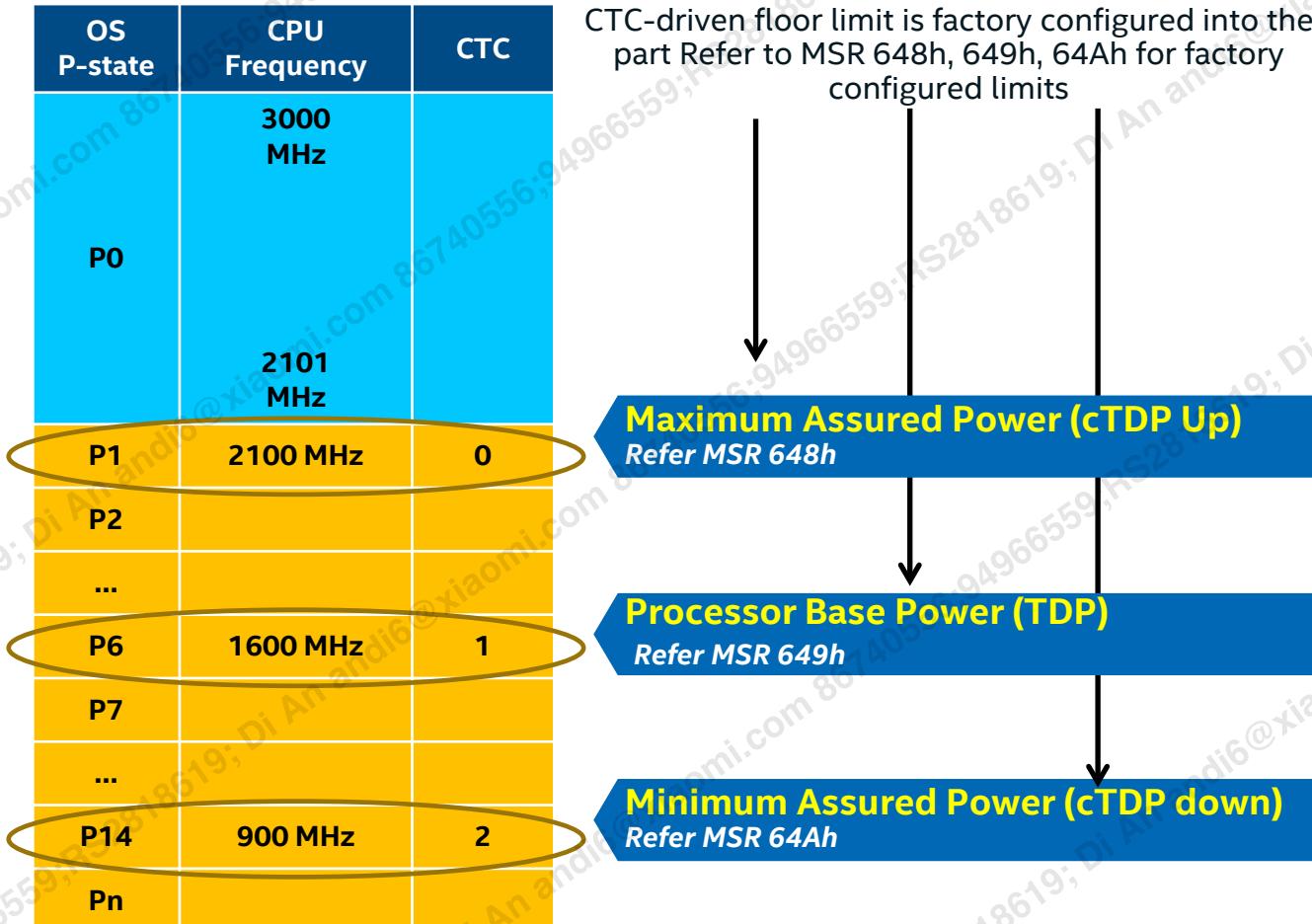
Example Base Power level 0

- PL1 = 28 W
- CTC = 2
- TAR = 20
- PPC = P1

Customer can configure the desired base power.

Only valid for systems running Windows* with speed shift disabled

7.1.4 Processor Base Power (TDP) CTC / Power Limit Relationship



Note: Frequencies and power numbers shown are for example only

Only valid for systems running Windows* with speed shift disabled

7.1.5 cTDP P-State/TAR Relationship

P0 is Historic Turbo Operation Region

Normally Turbo only operates when OS requests P0 (non-cTDP parts)

PPC (ACPI Perf Present Capabilities Obj)

cTDP will redefine the **maximum P-state** the OS can request (ceiling), defining the OS selectable frequency range

OS P-state	CPU Ratio
P0	30
...	...
P2	22
P1	21
...	...
P6	20
P7	16
...	...
P14	15
Pn	9
	8

cTDP Turbo Region

TAR (Turbo_Activation_Ratio)

Redefines where Turbo can start operation from (highest frequency ratio CPU should treat as request for no turbo)

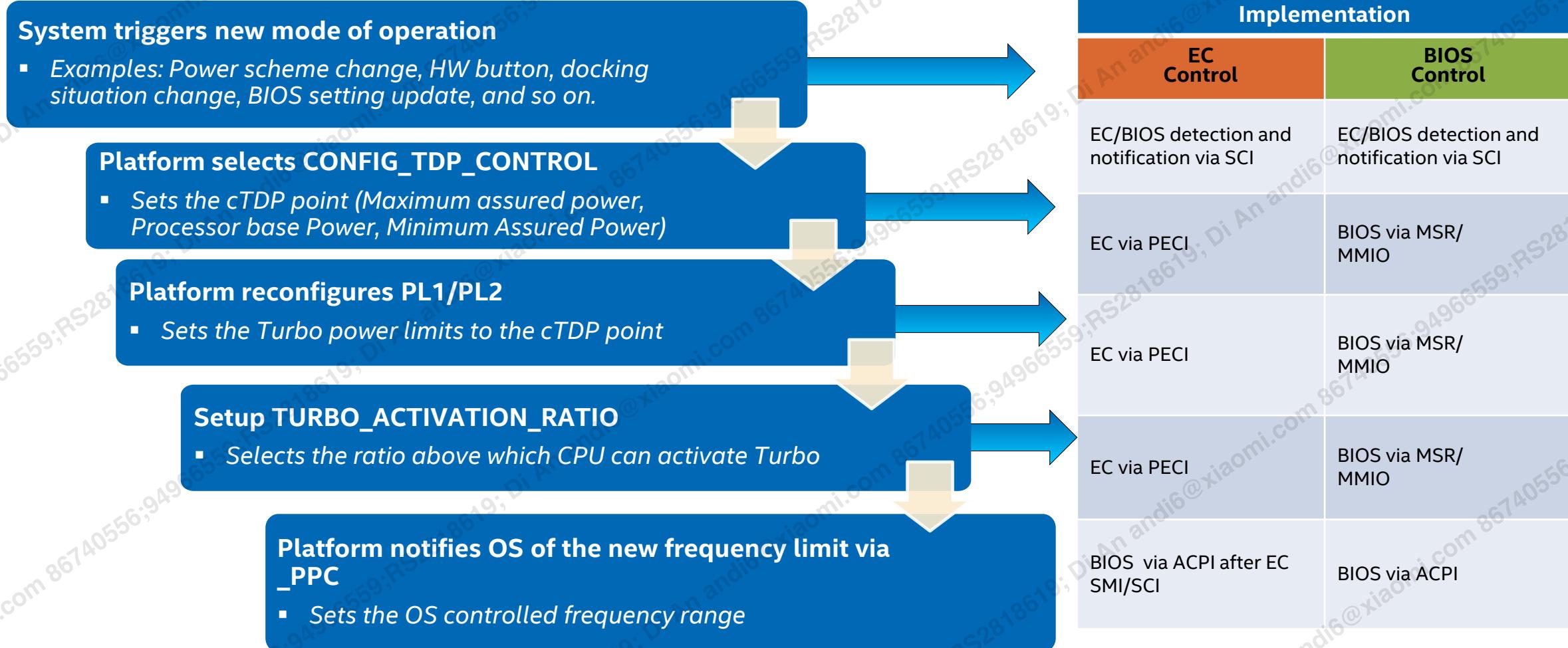
PPC and TAR redefine when Turbo can begin



Note: Frequencies and power numbers shown are examples only

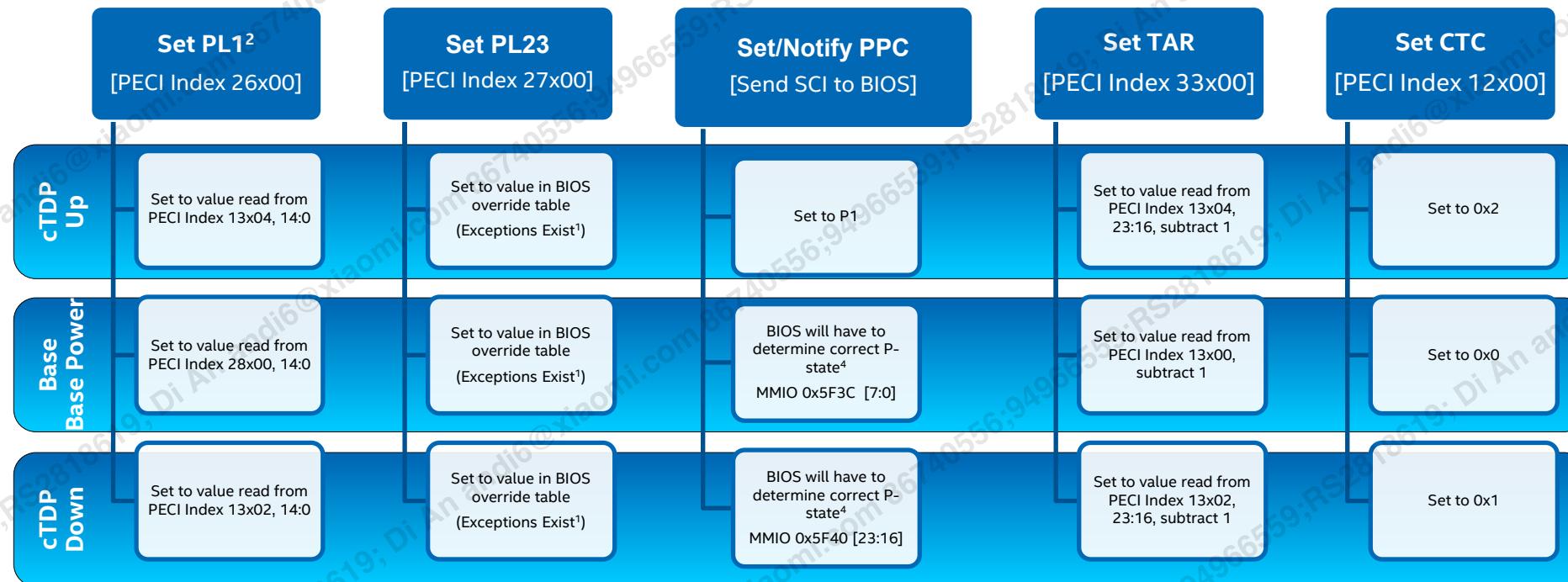
Only valid for systems running Windows* with speed shift disabled

7.2 High-Level Flow of cTDP Operation and Implementation Options



Only valid for systems running Windows* with speed shift disabled

7.2.1 EC Control Implementation Option



¹PL2 should be set in-line with maximum power-delivery sustained power capability. As such, the PL2 should remain at the default level even with cTDP change if the system can support it for maximum performance.

²Must also set Tau and enable bit; for example: 0x00DC80C8.

³Must also set enable bit; for example: 0x000080FA.

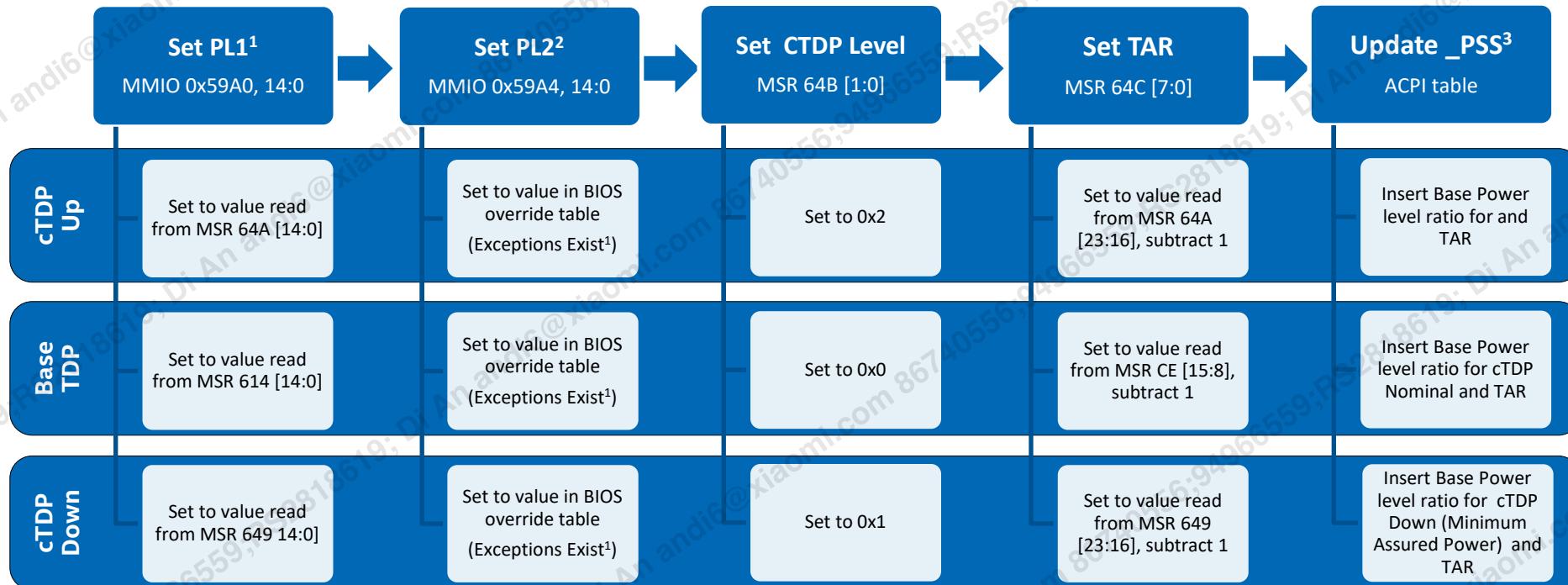
⁴BIOS looks up ratio, sets PPC to that level. If ratio is not in p-state table, set p-state to next higher ratio.

Notes:

- Moving to higher Base Power Order: PL1 → PL2 → PPC → TAR → CTC.
- Moving to lower Base Power Order: CTC → TAR → PPC → P21 → PL1.
- Refer Raptor Lake FAS for more details.

Only valid for systems running Windows* with speed shift disabled

7.2.2 BIOS Control Required Settings



¹MMIO PL1 value will match the desired cTDP boot level PL1 value. BIOS must choose what cTDP level to boot with.

²The PL2 level will be the same for all cTDP levels for a given CPU.

³Only applies to legacy Intel Speed Step Technology. Not applicable when using Intel Speed Shift.

Note: Refer to Raptor Lake FAS (TBD) for more details.

Only valid for systems running Windows* with speed shift disabled

7.3 cTDP Registers Summary

Read Only Registers

Register Name	Description	Comments
PLATFORM_INFO MSR: 0xCE PCI: No Interface	CONFIG_TDP_NUM_LEVELS [34:33] This register is used to discover the Configurable Base Power capability and indicates number of available cTDP points	0 = Feature not supported and only one Base Power point exists (as defined by existing PACKAGE_POWER_SKU MSR)
CONFIG_TDP_NOMINAL MSR: 0x648 PCI: Index 13 Parameter 0	This register provides the details of the Base Power point for which the processor point was designed	The information includes the Base TDP and the spec frequency associated with the Base TDP point
CONFIG_TDP_LEVEL_1 CONFIG_TDP_LEVEL_2 MSR: 0x649 and 0x64A PCI: Index 13 Parameter 2, 3, 4, 5	This register is used to discover the Configurable Base Power frequencies and the corresponding Base Power power	Details of the additional Configurable Processor Base Power (TDP) points like the Package TDP value, the spec frequency, and max/min power limits values for each
PACKAGE_POWER_SKU MSR: 0x614 PCI: Index 28	PACKAGE_TDP_POWER [14:0] This register indicates the 'Base Base Power' value of the part	Max and min turbo power limits for part
CONFIG_TDP_CONTROL MSR: 0x64B PCI: Index 12 MMIO: MCHBAR 0x5F50	Used to select and read current Base Power point	This register picks the Base Power point that the processor should control and includes a lock bit to allow for static configurations
TURBO_ACTIVATION_RATIO MSR: 0x64C PCI: Index 33 MMIO: MCHBAR 0x5F54	Used to select the frequency ratio above which processor can activate Turbo	When the OS requested frequency ratio is above the TURBO_ACTIVATION_RATIO, then Turbo is activated and Turbo algorithms take over
TURBO_POWER_LIMIT MSR: 0x610 PCI: Index 26,27 MMIO: MCHBAR 0x59A0/A4	The existing TURBO_POWER_LIMIT register as defined for the processor allow for cTDP to define new power limits	PL1 – Long term power limit PL2 – Short term power limit

Registers supported in MSR, PCI, and MMIO

Note: Refer to Raptor Lake BIOS Writers Guide and for additional information.

Only valid for systems running Windows* with speed shift disabled

8.0 Software Tools

- 8.1 Turbo/Thermal Power Related Test Tools
- 8.2 Tools: Intel PECI Stress Tool
- 8.3 Setting PL2 vis PECI Stress Tool
- 8.4 Validate PL2 PECI Settings with RdPkgConfig()
- 8.5 Setting PL1 and TAU via PECI Stress Tool
- 8.6 Validate PL1 and TAU PECI settings with RdPkgConfig()
- 8.7 Power Thermal Analysis Tool (PTAT)
 - 8.7.1 PTAT Key Features
- 8.8 Power Meter Introduction
 - 8.8.1 Power Meter Tool Hardware Architecture
 - 8.8.2 Power Meter Tool Software Architecture

8.1 Turbo/Thermal Power Related Test Tools

Software Tool	Usage
PECI Stress Tool	<p>Testing PECI interface, writing and reading values over PECI bus using GUI interface *Requires use of PTID specifications. Contact Intel representatives for additional information.</p>
Power Thermal Analysis Tool (TAT)	<p>Mobile/Desktop Thermal Test Tool Provides Base Power-level software activity while collecting key thermally relevant parameters.</p>

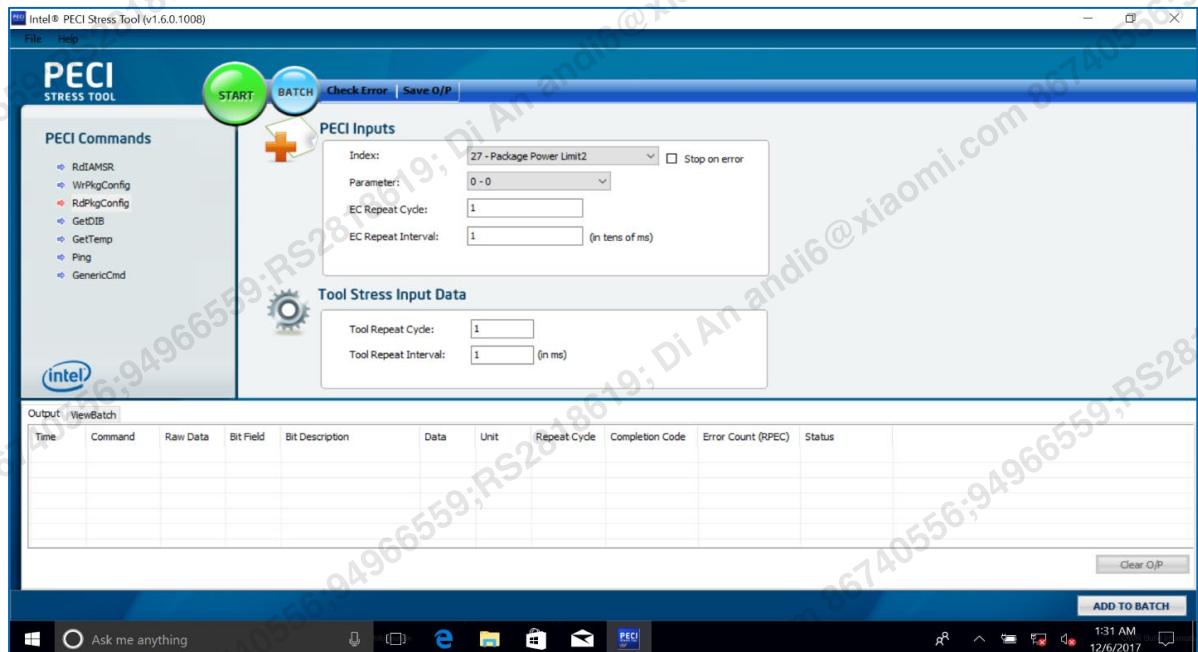
8.2 Tools: Intel PECL Stress Tool

- Intel® has created PECL validation tools:
 - Can be used to validate EC and PECL functionality on CRB platforms.
 - Requires EC/BIOS Firmware support on non-CRB platforms. No extra hardware required. BIOS should implement PTID soft device. The code is available as part of BIOS reference code.
 - Some functionality may be limited with SIO on Sugar Bay.
- GUI based tool:
 - Utilizes custom EC/BIOS firmware intermediate/field to expose PECL commands to the application.
 - Supports most of the Raptor Lake processor PECL commands.
- Specification:
 - Firmware Interface Specification described in RS-Power and Temperature Instrumentation ACPI Device Firmware Architecture Specification (FAS).
 - Reference Number: 27878

8.2 Tools: Intel PECL Stress Tool (Cont.)

■ Features

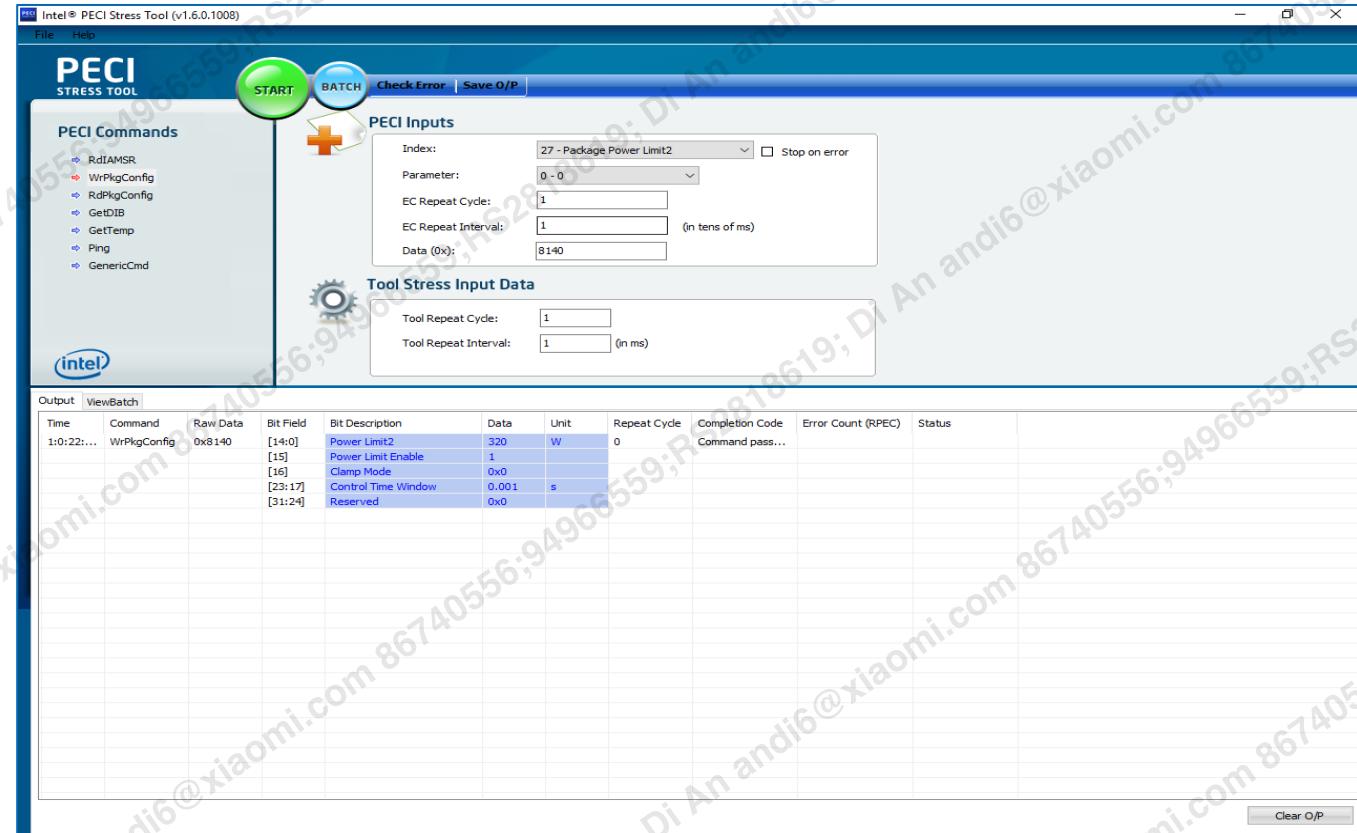
- Conforms to interfaces defined in RS-Power and Temperature Instrumentation ACPI Device Firmware Architecture Specification (FAS).
- Batch Execution of PECL commands.
- Ability to repeat command execution for several cycles.
- Ability to save output of the PECL command execution to a text file.



Note: Validation of PECL set limits assumes that BIOS set limits are higher than PECL limits.

8.3 Setting PL2 via PECL Stress Tool

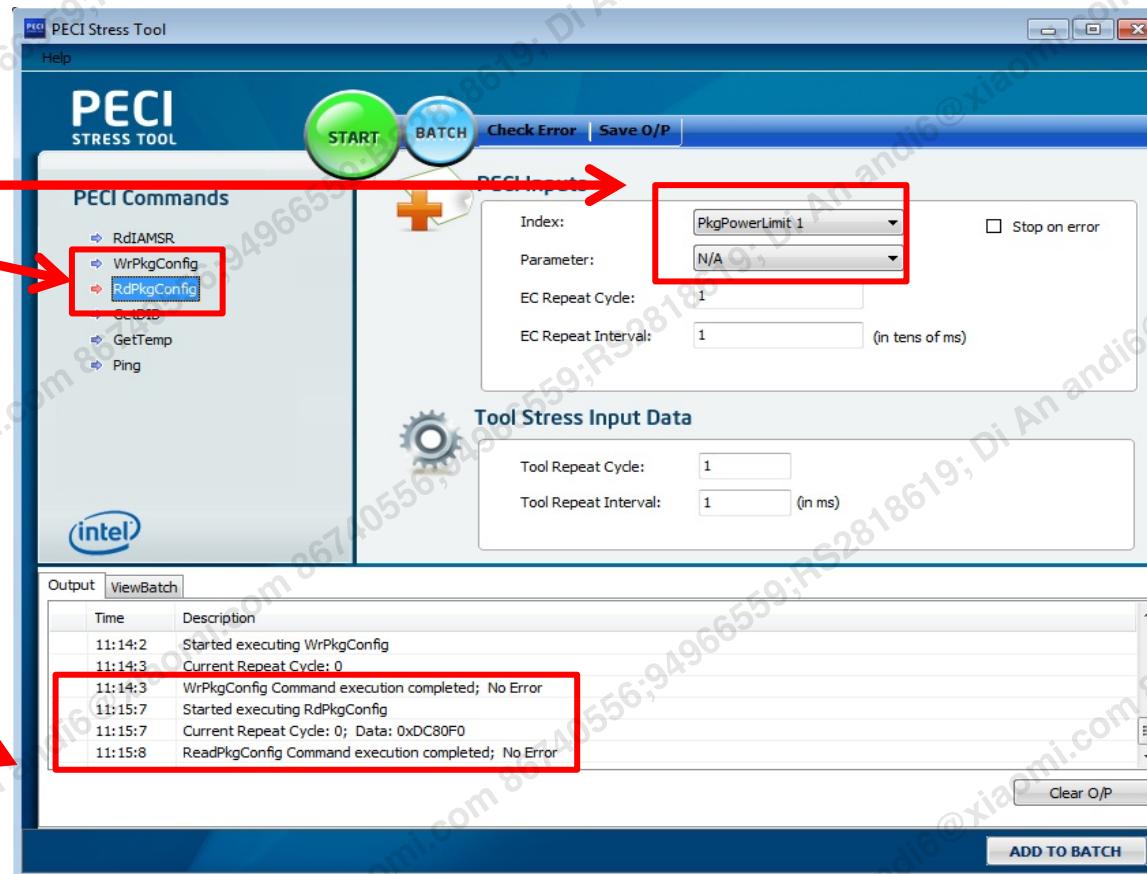
- Format is identical to MSRs.
- 1/8 W units
 - Ex. Program 40W to PL2
- $40.0 \text{ W} * 8 = 320 \text{ PECL power units}$
- $320d = 140h$
- So program **0x8140**, where 8h = 1000b represents an enabled bit.



Note: Validation of PECL set limits assumes that BIOS set limits are higher than PECL limits.

8.4 Validate PL2 PECI Settings with RdPkgConfig()

- Use RdPkgConfig() command to double check new PL2 values
- Note that read value matches what value was set for PL2 in previous foil
- No Error for command ensures accuracy



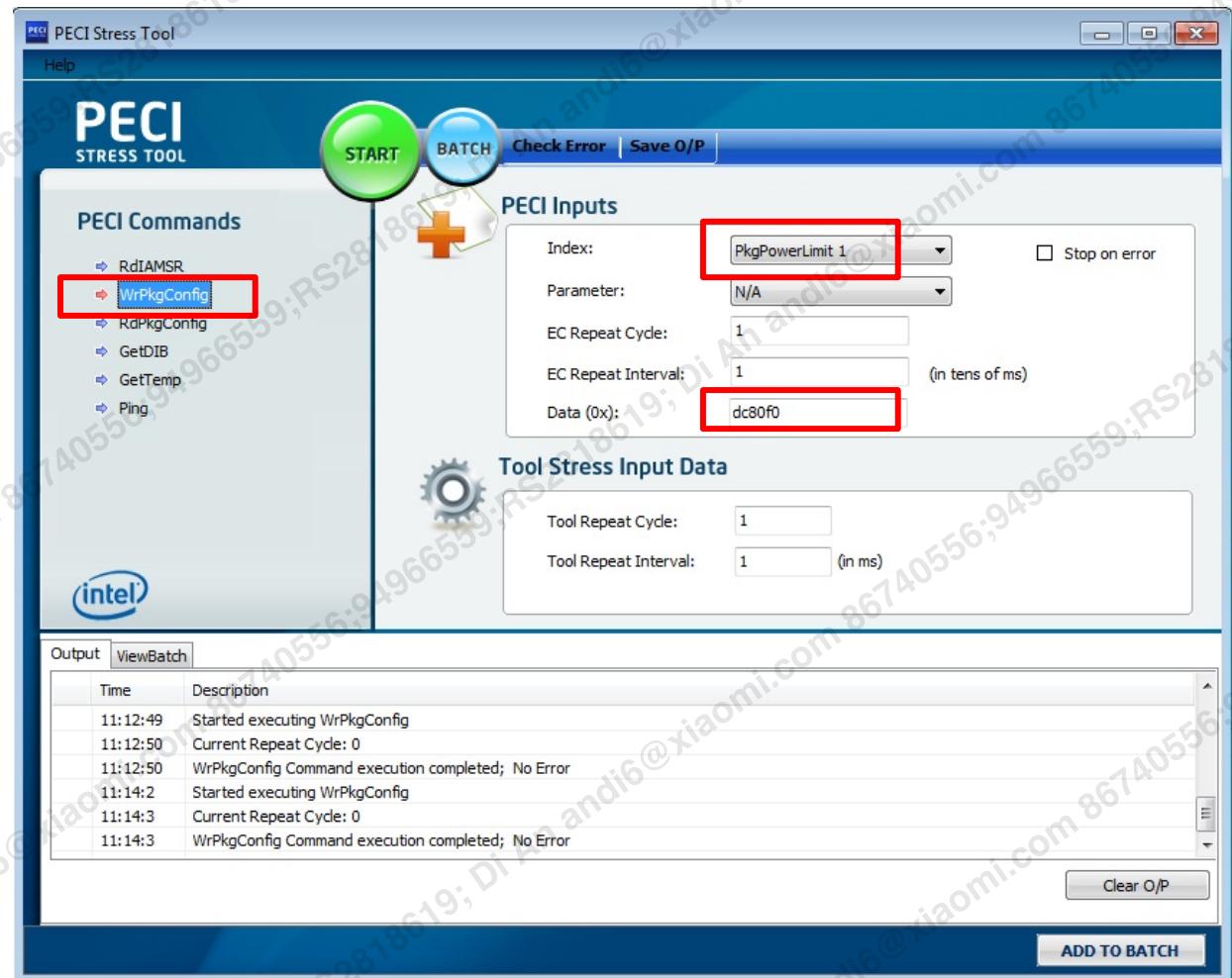
Always use RdPkgConfig() PECI command to validate that WrPkgConfig() PECI command has programmed the correct value

Note: Validation of PECI set limits assumes that BIOS set limits are higher than PECI limits.

8.5 Setting PL1 and Tau via PECL Stress Tool

Example: Program 30 W for PL1 and 28 seconds for Tau

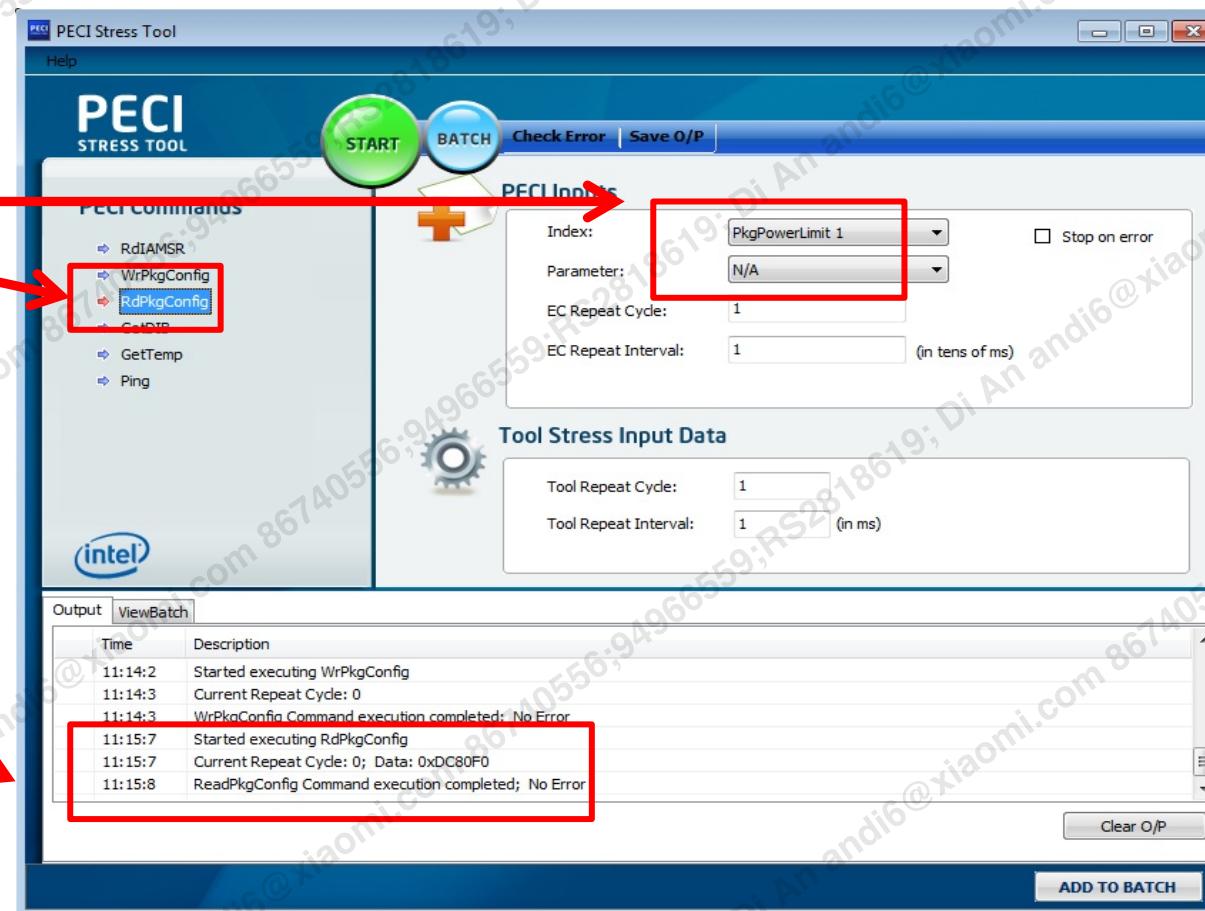
- Input **0xDC80F0**
- **80F0** – Format identical to PL2 on previous slide
- $\text{Tau (sec)} = 1.X' * 2^Y * \text{unit of time}$
- $X' = X_1 * 2^{-1} + X_0 * 2^{-2}$
- Programmed as $X_1 X_0 Y_4 Y_3 Y_2 Y_1 Y_0 b$
- Default time units (MSR 606h) are 0.976 ms
- 28 seconds $\rightarrow X = 11, Y = 01110$
- **11011100b = 0xDC**
 - Extra 0 represents power clamp bit
- For DT, 1 second Tau is 0x14 (assuming same time units)



Note: Validation of PECL set limits assumes that BIOS set limits are higher than PECL limits.

8.6 Validate PL1 and Tau PECI Settings with RdPkgConfig()

- Use RdPkgConfig() command to double check new PL1 and Tau values
- Note that read value matches what value was set for PL1 and Tau in previous foil
- No Error for command ensures accuracy



Always use RdPkgConfig() PECI command to validate that WrPkgConfig() PECI command has programmed the correct value.

Note: Validation of PECI set limits assumes that BIOS set limits are higher than PECI limits.

8.7 Power Thermal Analysis Tool (PTAT)

intel. Intel® Power and Thermal Analysis Tool 1.0.1002 Connected to : ADL

System Information Monitor Alerts Workload Control PTAT Log Analysis Scripts Graph Live Analysis

Monitor All
 CPU Component
 PCH Component
 CState Component
 Memory Component
 Topology Info
 Battery Component

List View Grid View Stop Monitor Start Logging

CPU Component	CPU0	CPU1	CPU2
Type	Value		
is CPU Throttling	0	0	0
Frequency(MHz)	900	1000	2500
DTS(Degree C)	28	28	29
Target PState Request Ratio	24	24	24
Current PState Ratio	9	12	25
Turbo Capability	Supported and Enabled	Supported and Enabled	Supported and Enabled
Core Type	Big Core	Big Core	Big Core

CPU Component	CPU5	CPU3	CPU4
Type	Value		
is CPU Throttling	0	0	0
Frequency(MHz)	2451	2552	2214

8.7.1 PTAT Key Features

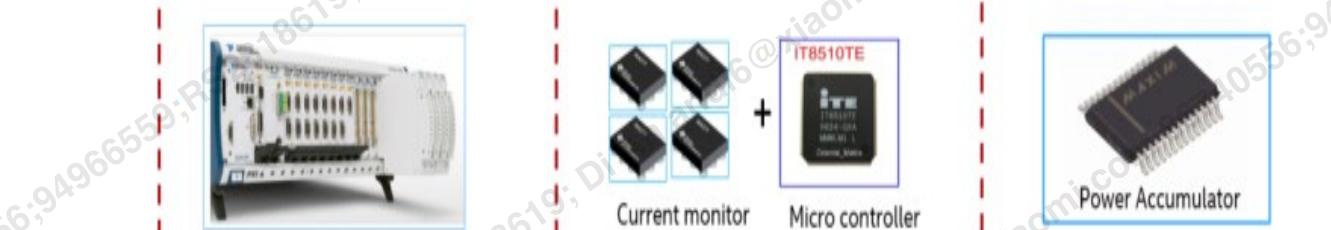
- Extremely Robust Design
 - Launches quickly and has very low CPU utilization.
 - Power stress workloads automatically loaded in the tool.
 - Tool supports multi OS options (Windows*, Linux*, Chrome*).
- Flexible Monitoring of Parameters
 - PTAT6 gives the flexibility to monitor and log limited parameters.
 - Revamp of "Graph" feature. Support for live data up to 12 hours and offline graph support by loading TAT generated logs.
- Transfer Preferred Settings from One Machine to Another
 - Once you have selected the parameters to monitor/log along with polling period, logger name and so on, save the "workspace".
 - Workspace and Script XML files can be transferred to other machines or operating systems to preserve your preferred settings.

8.7.1 PTAT Key Features (Cont.)

- Command Prompt Launch Support
 - PTAT can be run without launching the GUI; most functionalities present in the UI are available through the command prompt.
- Remote debug
 - PTAT can connect to a remote system using IP-address for seamless debugging.
 - Cross OS remote debug is supported. For example: from a Windows* machine (Host), you can connect to a Chrome* machine (Target) and continue to debug on the Chrome* machine.

8.8 Power Meter Introduction

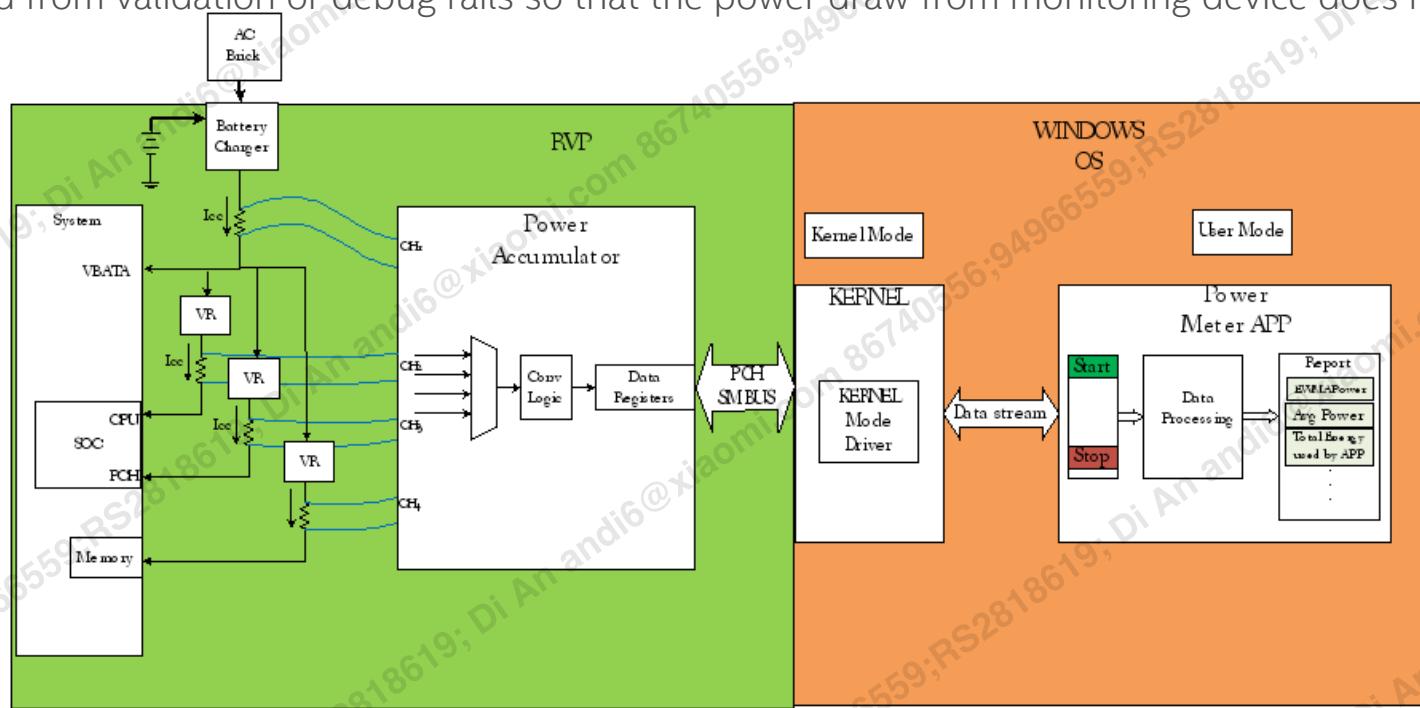
- The existing solutions for power measurement requires a target and a host infrastructure interlinked by a complex set of cables.
- Goals for designing the Power Meter solution:
 - Power measurement **without** wires.
 - Zero learning curve for end user and no prior skills required on power measurement.
 - Self-explanatory software.
 - Cost under \$5/per unit.
 - No need for additional host machines or lab infrastructure.
 - Available on all client reference validation platforms.



Method	National Instruments DAQ	Current Monitor + Micro Controller	Power Meter (NEW)
Cost	~(50000 - 75000) \$	~(60 - 70) \$	~0.5-3.0 \$ for 4channels
Configuration	RVP + Headers	SDS	RVP (inbuilt)
Platforms	Big Core / Small Core	Big Core only (but selective platforms)	Big Core / Small Core
Target Users	PnP Team	PnP Team and SDS users	Development, Integration, Validation, SoC and Ingredient Teams
Pro	100+ rails Accurate measurement	16 – 32 rails Form factor inbuilt	4 rails Zero learning curve and ease of use
Cons	Complex setup Requires niche skills	Limited deployment	~(95)% accuracy

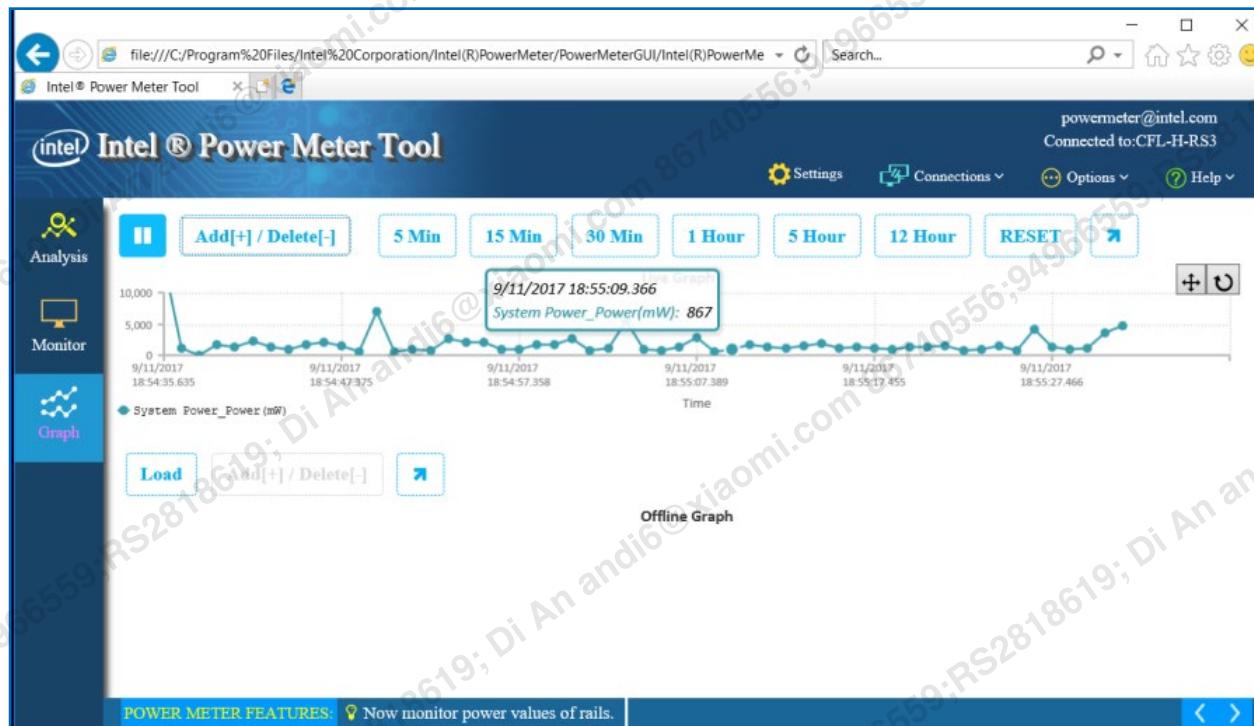
8.8.1 Power Meter Tool Hardware Architecture

- The hardware solution uses a Power Accumulator IC that monitors 4 power rails in a round-robin fashion.
- The power data is converted into digital data, which is accumulated in a register that can be accessed by the host through I2C/SMBUS interface.
- The power measurement is done using existing sense resistors on platform rails and tapping the Kelvin sense lines from these to the Power Accumulator inputs.
- The sense resistor value is selected to ensure that the voltage droop across it is within the required voltage range for the power accumulator to guarantee > 95% accurate measurement.
- The device itself is powered from validation or debug rails so that the power draw from monitoring device does not show up in the system power.



8.8.2 Power Meter Tool Software Architecture

- The software is a simple user interface that will allow to start/stop the power measurement.
- A user can start the power measurement, run the workload, and once stopped, the average power consumed is displayed.
- The software also provides ability to perform remote power measurements, live graphs, and offline analysis of captured data.
- The accuracy of the power measurement is maintained for a given workload since the software consumes very minimal CPU cycles.



9.0 Checklist

- 9.1 Routing Checklist
- 9.2 Turbo Initialization and Real -Time Control
- 9.3 Power Delivery Checklist
- 9.4 Thermal Checklist
- 9.5 Validation Checklist
- 9.6 Basic Function Checklist

9.1 Routing Checklist

Check	Task	Details	Owner	References
<input type="checkbox"/>	Route Psys using available option (Optional)	Required for platform power limits (Psys power limits)	Board Designer	Refer IMVP9 PWM VR Vendor Enabling Specification (573417)
<input type="checkbox"/>	Route PROCHOT#	Required for system thermal protection	Board Designer	Refer Raptor Lake Platform Platform Design Guide (TBD)
<input type="checkbox"/>	Route SVID bus from VR to processor	<ul style="list-style-type: none"> Required for VR functionality and VR thermal protection Required for power monitoring and for Turbo function (IMON) 	Board Designer	Refer Raptor Lake Platform Design Guide (TBD)
<input type="checkbox"/>	Route PECI	Required for EC-based Turbo control and processor temperature monitoring	Board Designer	
<input type="checkbox"/>	Processor power delivery layout	Required for impedance control, decoupling cap design and other power delivery layout recommendations	Power Delivery Engineer	Refer Power Delivery chapter in this slide set (Slide 75) and Raptor Lake Platform Design Guide (TBD)

9.1 Routing Checklist (Cont.)

Check	Task	Details	Owner	References
<input type="checkbox"/>	Route VR_HOT#	Required for VR thermal protection	Board Designer Power Delivery Engineer	Refer Raptor Lake Platform Design Guide (TBD)
<input type="checkbox"/>	Implement temperature sensing for VR hottest components and skin temperature	Required for VR and skin thermal protection	Board Designer Power Delivery Engineer Thermal Engineer	
<input type="checkbox"/>	Implement Platform Power Monitoring	Recommended to prevent possible AC Adapter over-current protection from occurring	Board Designer EC firmware Power Delivery Engineer	Refer Raptor Lake Platform Design Guide (TBD)
<input type="checkbox"/>	Additional routing for Platform Power Management as required, depending on implementation approach	Depends on platform power management implementation	Board Designer Power Delivery Engineer	

9.2 Turbo Initialization and Real-Time Control

Check	Task	Details	Owner	References
<input type="checkbox"/>	Enable Turbo	<ul style="list-style-type: none"> CPU(EAX=6):EAX[1]=1 MSR 1A0h bit 38 = 0 MSR 199h bit 32 = 0 	BIOS Engineer Thermal Engineer	
<input type="checkbox"/>	Initialize Power_Limit_1 - PL1 (MSR 0x610)	<ul style="list-style-type: none"> HW Default = Base Power Set to match thermal solution cooling capacity (sustained power level) Set to limit skin temperature from exceeding design targets 	BIOS Engineer Thermal Engineer	
<input type="checkbox"/>	Initialize Power_Limit_2 - PL2 (MSR 0x610)	<ul style="list-style-type: none"> Assess capability and set value based on platform power limitations (AC brick, battery or PSU limitations) and heat pipe Qmax. Do not set lower than necessary to prevent performance loss. HW Default = 1.25 x PL1 	BIOS Engineer Power Delivery Engineer Thermal Engineer	
<input type="checkbox"/>	Initialize Power_Limit_1 time constant - Tau (MSR 0x610)	<ul style="list-style-type: none"> Use the following value unless testing suggests a smaller value will reduce TCC activation risk or set to larger value if thermal solution has higher thermal capacitance and can handle longer durations above Base Power: Mobile/Halo: 28 seconds or Desktop: 8 seconds Avoid setting values less than 100 ms. 	BIOS Engineer Thermal Engineer	Raptor Lake Platform Firmware Architecture Specification (TBD) (Intel Secret)
<input type="checkbox"/>	Implement real-time control of Power_Limit_2 via Embedded Controller WrPkgConfig(27) if the EC is used for platform power control	<ul style="list-style-type: none"> Based on platform power limit consideration Assess capability and set value based on platform power limitations – do not set lower than necessary to prevent performance loss. 	Power Delivery Engineer EC Firmware	
<input type="checkbox"/>	Implement all real-time control and monitoring of processor via PECI	<ul style="list-style-type: none"> Only initialize Turbo registers via MSR interface Real-time controls are suggested via PECI interface Frequent PECI polling can impact battery life, except for the GetTemp() command 	BIOS Engineer EC Firmware Engineer	

9.2 Turbo Initialization and Real-Time Control (Cont.)

Check	Task	Details	Owner	References
<input type="checkbox"/>	Program VR IccMax limit (BIOS Mailbox)	The value programmed by the BIOS will override the VR controller value	<ul style="list-style-type: none"> ▪ BIOS Engineer ▪ Power Delivery Engineer 	Raptor Lake Platform Firmware Architecture Specification
<input type="checkbox"/>	Check to ensure that UNCORE_RATIO_LIMITS MSR (MSR 0x620) is set to CPU defaults or 0x00/0xFF	Required to enable full PCU control	<ul style="list-style-type: none"> ▪ BIOS Engineer 	Platform Environmental Control Interface (PECI) 3.0 Implementation Guide
<input type="checkbox"/>	Setup VR Average Current Limits VR_TDC (BIOS Mailbox)	Setting will be design dependent	<ul style="list-style-type: none"> ▪ BIOS Engineer ▪ Thermal Engineer ▪ Power Delivery Engineer 	<p>Turbo and Platform Power Management – Hardware and Firmware Design Considerations.</p> <p>Contact your local CAE for latest documentation related to these subjects</p>
<input type="checkbox"/>	Program PL4 limit (MSR 0x601)	<p>The max processor power</p> <p>Optional – Use protection with Dynamic Battery Power Technology as battery drains power</p>	<ul style="list-style-type: none"> ▪ BIOS Engineer ▪ Power Delivery Engineer 	Raptor Lake Platform Firmware Architecture Specification
<input type="checkbox"/>	Program TCC Activation Offset (MSR 0x1A2)	<p>Must be set lower than ACPI _PSV and _CRT trip points (if used)</p> <p>Optional – Use as HW thermal protection</p>	<ul style="list-style-type: none"> ▪ Thermal Engineer 	
<input type="checkbox"/>	Setup Psys configuration in BIOS mailbox (optional)	Required to enable Psys functions	<ul style="list-style-type: none"> ▪ BIOS Engineer 	
<input type="checkbox"/>	Setup Platform Level Power Limits PsysPL1, PsysPL2, PsysPL3 (MSR 0x65C, 0x615) Default: Disabled	Optional – setting will be design dependent	<ul style="list-style-type: none"> ▪ BIOS Engineer ▪ Thermal Engineer ▪ Power Delivery Engineer 	

9.3 Power Delivery Checklist

Check	Task	Details	Owner	References
<input type="checkbox"/>	VR complies with processor electrical requirements	<ul style="list-style-type: none"> IccMax needed for max Turbo Icc_TDC needed for VR thermal validation SVID needed for thermal management/protection IMON required for power monitoring and IMON accuracy must meet IMVP9 specifications. 	<ul style="list-style-type: none"> Power Delivery Engineer Thermal engineer 	<ul style="list-style-type: none"> Raptor Lake External Design Specification (TBD) Refer Raptor Lake U P H Platform Design Guide (686872) Refer to IMVP9 PWM VR Vendor Enabling Specification(573417)
<input type="checkbox"/>	Validate VR electrical capability	<ul style="list-style-type: none"> IccMax, Icc_TDC, decoupling, and so on. Use VRTT (VR test tool) 	Power Delivery Engineer	<ul style="list-style-type: none"> Platform Power Validation Plan (Contact local FAE for availability).
<input type="checkbox"/>	Checking VR capability against BIOS settings	<ul style="list-style-type: none"> Check VR IccMax via SVID (VR test tool) Check processor IccMax and Icc_TDC via BIOS mailbox BIOS setting values should be equal to VR capability or else a limit can be imposed. 	Power Delivery Engineer, BIOS engineer	<ul style="list-style-type: none"> Platform Power Validation Plan (Contact local FAE for availability).
<input type="checkbox"/>	Test VR thermals within form factor system	<ul style="list-style-type: none"> Use thermal validation tool (TAT for mobile, PTU for desktop) or resistive load to stress VR at Icc_TDC Verify power limits and determine time constants 	Refer	<ul style="list-style-type: none"> Refer to Thermal tools Section (Slide 68) in this document

9.3 Power Delivery Checklist (Cont.)

Check	Task	Details	Owner	References
<input type="checkbox"/>	Implement VR thermal protection	<ul style="list-style-type: none"> Calibrate thermistor sensing trip points Consider SVID thermal alert as specified in IMVP9 Confirm thermistor location SVID routing to processor VR_HOT# pin routed to PROHOT# input 	Power Delivery Engineer, Thermal Engineer, Board Designer	<ul style="list-style-type: none"> Refer Raptor Lake Platform Design Guide (TBD) Consult with your VR supplier for thermistor recommendations Refer to IMVP9 PWM VR Vendor Enabling Specification (573417)
<input type="checkbox"/>	Determine platform power delivery capabilities	<ul style="list-style-type: none"> Consider AC brick and battery capabilities Consider implementing Narrow VDC (NVDC) or HPB (Hybrid Power Boost) charger Consider PROCHOT# for brick max peak power protection Consider Fast PROCHOT# for battery max peak power protection Consider enabling Psys in IMVP VR Consider Dynamic Battery Power Technology 	Platform Power Delivery Engineer	<ul style="list-style-type: none"> Refer Power Delivery chapter in this slide set and power delivery design guide Refer Doc TBD for additional information on Dynamic Battery Power Technology Refer Raptor Lake Platform Design Guide (TBD)
<input type="checkbox"/>	Implement platform power delivery management	<ul style="list-style-type: none"> Consider Intel® Dynamic Tuning Power Boss Consider dynamically adjusting PL4 based on the battery max peak power capability Consider enabling PsysPL1/Tau, PsysPL2 and PsysPL3 Consider enabling PL3 to provide peak power duty cycle control and to mitigate battery reliability risks Options may require changes to EC FW, charger design and routing depending on implementation approach 	Platform Power Delivery Engineer, EC FW Engineer, BIOS Engineer, Board Designer	<ul style="list-style-type: none"> Intel® Dynamic Tuning Technology Feature Enabling User Guide (572349)
<input type="checkbox"/>	Implement VR thermal protection	<ul style="list-style-type: none"> Calibrate thermistor sensing trip points Consider SVID thermal alert as specified in IMVP9. Confirm thermistor location SVID routing to processor VR_HOT# pin routed to PROHOT# input 	Power Delivery Engineer, Thermal Engineer, Board Designer	<ul style="list-style-type: none"> Refer Raptor Lake Platform Design Guide (TBD) Consult with VR supplier for thermistor recommendations Refer to IMVP9 PWM VR Vendor Enabling Specification(573417)

9.4 Thermal Checklist

Check	Task	Details	Owner	References
<input type="checkbox"/>	Design CPU thermal solution to meet Base Power	<ul style="list-style-type: none"> ▪ Confirm that CPU DTS temperature does not reach Tjmax under sustained Base Power workload conditions 	<ul style="list-style-type: none"> ▪ Thermal Engineer 	<ul style="list-style-type: none"> ▪ Raptor Lake External Design Specification (TBD) ▪ Raptor Lake Thermal Mechanical Design Guide (TBD)
<input type="checkbox"/>	Determine thermal power limits and check thermal response	<ul style="list-style-type: none"> ▪ Measure thermal power limits ▪ Conduct thermal validation to ensure no significant TCC activation with Tau setting 	<ul style="list-style-type: none"> ▪ Thermal Engineer 	
<input type="checkbox"/>	Thermally characterize VR within form factor system	<ul style="list-style-type: none"> ▪ Use thermal validation tool (TAT for mobile, PTU for desktop) or resistive load ▪ Verify power limits and determine time constants 	<ul style="list-style-type: none"> ▪ Thermal Engineer ▪ Power Delivery Engineer 	<ul style="list-style-type: none"> ▪ TAT User Guide
<input type="checkbox"/>	Verify system acoustics with Turbo	<ul style="list-style-type: none"> ▪ Customer proprietary methods 	Acoustic Engineer	
<input type="checkbox"/>	Strongly recommend additional sensors for monitoring and controlling system temperatures (skin, components, and so on) if implementing DPPM for your system thermal management		<ul style="list-style-type: none"> ▪ Thermal Engineer ▪ Acoustic Engineer 	<ul style="list-style-type: none"> ▪ Raptor Lake Thermal Mechanical Design Guide (TBD) and other documents. ▪ DPPM for Raptor Lake Platform ULT

9.5 Validation Checklist

Check	Task	Details	Sample Capability	Owner	References
<input type="checkbox"/>	Performance	Characterization testing should begin with ES2, with final validation not recommended until QS silicon. Earlier silicon may yield significant performance differences from production silicon depending on the workload	QS and later	Performance Validation	<ul style="list-style-type: none"> Refer to Performance Validation Section Review Dear Customer Letter (DCL) for your samples to determine suitability for planned testing
<input type="checkbox"/>	Platform Power	Early testing of platform power management implementation	ES1 and later	Power Delivery Engineer	<ul style="list-style-type: none"> Refer to Raptor Lake PCH External Design Specification Vol2 (TBD)
<input type="checkbox"/>	Core Power	Early testing of core power delivery	Use VTT tools and electronic loads	Power Delivery Engineer	<ul style="list-style-type: none"> Platform Power Validation Plan (Contact local FAE for availability)
<input type="checkbox"/>	Processor Thermal	<p>Initial testing with TTV and ES2. Ensure complete understanding of various limitations with respect to TTV and ES2 usages.</p> <p>Complete and final thermal validation of a design shall be carried out with QS samples.</p>	ES2 Thermal Samples	Thermal Engineer	<ul style="list-style-type: none"> Refer to Thermal Protection of Voltage Regulators for IMVP-7/VR-12 with Turbo Boost Technologies (442493). While this doc is for an older IMVP the concepts and methods still apply. Thermal Protection of Voltage Regulators for IMVP-7/VR-12 with Turbo Boost Technologies - White Paper - Raptor Lake External Design Specification (TBD) Raptor Lake Thermal Mechanical Design Guide (TBD)

9.5 Validation Checklist (Cont.)

Check	Task	Details	Sample Capability	Owner	References
<input type="checkbox"/>	VR Thermal	Calibrate/test thermistor	Use VTT tools	Thermal Engineer	<ul style="list-style-type: none"> Refer to Thermal Protection of Voltage Regulators for IMVP-7/VR-12 with Turbo Boost Technologies (442493). While this doc is for an older IMVP the concepts and methods still apply.
<input type="checkbox"/>	System Thermal		ES2 Thermal Samples	Thermal Engineer	<ul style="list-style-type: none"> Refer to IMVP9 PWM VR Vendor Enabling Specification (573417) Raptor Lake External Design Specification (TBD) Raptor Lake Thermal Mechanical Design Guide (TBD)
<input type="checkbox"/>	Acoustics	Understand impact of faster temperature changes on fan acoustics	ES1 and later	Acoustics Engineer	Per customer proprietary methods

Expected functionality at sample stepping

(subject to change, refer to sample 'Dear Customer Letters' for specific sample limitations)

Stepping	Thermal/Power	Turbo Functional	Performance	Comments
ES1	No	Yes ¹	No	¹ Limited frequency, non-POR Turbo limits, with uncalibrated power meters and thermal sensors
ES2	Yes	Yes	Not recommended	Beta graphics driver
QS	Yes	Yes	Yes	Beta graphics driver

9.6 Basic Function Checklist

Check	Task	Details	Owner	References
<input type="checkbox"/>	Verify maximum IA frequencies	Check max single core, dual core and quad core frequencies	Validation Engineer	Per customer proprietary methods
<input type="checkbox"/>	Verify P1 IA frequencies	Check that CPU operates at P1 with Turbo disabled	Validation Engineer	
<input type="checkbox"/>	Verify graphics maximum dynamic frequency	Check that graphics will operate at maximum dynamic frequency	Validation Engineer	
<input type="checkbox"/>	Verify LFM frequencies	Check IA and GT LFM frequencies by asserting PROCHOT#	Validation Engineer	
<input type="checkbox"/>	Verify Turbo frequency is reduced if PL1 limit is reached	Frequency will be reduced enough to meet PL1 limit, but should not reduce below P1 frequency	Validation Engineer	
<input type="checkbox"/>	Verify Turbo frequency is reduced if PL2 limit is reached	Frequency will be reduced enough to not exceed PL2 limit	Validation Engineer	

10.0 References

- 10.1 Intel® Dynamic Tuning Collateral References
- 10.2 Other Collateral References

10.1 Intel® Dynamic Tuning Collateral References

Document/Software	Document Number /Location
Intel® Dynamic Tuning Feature Enabling User Guide Revision 0.81	572349
Intel® Dynamic Tuning 8.x BIOS Specification Revision 1.3.13	541817
Intel® Dynamic Tuning Configuration Guide Rev 1.0	575150
2019 Intel® Dynamic Tuning Technology Configuration Guide	607821

10.2 Other Collateral References

Document/Software	Document Number /Location
Raptor Lake Processor External Design Specification, Volume 1 of 2	640555
Raptor Lake U P H Platform Design Guide	686872
Alder Lake-S and Raptor Lake-S Platform Thermal and Mechanical Design Guide	619907
Intel® Speed Shift Technology OEM Update – Product Technical Overview	560934
Intel® Speed Shift Technology (HWP) and Overclocking Interaction on 6th Generation Intel® Core™ Processor Family-based Platforms Architecture Guide	561173
Client Technical Training: Ice Lake Everest	PWD204
Reading and Overriding Power Delivery via BIOS Technical Advisory	626935
New BIOS Debug Logs for VR Power/Thermal Technical Advisory	614453

