



1. Description

1.1. Project

Project Name	harurobo_main_2
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 6.4.0
Date	03/17/2022

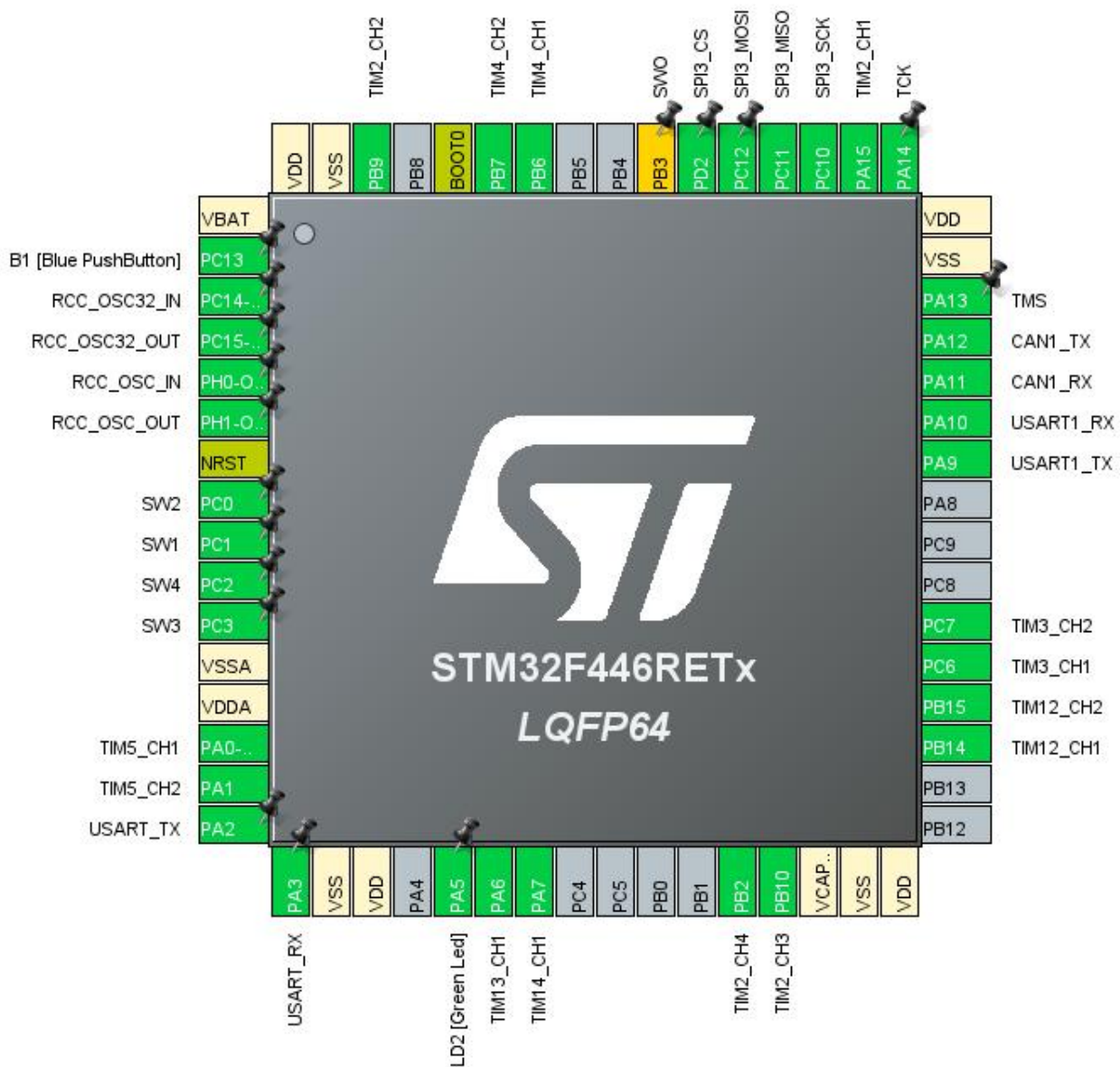
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	SW2
9	PC1 *	I/O	GPIO_Input	SW1
10	PC2 *	I/O	GPIO_Input	SW4
11	PC3 *	I/O	GPIO_Input	SW3
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM5_CH1	
15	PA1	I/O	TIM5_CH2	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	TIM13_CH1	
23	PA7	I/O	TIM14_CH1	
28	PB2	I/O	TIM2_CH4	
29	PB10	I/O	TIM2_CH3	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	TIM12_CH1	
36	PB15	I/O	TIM12_CH2	
37	PC6	I/O	TIM3_CH1	
38	PC7	I/O	TIM3_CH2	
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
44	PA11	I/O	CAN1_RX	
45	PA12	I/O	CAN1_TX	
46	PA13	I/O	SYS_JTMS-SWDIO	TMS

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
50	PA15	I/O	TIM2_CH1	
51	PC10	I/O	SPI3_SCK	
52	PC11	I/O	SPI3_MISO	
53	PC12	I/O	SPI3_MOSI	
54	PD2 *	I/O	GPIO_Output	SPI3_CS
55	PB3 **	I/O	SYS_JTDO-SWO	SWO
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
62	PB9	I/O	TIM2_CH2	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated



5. Software Project

5.1. Project Settings

Name	Value
Project Name	harurobo_main_2
Project Folder	C:\Users\nikud\Documents\STM32CubeIDE\harurobo_main_2
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART2_UART_Init	USART2
4	MX_CAN1_Init	CAN1
5	MX_SPI3_Init	SPI3
6	MX_TIM2_Init	TIM2
7	MX_TIM3_Init	TIM3
8	MX_TIM4_Init	TIM4
9	MX_TIM5_Init	TIM5
10	MX_TIM12_Init	TIM12
11	MX_TIM13_Init	TIM13

Rank	Function Name	Peripheral Instance Name
12	MX_TIM14_Init	TIM14
13	MX_USART1_UART_Init	USART1
14	MX_TIM7_Init	TIM7

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

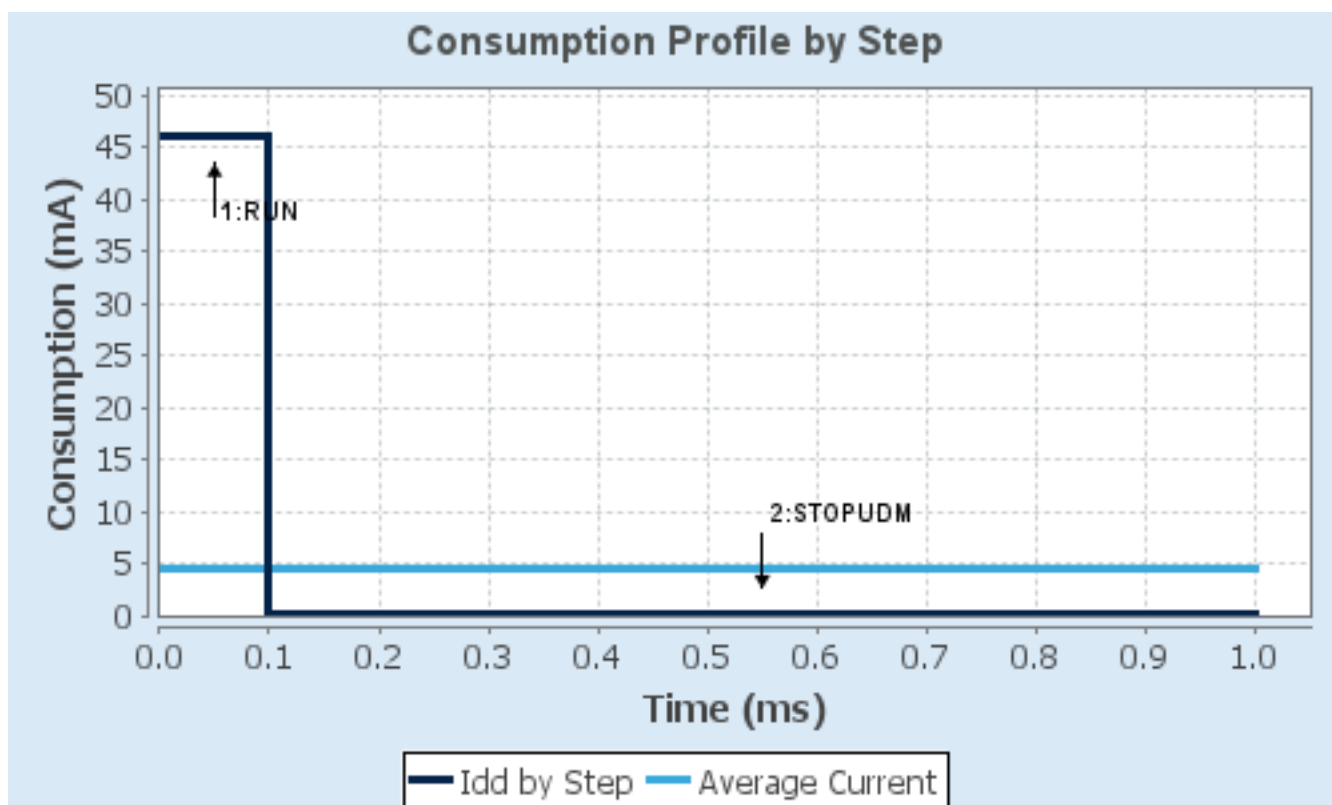
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/P REFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 μ A
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. CAN1

mode: Activated

7.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	6 *
Time Quantum	142.85714285714286 *
Time Quanta in Bit Segment 1	11 Times *
Time Quanta in Bit Segment 2	2 Times *
Time for one Bit	2000 *
Baud Rate	500000 *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
Power Parameters:	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3
Power Over Drive	Disabled

7.3. SPI3

Mode: Full-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:	
Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	64 *
Baud Rate	656.25 KBits/s *
Clock Polarity (CPOL)	High *
Clock Phase (CPHA)	2 Edge *
Advanced Parameters:	
CRC Calculation	Disabled
NSS Signal Type	Software

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	2000 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.6. TIM3

Combined Channels: Encoder Mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
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Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Trigger Output (TRGO) Parameters:	
Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1 and TI2 *
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
_____ Parameters for Channel 2 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.7. TIM4

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Trigger Output (TRGO) Parameters:	
Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1 and TI2 *
_____ Parameters for Channel 1 _____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.8. TIM5

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	2000 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.9. TIM7

mode: Activated

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	55 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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7.10. TIM12

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	83 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.11. TIM13

mode: Activated

Channel1: PWM Generation CH1

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	83 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.12. TIM14

mode: Activated

Channel1: PWM Generation CH1

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	83 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. USART1

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.14. USART2

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA12	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM2	PB2	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM13	PA6	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM14	PA7	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_RX
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC0	GPIO_Input	Input mode	Pull-up *	n/a	SW2
	PC1	GPIO_Input	Input mode	Pull-up *	n/a	SW1
	PC2	GPIO_Input	Input mode	Pull-up *	n/a	SW4
	PC3	GPIO_Input	Input mode	Pull-up *	n/a	SW3
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_CS

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 TX interrupt	unused		
CAN1 RX0 interrupt	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
TIM7 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART1 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware					
System Core	Analog	Timers	Connectivity	Multimedia	Computing
DMA		TIM2 ✓	CAN1 ✓		
GPIO ⚠		TIM3 ✓	SPI3 ✓		
NVIC ✓		TIM4 ✓	USART1 ✓		
RCC ✓		TIM5 ✓	USART2 ✓		
SYS ✓		TIM7 ✓			
		TIM12 ✓			
		TIM13 ✓			
		TIM14 ✓			

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00141306.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00135183.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00155929.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
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Application note http://www.st.com/resource/en/application_note/DM00373474.pdf
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Application note http://www.st.com/resource/en/application_note/DM00725181.pdf