Section 1: Team

at_your_own_risc

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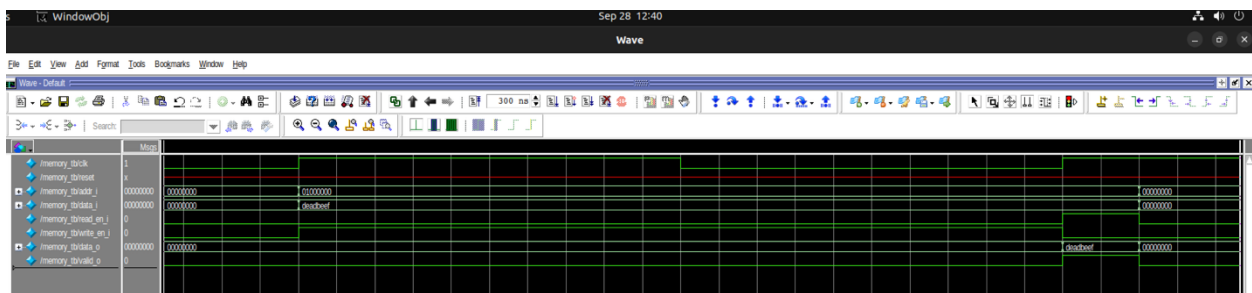# Section 2: ModelSim Waveform

Figure 1 - Waveform showing a write followed by an immediate read. Test Case 1 in memory_tb.sv
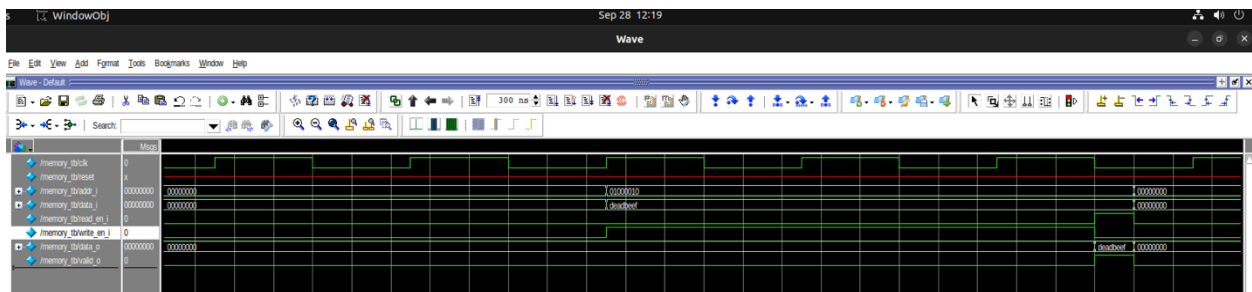

Figure 2 - Waveform showing asynchronous read. Test Case 7 in memory_tb.sv. Note the async read occurs on the far right of the waveform.

Section 3: Reflection

This project deliverable came with many challenges. The first was the conditions for reading and writing in the memory module. We had attempted to use the raw signal **addr_i** but failed to account for the offset of **BASE_ADDR,** this led to an always false condition and prevented both read and write from occurring. This manifested as a singular correct write and read at the base address, but subsequent addresses failed. Additionally, when I changed the condition to use the **address** signal, I failed to account for the byte width of each address, this manifested in failed tests for out of bound read and writes in my

testbench. To address this, I changed the read/write conditions to **address <= `MEM_DEPTH – 4**** which accounts for the 4-byte (32-bit) data width at each address. As best as we understand it, ***MEM_DEPTH*** is the size of memory given in bytes.

The next and most difficult challenge was to get the pattern_dump files and .vcd files to show correct data and waveform data, respectively. Given that our modules passed all three tests, we were surprised that our dump files continually showed only 1000000, while our .vcd files remained completely empty after all three tests. We successfully replicated the issue on our local system, a virtual machine and the EA machines from the EECS Virtual Lab, with both verilator and ModelSim. Troubleshooting yielded no improved results and the TA, Minhyeok, has visually seen our problem over a live zoom session. As of writing this, no progress has been made. The above waveforms were from our own testbench.