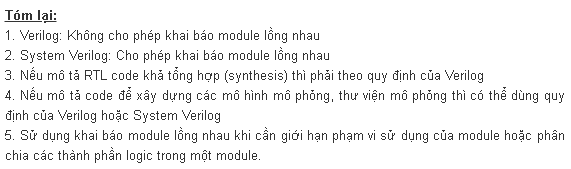
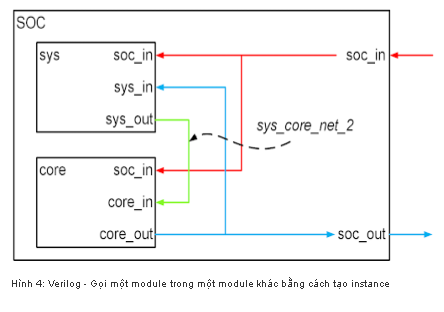
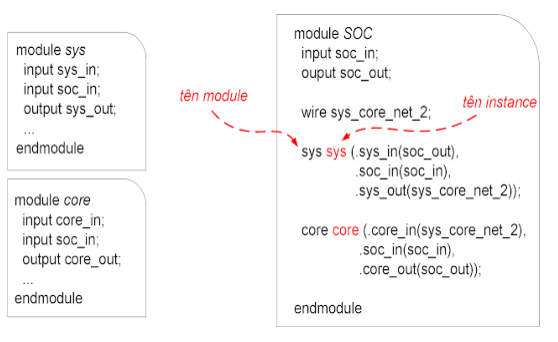
1. Sự khác biệt khi gọi module giữa SystemVerilog và Verilog

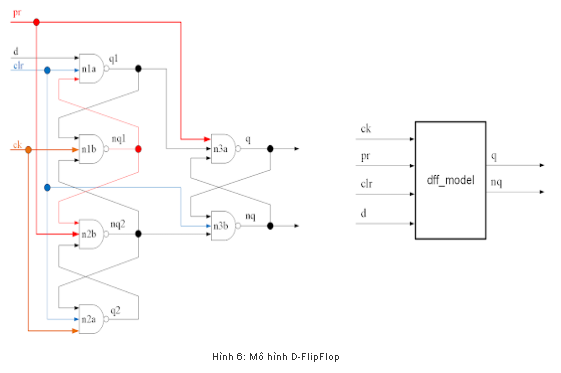


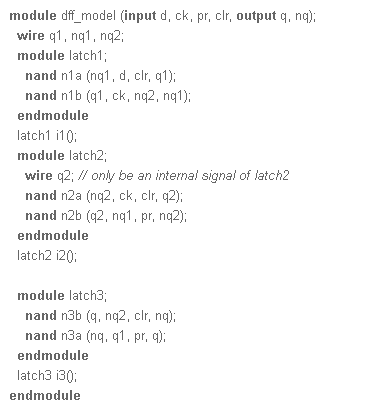
Cách lồng module trong Verilog

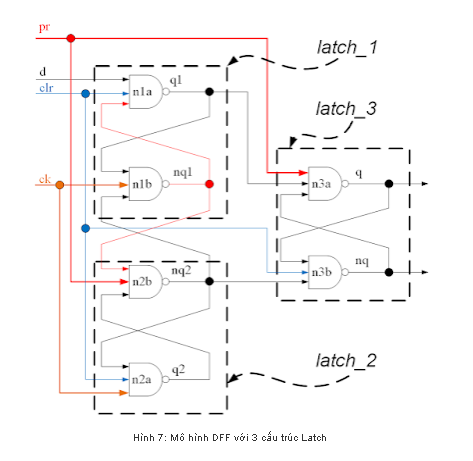




Cách lồng module trong SystemVerilog







1. adfafaw