1/9″ VGA CMOS Image Sensor

GC0329

DataSheet

V1.0

2011-09-01

GalaxyCore Inc.

Content

1. Sensor Overview

1.1 General Description

The GC0329 features 640V x 480H resolution with 1/9-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC, and embedded image signal processor.

The full scale integration of high-performance and low-power functions makes the GC0329 best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB(Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB565,YCbCr 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/9 inch
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer
- Support adjusting Voltage of IO
- Windowing support
- Horizontal /Vertical mirror
- Image processing module
- Package: CSP

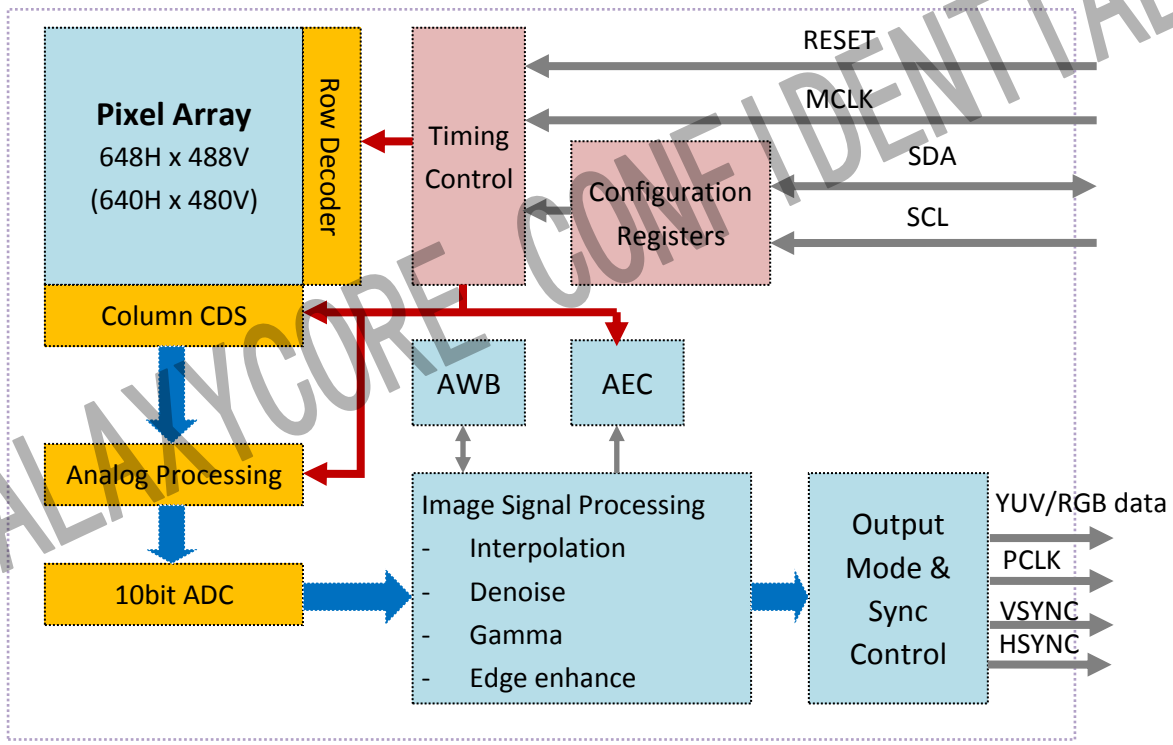
1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

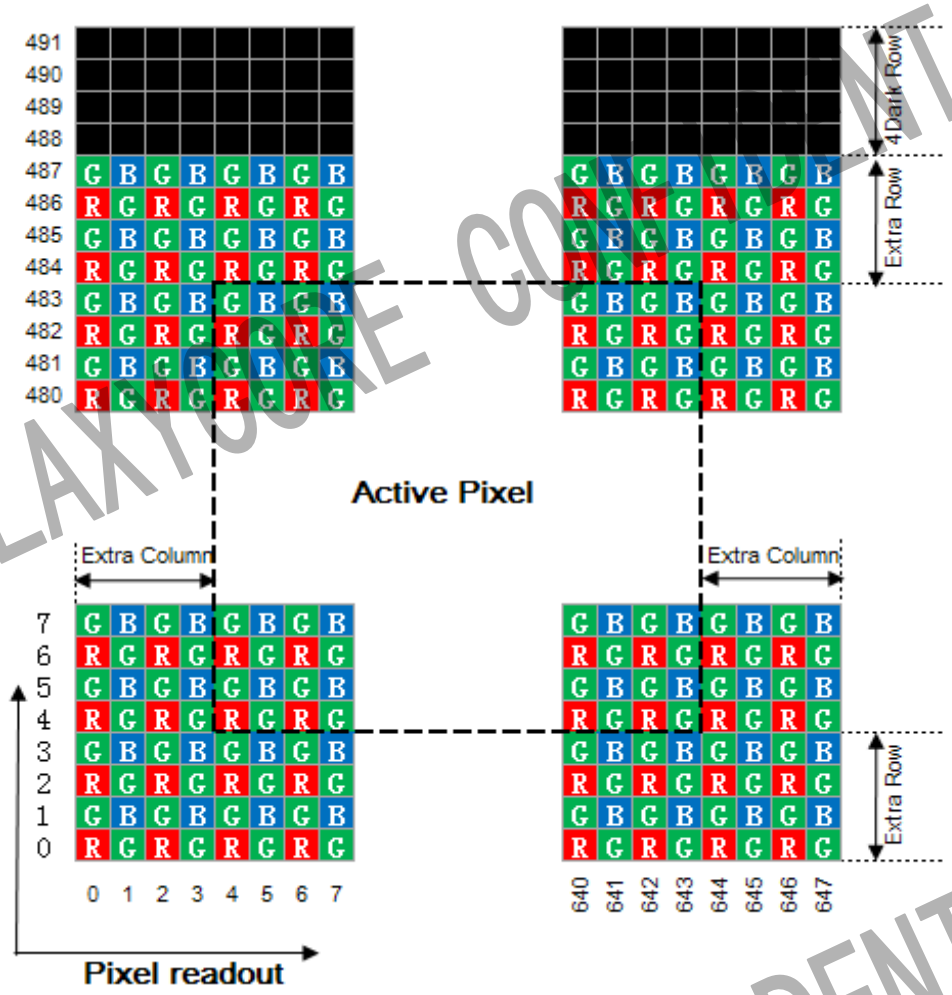
Parameter	Typical value
Optical Format	1/9 inch
Pixel Size	2.5um x 2.5um
Active pixel array	648 x 488
ADC resolution	10 bit ADC
Max Frame rate	30fps@24Mhz,VGA
Power Supply	AVDD28: 2.7 ~ 3.0V IOVDD: 1.7 ~ 3.0V
Power Consumption	70mW @ 30fps VGA, 10μA @ standby
SNR	40dB
Dark Current	15mV/s at 60℃
Sensitivity	1.0V/(Lux·sec)
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	27º(linear)
Package type	CSP

1.5 Block Diagram



GC0329 has an active image array of 648x488 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, denoise, color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

1.6 Pixel Array



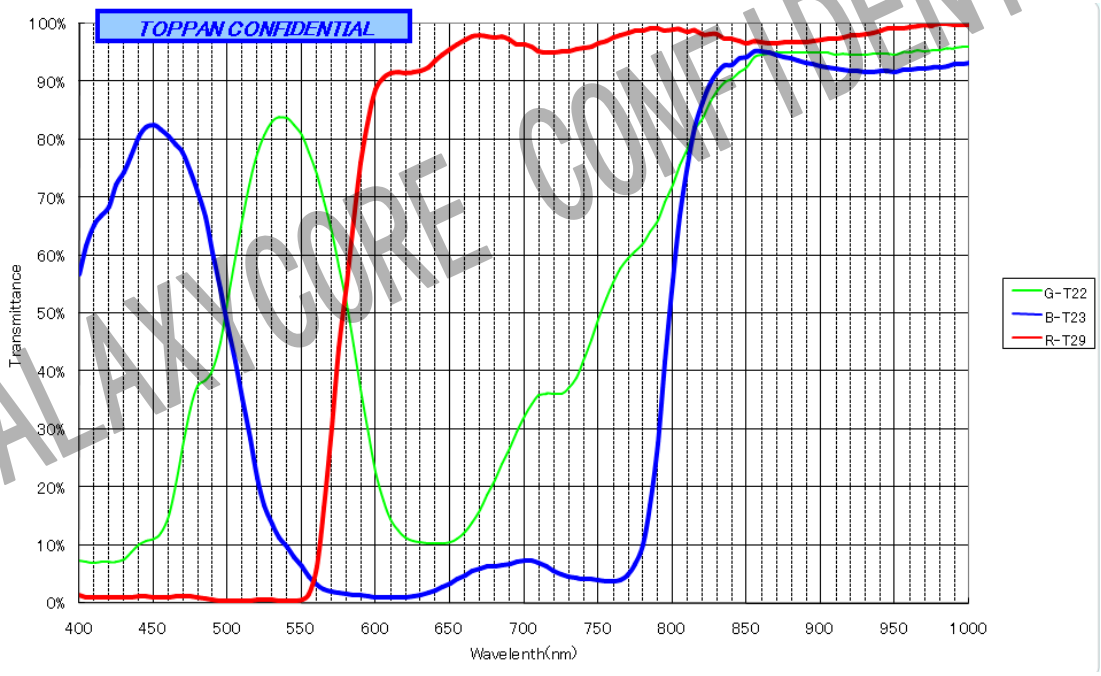
Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 647. If flip in column, column is read out from 647 to 0.

If no flip in row, row is read out from 0 to 487. If flip in row, row is read out from 487 to 0.

2. Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



3. Two-wire Serial Bus Communication

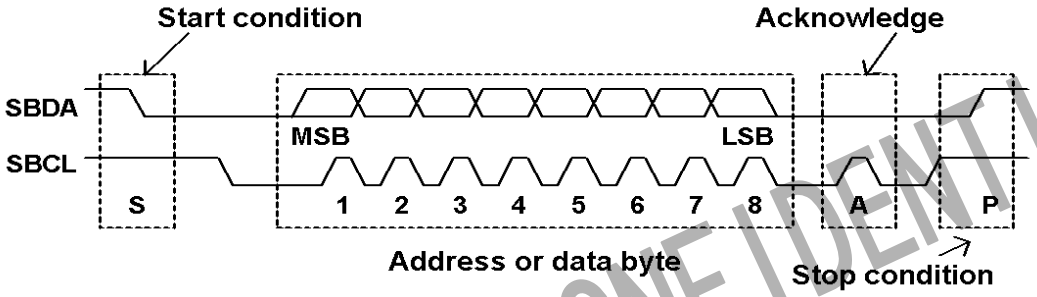
GC0329 Device Address:

serial bus write address = 0x62, serial bus read address = 0x63

3.1 Protocol

The host must perform the role of a communications master and GC0329 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	62H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	62H	A	Register Address	A	Data(1)	A	.....	Data(N)	A	P

Single Register Reading:

S	62H	A	Register Address	A	S	63H	A	Data	NA	P

Notes:

From master to slave　　From slave to master

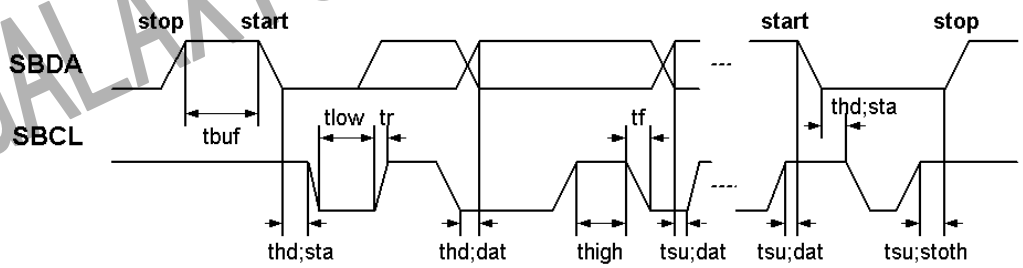
S: Start condition　　**P:** Stop condition

A: Acknowledge bit　　**NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

3.2 Serial Bus Timing

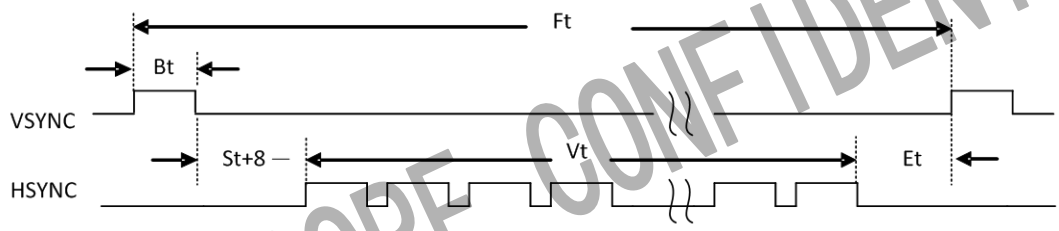


Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

4. Application

4.1 Timing

Suppose Vsync is low active and Hsync is high active, and ouput format is YCbCr/RGB565, then the timing of vsync and hsync is bellowing(take capture mode for example，preview mode is the same):



Ft =VB+ Vt +8 （unit is row_time）

VB = Bt + St + Et， Vblank/Dummy line，setting by register 0x07 and 0x08.

Ft -> Frame time，one frame time

Bt -> Blank time，Vsync no active time.

St -> Start time，setting by register 0x12.

Et –> End time，setting by register 0x13.

Vt -> valid line time. VGA is 480，Vt=win_height-8，win_height is setting by register 0x0d & 0x0e(488).

When exp_time <= win_height+VB，Bt=VB-St-Et。Frame rate is controlled by window_height+VB.

When exp_time > win_height+VB，Bt=exp_time-win_height-St-Et。Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = Hb + Sh_delay + win_width + 4.

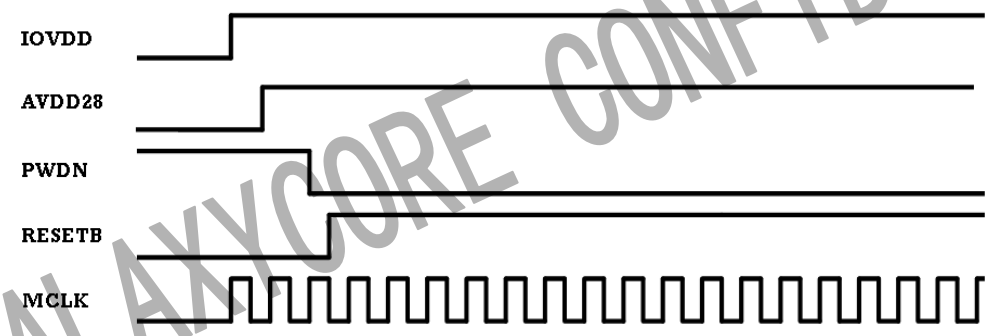
Hb –> HBlank or dummy pixel，Setting by register 0x05 and 0x06.

Sh_delay -> Setting by register 0x11.

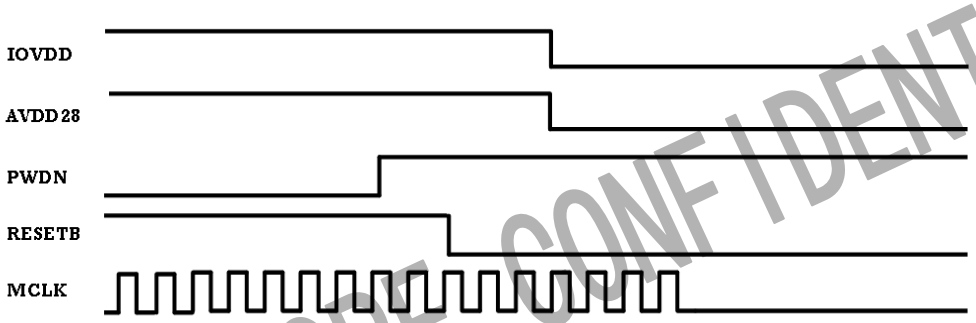
win_width -> Setting by register 0x0f and 0x10, win_width = 640, final_output_width + 8. So for VGA, we should set win_width as 648.

4.2 Power on/off sequence

4.2.1 Power On Sequence



4.2.2 Power Off Sequence



5. DC Parameters

Symbol		Parameter	Min	Typ	Max	Unit
SUPPLY						
V_{AVDD28}		Power Supply	2.7	2.8	3.0	V
V_{IOVDD}		Power Supply(Digital I/O)	1.7	2.8	3.0	V
I_{AVDD28}		Active(Operating) Current	--	8	24	mA
I_{IOVDD}	**1.8V**		--	12	24	mA
	2.8V		--	15	24	mA
$I_{DDS-PWDN}$		Standby Current	--	10	--	uA
Digital Input(Typical conditions: AVDD28 = 2.8V，IOVDD = 1.8V)						
V_{IH}		Input voltage HIGH	1.4			V
V_{IL}		Input voltage LOW			0.6	V
Digital Input(Typical conditions: AVDD28 = 2.8V，IOVDD = 1.8V)						
V_{OH}		Output voltage HIGH	1.6			V
V_{OL}		Output voltage LOW			0.2	V

6. Register List

SYS_REG

Address	Name	Width	Default Value	R/W	Description
0xf0	switch_data_pad_en_mode output_enable	5	0x00	RW	[4] switch_data_pad [3] NA [2] pclk_en [1] hsync_en [0] vsync_en
0xf1	switch_data_o	5	0x00	RW	[4] switch data output enable

	utput_en normal_data_ output_en				[3:1] NA [0] normal data output enable
0xf3	Pad_updn Pwd_dn	8	0x00	RW	[7:6] sync [5:4] pclk [3:2] data 0 0: not pull 0 1: pull down 1 0: pull up 1 1: illegal [1] NA [0] Pwdn_dn 0: pull down 1: floating
0xf5	Rec_bandwidt h	2	0x00	RW	[7:2] NA [1:0] rec_bandwidth 00: 1 bit 01: 2 bits 10: 4 bits 11: invalid
0xfa	clk_div_mode	3	0x00	RW	[7:4]+1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division Mclk by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	I2C_device_I D	7	0x62	RW	[7:1] I2C device ID [0] NA
0xfc	Analog_pwc	3	0x03	RW	[7:5] NA [4] digital_clock_enable [3] NA [2] da25_en [1] da18_en [0] analog power down
0xfe	Reset related	8	0x00	RW	[7] soft_reset , register value reset [6] SPI_receiver_reset

					[5] NA [4] CISCTL restart [3:2] NA [1:0] page select 0 0: page 0 0 1: page 1

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x00	Chip_ID	8	0xC0	RO	Chip ID
P0:0x03	Exposure[11:8]	4	0x00	RW	[7:5] NA [3:0] exposure[11:8],use line processing time as the unit.
P0:0x04	Exposure[7:0]	8	0x96	RW	Exposure[7:0], controlled by AEC if AEC is in function
P0:0x05	HB[11:8]	4	0x00	RW	Horizontal blanking, unit pixel clock
P0:0x06	HB[7:0]	8	0x6a		
P0:0x07	VB[11:8]	4	0x00	RW	Vertical blanking, if current exposure < (VB + window Height) , frame rate will be (VB + window Height); otherwise frame rate will be determined by exposure
P0:0x08	VB[7:0]	8	0x70		
P0:0x09	Row_start[8]	1	0x00	RW	Defines the starting row of the pixel array
P0:0x0a	Row_start[7:0]	8	0x00		
P0:0x0b	Column start[9:8]	2	0x00	RW	Defines the starting column of the pixel array
P0:0x0c	Column start[7:0]	8	0x02		
P0:0x0d	Window height[8]	1	0x01	RW	[7:1] NA [0] Window height high bit
P0:0x0e	Window height[7:0]	8	0xe8	RW	Window height low 8 Bit
P0:0x0f	Window width[9:8]	2	0x02	RW	[7:2] NA [1:0] Window width high bit
P0:0x10	Window width[7:0]	8	0x88	RW	window width low bit
P0:0x11	sh_delay	8	0x2a	RW	sh_delay
P0:0x12	Vs_st	8	0x04	RW	number of Row time from frame start to first HSYNC valid

P0:0x13	Vs_et	8	0x04	RW	number of Row time from last HSYNC valid to frame end Notice the relation with VB, VB > vs_st+vs_et
P0:0x14	Analog mode1	8	0xc0	RW	Reserved.
P0:0x15	rsgg_width	4	0x08	RW	[7:4] NA [3:0] rsgg_width, X2
P0:0x16	Analog mode2	3	0x00	RW	Reserved.
P0:0x17	CISCTL_mode 1	8	0x00	RW	[7] HSYNC always [6] Reserved. [5:4] CFA sequence [3:2] dark CFA sequence [1] Updown [0] mirror
P0:0x18	CISCTL_mode 2	8	0x0a	RW	Reserved.
P0:0x19	CISCTL_mode 3	8	0x05	RW	Reserved.
P0:0x1a	CISCTL_mode 4	8	0x00	RW	Reserved.
P0:0x1b	Rsh_width	8	0x44	RW	[7:4] restg_width [3:0] sh_width
P0:0x1c	Tsp_width	8	0x1d	RW	[7:2] tx_width [1:0] space_width
P0:0x1e	Analog_mode 3	8	0x17	RW	[7:2] Reserved. [1] clk_delay_en [0] NA
P0:0x1f	Analog_mode 4	5	0x00	RW	Reserved.
P0:0x20	Analog_mode 5	8	0x00	RW	[7:4] NA [3:2] da18_r [1] rowclk_mode [0]adclk_mode
P0:0x21	Analog_mode 6	8	0x40	RW	Reserved.
P0:0x22	Analog_mode 7	8	0xba	RW	[7] vref_en [6:4] da_vref [3:2] NA [1:0] da25_r
P0:0x23	Analog_mode 8	8	0x01	RW	Reserved.
P0:0x24	Pad driver	8	0x15	RW	[7:6] NA [5:4] sync pad driving current(HS,VS)

					[3:2] data pad driving current(D0~D7) [1:0] pclk pad driving current

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x26	Blk_mode1	8	0x27	RW	[7] dark_current_mode [6:4] BLK_smooth_speed [3:2] BLK_row_select_mode [1] dark_current_en [0] offset_en
P0:0x28	BLK_limit_value	7	0x3f	RW	When Dark data big than it, while get this to replace it for protect dark data. low align 11bits
P0:0x29	global_offset	8	0x00	RW	[7] Reserved. [6:0] low align 11bits
P0:0x2a	current_G1_offset	7		RO	[7] NA [6:0] Current_G1_offset
P0:0x2b	current_R1_offset	7		RO	[7] NA [6:0] Current_R1_offset
P0:0x2c	current_B2_offset	7		RO	[7] NA [6:0] Current_B2_offset
P0:0x2d	current_G2_offset	7		RO	[7] NA [6:0] current_G2_offset
P0:0x2e	current_G1_dark_current	7		RO	[7] NA [6:0] Current_G1_dark_current
P0:0x2f	current_R1_dark_current	7		RO	[7] NA [6:0] Current_R1_dark_current
P0:0x30	Current_B2_dark_current	7		RO	[7] NA [6:0] Current_B2_dark_current
P0:0x31	current_G2_dark_current	7		RO	[7] NA [6:0] Current_G2_dark_current
P0:0x32	Exp_rate_darkc	8	0x04	RW	Low 8 bits of 0.12, 4 means when exp =1024, dark current portion is 4
P0:0x33	offset_submode offset_ratio_G1	8	0x18	RW	[7:6] offset submode [5:0] offset ratio of G1 channel ,1.5 bits
P0:0x34	offset_ratio_G2	6	0x18	RW	[5:0] offset ratio of G2 channel ,1.5 bits

P0:0x35	offset_ratio_R1	6	0x18	RW	[5:0] offset ratio of R1 channel ,1.5 bits
P0:0x36	offset_ratio_B2	6	0x18	RW	[5:0] offset ratio of B2 channel ,1.5 bits
P0:0x37	darkc_submode dark_current_ratio_G1	6	0x18	RW	[7:6] darkc submode [5:0] dark current ratio of G1 channel
P0:0x38	dark_current_ratio_G2	6	0x18	RW	[5:0] offset ratio ofG2 channel, 1.5bits
P0:0x39	dark_current_ratio_R1	6	0x18	RW	[5:0] offset ratio of R1 channel, 1.5bits
P0:0x3a	dark_current_ratio_B2	6	0x18	RW	[5:0] offset ratio of B2 channel, 1.5bits
P0:0x3b	manual_R1_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3c	manual_G1_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3d	manual_G2_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3e	manual_B2_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3f	Black_mode	8	0xf6	RW	Reserved.

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Block_enable_1	8	0xff	RW	[7] BKS enable [6] gamma enable [5] CC enable [4] Edge Enhancement enable [3] Interpolation enable [2] Noise removal enable [1] Defect removal enable [0] Lens-shading correction enable
P0:0x41	Block_enable_2	8	0xff	RW	[7] NA [6] low light Y enable [5] skin detection enable [4] skin Y enable [3] new skin mode [2] autogray enable

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					[1] Y gamma enable [0] NA
P0:0x42	AAAA_enable	8	0x18	RW	[7] Auto Saturation enable [6] auto EE enable [5] auto DN enable [4] auto DD enable [3] auto LSC enable [2] ABS enable [1] AWB enable [0] ACE enable
P0:0x43	special_effect	8	0x00	RW	[7:3] NA [2] Reserved. [1] CbCr fixed enable [0] Inverse color
P0:0x44	Output_format	8	0x22	RW	[7] NA [6] smooth_Y [5] averaging_neighbour_chroma [4:0]output data mode 5'h00 Cb Y Cr Y 5'h01 Cr Y Cb Y 5'h02 Y Cb Y Cr 5'h03 Y Cr Y Cb 5'h04 LSC bypass, C/Y 5'h05 LSC bypass, Y/C 5'h06 RGB 565 5'h0f bypass 10bits 5'h11 only Y 5'h12 only Cb 5'h13 only Cr 5'h14 only R 5'h15 only G 5'h16 only B 5'h17 switch odd/even column /row to controls output bayer pattern P0:0x4e[6:5]: 0 0: RGBG 0 1: RGGB 1 0: BGGR 1 1: GBRG 5'h18 DNDD_out_mode 5'h19 LSC_out_mode
P0:0x46	sync_mode	8	0x3f	RW	Synchronize signal output mode

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					[7] data delay half [6] hsync delay half [5] allow pclk around hsync [4] allow pclk around vsync [3] pclk gated mode 0: not gated 1: gated [2] pclk polarity 0: invert of isp_2pclk(isp_pclk) 1: same as isp_2pclk(isp_pclk) [1] HSync polarity 0: low valid 1: high valid [0] VSync polarity 0: low valid 1: high valid
P0:0x47	DT_mode	3	0x03	RW	Reserved.
P0:0x48	DT_bit	8	0x00	RW	Reserved.
P0:0x49	bypass_mode	8	0x83	RW	Reserved.
P0:0x4a	Clock_gating_en	8	0x81	RW	Reserved.
P0:0x4b	debug_mode1	8	0xca	RW	[7:2] Reserved. [1] AWB_gain_mode [0] more boundary mode
P0:0x4c	debug_mode2	8	0x00	RW	[7:3] Reserved. [2] input test image [1] LSC test image [0] test image after EEINP
P0:0x4d	Debug_mode3	8	0x01	RW	[7:4] test image fix value [3] test image fix value mode [2] NA [1] INBF enable [0] gain mode
P0:0x4e	Bayer_mode	8	0x09	RW	[7] sync header mode [6] odd even row switch [5] odd even column switch [4:0] Reserved.
P0:0x4f	AEC_EN	1	0x00	RW	[7:1] NA [0] AEC enable
P0:0x50	Crop_win_mode	1	0x00	RW	[7:1] NA [0] Crop out Window mode
P0:0x51	Crop_win_y1[	2	0x00	RW	[7:2]NA

	9:8]				[1:0]Crop _win_y1[9:8] Bit[9]: 0 : [8:0] is valid, forward 1 : [5:0] is valid, backward
P0:0x52	Crop_win_y1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x53	Crop_win_x1[10:8]	3	0x00	RW	[7:3] NA [2:0] Crop _win_y1[10:8] Bit[10]: 0 : [9:0] is valid, forward 1 : [3:0] is valid, max is 8, backward
P0:0x54	Crop_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x55	Out window height[8]	1	0x01	RW	Out window height[8]
P0:0x56	Out window height[7:0]	8	0xe0	RW	Out window height[7:0]
P0:0x57	Out window width[9:8]	2	0x02	RW	Out window width[9:8]
P0:0x58	Out window width[7:0]	8	0x80	RW	Out window width[7:0]
P0:0x59	subsample	8	0x11	RW	[7:4] subsample row ratio [3:0] subsample col ratio
P0:0x5a	Sub_mode	6	0x0e	RW	[5] use or cut row [4] use or cut col [3] vacancy zero mode [2] remove 00 mode [1] neighbor average mode [0] subsample extend pclk
P0:0x5b	Sub_row_N1	8	0x02	RW	[7:4] sub_row_num1 [3:0] sub_row_num2
P0:0x5c	Sub_row_N2	8	0x04	RW	[7:4] sub_row_num3 [3:0] sub_row_num4
P0:0x5d	Sub_row_N3	8	0x00	RW	[7:4] sub_row_num5 [3:0] sub_row_num6
P0:0x5e	Sub_row_N4	8	0x00	RW	[7:4] sub_row_num7 [3:0] sub_row_num8
P0:0x5f	Sub_col_N1	8	0x02	RW	[7:4] sub_col_num1 [3:0] sub_col_num2
P0:0x60	Sub_col_N2	8	0x04	RW	[7:4] sub_col_num3 [3:0] sub_col_num4
P0:0x61	Sub_col_N3	8	0x00	RW	[7:4] sub_col_num5

					[3:0] sub_col_num6
P0:0x62	Sub_col_N4	8	0x00	RW	[7:4] sub_col_num7 [3:0] sub_col_num8

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0x70	Global_gain	8	0x40	RW	Global gain, 2.6 bits
P0:0x71	Auto_pregain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0x72	Auto_postgain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0x73	Channel_gain_R	8	0x80	RW	R channel pre gain, 1.7 bits
P0:0x74	Channel_gain_G1	8	0x80	RW	G1 channel pre gain, 1.7 bits
P0:0x75	Channel_gain_G2	8	0x80	RW	G2 channel pre gain, 1.7 bits
P0:0x76	Channel_gain_B	8	0x80	RW	B channel pre gain, 1.7 bits
P0:0x77	AWB_R_gain	8	0x50	RO	Red channel gain from auto white balancing, 2.6 bits
P0:0x78	AWB_G_gain	8	0x40	RO	Green channel gain from auto white balancing, 2.6 bits
P0:0x79	AWB_B_gain	8	0x48	RO	Blue channel gain from auto white balancing, 2.6 bits
P0:0x7a	R_ratio	8	0x80	RW	R_ratio, 1.7 bits
P0:0x7b	G_ratio	8	0x80	RW	G_ratio, 1.7 bits
P0:0x7c	B_ratio	8	0x80	RW	B_ratio, 1.7 bits

LSC

Address	Name	Width	Default Value	R/W	Description
P1:0xa0	LSC_YCP_EN	1	0x00	RW	[7:1] NA [0] LSC_YCP_EN
P1:0xa1	LSC_row_center	7	0x3c	RW	LSC row center, the real value is this setting X2
P1:0xa2	LSC_col_center	8	0x50	RW	LSC col center, the real value is this setting X2
P1:0xa4	LSC_para_sig	6	0x00	RW	[6] LSC_Q1_red_b1_signed

	n1				[5] LSC_Q1_green_b1_signed [4] LSC_Q1_blue_b1_signed [2] LSC_Q2_red_b1_signed [1] LSC_Q2_green_b1_signed [0] LSC_Q2_blue_b1_signed
P1:0xa5	LSC_para_sign2	6	0x00	RW	[6] LSC_Q3_red_b1_signed [5] LSC_Q3_green_b1_signed [4] LSC_Q3_blue_b1_signed [2] LSC_Q4_red_b1_signed [1] LSC_Q4_green_b1_signed [0] LSC_Q4_blue_b1_signed
P1:0xa6	LSC_para_sign3	6	0x00	RW	[6] LSC_Q1_red_b4_signed [5] LSC_Q1_green_b4_signed [4] LSC_Q1_blue_b4_signed [2] LSC_Q2_red_b4_signed [1] LSC_Q2_green_b4_signed [0] LSC_Q2_blue_b4_signed
P1:0xa7	LSC_para_sign4	6	0x00	RW	[6] LSC_Q3_red_b4_signed [5] LSC_Q3_green_b4_signed [4] LSC_Q3_blue_b4_signed [2] LSC_Q4_red_b4_signed [1] LSC_Q4_green_b4_signed [0] LSC_Q4_blue_b4_signed
P1:0xa8	LSC_Q1_red_b1	8	0x20	RW	LSC_Q1_red_b1
P1:0xa9	LSC_Q1_green_b1	8	0x20	RW	LSC_Q1_green_b1
P1:0xaa	LSC_Q1_blue_b1	8	0x20	RW	LSC_Q1_blue_b1
P1:0xab	LSC_Q2_red_b1	8	0x20	RW	LSC_Q2_red_b1
P1:0xac	LSC_Q2_green_b1	8	0x20	RW	LSC_Q2_green_b1
P1:0xad	LSC_Q2_blue_b1	8	0x20	RW	LSC_Q2_blue_b1
P1:0xae	LSC_Q3_red_b1	8	0x20	RW	LSC_Q3_red_b1
P1:0xaf	LSC_Q3_green_b1	8	0x20	RW	LSC_Q3_green_b1
P1:0xb0	LSC_Q3_blue_b1	8	0x20	RW	LSC_Q3_blue_b1
P1:0xb1	LSC_Q4_red_	8	0x20	RW	LSC_Q4_red_b1

	b1				
P1:0xb2	LSC_Q4_green_b1	8	0x20	RW	LSC_Q4_green_b1
P1:0xb3	LSC_Q4_blue_b1	8	0x20	RW	LSC_Q4_blue_b1
P1:0xb4	LSC_right_red_b2	8	0x20	RW	LSC_right_red_b2
P1:0xb5	LSC_right_green_b2	8	0x20	RW	LSC_right_green_b2
P1:0xb6	LSC_right_blue_b2	8	0x20	RW	LSC_right_blue_b2
P1:0xb7	LSC_right_red_b4	8	0x20	RW	LSC_right_red_b4
P1:0xb8	LSC_right_green_b4	8	0x20	RW	LSC_right_green_b4
P1:0xb9	LSC_right_blue_b4	8	0x20	RW	LSC_right_blue_b4
P1:0xba	LSC_left_red_b2	8	0x20	RW	LSC_left_red_b2
P1:0xbb	LSC_left_green_b2	8	0x20	RW	LSC_left_green_b2
P1:0xbc	LSC_left_blue_b2	8	0x20	RW	LSC_left_blue_b2
P1:0xbd	LSC_left_red_b4	8	0x20	RW	LSC_left_red_b4
P1:0xbe	LSC_left_green_b4	8	0x20	RW	LSC_left_green_b4
P1:0xbf	LSC_left_blue_b4	8	0x20	RW	LSC_left_blue_b4
P1:0xc0	LSC_up_red_b2	8	0x20	RW	LSC_up_red_b2
P1:0xc1	LSC_up_green_b2	8	0x20	RW	LSC_up_green_b2
P1:0xc2	LSC_up_blue_b2	8	0x20	RW	LSC_up_blue_b2
P1:0xc3	LSC_up_red_b4	8	0x20	RW	LSC_up_red_b4
P1:0xc4	LSC_up_green_b4	8	0x20	RW	LSC_up_green_b4
P1:0xc5	LSC_up_blue_b4	8	0x20	RW	LSC_up_blue_b4
P1:0xc6	LSC_down_re	8	0x20	RW	LSC_down_red_b2

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	d_b2				
P1:0xc7	LSC_down_green_b2	8	0x20	RW	LSC_down_green_b2
P1:0xc8	LSC_down_blue_b2	8	0x20	RW	LSC_down_blue_b2
P1:0xc9	LSC_down_red_b4	8	0x20	RW	LSC_down_red_b4
P1:0xca	LSC_down_green_b4	8	0x20	RW	LSC_down_green_b4
P1:0xcb	LSC_down_blue_b4	8	0x20	RW	LSC_down_blue_b4

DNDD

Address	Name	Width	Default Value	R/W	Description
P0:0x80	DN_mode_en	8	0x87	RW	[7:5] Reserved. [4] zero weight mode [3] share mode [2] c weight adapt mode [1] DN LSC mode [0] DN b mode
P0:0x81	DN_mode_ratio	8	0x22	RW	[7:6] bad ratio [5:4] C weight adaptive ratio [3:2] DN LSC ratio [1:0] DN b mode ratio
P0:0x82	DN_bilat_b_base	7	0x15	RW	[7] NA [6]DN inc or dec [5:0] DN B base
P0:0x83	DN_bilat_n_base DN_C_weight	8	0x05	RW	[7:4] Base noise level of each frame [3:0] base center pixel weight
P0:0x84	DD_dark_bright_TH	4	0xe5	RW	[7:4] DD dark threshold [3:0] DD bright threshold
P0:0x85	DD_flat_TH	6	0x86	RW	[7:4] DD_TH -1 [3:0] DD_TH -2
P0:0x86	DD_limit DD_ratio	6	0xf2	RW	[7:4] DD_limit [3:2] NA [1:0] DD_ratio
P0:0x87	DN_b_in_dark1	6	0xca	RW	[7] DN B in dark enable [6] DD select weight [5:4] NA

					[3:0] DD mm TH
P0:0x88	DN_b_in_dark2	8	0xff	RW	[7:4] DN b in dark threshold [3:0] DN b in dark slope
P0:0x89	DN_BCR_mode	2	0x00	RW	[1:0] DN BCR mode

INTPEE

Address	Name	Width	Default Value	R/W	Description
P0:0x90	EEINTP mode1	8	0xac	RW	[7] edge1 mode [6] HP3 mode [5] edge2 mode [4] NA [3] LP interpolation enable [2] LP edge enable [1:0] LP edge mode
P0:0x91	EEINTP mode2	8	0x00	RW	[7] HP mode [5] only 2 direction [4] fixed direction threshold [3] defect map [2] edge direction [1] BCR EEINTP mode1 [0] BCR EEINTP mode2
P0:0x92	Direction TH1	6	0x05	RW	[7:6] NA Lower Criteria for direction detection
P0:0x93	Direction TH2	6	0x3f	RW	[7:6] NA Upper Criteria for direction detection
P0:0x94	Diff_HV_TI_TH Direction diff TH	8	0x05	RW	[7:4] Diff_HV_TI_TH [3:0] Direction diff TH
P0:0x95	Edge1 effect Edge2 effect	8	0x45	RW	[7:4] edge1 effect [3:0] edge2 effect Controlled by user or ASDE
P0:0x96	Edge_pos_ratio Edge_neg_ratio	8	0x88	RW	[7:4] positive edge ratio , 1.3bits [3:0] negative edge ratio , 1.3bits
P0:0x97	Edge1_max Edge1_min	8	0x81	RW	[7:4] edge1 max [3:0] edge1 min
P0:0x98	Edge2_max	8	0x81	RW	[7:4] edge2 max

	Edge2_min				[3:0] edge2 min
P0:0x99	Edge1_th Edge2_th	8	0x22	RW	[7:4] edge1 threshold [3:0] edge2 threshold
P0:0x9a	Edge_pos_max Edge_neg_max	8	0xff	RW	[7:4] positive edge max [3:0] negative edge max

CC

Address	Name	Width	Default Value	R/W	Description
P0:0xb3	CC Matrix C11	8	0x45	RW	R channel coefficient 1, S1.6
P0:0xb4	CC Matrix C12	8	0x00	RW	G channel coefficient 1, S1.6
P0:0xb5	CC Matrix C13	8	0x00	RW	B channel coefficient 1, S1.6
P0:0xb6	CC Matrix C21	8	0x00	RW	R channel coefficient 2, S1.6
P0:0xb7	CC Matrix C22	8	0x45	RW	G channel coefficient 2, S1.6
P0:0xb8	CC Matrix C23	8	0xf0	RW	B channel coefficient 2, S1.6
P0:0xbc	CC Matrix C41	5	0x00	RW	R channel offset coefficient, S4
P0:0xbd	CC Matrix C42	5	0x00	RW	G channel offset coefficient, S4
P0:0xbe	CC Matrix C43	5	0x00	RW	B channel offset coefficient, S4

RGB GAMMA

Address	Name	Width	Default Value	R/W	Description
P0:0xbf	Gamma_0	8	0x10	RW	Each out value of knee_i. Knee0=0
P0:0xc0	Gamma_1	8	0x20	RW	Knee1=8
P0:0xc1	Gamma_2	8	0x38	RW	Knee2=16
P0:0xc2	Gamma_3	8	0x4E	RW	Knee3=24
P0:0xc3	Gamma_4	8	0x63	RW	Knee4=32
P0:0xc4	Gamma_5	8	0x76	RW	Knee5=40
P0:0xc5	Gamma_6	8	0x87	RW	Knee6=48
P0:0xc6	Gamma_7	8	0xa2	RW	Knee7=64
P0:0xc7	Gamma_8	8	0xb8	RW	Knee8=80
P0:0xc8	Gamma_9	8	0xca	RW	Knee9=96
P0:0xc9	Gamma_10	8	0xd8	RW	Knee10=112
P0:0xca	Gamma_11	8	0xe3	RW	Knee11=128
P0:0xcb	Gamma_12	8	0xe9	RW	Knee12=144
P0:0xcc	Gamma_13	8	0xf0	RW	Knee13 =160
P0:0xcd	Gamma_14	8	0xf8	RW	Knee14 = 192

P0:0xce	Gamma_15	8	0xfd	RW	Knee15 = 224
P0:0xcf	Gamma_16	8	0xff	RW	Knee16 = 256

Y GAMMA

Address	Name	Width	Default Value	R/W	Description
P0:0x63	Y_Gamma_0	8	0x00	RW	Knee0=0
P0:0x64	Y_Gamma_1	8	0x10	RW	Knee1=8
P0:0x65	Y_Gamma_2	8	0x1c	RW	Knee2=16
P0:0x66	Y_Gamma_3	8	0x30	RW	Knee3=32
P0:0x67	Y_Gamma_4	8	0x43	RW	Knee4=48
P0:0x68	Y_Gamma_5	8	0x54	RW	Knee5=64
P0:0x69	Y_Gamma_6	8	0x65	RW	Knee6=80
P0:0x6a	Y_Gamma_7	8	0x75	RW	Knee7=96
P0:0x6b	Y_Gamma_8	8	0x93	RW	Knee8=128
P0:0x6c	Y_Gamma_9	8	0xb0	RW	Knee9=160
P0:0x6d	Y_Gamma_10	8	0xcb	RW	Knee10=192
P0:0x6e	Y_Gamma_11	8	0xe6	RW	Knee11=224
P0:0x6f	Y_Gamma_12	8	0xff	RW	Knee12=255

YCP

Address	Name	Width	Default Value	R/W	Description
P0:0xd0	Global saturation	8	0x40	RW	Global saturation, controlled by ASDE & CC_STA_AWB
P0:0xd1	saturation_Cb	8	0x40	RW	Cb saturation 3.5bits, 0x20=1.0
P0:0xd2	saturation_Cr	8	0x40	RW	Cr saturation 3.5bits, 0x20=1.0
P0:0xd3	luma_contrast	8	0x40	RW	Luma_contrast, can be adjusted via contrast center 2.6bits, 0x40=1.0
P0:0xd4	Contrast center	8	0x80	RW	Contrast center value
P0:0xd5	Luma_offset	8	0x00	RW	Add offset on luma value. S7.
P0:0xd6	skin_Cb_center	8	0xe8	RW	Cb criteria for skin detection.
P0:0xd7	skin_Cr_center	4	0x18	RW	Cr criteria for skin detection.

P0:0xd8	Skin radius square	8	0x28	RW	Defines skin range
P0:0xd9	Skin brightness THD	8	0xe3	RW	[7:4] skin brightness high threshold [3:0] skin brightness low threshold
P0:0xda	Fixed_Cb	8	0x00	RW	Fixed Cb value to achieve special effect
P0:0xdb	Fixed_Cr	8	0x00	RW	Fixed Cr value to achieve special effect
P0:0xdd	Edge mode	8	0xb8	RW	[7:0] Reserved.
P0:0xde	auto-gray mode Sa_autogray	6	0x36	RW	[5:4] provide 4 modes to decrease saturation [3:0] sa_autogray, proposed gray slope in Cb, Cr domain
P0:0xdf	Saturation_sub_strength	8		RO	Chroma offset in low light
P0:0xed	YCP_Sat_dec_en	1	0x00	RW	YCP_Sat_dec_en
P0:0xee	YCP_Sat_dec_slope	8	0x20	RW	YCP_Sat_dec_slope
P0:0xef	YCP_Sat_dec_start	8	0x30	RW	YCP_Sat_dec_start

ABS

Address	Name	Width	Default Value	R/W	Description
P1:0x9a	ABS_range_compesate ABS_skip_frame	7	0x03	RW	[7:4] X4+3, add "more range" to enlarge more stretch [3] NA [2:0] Set number of frames to be skipped in ABS adjustment
P1:0x9b	ABS_stop_margin	4	0x02	RW	[7:4] NA [3:0] margin for ABS to stop adjustment
P1:0x9c	Y_S_compensate ABS_manual_K	8	0x01	RW	[7:4] Y stretch compensate [3:0] manual ABS slope adjustment, default 0
P1:0x9d	Y_stretch_limit	8	0x20	RW	[7:0] Y stretch limit

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P1:0x9e	Y_tilt	8		RO	[7:0] the corner point, stretch Y if less than it
P1:0x9f	Y_stretch_K	8		RO	[7:0] the slope ABS calculated for Y less than Y_tilt, 2.6bits

AEC

Address	Name	Width	Default Value	R/W	Description
P1:0x10	AEC_mode1	8	0x40	RW	[7] Reserved. [6] measure point [5] exp mode [4:3] NA [2] AEC gain mode [1:0] skip mode
P1:0x11	AEC_mode2	8	0x21	RW	[7] fix target [6:4] AEC take action every N frame [3:2] close frame number to eliminate bad frame [1] change exposure gain mode [0] dead zone mode
P1:0x12	AEC_mode3	8	0x20	RW	[7] map measure point [6:4] center weight mode [3:2] skin weight mode [1:0] Reserved.
P1:0x13	AEC_target_Y_start	8	0x48	RW	expected luminance value
P1:0x14	Y_average	8		RO	Current frame luminance average
P1:0x15	AEC_high_low_range	8	0xf2	RW	[7:4] x16, count limit for high luminance pixels [3:0] x4, count limit for low luminance pixels
P1:0x17	AEC_ignore	5	0x18	RW	[7] AEC ignore enable [6:5] AEC ignore select mode [4] Reserved. [3:0] AEC ignore number
P1:0x1a	AEC_slow_margin AEC_slow_speed	7	0x91	RW	[7:4] AEC slow margin [3] NA [2:0] AEC slow speed
P1:0x1b	AEC_fast_margin	7	0x96	RW	[7:4] AEC fast margin, X4 [3] NA

	AEC_fast_speed				[2:0] AEC fast speed
P1:0x1c	AEC_exp_change_gain_ratio	8	0x96	RW	Gain change criteria, float 1.7, default use 1.2x
P1:0x1d	AEC_step2	8	0x01	RW	Reserved.
P1:0x1e	AEC_I_frames AEC_D_ratio	6	0x33	RW	[7:6] NA [5:4] Y difference selection mode [3:0] differential coefficient in AEC control algorithm
P1:0x1f	AEC_I_stop_L_margin	7	0x07	RW	[7] NA [6:0] x2, Will be used as AEC convergence margin when P0:0xd1[0]=0
P1:0x20	AEC_I_stop_margin AEC_I_ratio	8	0x41	RW	[7:4] AEC adjust stop margin [3:0] integration coefficient
P1:0x21	AEC_max_pose_dg_gain	8	0xc0	RW	The max post-gain AEC can output.
P1:0x22	AEC_max_pre_dg_gain	8	0x60	RW	The max pre-gain AEC can output.
P1:0x29	AEC_anti_flicker_step[11:8]	4	0x00	RW	Anti-flicker step
P1:0x2a	AEC_anti_flicker_step[7:0]	8	0x96	RW	
P1:0x2b	AEC_exp_level_0[11:8]	4	0x02	RW	Exposure level 0
P1:0x2c	AEC_exp_level_0[7:0]	8	0x58	RW	
P1:0x2d	AEC_exp_level_1[11:8]	4	0x03	RW	Exposure level 1
P1:0x2e	AEC_exp_level_1[7:0]	8	0x84	RW	
P1:0x2f	AEC_exp_level_2[11:8]	4	0x07	RW	Exposure level 2
P1:0x30	AEC_exp_level_2[7:0]	8	0x08	RW	
P1:0x31	AEC_exp_level_3[11:8]	4	0x0d	RW	Exposure level 3
P1:0x32	AEC_exp_level_3[7:0]	8	0x7a	RW	
P1:0x33	AEC_max_exp	6	0x20	RW	[5:4]Max level setting

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	_level AEC_exp_min _l[11:8]				[3:0] exp_min[11:8]
P1:0x34	AEC_exp_min _l[7:0]	8	0x04	RW	exp_min[7:0]

ASDE

Address	Name	Width	Default Value	R/W	Description
P1:0x18	AEC_luma_div	8	0x05	RW	[7:4] for AWB [3:0] for ASDE
P0:0x9c	ASDE_DN_b_slope	4	0x06	RW	[3:0] ASDE_DN_b_slope
P0:0x9d	ASDE_DN_bilat_b	6		RO	
P0:0x9e	ASDE_DN_n_slope ASDE_DN_c_slope	8	0xea	RW	[7:4] ASDE_DN_n_slope [3:0] ASDE_DN_c_slope
P0:0x9f	ASDE_DN_bilat_n ASDE_DN_C_coeff[4:1]	8		RO	
P0:0xa0	ASDE_DD_bright_th_slope ASDE_DD_limit_slope	8	0x5f	RW	[7:4] ASDE_DD_bright_th_slope [3:0] ASDE_DD_limit_slope
P0:0xa1	ASDE_DD_bright_th ASDE_DD_limit	8		RO	
P0:0xa2	ASDE_EE1_effect_slope ASDE_EE2_effect_slope	8	0x12	RW	[7:4] ASDE_EE1_effect_slope [3:0] ASDE_EE2_effect_slope
P0:0xa3	ASDE_edge1_effect ASDE_edge2_effect	8		RO	
P0:0xa4	ASDE_auto_s	8	0x10	RW	auto saturation decrease slope

	aturation_dec_slope				
P0:0xa5	ASDE_auto_saturation_low_limit ASDE_sub_saturation_slope	8	0x31	RW	[7:4] auto saturation low limit [3:0] sub saturation slope
P0:0xa6	ASDE_DD_mm_TH ASDE_DD_mm_TH_slop	8		RO	
P0:0xa7	ASDE_low_luma_value_th	8	0x60	RW	ASDE low luminance value threshold
P0:0xa8	ASDE_LSC_gain_dec_slope	8	0x80	RW	ASDE LSC gain decrease slope
P0:0xa9	ASDE_LSC_dec_value	8		RO	
P1:0xe4	AEC_luma_value	8		RO	For ASDE statistics

Measure Window

Address	Name	Width	Default Value	R/W	Description
P1:0x06	big_win_x0	8	0x08	RW	Window setting for AEC & AWB
P1:0x07	big_win_y0	8	0x06	RW	
P1:0x08	big_win_x1	8	0xa8	RW	
P1:0x09	big_win_y1	8	0xf4	RW	

AWB

Address	Name	Width	Default Value	R/W	Description
P1:0x50	AWB_RGB_high	8	0xf5	RW	Defines the high RGB range of gray pixel to be selected
P1:0x51	AWB_Y_to_C_diff2	8	0x18	RW	Gray pixel criteria
P1:0x52	AWB_Y_to_C_diff2_big	8	0x10	RW	Gray pixel criteria when big_C mode enable
P1:0x53	AWB_C_inter	8	0x20	RW	Cr and Cb line 1
P1:0x54	AWB_C_inter2	8	0x40	RW	Cr and Cb line 2
P1:0x55	AWB_C_max	8	0x20	RW	Chroma limit

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P1:0x56	AWB_C_max_big	8	0x60	RW	Chroma limit when big_C mode enable
P1:0x57	AWB_Y_high	8	0xa0	RW	Give high luminance point more weight
P1:0x58	AWB_number_limit	8	0xa0	RW	Number limit, X4
P1:0x59	AWB_adjust_mode AWB_auto_window Sel_point Skip_mode	8	0x08	RW	[5:4] AWB adjust mode [3] AWB auto window [2] AWB sample location [1:0] AWB skip mode
P1:0x5a	Light_gain_range	4	0x30	RW	[7:4] NA [3:0]dark mode low luma range
P1:0x5b	move_TH move_number_limit	8	0x62	RW	[7:4] AWB move threshold [3:0] move number limit
P1:0x5c	show_and_mode	8	0x34	RW	[7:0] Reserved.
P1:0x5d	adjust_speed adjust_margin	7	0x42	RW	[7] NA [6:4] AWB gain adjust speed [3:0] AWB margin
P1:0x5e	every_N light_temp_mode	6	0x29	RW	[7:6] NA [5:4] AWB every N [3:2] Smooth mode 1 0: no smooth 0 1: FIR smooth [1] NA [0] using color temperature curve method
P1:0x5f	R_5k_gain	8	0x42	RW	R_5k gain
P1:0x60	B_5k_gain	8	0x43	RW	B_5k gain
P1:0x61	AWB_sinT	8	0xc2	RW	AWB sinT
P1:0x62	AWB_cosT	8	0xa8	RW	AWB cosT
P1:0x63	AWB_X1_cut	8	0x18	RW	Defines color temperature curve range in Cb,Cr domain. Float 2.6
P1:0x64	AWB_X2_cut	8	0x40	RW	
P1:0x65	AWB_Y1_cut	8	0xd0	RW	
P1:0x66	AWB_Y2_cut	8	0xf5	RW	
P1:0x67	AWB_R_gain_limit	8	0x70	RW	channel gain limit for R, G, B. Float 2.6
P1:0x68	AWB_G_gain_limit	8	0x58	RW	

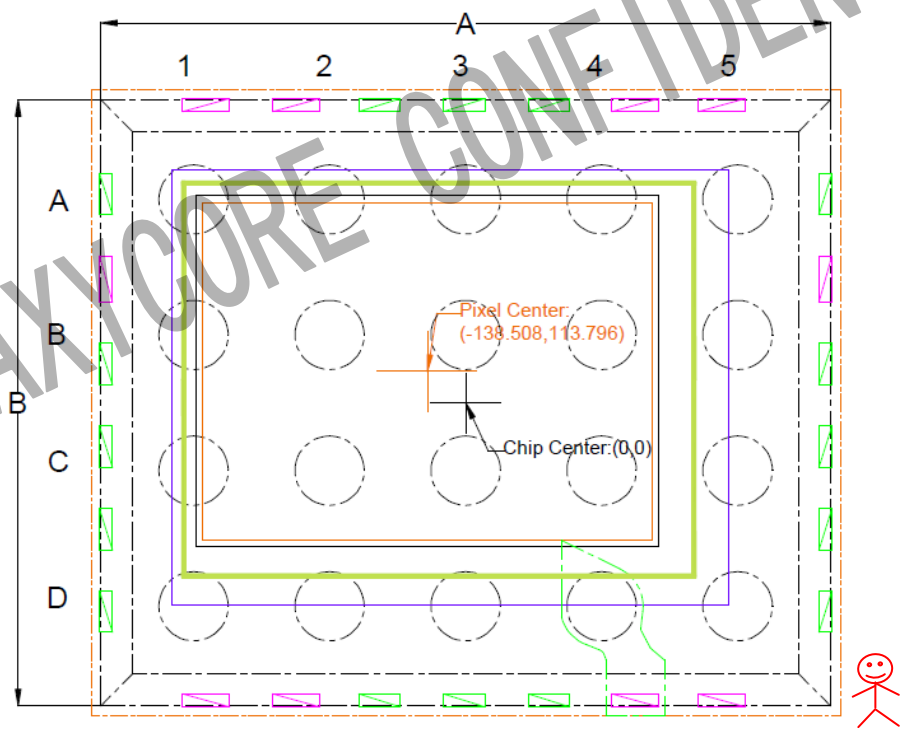
P1:0x69	AWB_B_gain_limit	8	0x78	RW	
P1:0x6a	AWB_small_win_width_step	8	0x4f	RW	When auto_awb_window is 0,can be write
P1:0x6b	AWB_small_win_height_step	8	0x3a	RW	When auto_awb_window is 0,can be write
P1:0x6c	AWB_C_inter_big	8	0x80	RW	AWB_C_inter_big
P1:0x6d	AWB_C_inter2_big	8	0x00	RW	AWB_C_inter2_big
P1:0x6e	AWB_outdoor_mode	7	0x00	RW	Reserved.
P1:0x70	AWB_C_number_limit	8	0x50	RW	AWB C number limit
P1:0x71	AWB_C_weight_mode	8	0x20	RW	Reserved.
P1:0x72	AWB_RGB_low	8	0x0a	RW	Defines the low RGB range of gray pixel to be selected
P1:0x73	AWB_uplow_luma_value	8	0xe0	RW	When Luma level bigger than this , enlarge AWB_RGB_low as pixel Y low range limit
P1:0x7f	AWB_CT_change_THD	6	0x20	RW	When yellow block than it should be adjust on time
P1:0x80	AWB_R_gain_out_h_limit	8	0x50	RW	AWB outdoor R gain high limit
P1:0x81	AWB_G_gain_out_h_limit	8	0x58	RW	AWB outdoor G gain high limit
P1:0x82	AWB_B_gain_out_h_limit	8	0x46	RW	AWB outdoor B gain high limit
P1:0x83	AWB_R_gain_out_l_limit	8	0x40	RW	AWB outdoor R gain low limit
P1:0x84	AWB_G_gain_out_l_limit	8	0x40	RW	AWB outdoor G gain low limit
P1:0x85	AWB_B_gain_out_l_limit	8	0x40	RW	AWB outdoor B gain low limit
P1:0x86	AWB_XR_cut	8	0x40	RW	Defines a larger color temperature curve range in Cb,Cr domain. Float 2.6
P1:0x87	AWB_XL_cut	8	0x7b	RW	
P1:0x88	AWB_YT_cut	8	0xfe	RW	
P1:0x89	AWB_YB_cut	8	0xa0	RW	

One plus one mode

Address	Name	Width	Default Value	R/W	Description
P0:0xab	Transmitter_freq_div	4	0x00	RW	[3:0] SPI transmitter freq div
P0:0xac	Pad_delay_cnt	8	0x20	RW	Delay of pad switch input/output
P0:0xad	Hsync_isp_width[9:8] High_speed_mode Rec_regw_mode Rec_pos_sample Rec_enable	8	0x00	RW	[7:6] NA [5:4] Image width received [9:8] [3] High_speed_mode [2] the mode of generate regw Set 1 if receive dark data to support BLK [1] select the sample edge of SPI signal [0] SPI receiver enable
P0:0xae	Hsync_isp_width[7:0]	8	0xf8	RW	Image width received [7:0]
P0:0xaf	Hsync_delay_cnt	8	0x40	RW	Space between hsync_ad and hsync_isp

7. Pin Description

7.1 GC0329 CSP package Top view（unit:μm）



7.2 CSP ball description

	1	2	3	4	5
A	**AVDD25**	**HSYNC**	**VSYNC**	**SBCL**	**D<7>**
B	**AVDD28**	**RESETB**	**SBDA**	**D<6>**	**D<5>**
C	**GND**	**POWERDOWN**	**D<2>**	**PCLK**	**D<4>**
D	**INCLK**	**D<0>**	**D<1>**	**D<3>**	**IOVDD**

7.3 GC0329 chip pin description

Pin	Name	Pin Type	Description
A1	**AVDD25**	POWER	Internal analog voltage. Please connect 0.1μF or 0.47μF capacity to ground.
A2	**HSYNC**	Output	HSYNC output

A3	**VSYNC**	Output	VSYNC output
A4	**SBCL**	Input	Two-wire serial bus, clock
A5	**D<7>**	Output	YUV/RGB data output bit[7]
B1	**AVDD28**	Power	Main power supply pin, typical 2.8V, Please connect 0.1μF or 0.47μF capacity to ground.
B2	**RESETB**	Input	Chip reset control: 0: chip reset 1: normal work
B3	**SBDA**	I/O	Two-wire serial bus, data
B4	**D<6>**	Output	YUV/RGB data output bit[6]
B5	**D<5>**	Output	YUV/RGB data output bit[5]
C1	**GND**	Ground	Chip ground
C2	**POWERDOWN**	Input	Sensor power down control: 0: normal work 1: standby
C3	**D<2>**	Output	YUV/RGB data output bit[2]
C4	**PCLK**	Output	Pixel clock output
C5	**D<4>**	Output	YUV/RGB data output bit[4]
D1	**INCLK**	Input	Main clock
D2	**D<0>**	Output	YUV/RGB data output bit[0]
D3	**D<1>**	Output	YUV/RGB data output bit[1]
D4	**D<3>**	Output	YUV/RGB data output bit[3]
D5	**IOVDD**	Power	Power Supply for I/O circuits, 1.7~3.0V. Please connect 0.1μF or 0.47μF capacity to ground.

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7.4 CSP package mechanical drawing (unit: μm)