ARM®-based 32-bit Cortex®-M4 MCU with 16 KB to 64 KB Flash, sLib, 10 timers, 1 ADC, 1 COMP, 7 communication interfaces

Feature

- **Core: ARM® 32-bit Cortex®-M4 CPU**
  - 120 MHz maximum frequency, with a memory protection unit (MPU)
  - Single-cycle multiplication and hardware division
  - DSP instructions
- **Memories**
  - 16 Kbytes to 64 Kbytes of main Flash instruction/data memory
  - 4 Kbytes of system memory used as a Bootloader or as a general instruction/data memory (one-time-configured)
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - 8 Kbytes to 16 Kbytes of SRAM
- **CRC calculation unit**
- **Reset and supply management**
  - 2.4 to 3.6 V application supply and I/Os
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, and Standby; 4 x WKUP pins can wake up standby mode
  - Supports 5 x 32-bit backup registers
- **Clock management**
  - 4 to 25 MHz crystal oscillator
  - Internal 48 MHz factory-trimmed RC (accuracy 1 % at T_A = 25 °C, 2 % at T_A = -40 to +105 °C)
  - PLL flexible 31 to 500 multiplication and 1 to 15 division factor
  - Internal 40 kHz RC
  - 32 kHz oscillator
- **Up to 39 fast I/Os**
  - All mappable on external interrupt vectors
  - Almost all 5V-tolerant
  - All fast I/Os, control registers accessible with f_{AHB} speed
- **5-channel DMA controller**
- **One 12-bit 2 MSPS A/D converter, up to 15 external channels**
- **One comparator, 5 external channels and 1 internal voltage reference**
- **Up to 10 timers**
  - 1 x 16-bit 7-channel advanced timers, 6-channel PWM output with dead-time generator and emergency stop
  - Up to 5 x 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 1 x 16-bit basic timer
  - 2 x watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with alarm, subsecond accuracy, hardware calendar and calibration**
- **Up to 7 communication interfaces**
  - 2 x I^2C interfaces (SMBus/PMBus)
  - 2 x USARTs supporting master synchronous SPI and modem control, with ISO7816 interface, LIN, IrDA; swappable TX/RX pins
  - 2 x SPIs (50 Mbit/s), both with I^2S interface multiplexed
  - Infrared transmitter
- **Serial wire debug (SWD) interface**
- **96-bit unique ID (UID)**
- **Operating temperatures: -40 °C to +105 °C**
- **Packages**
  - LQFP48 7 x 7 mm
  - LQFP32 7 x 7 mm
  - LQFP32 5 x 5 mm
  - QFN32 4 x 4 mm
  - QFN28 4 x 4 mm
  - TSSOP20 6.5 x 4.4 mm

Table 1. Device summary

Flash	Part number
64 KBytes	AT32F421C8T7, AT32F421K8T7, AT32F421K8U7, AT32F421K8U7-4, AT32F421G8U7, AT32F421F8P7
32 KBytes	AT32F421C6T7, AT32F421K6T7, AT32F421K6U7, AT32F421K6U7-4, AT32F421G6U7, AT32F421F6P7
16 KBytes	AT32F421C4T7, AT32F421K4T7, AT32F421K4U7, AT32F421K4U7-4, AT32F421G4U7, AT32F421F4P7

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the AT32F421 microcontrollers.

The AT32F421 datasheet should be read in conjunction with the AT32F421 reference manual. For information on programming, erasing, and protection of the internal Flash memory please also refer to the AT32F421 reference manual.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website at the following address:

http://infocenter.arm.com

2 Description

The AT32F421 incorporates the high-performance ARM® Cortex®-M4 32-bit RISC core with operating frequency maximum 120 MHz. The Cortex®-M4 core features a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The AT32F421 incorporates high-speed embedded memories (up to 64 Kbytes of Flash memory and 16 Kbytes of SRAM), enhanced I/Os and peripherals connected to two APB buses. Any block of the Flash memory can be protected by the sLib, functioning as a security area with code-executable only.

The AT32F421 offers one 12-bit ADC, 1 analog comparator, five general-purpose 16-bit timers, and one advanced timer for motor control, as well as standard and advanced communication interfaces, up to two I^2Cs, two SPIs (both multiplexed as I^2Ss), two USARTs, and an infrared transmitter.

The AT32F421 operates in the -40 to +105 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

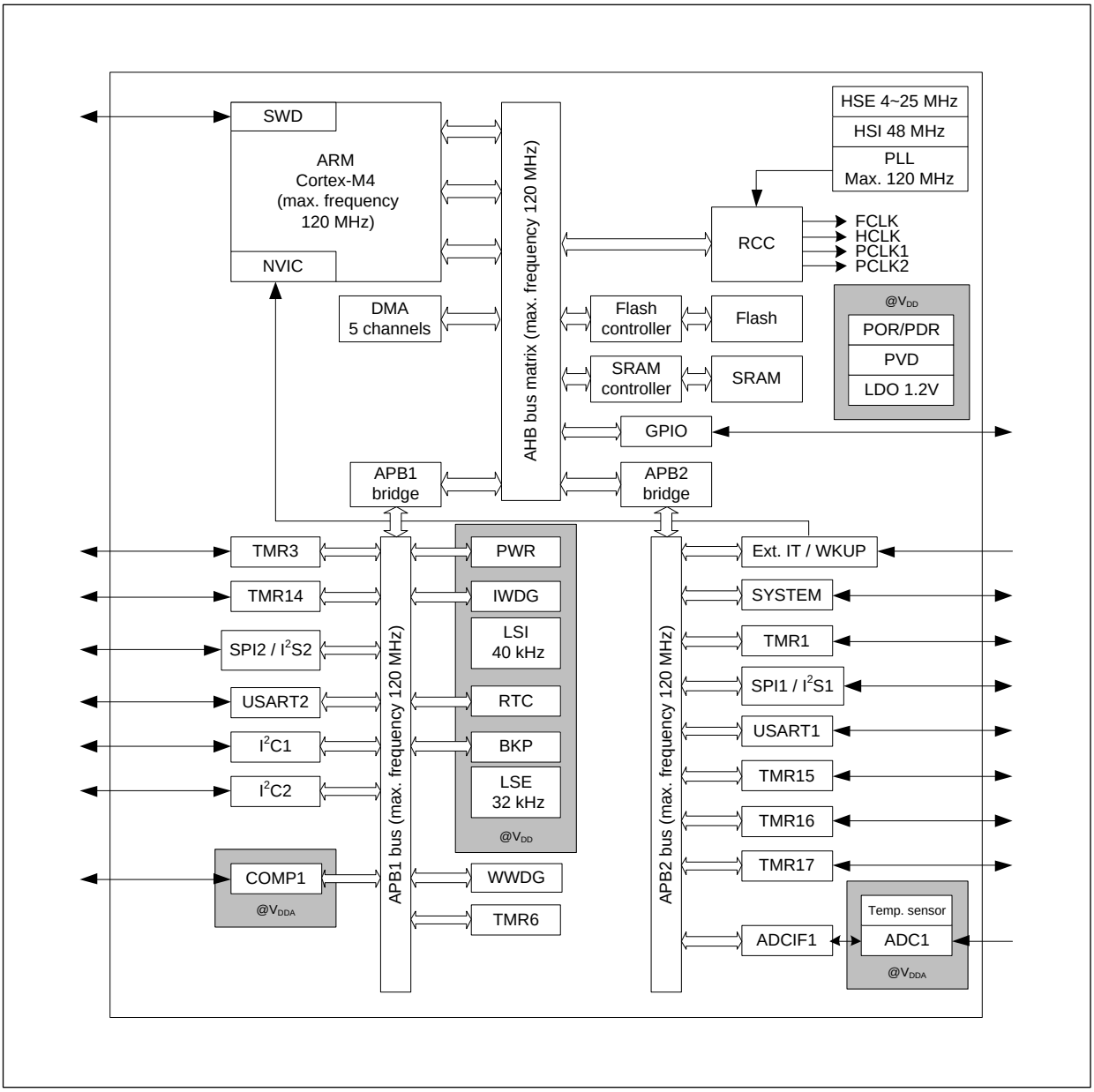
The AT32F421 offers devices in six different package types: from 20 pins to 48 pins. Depending on the different packages, the pin-to-pin is completely compatible among devices, and also the software and functionality. Only different sets of peripherals are included. The description below gives an overview of the complete range of peripherals proposed in different devices.

Table 2. AT32F421 features and peripheral counts

Part Number		AT32F421xxP7			AT32F421xxU7			AT32F421xxU7-4			AT32F421xxU7			AT32F421xxT7			AT32F421xxT7		
		F4	F6	F8	G4	G6	G8	K4	K6	K8	K4	K6	K8	K4	K6	K8	C4	C6	C8
CPU frequency (MHz)		120																	
Flash (KBytes)		16	32	64	16	32	64	16	32	64	16	32	64	16	32	64	16	32	64
SRAM (KBytes)		8	16	16	8	16	16	8	16	16	8	16	16	8	16	16	8	16	16
Timers	Advanced	1			1			1			1			1			1		
	16-bit general-purpose	5			5			5			5			5			5		
	Basic	1			1			1			1			1			1		
	SysTick	1			1			1			1			1			1		
	IWDG	1			1			1			1			1			1		
	WWDG	1			1			1			1			1			1		
	ERTC	1			1			1			1			1			1		
Communication	I^2C	2			2			2			2			2			2		
	SPI/I^2S	1/1(1)			2/2			2/2			2/2			2/2			2/2		
	USART+UART	1+1(2)			2+0			2+0			2+0			2+0			2+0		
	IR	1			1			1			1			1			1		
Analog	12-bit ADC numbers/ channels	1			1			1			1			1			1		
		9			10			11			11			10			15		
	Comparator	1			1			1			1			1			1		
GPIO		15			23			27			27			25			39		
Operating temperature		-40 °C to +105 °C																	
Package		TSSOP20 6.5 x 4.4 mm			QFN28 4 x 4 mm			QFN32 4 x 4 mm			QFN32 5 x 5 mm			LQFP32 7 x 7 mm			LQFP48 7 x 7 mm		

(1) Only SPI1 exists on TSSOP20 package.
(2) All pins of USART2 are available on TSSOP20 package. USART1 only has TX and RX pins and is used as UART restrictedly.

Figure 1. AT32F421 block diagram



3 Overview

3.1 ARM® Cortex®-M4 core and DSP instruction set

The ARM Cortex®-M4 is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex®-M4 32-bit RISC processor features exceptional code efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

With its embedded ARM core, the AT32F421 is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the AT32F421.

3.2 Memories

3.2.1 Embedded Flash memory

Up to 64 Kbytes of embedded Flash is available for storing programs and data. User can configure any part of the Flash memory protected by the sLib, functioning as a security area with code-executable only but non-readable. sLib is a mechanism that protects the intelligence of solution venders and facilitates the second-level development by customers.

There are 4 Kbytes of system memory embedded on the AT32F421, in which the Bootloader is resided. If the Bootloader is not used, this block can be one-time configured as a general purpose instruction/data area.

Option Bytes are included. They are used to configure hardware behaviours such as read/write protection and software/hardware watchdog. The read and write protection of the embedded Flash can be configured individually with Option Bytes. Two read protection levels are defined.

3.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to eight protected areas that can in turn be divided up into eight subareas. The protection area sizes are between 32 bytes and the whole 4 Gbytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.2.3 Embedded SRAM

Up to 16 Kbytes of SRAM is embedded and it can be accessed (read/write) at CPU clock speed with 0 wait state.

3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.4 Interrupts and events

3.4.1 Nested vectored interrupt controller (NVIC)

The AT32F421 embeds a nested vectored interrupt controller able to manage 16 priority levels and handle up to 28 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.4.2 External interrupt/event controller (EXTI)

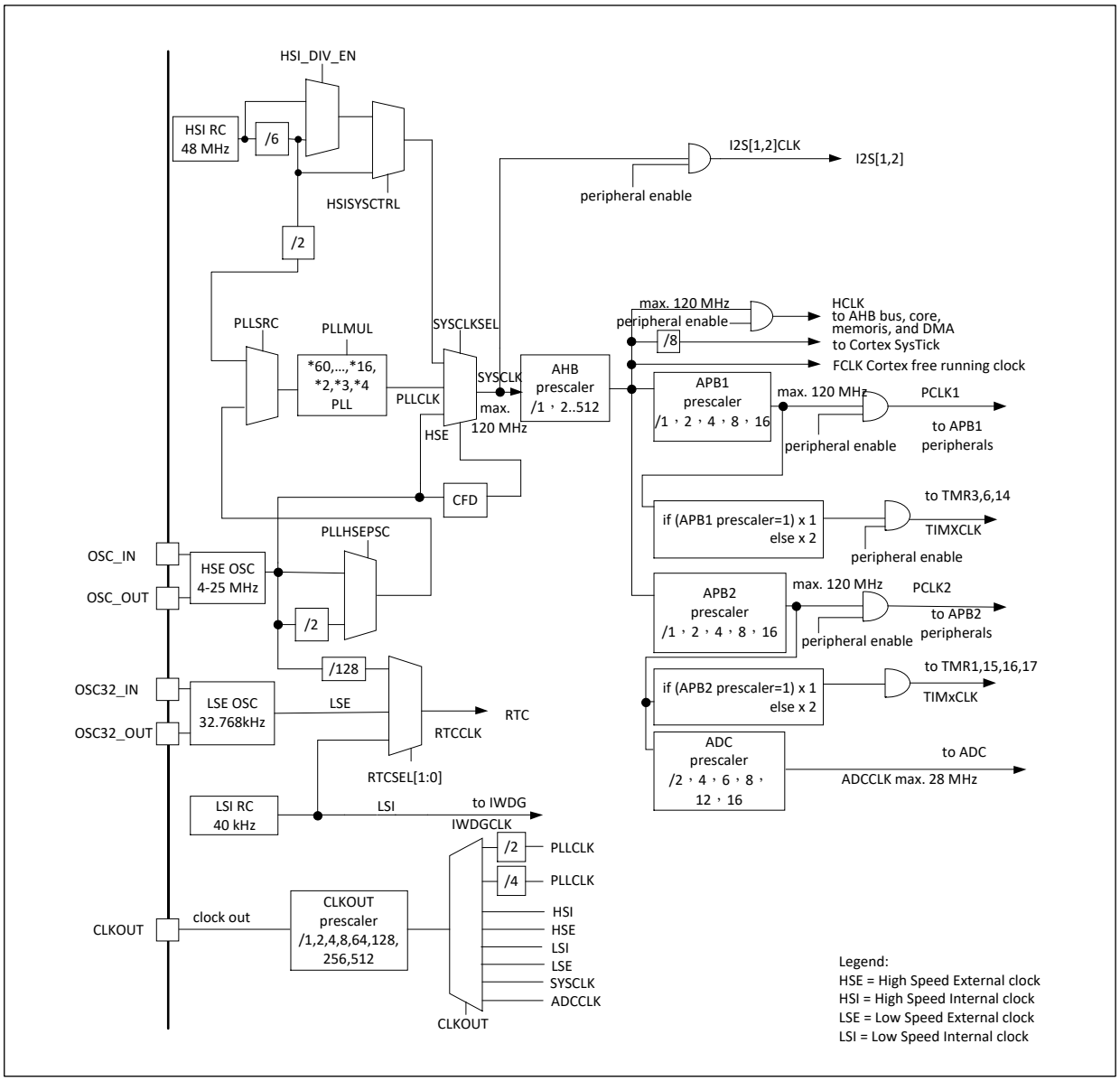
The external interrupt/event controller consists of 20 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, or both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal AHB clock period. Up to 16 GPIOs can be selected to the external interrupt lines.

3.5 Clocks and startup

System clock selection is performed on startup, however the internal RC 48 MHz oscillator (HSI) through a divided-by-6 divider (8 MHz) is selected as default CPU clock on reset. An external 4 to 25 MHz clock (HSE) can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator (HSI). A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, and the APB (APB1 and APB2) domains. The maximum frequency of the AHB and APB domain is 120 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



3.6 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The bootloader is stored in system memory. It is used to reprogram the Flash memory through USART1 or USART2. *Table 3* provides the supporting interfaces of the Bootloader to different AT32F421 part numbers and pin configurations.

Table 3. The Bootloader supporting pin configurations

Interface	Pin
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX PA3: USART2_RX

3.7 Power supply management

3.7.1 Power supply schemes

- V_{DD} = 2.4～3.6 V: external power supply for I/Os, ERTC, external 32 kHz oscillator, backup registers and internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.4～3.6 V: external analog power supplies for ADC and COMP. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

For more detail on how to connect power pins, refer to *Figure 11.*

3.7.2 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.4 V. The device remains in reset mode when V_{DD} is below a specified threshold ($V_{POR/PDR}$), without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 11* and *Table 12* for the characteristic values of $V_{POR/PDR}$ and V_{PVD}.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power down.

- Main mode (MR) is used in the nominal regulation mode (Run) or in the Stop mode
- Low-power mode (LPR) can be used in the Stop mode
- Power down mode is used in Standby mode: the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption of the regulator (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

3.7.4 Low-power modes

The AT32F421 supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator is put in normal mode (MR) or low-power mode (LPR), among them, the low-power mode can also adjust the output voltage of voltage regulator to further reduce the power consumption.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the ERTC alarm/tamper/timestamp event, or COMP wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup and RTC domains.
  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUPx pin, or an ERTC alarm/tamper/timestamp event occurs.

Note: The ERTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Direct memory access (DMA)

The flexible 5-channel general-purpose DMAs are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers.

The DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPIs, I^2Ss, I^2Cs, USARTs, all timers TMRx (except for TMR14), and ADC.

3.9 ERTC (enhanced real-time clock) and backup registers

The backup domain includes:

- The enhanced real-time clock (ERTC)
- Five 32-bit backup registers

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value is also available in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms with wake up from Stop or Standby mode capability
- On-the-fly correction from 1 to 32767 ERTC clock pulses during. This can be used to synchronize the ERTC with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate quartz crystal inaccuracy.
- Anti-tamper detection pin with programmable filter. The MCU can wake up from Stop or Standby mode on tamper event dectecton.

- Time stamp feature can be used to save calendar content. This function can be triggered by an event by and event on the timestamp pin or by a tamper event. The MCU can wake up from Stop or Standby mode on timestamp event dectecton.
- Reference clock detection: a more precise secondary clock source (50 or 60 Hz) can be used to enhance the calendar precision.

The alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 20 bytes of user application data. Backup registers are not reset by a system, or when the device wakes up from the Standby mode.

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The ERTC clock sources can be:

- A 32.768 kHz external crystal, external resonator, or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 40 kHz)
- The high-speed external clock (HSE) divided by 32

3.10 Timers and watchdogs

The AT32F421 devices include one advanced timer, five general-purpose timers, one basic timer, two watchdog timers, and a SysTick timer.

The table below compares the features of different timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TMR15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TMR16 TMR17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

3.10.1 Advanced timers (TMR1)

An advanced timers (TMR1) can be seen a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0~100%)
- One-pulse mode output

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR timers which have the same architecture. The advanced timer can therefore work together with the general-purpose timers via the link feature for synchronization or event chaining.

3.10.2 General-purpose timers (TMR3, TMR14, TMR15, TMR16, and TMR17)

There are five synchronizable general-purpose timers embedded in the AT32F421. Each timer can be used to generate PWM output or as a time base.

- **TMR3**

  The TMR3 timer is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. It features four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs.

  The TMR3 general-purpose timer can work together with the advanced timers via the Timer link feature for synchronization or event chaining. TMR3 can be used to generate PWM outputs, and is capable of handling quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors.

  In debug mode, the counter can be frozen. TMR3 has independent DMA request generation.

- **TMR14**

  TMR14 is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channel for input capture/output compare, PWM, or one-pulse mode output. It can be synchronized with the full-featured general-purpose timers. It can also be used as simple time bases.

  In debug mode, the counter can be frozen.

- **TMR15, TMR16 and TMR17**

  These timers are based on a 16-bit auto-reload upcounter, a 16-bit prescaler. TMR15 features two channels and one complementary channel. TMR16 and TMR17 have one channel and one complementary channel. All channels can be used for input capture/output compare, PWM, or one-pulse mode output.

  They can be synchronized with the full-featured general-purpose timers via the Timer link feature for synchronization or event chaining.

  In debug mode, the counter can be frozen. These timers have independent DMA request generation.

3.10.3 Basic timers (TMR6)

This timer is used as a generic 16-bit basic time base.

3.10.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.10.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.10.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.11 Inter-integrated circuit interface (I^2C)

Two I^2C bus interfaces can operate in multi-master and slave modes. They can support standard (up to 100 kHz) and fast modes (up to 400 kHz). The I^2C bus frequency can be increased up to 1 MHz. For more details, please contact your nearest Artery sales office for technical support.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

3.12 Universal synchronous/asynchronous receiver transmitter (USART)

The AT32F421 embeds two universal synchronous/asynchronous receivers/transmitters (USART1 and USART2).

These two USART interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, master synchronous communication, single-wire half-duplex communication mode, and have LIN Master/Slave capability. These two USART interfaces also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant). These two USART interfaces can be served by the DMA controller. TX/RX pins are swappable configuration.

Two USARTs are able to communicate at speeds of up to 7.5 Mbit/s.

3.13 Serial peripheral interface (SPI)/Inter-integrated sound interface (I^2S)

Two SPIs are able to communicate up to 50 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC modes.

Two standard I^2S interfaces (multiplexed with SPI) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Both SPIs can be served by the DMA controller.

3.14 Infrared transmitter (IR)

The AT32F421 device provides an infrared transmitter solution. The solution is based on the internal connection between TMR16, USART1 or USART2 and TMR17. TMR17 is used to provide the carrier frequency, and TMR16, USART1 or USART2 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR16 channel 1 and TMR17 channel 1 must be correctly configured to generate the correct waveform. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

3.15 General inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O's alternate function configuration can be locked, if needed, in order to avoid spurious writing to the I/Os registers.

3.16 Analog to digital converter (ADC)

One 12-bit analog-to-digital converters are embedded into AT32F421 devices and it has up to 15 external channels and 3 internal channels (temperature sensor, internal reference voltage, and V_{SSA}), performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced timer (TMR1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize ADC conversion and timers.

3.16.1 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.4 V ≤ V_{DDA} ≤ 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.16.2 Internal reference voltage (V_{REFINT})

The internal reference voltage (V_{REFINT}) provides a stable voltage output for ADC and comparators. The V_{REFINT} is internally connected to the ADC_IN17 input channel which is used to convert the V_{REFINT} output voltage into a digital value.

3.17 Comparator (COMP)

The AT32F421 embeds one rail-to-rail comparator with programmable reference voltage (internal or external), hysteresis, speed, selectable output polarity, output blanking and noise filter.

The reference voltage can be one of the following:

- External I/O
- Internal voltage reference or submultiple (1/4, 1/2, 3/4). Refer to *Table 13* for the value and precision of the internal voltage reference.

The comparator can wake up Stop mode, and also can generate interrupts and breaks for timers.

3.18 Serial wire debug port (SW-DP)

The ARM SW-DP Interface is embedded, and is a serial wire debug port that enables a serial wire debug to be connected to the target to implement the programming and debugging of the target.

4 Pinouts and pin descriptions

Figure 3. AT32F421 LQFP48 pinout

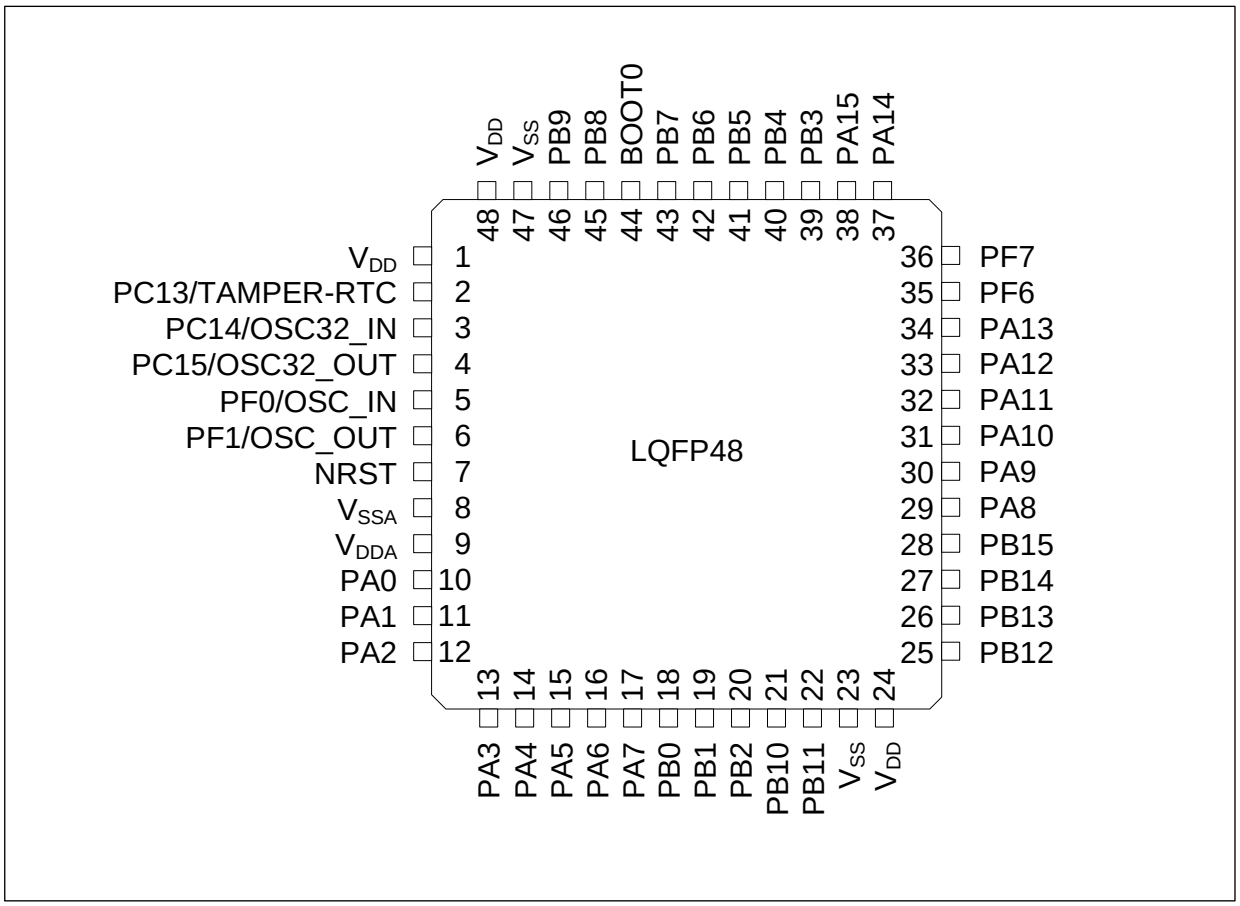


Figure 4. AT32F421 LQFP32 pinout

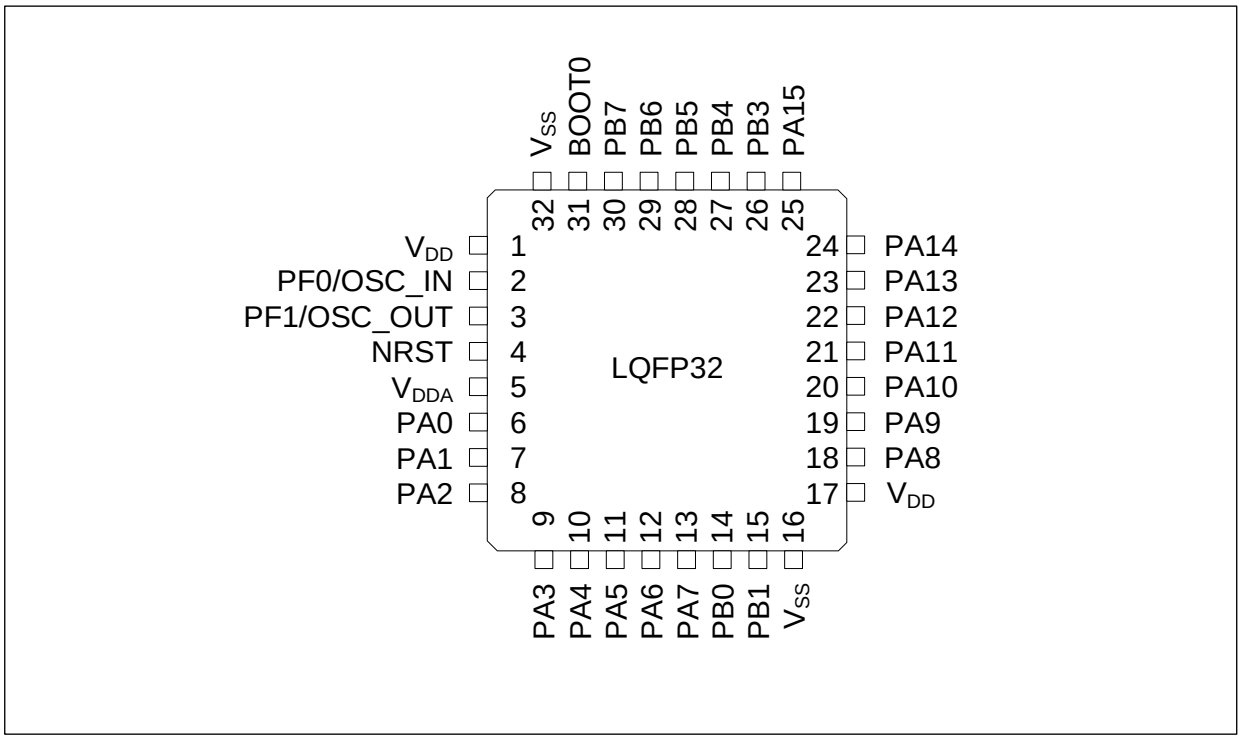


Figure 5. AT32F421 QFN32 pinout

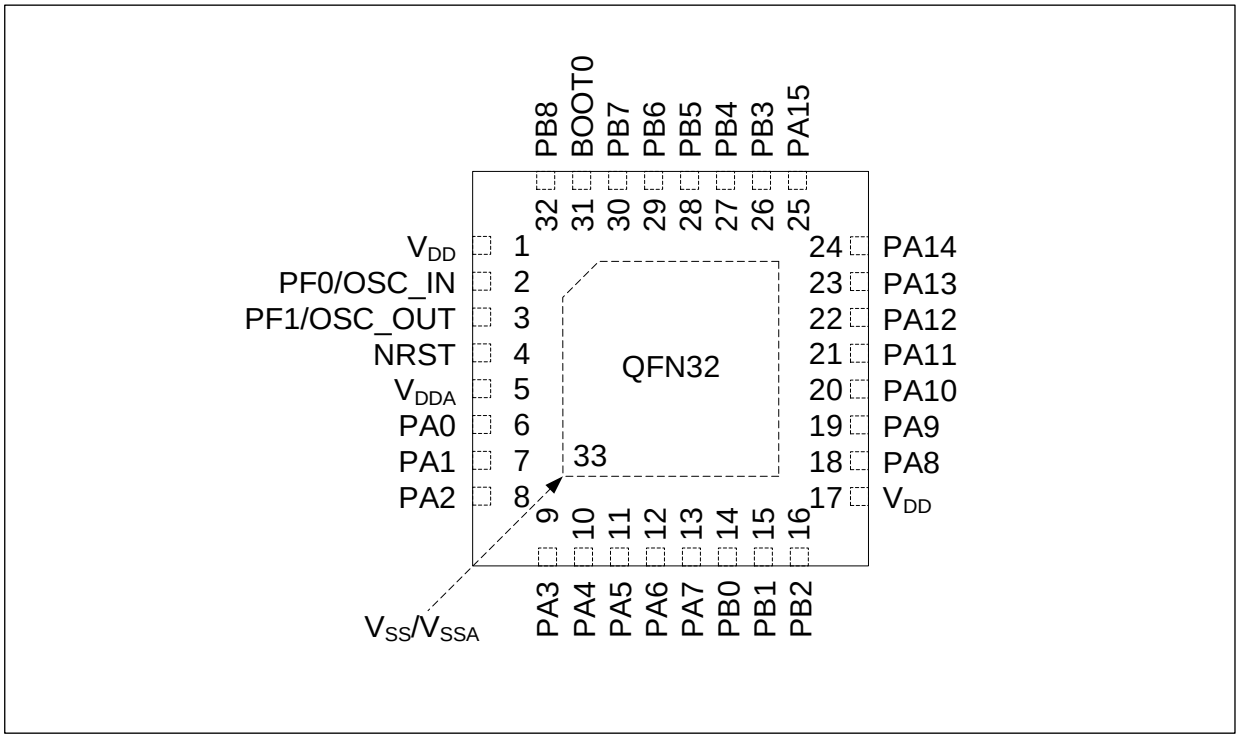


Figure 6. AT32F421 QFN28 pinout

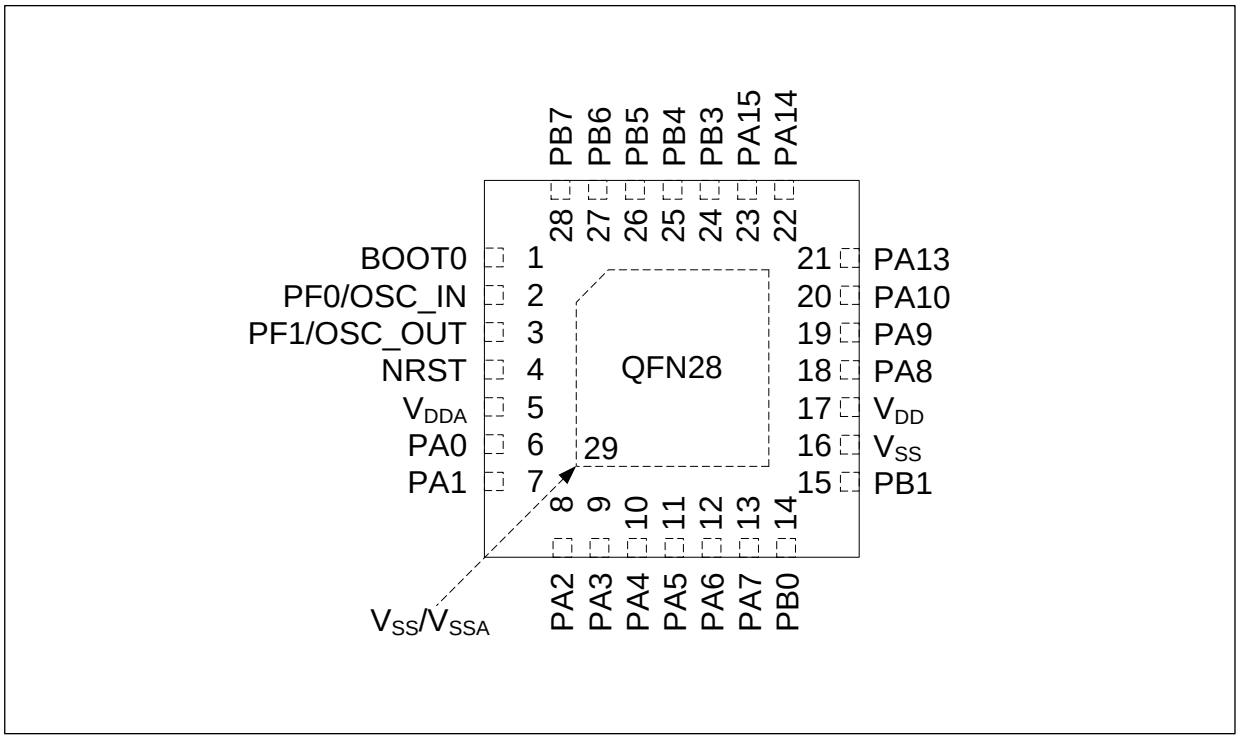
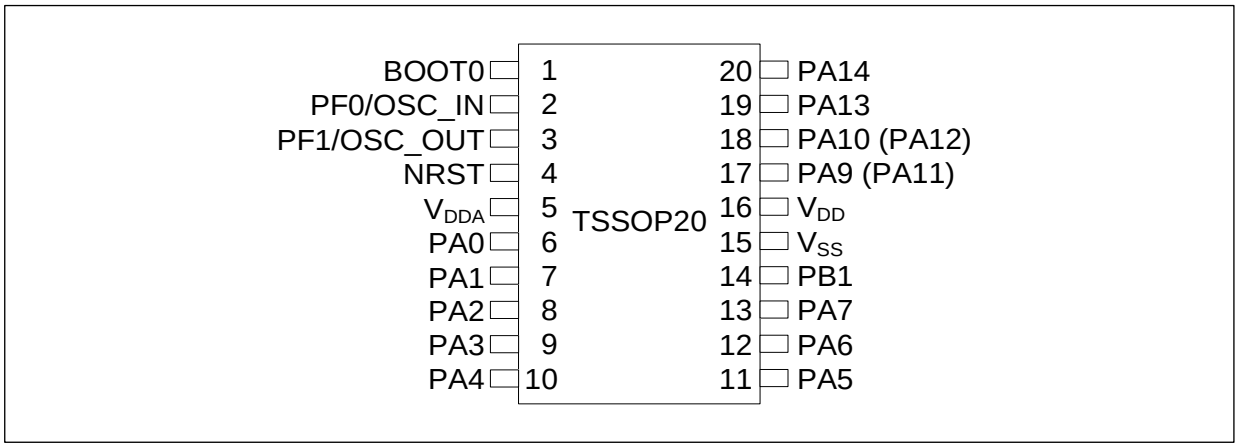


Figure 7. AT32F421 TSSOP20 pinout



The table below is the pin definition of the AT32F421. ”-” presents there is no such pinout on the related package.

Table 5. AT32F421 series pin definitions

Pin number					Pin name (after reset)	Pin type(1)	I/O level(2)	Alternate function	Additional function
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
-	-	1	1	1	V_{DD}	S	-	Digital power supply	
-	-	-	-	2	PC13	I/O	FT	-	TAMPER-RTC / WKUP2
-	-	-	-	3	PC14 / OSC32_IN (PC14)	I/O	TC	-	OSC32_IN
-	-	-	-	4	PC15 / OSC32_OUT (PC15)	I/O	TC	-	OSC32_OUT
2	2	2	2	5	PF0 / OSC_IN (PF0)	I/O	TC	I2C1_SDA	OSC_IN
3	3	3	3	6	PF1 / OSC_OUT (PF1)	I/O	TC	I2C1_SCL	OSC_OUT
4	4	4	4	7	NRST	I/O	R	Device reset input / internal reset input (active low)	
-	-	-	-	8	V_{SSA} / V_{REF-}	S	-	Analog ground / negative reference voltage	
5	5	5	5	9	V_{DDA} / V_{REF+}	S	-	Analog power supply / positive reference voltage	
6	6	6	6	10	PA0	I/O	FTa	TMR1_ETR / USART2_CTS / I2C2_SCL / COMP_OUT	ADC_IN0 COMP_INP2 / COMP_INM6 / WKUP1
7	7	7	7	11	PA1	I/O	FTa	TMR15_CH1N / USART2_RTS / I2C2_SDA / EVENTOUT	ADC_IN1 / COMP_INP1
8	8	8	8	12	PA2	I/O	FTa	TMR15_CH1 / USART2_TX	ADC_IN2 / COMP_INM7
9	9	9	9	13	PA3	I/O	FTa	TMR15_CH2 / USART2_RX / I2S2_MCK	ADC_IN3
10	10	10	10	14	PA4	I/O	FTa	TMR14_CH1 / USART2_CK / SPI1_NSS / I2S1_WS	ADC_IN4/ COMP_INM4
11	11	11	11	15	PA5	I/O	FTa	SPI1_SCK / I2S1_CK	ADC_IN5 / COMP_INP0 / COMP_INM5
12	12	12	12	16	PA6	I/O	FTa	TMR1_BKIN / TMR3_CH1 / TMR16_CH1 / SPI1_MISO / I2S1_MCK / I2S2_MCK / COMP_OUT / EVENTOUT	ADC_IN6
13	13	13	13	17	PA7	I/O	FTa	TMR1_CH1N / TMR3_CH2 / TMR14_CH1 / TMR17_CH1 / SPI1_MOSI / I2S1_SD / EVENTOUT	ADC_IN7
-	14	14	14	18	PB0	I/O	FTa	TMR1_CH2N / TMR3_CH3 / USART2_RX / I2S1_MCK / EVENTOUT	ADC_IN8
14	15	15	15	19	PB1	I/O	FTa	TMR1_CH3N / TMR3_CH4 / TMR14_CH1 / SPI2_SCK / I2S2_CK	ADC_IN9
-	-	16	-	20	PB2	I/O	FTa	TMR3_ETR	ADC_IN10

Pin number					Pin name (after reset)	Pin type[1]	I/O level[2]	Alternate function	Additional function
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
-	-	-	-	21	PB10	I/O	FT	SPI2_SCK / I2S2_CK / I2C2_SCL	-
-	-	-	-	22	PB11	I/O	FT	I2C2_SDA / EVENTOUT	-
15	16	-	16	23	V_{SS}	S	-	Digital ground	
16	17	17	17	24	V_{DD}	S	-	Digital power supply	
-	-	-	-	25	PB12	I/O	FTa	TMR1_BKIN / TMR15_BKIN / SPI2_NSS / I2S2_WS / I2C2_SMBA / EVENTOUT	ADC_IN11
-	-	-	-	26	PB13	I/O	FTa	TMR1_CH1N / SPI2_SCK / I2S2_CK / I2C2_SCL	ADC_IN12
-	-	-	-	27	PB14	I/O	FTa	TMR1_CH2N / TMR15_CH1 / SPI2_MISO / I2S2_MCK / I2C2_SDA	ADC_IN13
-	-	-	-	28	PB15	I/O	FTa	TMR1_CH3N / TMR15_CH2 / TMR15_CH1N / SPI2_MOSI / I2S2_SD	ADC_IN14 / RTC_REFIN / WKUP7
-	18	18	18	29	PA8	I/O	FT	TMR1_CH1 / USART1_CK / UART2_TX / I2C2_SCL / CLKOUT / EVENTOUT	-
17	19	19	19	30	PA9	I/O	FT	TMR1_CH2 / TMR15_BKIN / USART1_TX / I2C1_SCL / I2C2_SMBA / CLKOUT	-
18	20	20	20	31	PA10	I/O	FT	TMR1_CH3 / TMR17_BKIN / USART1_RX / I2C1_SDA	-
17[3]	-[4]	21	21	32	PA11	I/O	FT	TMR1_CH4 / USART1_CTS / I2C1_SMBA / I2C2_SCL / COMP_OUT / EVENTOUT	-
18[3]	-[4]	22	22	33	PA12	I/O	FT	TMR1_ETR / USART1_RTS / I2C2_SDA / EVENTOUT	-
19	21	23	23	34	PA13 (SWDIO[5])	I/O	FT	PA13 / IR_OUT / SPI2_MISO / I2S2_MCK	-
-	-	-	-	35	PF6	I/O	FT	I2C2_SCL	-
-	-	-	-	36	PF7	I/O	FT	I2C2_SDA	-
20	22	24	24	37	PA14 (SWCLK[5])	I/O	FT	PA14 / USART2_TX / SPI2_MOSI / I2S2_SD	-
-	23	25	25	38	PA15	I/O	FT	USART2_RX / SPI1_NSS / I2S1_WS / SPI2_NSS / I2S2_WS / EVENTOUT	-
-	24	26	26	39	PB3	I/O	FT	SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / EVENTOUT	-
-	25	27	27	40	PB4	I/O	FT	TMR3_CH1 / TMR17_BKIN / SPI1_MISO / I2S1_MCK / SPI2_MISO / I2S2_MCK / I2C2_SDA / EVENTOUT	-

Pin number					Pin name (after reset)	Pin type(1)	I/O level(2)	Alternate function	Additional function
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
-	26	28	28	41	PB5	I/O	FT	TMR3_CH2 / TMR16_BKIN / SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / I2C1_SMBA	WKUP6
-	27	29	29	42	PB6	I/O	FT	TMR16_CH1N / USART1_TX / I2S1_MCK / I2C1_SCL	-
-	28	30	30	43	PB7	I/O	FT	TMR17_CH1N / USART1_RX / I2C1_SDA	-
1	1	31	31	44	BOOT0	I	B	Boot mode selection 0	
-	-	32	-	45	PB8	I/O	FT	TMR16_CH1 / I2C1_SCL	
-	-	-	-	46	PB9	I/O	FT	TMR17_CH1 / IR_OUT / SPI2_NSS / I2S2_WS / I2S1_MCK / I2C1_SDA / EVENTOUT	
-	-	-	32	47	V_{SS}	S	-	Digital ground	
-	-	-	-	48	V_{DD}	S	-	Digital power supply	
-	29	33	-	-	EPAD (V_{SS}/V_{SSA})	S	-	Digital ground / Analog ground	

(1) I = input, O = output, S = supply.

(2) TC = standard level, FT = general 5 V tolerant, FTa = 5 V tolerant with analog functions, R = bidirectional reset pin with embeded weak pull-up resistor, B = dedicated BOOT0 pin with embeded weak pull-down resistor. FTa is 5 V tolerant pin when set as input floating, input pull-up, or input pull-down; when set as analog mode, it loses 5 V tolerant characteristic, in this case, the input level must be less than VDD + 0.3V.

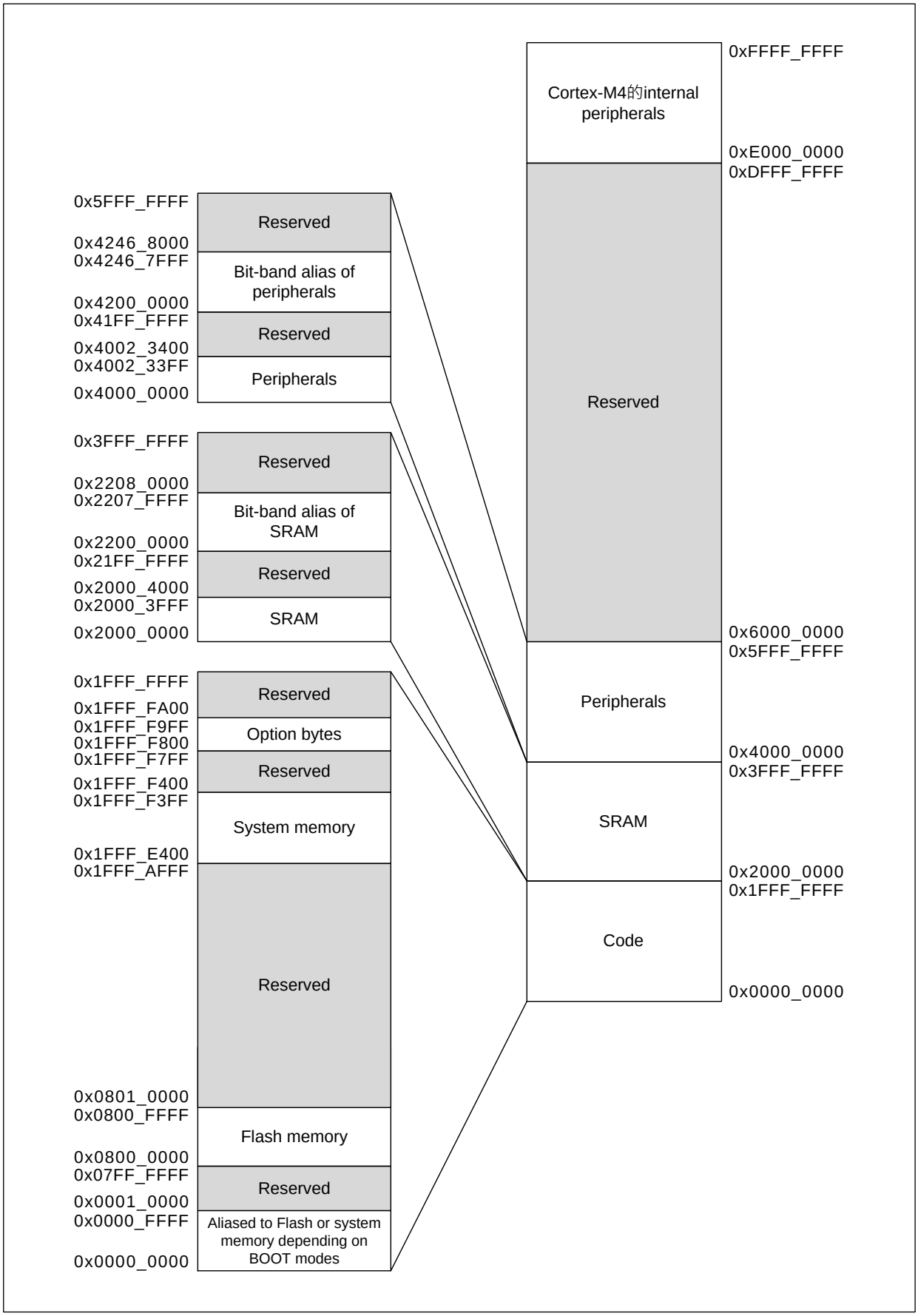
(3) On TSSOP20 package, PA11/PA12 and its alternate function can be remapped to replace the original PA9/PA10 and its alternate function by software.

(4) On QFN28 package, PA11 and PA12 should be treated as unconnected pins (even they are not available on the package.) They are not forced to a defined level by hardware. It is suggested to configure the state of these two pins as a defined level or analog mode to prevent unnecessary leakage current.

(5) After reset, PA13/PA14 pin is configured as alternate function SWDIO and SWCLK, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

5 Memory mapping

Figure 8. Memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production with an ambient temperature at T_A = 25 °C and T_A = T_A max.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V. They are given only as design guidelines and are not tested.

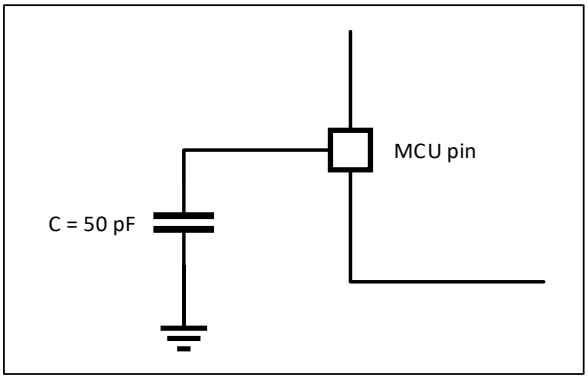
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

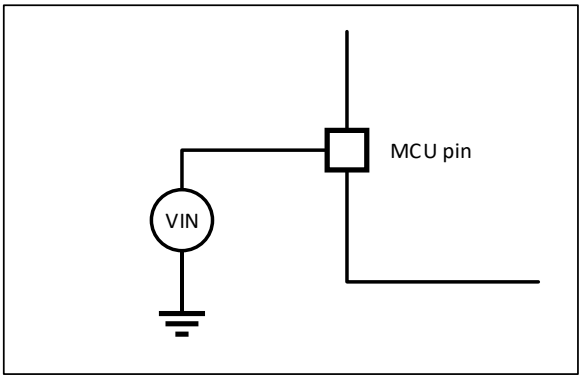
Figure 9. Pin loading conditions



6.1.5 Pin input voltage

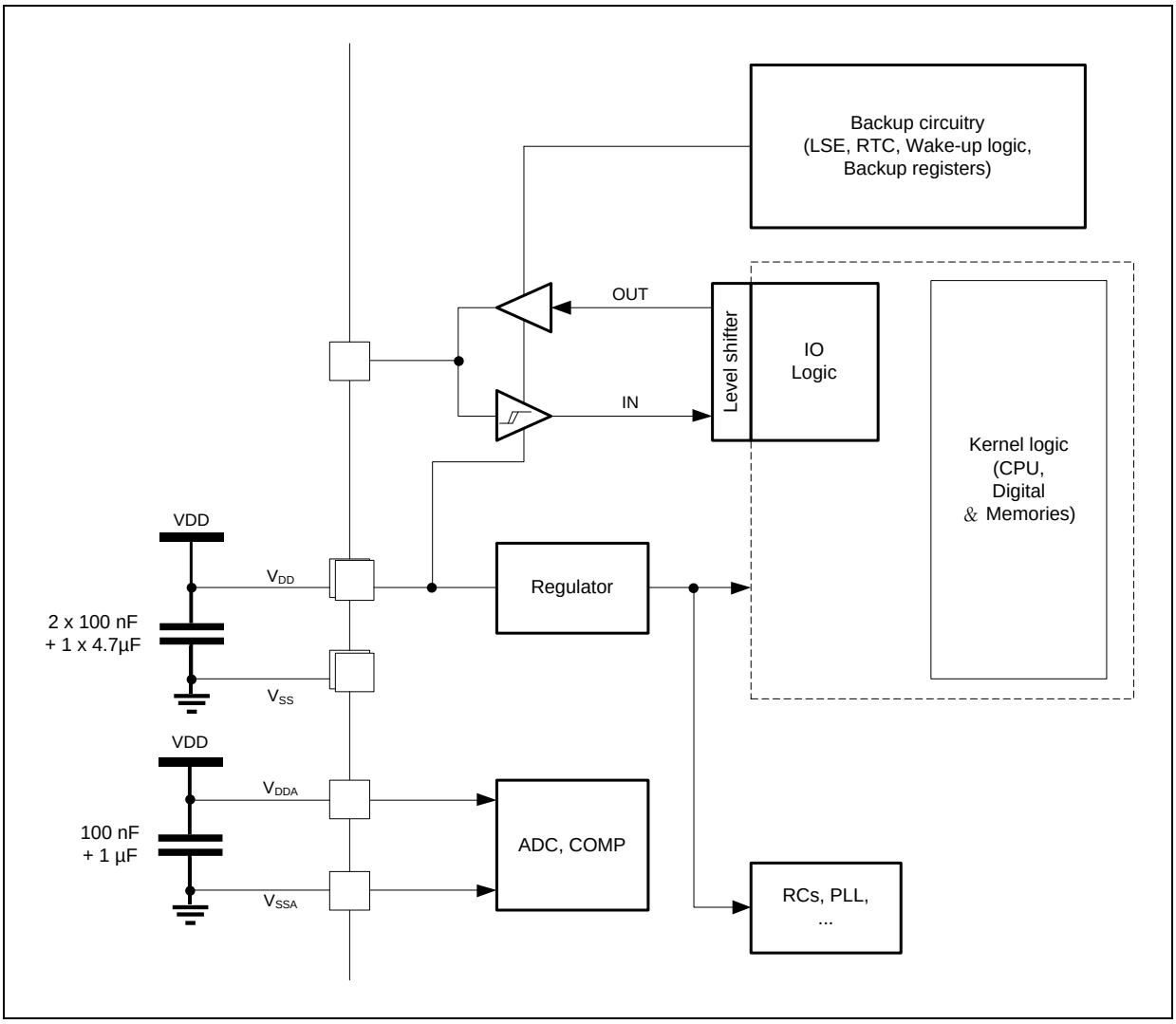
The input voltage measurement on a pin of the device is described in *Figure 10.*

Figure 10. Pin input voltage



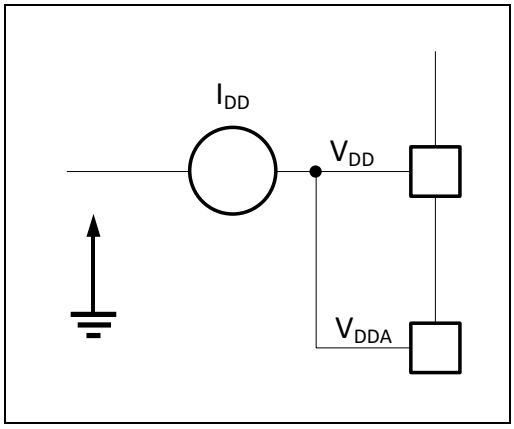
6.1.6 Power supply scheme

Figure 11. Power supply scheme



6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6*, *Table 7*, and *Table 8* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	6.0	
	Input voltage on FTa pins set as input floating, input pull-up ,or input pull-down mode			
	Input voltage on TC pins	V_{SS}-0.3	4.0	
	Input voltage on FTa pins set as analog mode			
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 7. Current characteristics

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

(1) All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	120	
f_{PCLK2}	Internal APB2 clock frequency	-	0	120	
V_{DD}	Standard operating voltage	-	2.4	3.6	V
V_{DDA}(1)	Analog operating voltage	Must be the same potential as V_{DD}(1)	2.4	3.6	V
P_D	Power dissipation: T_A = 105 °C	LQFP48 (7 x 7 mm)	-	230	mW
		LQFP32 (7 x 7 mm)	-	243	
		QFN32 (5 x 5 mm)	-	503	
		QFN32 (4 x 4 mm)	-	446	
		QFN28 (4 x 4 mm)	-	446	
		TSSOP20 (6.5 x 4.4 mm)	-	194	
T_A	Ambient temperature	-	-40	105	°C

(1) It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

6.3.2 Operating conditions at power-up / power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in *Table 9*.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	ms/V
	V_{DD} fall time rate		20	∞	μs/V

6.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9.*

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.62(1)	1.88	2.16(2)	V
		Rising edge	1.73(2)	2.06	2.4	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	180	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	-	4.5	-	ms

(1) The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
(2) Guaranteed by design, not tested in production.

Figure 13. Power on reset/power down reset waveform

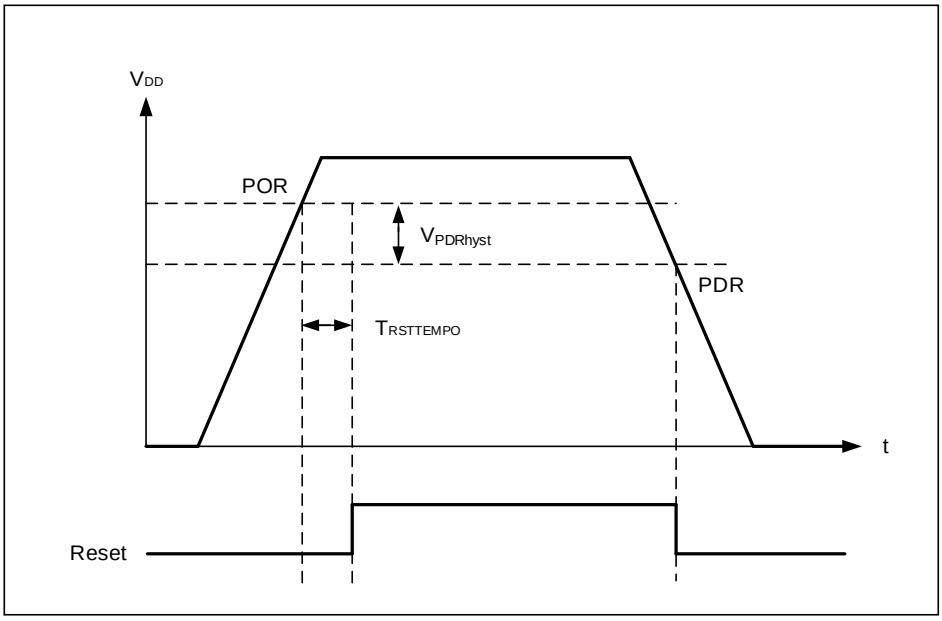


Table 12. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD1}	PVD threshold 1 (PLS[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2 (PLS[2:0] = 010)	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3 (PLS[2:0] = 011)	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4 (PLS[2:0] = 100)	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5 (PLS[2:0] = 101)	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6 (PLS[2:0] = 110)	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7 (PLS[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$I_{DD\ (PVD)}$	PVD current consumption	-	-	20	30(2)	µA

(1) PLS[2:0] = 001 level may not be used because it is lower than V_{PDR}. .
(2) Guaranteed by design, not tested in production

6.3.4 Embedded reference voltage

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 13. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.17	1.20	1.23	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
T_{Coeff}(2)	Temperature coefficient	-	-120	-	120	ppm/°C

(1) Shortest sampling time can be determined in the application by multiple iterations.
(2) Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, and executed binary code.

The current consumption is measured as described in *Table 12*.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins in analog mode
- The Flash memory access time adjusted to the f_{HCLK} frequency (0 wait state from 0 to 32 MHz, 1 wait state from 33 to 64 MHz, 2 wait states from 65 to 96 MHz, 3 wait states above 96 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/8$

Table 14. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(2)	120 MHz	16.7	11.3	mA
			108 MHz	15.2	10.3	
			72 MHz	10.5	7.19	
			48 MHz	7.62	5.44	
			36 MHz	5.98	4.34	
			24 MHz	4.65	3.54	
			16 MHz	3.45	2.71	
			8 MHz	1.96	1.57	
			4 MHz	1.50	1.30	
			2 MHz	1.27	1.16	
			1 MHz	1.16	1.10	
			500 kHz	1.10	1.07	
			125 kHz	1.06	1.04	
		Running on high speed internal RC (HSI)	120 MHz	16.7	11.3	mA
			108 MHz	15.1	10.3	
			72 MHz	10.4	7.14	
			48 MHz	7.52	5.38	
			36 MHz	5.88	4.27	
			24 MHz	4.53	3.47	
			16 MHz	3.34	2.63	
			8 MHz	1.83	1.48	
			4 MHz	1.37	1.20	
			2 MHz	1.15	1.06	
			1 MHz	1.03	0.99	
			500 kHz	0.97	0.95	
			125 kHz	0.93	0.93	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(2) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(2)	120 MHz	12.2	4.99	mA
			108 MHz	11.1	4.59	
			72 MHz	7.76	3.38	
			48 MHz	5.81	2.89	
			36 MHz	4.60	2.42	
			24 MHz	3.70	2.25	
			16 MHz	2.80	1.83	
			8 MHz	1.60	1.11	
			4 MHz	1.30	1.05	
			2 MHz	1.15	1.02	
			1 MHz	1.07	1.00	
			500 kHz	1.03	0.99	
			125 kHz	1.00	0.98	
		Running on high speed internal RC (HSI)	120 MHz	12.1	4.88	mA
			108 MHz	11.0	4.47	
			72 MHz	7.65	3.27	
			48 MHz	5.70	2.78	
			36 MHz	4.49	2.30	
			24 MHz	3.59	2.13	
			16 MHz	2.68	1.71	
			8 MHz	1.47	0.98	
			4 MHz	1.17	0.93	
			2 MHz	1.02	0.89	
			1 MHz	0.94	0.88	
			500 kHz	0.90	0.87	
			125 kHz	0.87	0.86	

(1) Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.
(2) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins in analog mode
- The Flash memory access time adjusted to the f_{HCLK} frequency (0 wait state from 0 to 32 MHz, 1 wait state from 33 to 64 MHz, 2 wait states from 65 to 96 MHz, 3 wait states above 96 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/8$

The parameters given in *Table 16* and *Table 17* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 16. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	120 MHz	18.9	20.7	mA
			108 MHz	17.3	19.1	
			72 MHz	12.6	14.4	
			48 MHz	9.69	11.5	
			36 MHz	8.04	9.81	
			24 MHz	6.69	8.45	
			16 MHz	5.49	7.24	
			8 MHz	3.99	5.73	
		External clock(2), all peripherals disabled	120 MHz	13.5	15.2	mA
			108 MHz	12.4	14.2	
			72 MHz	9.29	11.0	
			48 MHz	7.52	9.26	
			36 MHz	6.41	8.14	
			24 MHz	5.60	7.33	
			16 MHz	4.76	6.49	
			8 MHz	3.61	5.35	

(1) Guaranteed by characterization results, not tested in production.
(2) External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 17. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	120 MHz	14.4	16.1	mA
			108 MHz	13.3	15.0	
			72 MHz	9.85	11.6	
			48 MHz	7.89	9.58	
			36 MHz	6.69	8.36	
			24 MHz	5.79	7.45	
			16 MHz	4.88	6.53	
			8 MHz	3.68	5.31	
		External clock(2), all peripherals disabled	120 MHz	7.06	8.70	mA
			108 MHz	6.66	8.30	
			72 MHz	5.45	7.09	
			48 MHz	4.96	6.57	
			36 MHz	4.48	6.12	
			24 MHz	4.31	5.93	
			16 MHz	3.89	5.53	
			8 MHz	3.18	4.81	

(1) Guaranteed by characterization results, not tested in production.
(2) External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max(2)		Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode(3)	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	445	450	4100	6750	µA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	205	210	2000	3315	
	Supply current in Standby mode	Low-speed oscillator and ERTC OFF	2.4	3.6	5.9	7.6	
		Low-speed oscillator and ERTC ON	3.2	5.1	7.2	9.2	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.
(3) RCC_AHBEN[4] (FLASHEN) must be set to 1 before entering the stop mode, otherwise the typical value will generate an additional power consumption of about 50 µA.

Figure 14. Typical current consumption in Stop mode with regulator in run mode vs. temperature at different V_{DD}

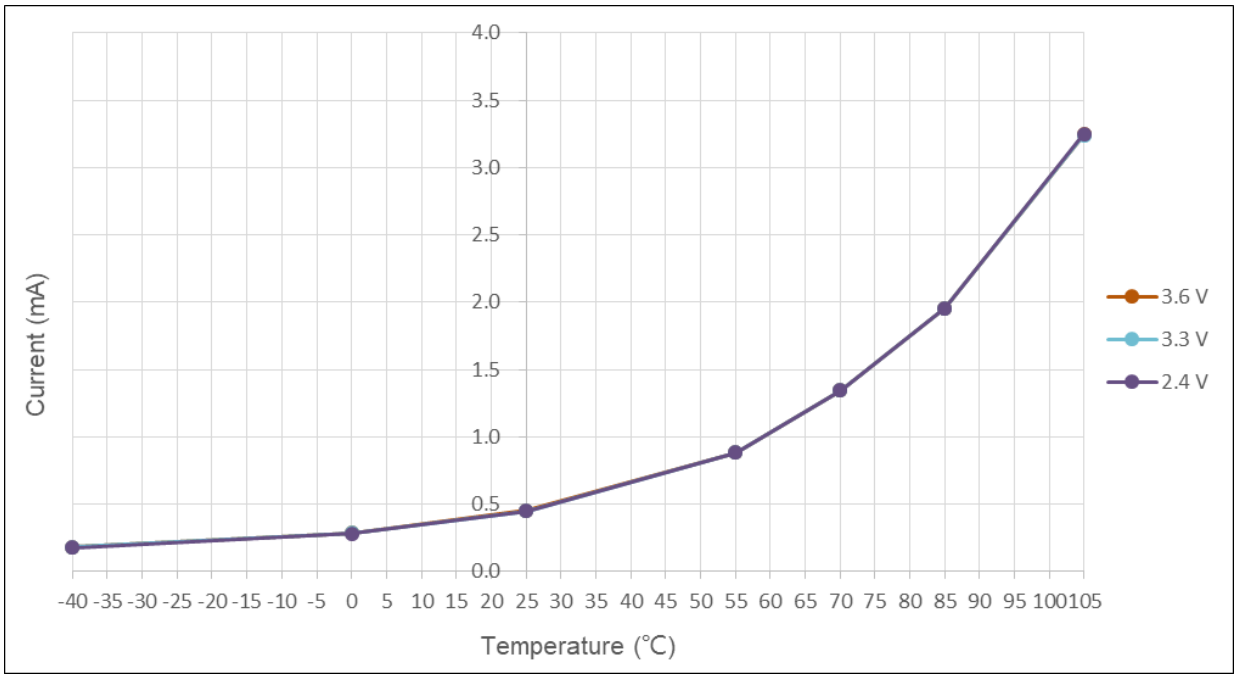


Figure 15. Typical current consumption in Stop mode with regulator with regulator in low-power mode vs. temperature at different V_{DD}

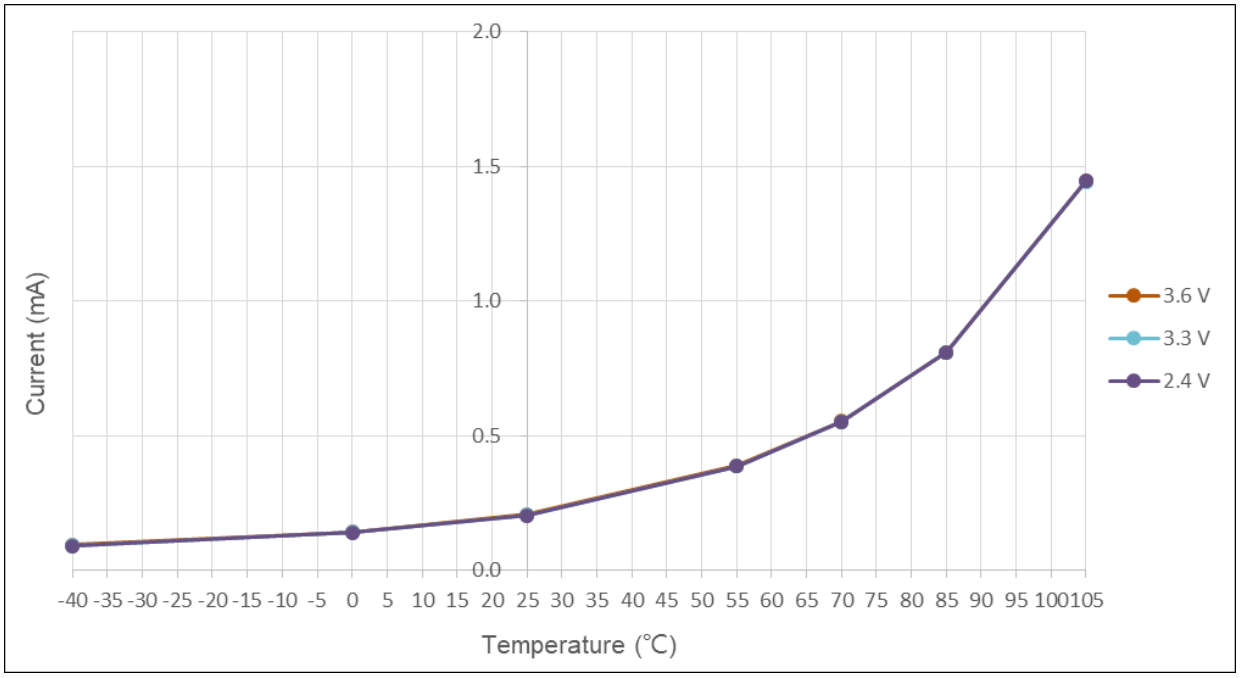
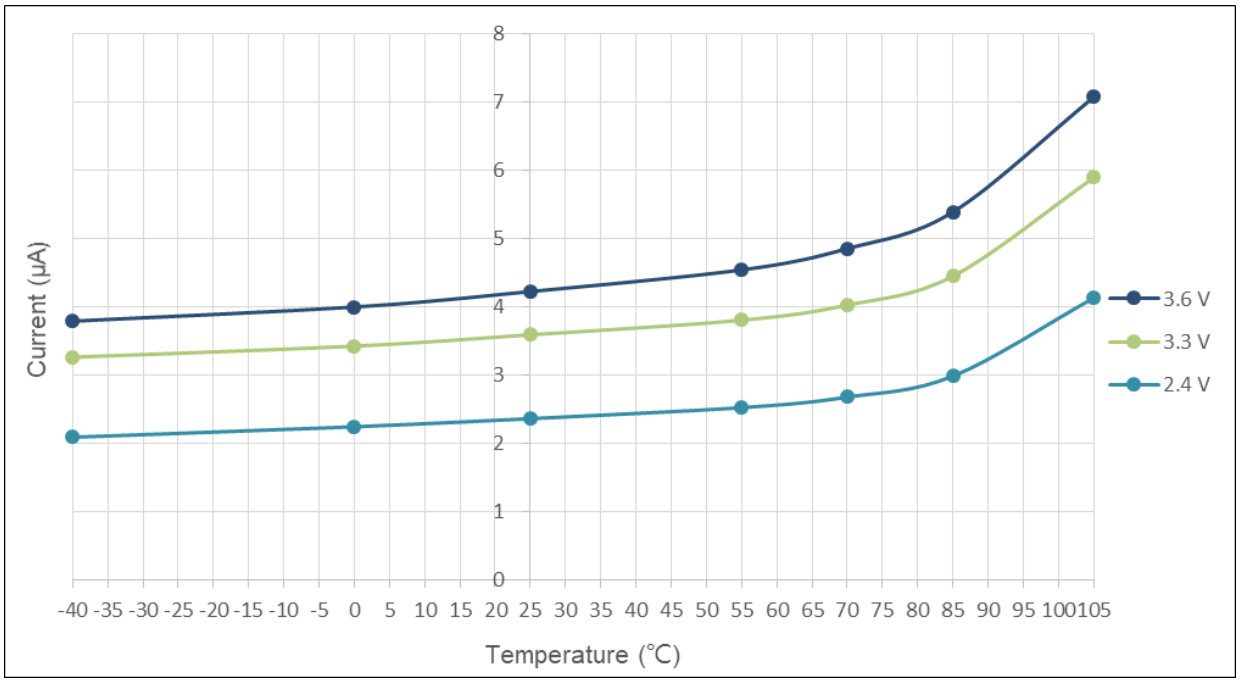


Figure 16. Typical current consumption in Standby mode vs. temperature at different V_{DD}



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- All I/O pins in analog mode
- All peripherals disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 19. Peripheral current consumption

Peripheral		Typ	Unit
AHB (up to120 MHz)	DMA1	2.15	μA/MHz
	SRAM	1.06	
	Flash	12.08	
	GPIOA	0.50	
	GPIOB	0.50	
	GPIOC	0.50	
	GPIOF	0.50	
	CRC	0.70	
APB1 (up to 120 MHz)	TMR3	6.29	
	TMR6	0.49	
	TMR14	2.28	
	SPI2/I^{2}S2	2.26	
	USART2	2.11	
	I^{2}C1	1.71	
	I^{2}C2	1.68	
	WWDG	0.20	
	PWR	0.39	
APB2 (up to 120 MHz)	SYSCFG/COMP	0.29	
	SPI1/I^{2}S1	2.03	
	USART1	2.12	
	TMR1	7.68	
	TMR15	4.65	
	TMR16	3.19	
	TMR17	3.41	
	ADC1	5.17	
	ACC	0.95	

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode, the HSE oscillator is disabled, and the input pin is a standard GPIO.

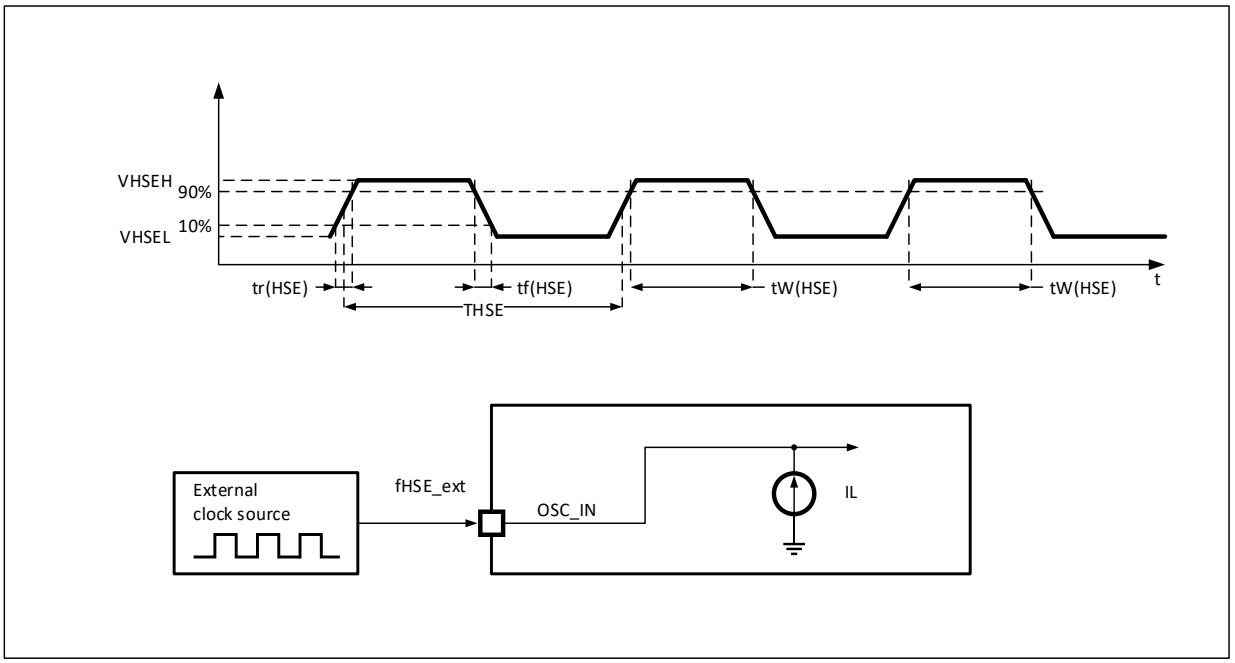
The external clock signal must take into account of the I/O characteristics in Section *6.3.13*. However, the recommended clock input waveform is presented in *Figure 17*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 17. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode, the LSE oscillator is disabled, and the input pin is a standard GPIO.

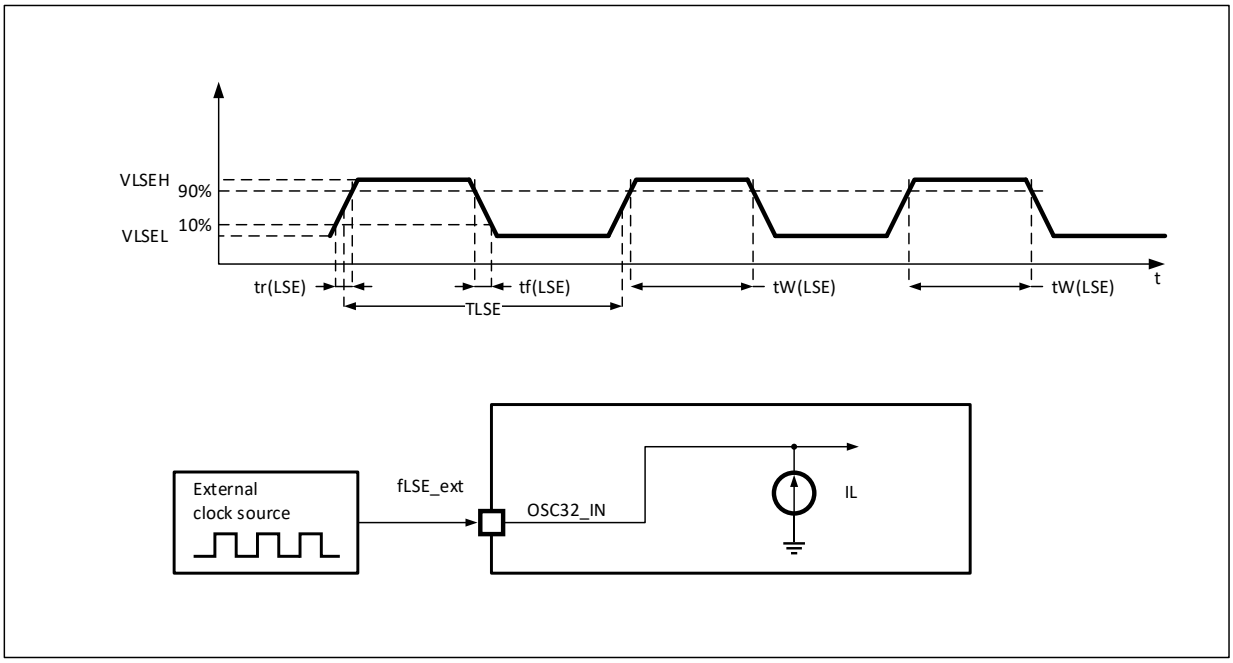
The external clock signal must take into account of the I/O characteristics in chapter *6.3.13*. However, the recommended clock input waveform is presented in *Figure 18*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)	-	-	-	50	ns
DuCy(LSE)	Duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

(1) Guaranteed by design, not tested in production.

Figure 18. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

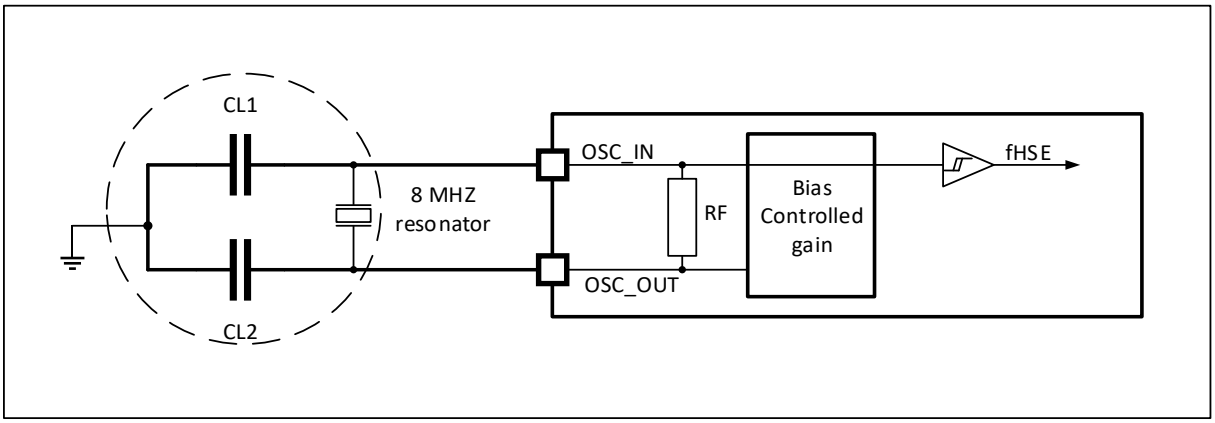
Table 22. HSE 4 to 25 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

(1) Resonator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 19. Typical application with an 8 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

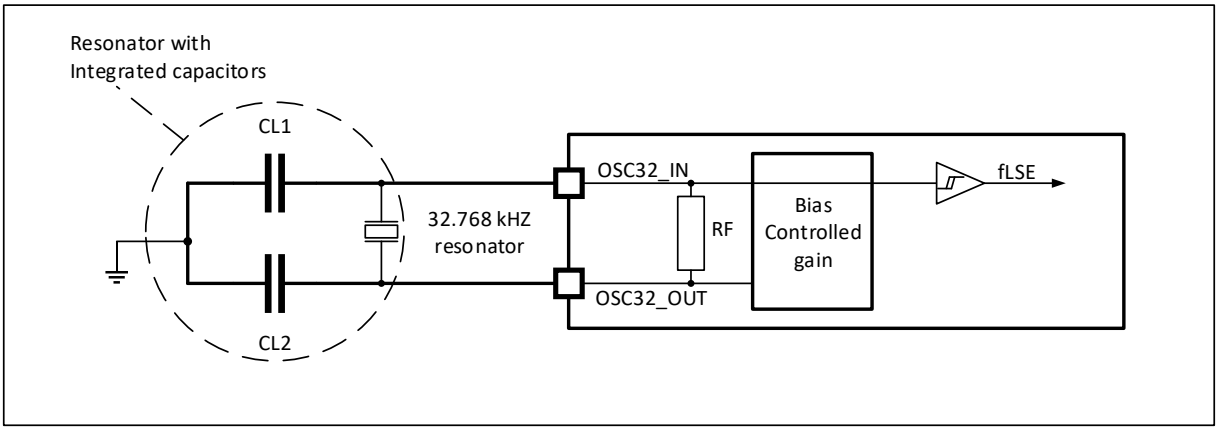
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LSE)}$	Startup time	V_{DD} is stabilized	-	180	-	ms

(1) Resonator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 20. Typical application with a 32.768 kHz crystal



Note: No external resistor is required between OSC32_IN and OSC32_OUT and it is also prohibited to add it.

6.3.7 Internal clock source characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

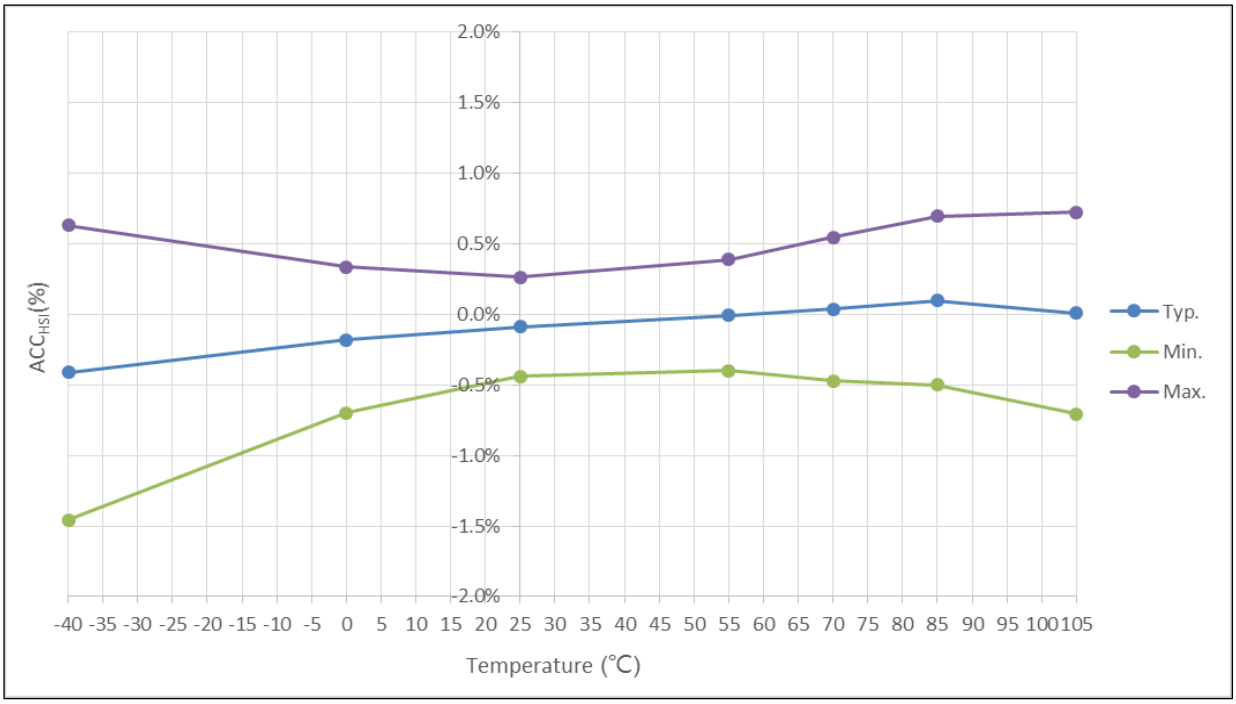
High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	48	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CTRL register		-1	-	1(2)	%
		Factory-calibrated(3)	T_A = -40 ~ 105 °C	-2	-	1.5	%
			T_A = -40 ~ 85 °C	-2	-	1.2	%
			T_A = 0 ~ 70 °C	-1.5	-	1.2	%
			T_A = 25 °C	-1	-	1	%
$t_{SU(HSI)}$(3)	HSI oscillator startup time	-		-	10	12	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-		-	220	290	µA

(1) V_{DD} = 3.3 V, T_A = -40~105 °C, unless otherwise specified.
(2) Guaranteed by design, not tested in production.
(3) Guaranteed by characterization results, not tested in production.

Figure 21. HSI oscillator frequency accuracy vs. temperature



Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	-	25	35	45	kHz

(1) V_{DD} = 3.3 V, T_A = -40 to 105 °C, unless otherwise specified.
(2) Guaranteed by characterization results, not tested in production.

6.3.8 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the HSI RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	3.3	μs
t_{WUSTOP}	Wakeup from Stop mode (regulator in run mode)	380	μs
	Wakeup from Stop mode (regulator in low-power mode)	450	
$t_{WUSTDBY}$	Wakeup from Standby mode	1250	μs

6.3.9 PLL characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock (2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	120	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by characterization results, not tested in production.
(2) Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.10 Memory characteristics

The characteristics in *Table 28* are given at T_A = -40 ~ 105 °C, unless otherwise specified.

Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
T_{PROG}	Programming time	T_A = -40 ~ 105 °C	-	40	60	µs
t_{ERASE}	Page erase time	T_A = -40 ~ 105 °C	-	6.4	8	ms
t_{ME}	Mass erase time	T_A = -40 ~ 105 °C	-	8	10	ms
I_{DD}	Supply current	Programming mode, V_{DD} = 3.3 V，f_{HCLK} = 8 MHz, T_A = 25 °C	-	1.95	-	mA
		Erase mode, V_{DD} = 3.3 V，f_{HCLK} = 8 MHz,T_A = 25 °C	-	1.62	-	

(1) Guaranteed by characterization results, not tested in production.

Table 29. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through one 47 µF and two 100 pF capacitors, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 30. EMS characteristics

Symb	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforms to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional disturbance, V_{DD} and V_{SS} input has one 47 µF capacitor and each V_{DD} and V_{SS} pin pair 0.1 µF	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 120 MHz, conforms to IEC 61000-4-4	3/A (2 kV)
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

6.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JS-001-2017 and JS-002-2014 standard.

Table 31. ESD absolute maximum ratings

Symbol	Parameter	Conditions	Class	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JS-001-2017	3A	6000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JS-002-2014	III	1000	

(1) Guaranteed by characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on 6 parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78E IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (200 mA)

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 33. I/O static characteristics

Symb	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	-	-0.3	-	0.28 * V_{DD} + 0.1	V
V_{IH}	TC I/O input high level voltage	-	0.31 * V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FTa I/O input high level voltage	Analog mode				
	FT I/O input high level voltage	-		-	5.5	
	FTa I/O input high level voltage	Input floating, input pull-up, or input pull-down				
V_{hys}	TC I/O Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
	FT and FTa I/O Schmitt trigger voltage hysteresis(1)		5% V_{DD}	-	-	-
I_{lkg}	Input leakage current(2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC I/O pin	-	-	±1	μA
		$V_{SS} \le V_{IN} \le 5.5V$ FT and FTa I/O pin	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	65	80	130	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	$V_{IN} = V_{DD}$	65	70	130	kΩ
C_{IO}	I/O pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
(2) Leakage could be higher than max if negative current is injected on adjacent pins.
(3) The pull-down resistor of BOOT0 exists permanently.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section *6.2*.

- The sum of the currents sourced by all I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all I/Os on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OL}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 4 mA	-	0.4	
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 5 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 8 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Maximum sourcing/sinking strength					
V_{OL}(1)	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}(1)	Output low level voltage	TTL standard, I_{IO} = 12 mA	-	0.4	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 36 mA	-	1.3	V
V_{OH}(1)	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}(1)	Output low level voltage	I_{IO} = 18 mA	-	0.4	
V_{OH}(1)	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	

(1) Guaranteed by characterization results.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Unless otherwise specified, the parameters given below are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 35. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	10	-	ns

6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

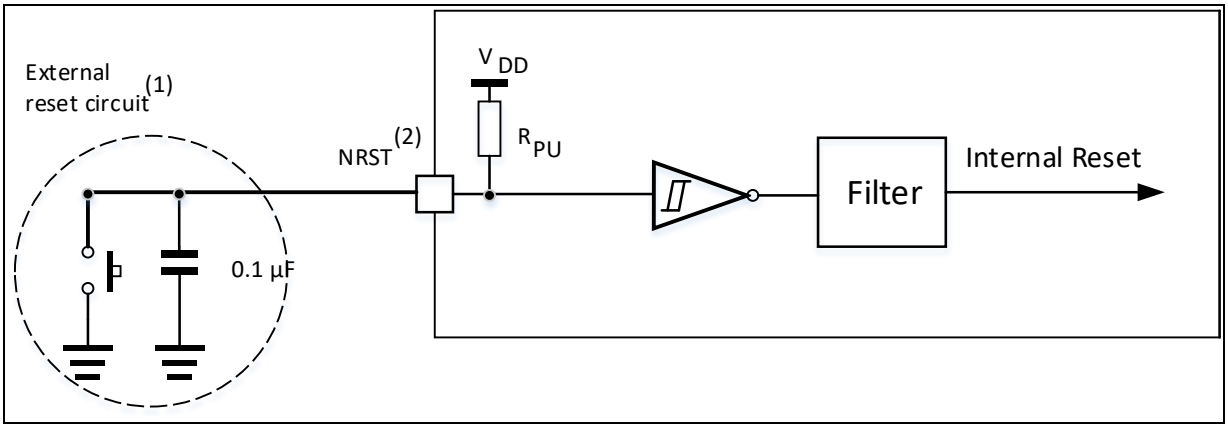
Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.3	-	0.72	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	400	-	mV
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	40	μs
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	80	-	-	μs

(1) Guaranteed by design.

Figure 22. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the V_{IL} (NRST) max level specified in *Table 36*. Otherwise the reset will not be taken into account by the device.

6.3.15 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to *6.3.13 I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 37. TMRx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 120 MHz	8.3	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz
		$f_{TMRxCLK}$ = 120 MHz	0	60	MHz

(1) TMRx is used as a general term to refer to the TMR1, TMR3, TRM6, and TMR14~17.

6.3.16 Communications interfaces

I²C interface characteristics

The SDA and SCL I/O requirements are met with the following restrictions: the I/O pins SDA and SCL mapped to are not ”true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Refer also to *6.3.13 I/O port characteristics* for more details on the input/output alternate function characteristics.

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more complete information, please contact your nearest Artery sales office for technical support.

SPI-I²S characteristics

Unless otherwise specified, the parameters given in *Table 38* for SPI or in *Table 39* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *6.3.13 I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 38. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$(1)	SPI clock frequency	Master mode	V_{DD} = 3.3 V, T_A = 25 °C	-	50	MHz
			V_{DD} = 3.3 V, T_A = 105 °C	-	40	
			V_{DD} = 2.4 V, T_A = 105 °C	-	36	
		Slave mode		-	$f_{PCLK}/2$	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF		-	6	ns
$t_{su(NSS)}$(1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$ + 10	-	ns
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 120 MHz, prescaler = 4		$t_{PCLK}/2$ - 2	$t_{PCLK}/2$ + 1	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode		4	-	ns
$t_{su(SI)}$(1)		Slave mode		5	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode		4	-	ns
$t_{h(SI)}$(1)		Slave mode		5	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode		0	18	ns
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)		-	22.5	ns
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)		-	6	ns
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)		11.5	-	ns
$t_{h(MO)}$(1)		Master mode (after enable edge)		2	-	

(1) Guaranteed by characterization results, not tested in production.
(2) The maximum clock frequency is highly dependent on the device and PCB layout. For more information, please contact your nearest Artery sales office for technical support.
(3) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(4) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 23. SPI timing diagram - slave mode and CPHA = 0

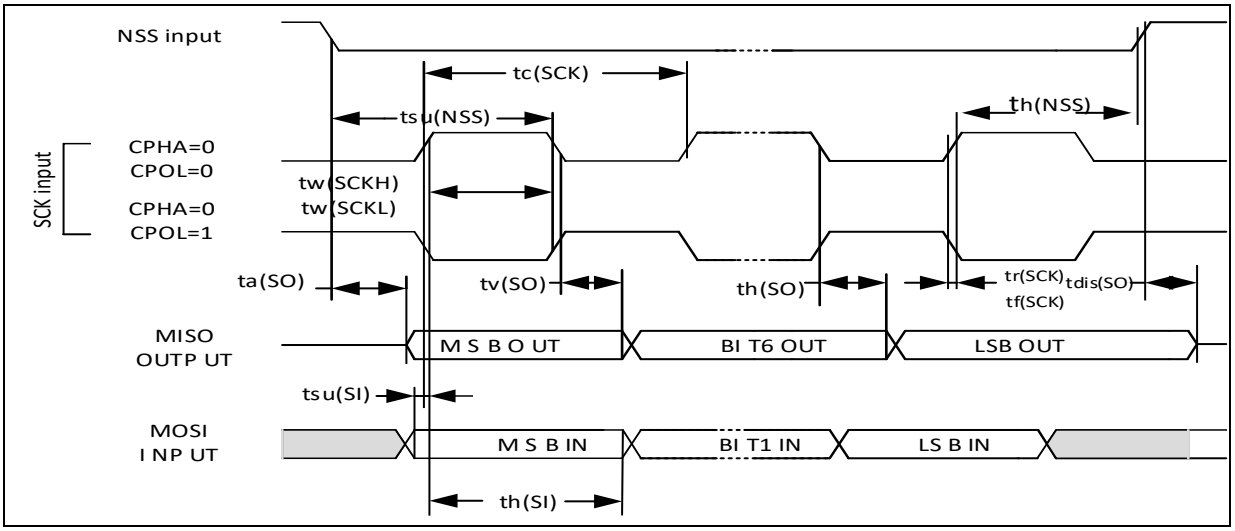
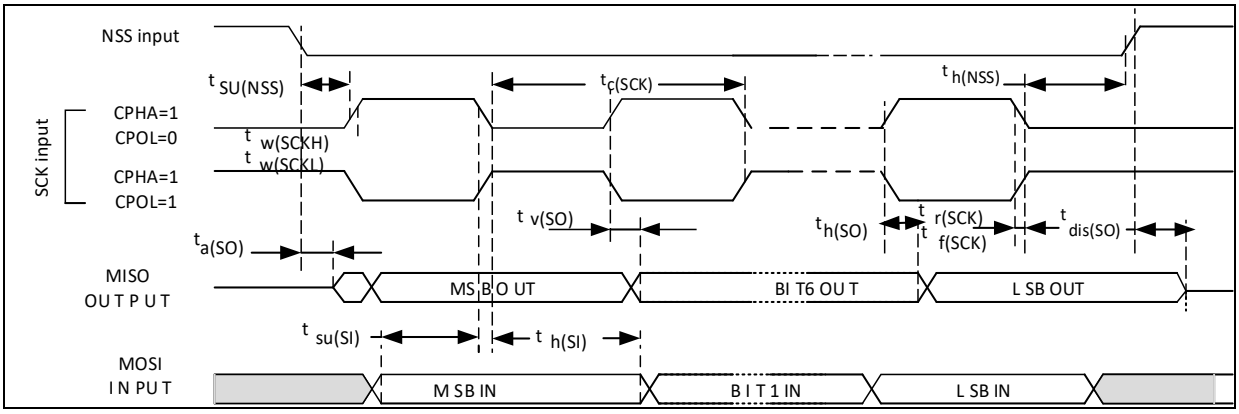
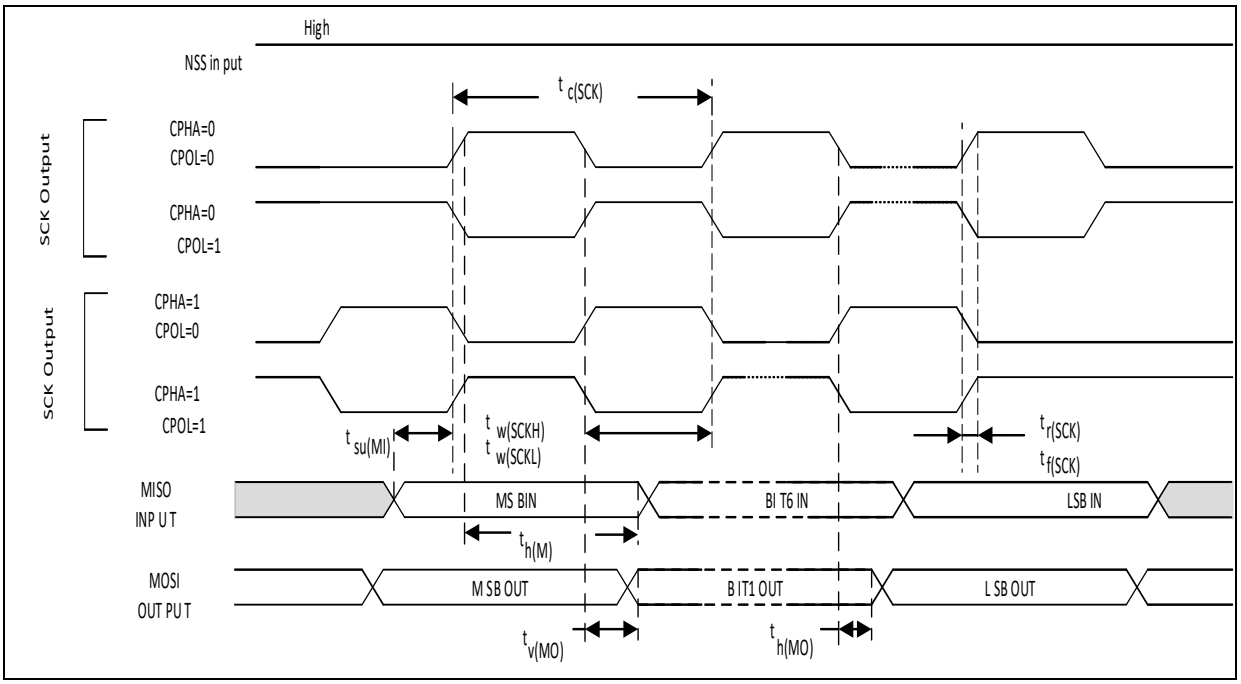


Figure 24. SPI timing diagram - slave mode and CPHA = 1(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 25. SPI timing diagram - master mode(1)



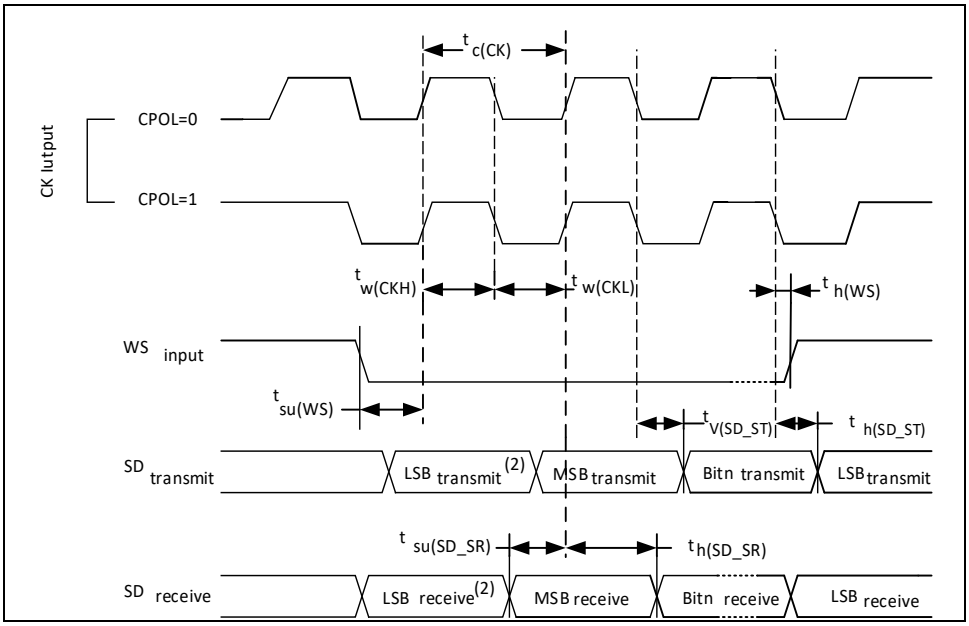
(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 39. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I²S clock frequency	Master mode (data: 16 bits, audio frequency = 48 kHz)	1.522	1.525	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	2	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	2	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	7	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{w(CKH)}$(1)	CK high and low time	Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$(1)			312	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	13	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	4	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

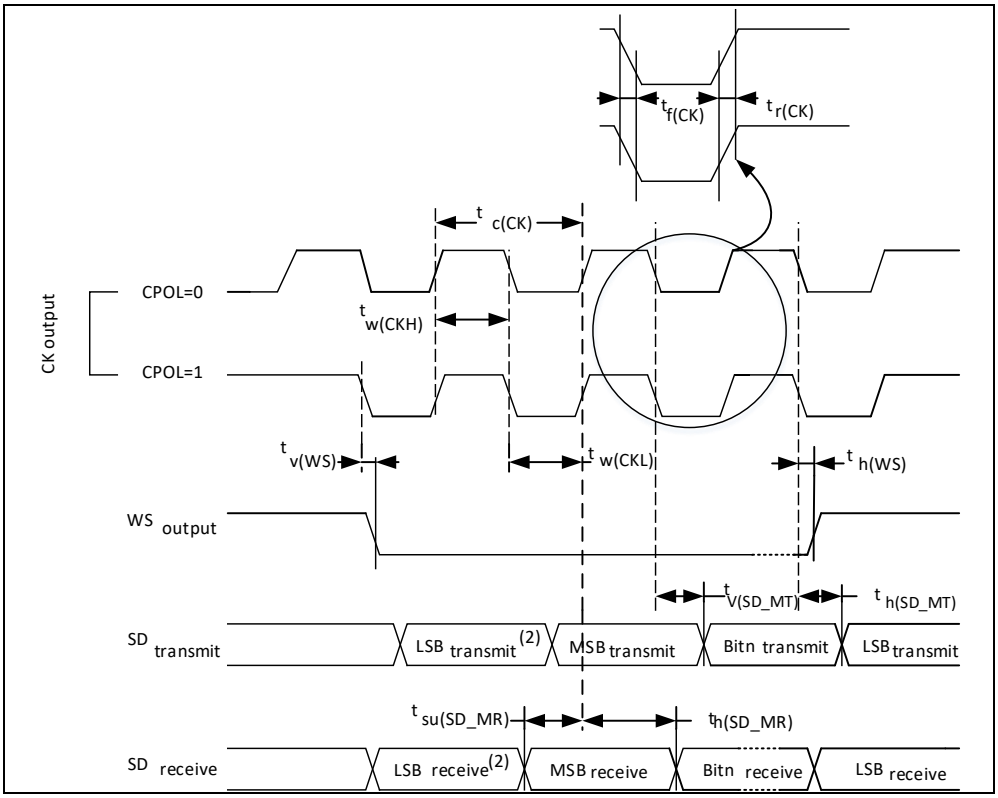
(1) Guaranteed by design and/or characterization results.
(2) Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.

Figure 26. I²S slave timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.
(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 27. I²S master timing diagram (Philips protocol)(1)



(1) Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
(2) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Table 40. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-	-	480(1)	560	μA
f_{ADC}	ADC clock frequency	-	0.6	-	28	MHz
f_S(2)	Sampling rate	-	0.05	-	2	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{REF-} internal tied to ground))	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	See *Table 41* and *Table 42* for details			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-	-	8.5	13-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz	6.61			μs
		-	185			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 28 MHz	-	-	107	ns
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 28 MHz	-	-	71.4	μs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	42			$1/f_{ADC}$
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz	0.5	-	9	μs
		-	14 to 252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} is internally connected to V_{DDA} and V_{REF-} to V_{SSA}.
(4) For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 40*.

Table 41 and *Table 42* are used to determine the maximum external impedance allowed for an error below 1 LSB.

Table 41. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.25
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

(1) Guaranteed by design.

Table 42. R_{AIN} max for f_{ADC} = 28 MHz(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

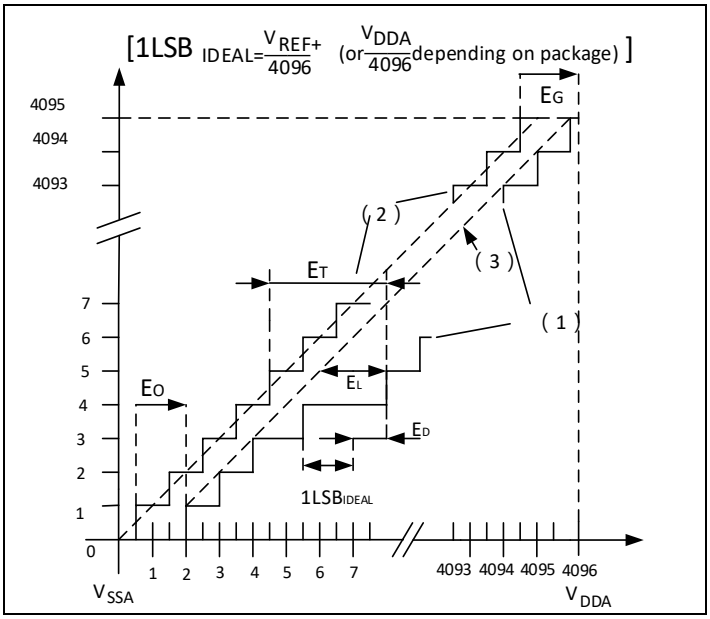
(1) Guaranteed by design.

Table 43. ADC accuracy(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0 to 3.6 V, T_A = 25 °C	+2	+3.5	LSB
EO	Offset error		+1	+2.5	
EG	Gain error		+1.5	+3	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4~3.6 V	±2	+4	
EO	Offset error		+1	+3	
EG	Gain error		+1.5	+3.5	
ED	Differential linearity error		±0.6	+1.5/-1	
EL	Integral linearity error		±1	±2.5	

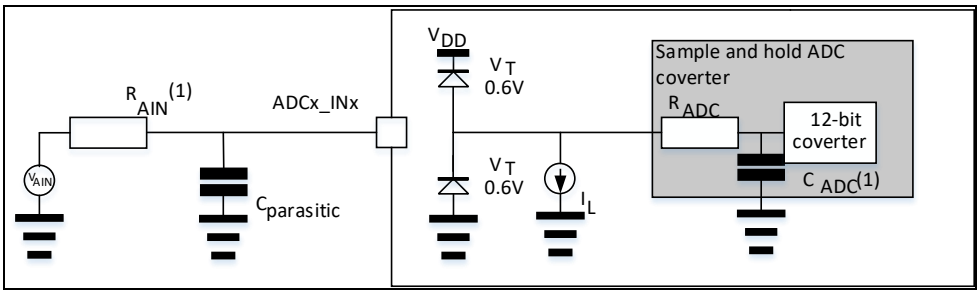
(1) ADC DC accuracy values are measured after internal calibration.
(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
(3) Guaranteed by characterization results, not tested in production.

Figure 28. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
EO = Offset Error: deviation between the first actual transition and the first ideal one.
EG =Gain Error: deviation between the last ideal transition and the last actual one.
ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 29. Typical connection diagram using the ADC



(1) Refer to *Table 40* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 11*. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

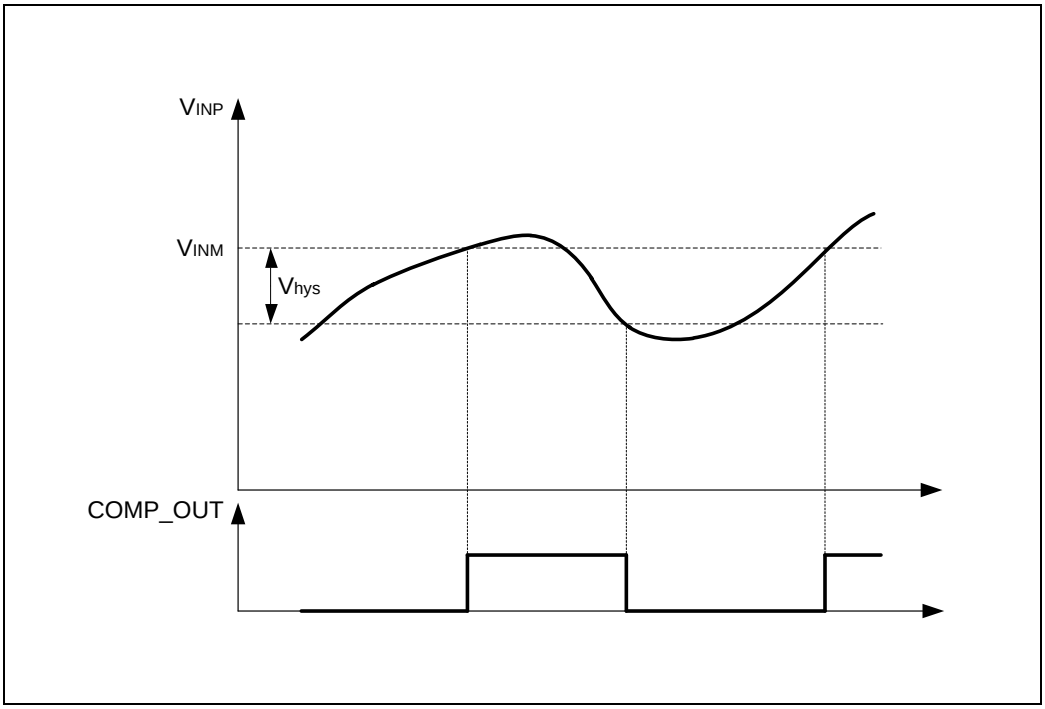
6.3.18 Comparator characteristics

Table 44. Comparator characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
t_{START}	Startup time	High speed mode	-	1.0	3.5	µs
		Medium speed mode	-	2.8	5	
		Low power mode	-	8	13	
		Ultra low power mode	-	12	18	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	High speed mode	-	40	100	ns
		Medium speed mode	-	240	320	
		Low power mode	-	500	820	
		Ultra low power mode	-	800	1800	
V_{offset}	Offset voltage	-	-	±4	±15	mV
V_{hys}	Hysteresis	No hysteresis	-	0	1	mV
		Low hysteresis	5	8	17	
		Medium hysteresis	10	18	37	
		High hysteresis	18	38	70	
I_{DDA}	Current consumption	High speed mode	-	40	61	µA
		Medium speed mode	-	9.7	13.9	
		Low power mode	-	3.2	4.7	
		Ultra low power mode	-	1.9	2.8	

(1) Guaranteed by characterization results, not tested in production.

Figure 30. Comparator hysteresis



6.3.19 Temperature sensor characteristics

Table 45. Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	T_A = -20 ~ 85 °C	-	±1	±1.5	ºC
		T_A = -40 ~ 105 °C	-	-	±2	
Avg_Slope(1)(2)	Average slope		-4.17	-4.30	-4.44	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC		1.22	1.28	1.34	V
t_{START}(3)	Startup time		-	-	100	µs
T_{S_temp}(3)(4)	ADC sampling time when reading the temperature		-	8.6	17.1	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.
(4) Shortest sampling time can be determined in the application by multiple iterations.

Obtain the temperature using the following formula:

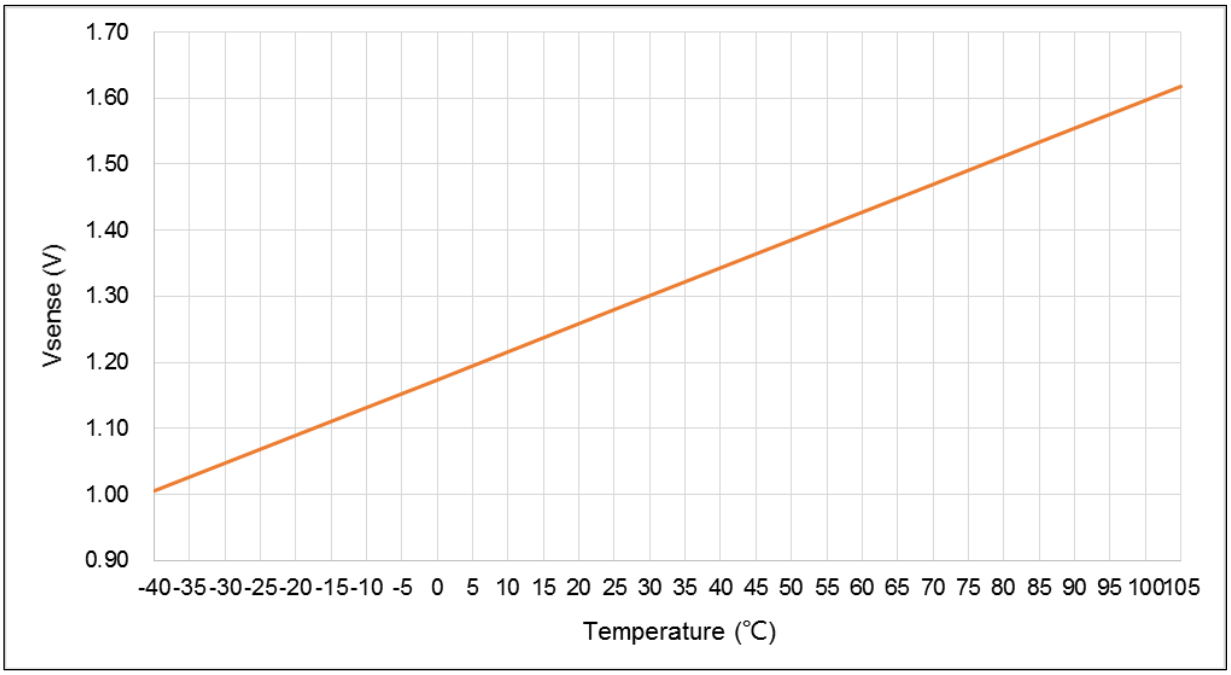
Temperature (in °C) = {(V_{25} - V_{SENSE}) / Avg_Slope} + 25.

Where,

V_{25} = V_{SENSE} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{SENSE} (given in mV/° C).

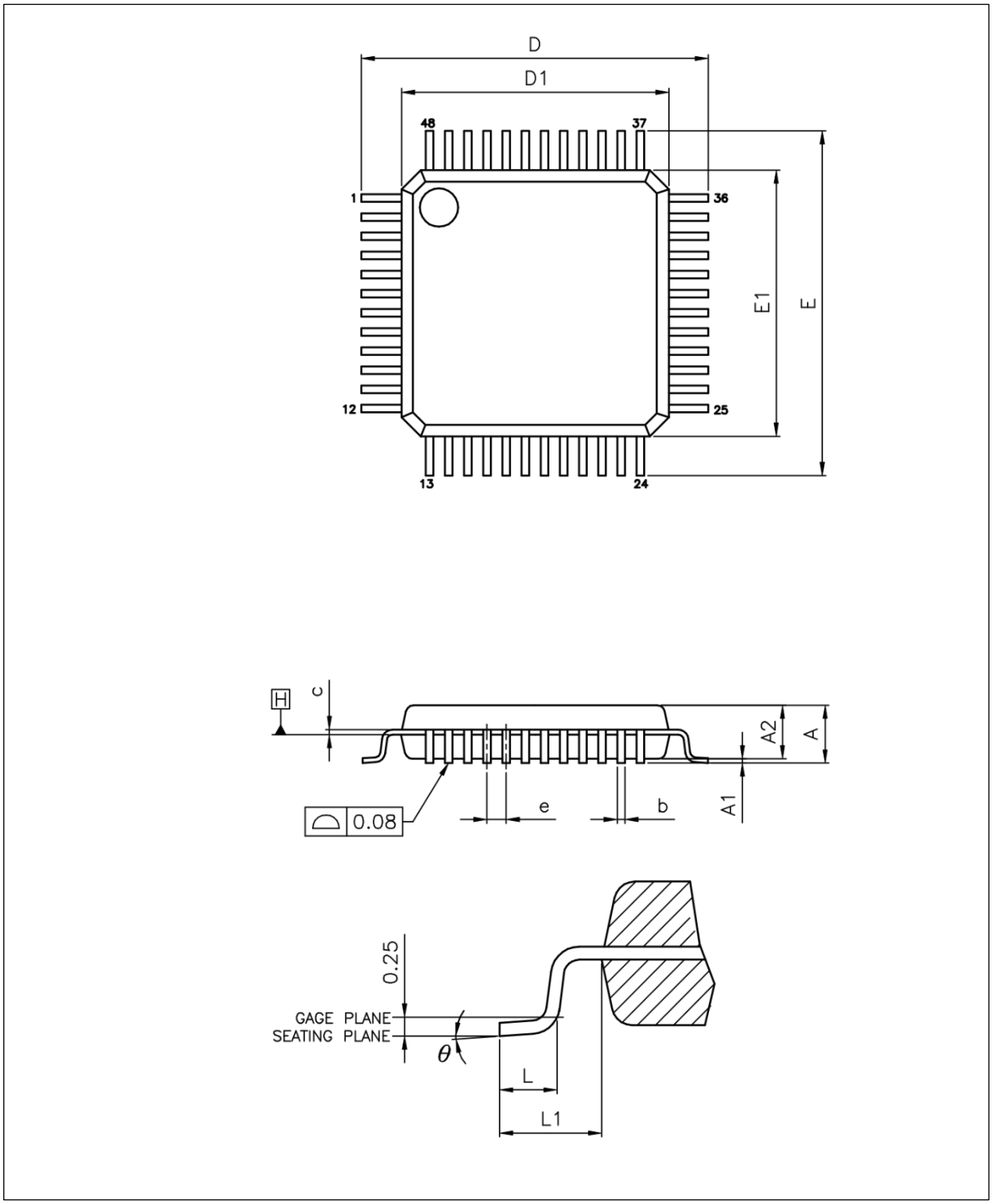
Figure 31. V_{SENSE} vs. temperature



7 Package information

7.1 LQFP48 – 7 x 7 mm package information

Figure 32. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 46. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

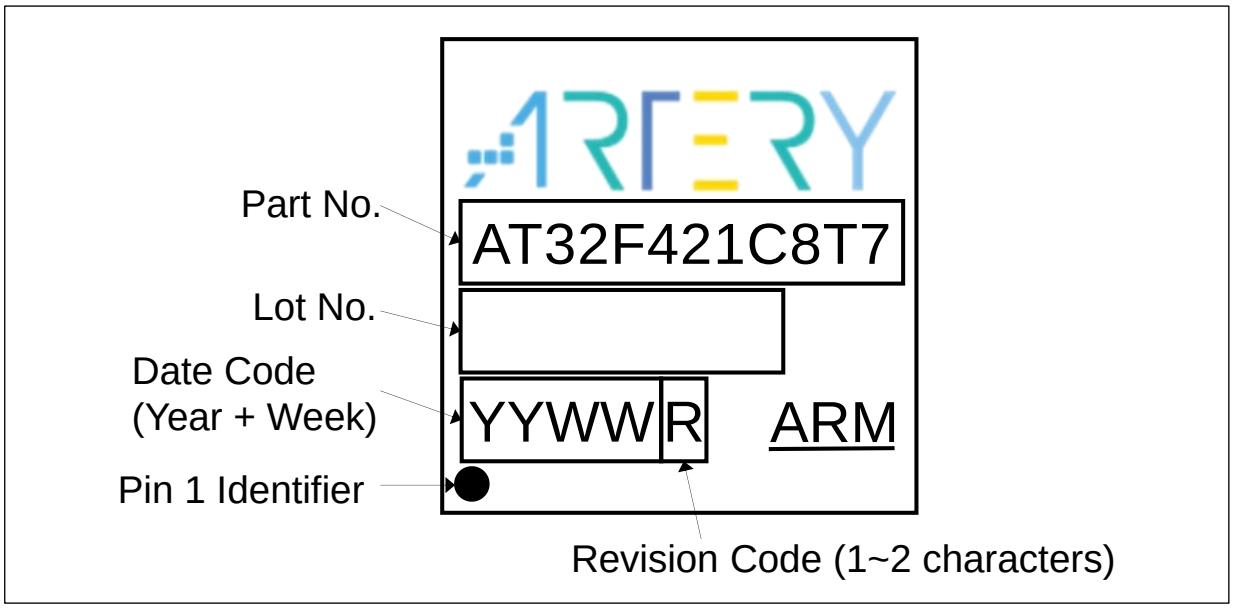
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	-	0.20	0.004	-	0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.50 BSC.			0.020 BSC.		
Θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP48 – 7 x 7 mm

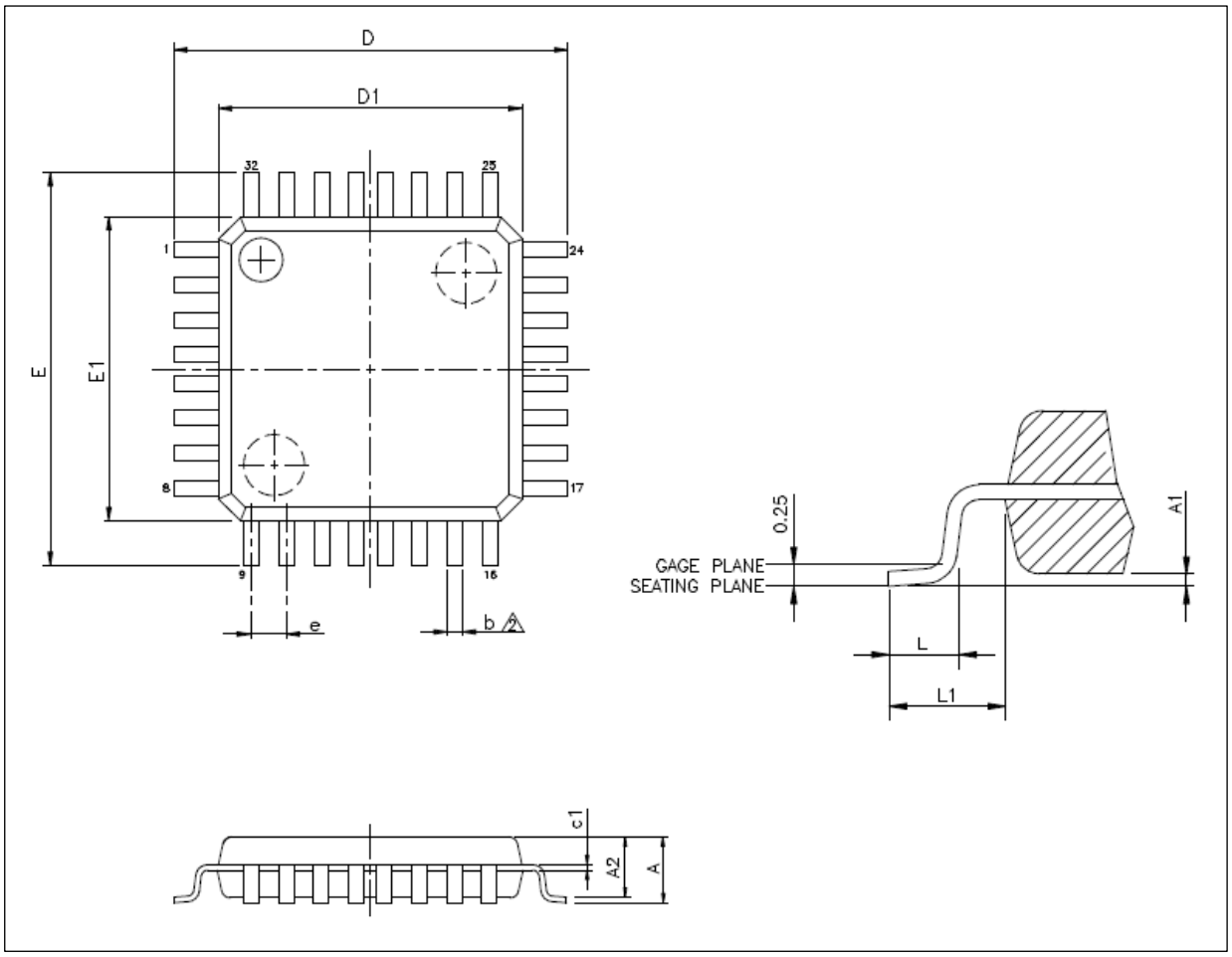
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 33. LQFP48 – 7 x 7 mm marking example (package top view)



7.2 LQFP32 – 7 x 7 mm package information

Figure 34. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package outline



(1) Drawing is not in scale.

Table 47. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package mechanical data

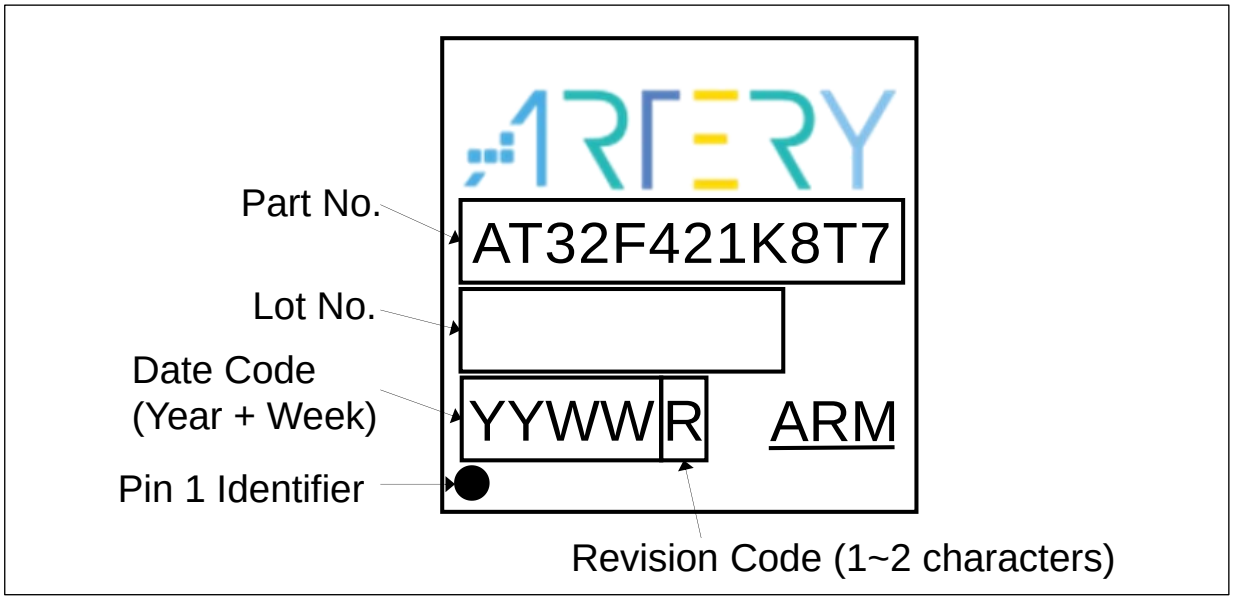
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	-	1.45	0.053	-	0.057
b	0.30	-	0.45	0.012	-	0.018
c	0.09	-	0.16	0.004	-	0.006
D	9.00 BSC.			0.345 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.345 BSC.		
E1	7.00 BSC.			0.276 BSC.		
e	0.80 BSC.			0.031 BSC.		
L	0.45	-	0.75	0.018	-	0.030
L1	1.00 REF.			0.039 REF.		

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for LQFP32 – 7 x 7 mm

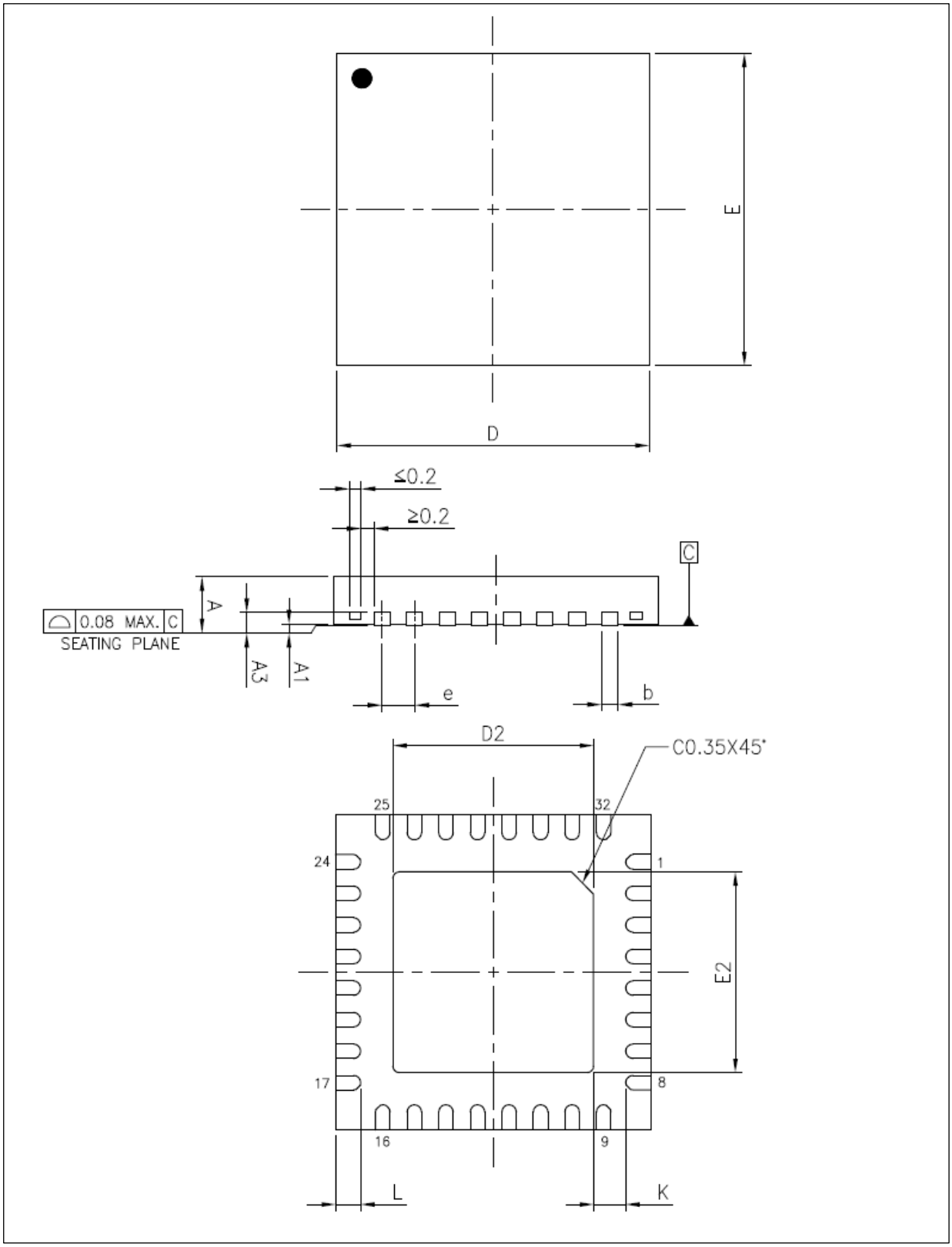
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 35. LQFP32 – 7 x 7 mm marking example (package top view)



7.3 QFN32 – 5 x 5 mm package information

Figure 36. QFN32 – 5 x 5 mm 32 pin fine-pitch quad flat package outline



(1) Drawing is not in scale.

Table 48. QFN32 – 5 x 5 mm 32 pin fine-pitch quad flat package mechanical data

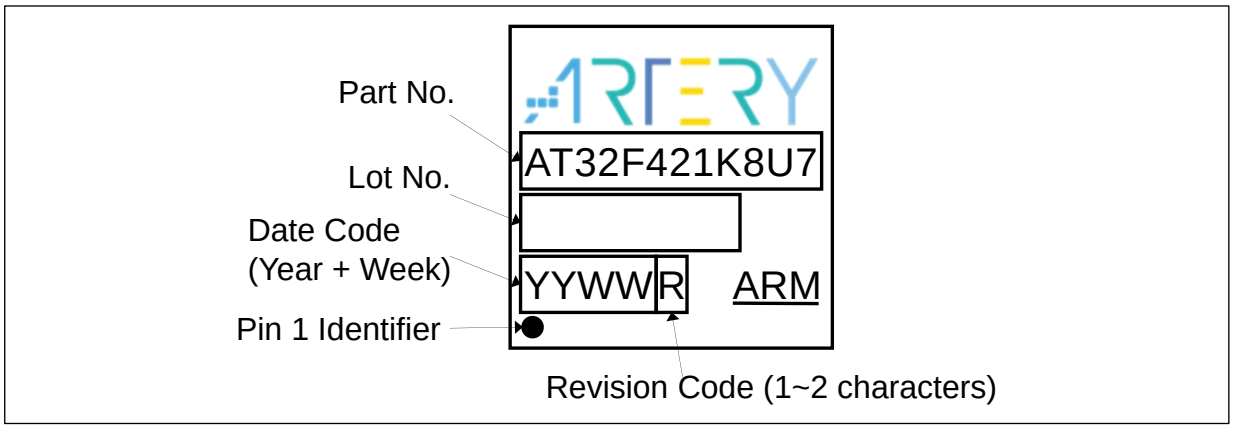
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.203 REF.			0.008 REF.	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		5.00 BSC.			0.197 BSC.	
D2	3.20	3.25	3.30	0.126	0.128	0.130
E		5.00 BSC.			0.197 BSC.	
E2	3.20	3.25	3.30	0.126	0.128	0.130
e		0.50 BSC.			0.020 BSC.	
K	0.20	-	-	0.008	-	-
L	0.35	0.40	0.45	0.014	0.016	0.018

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for QFN32 – 5 x 5 mm

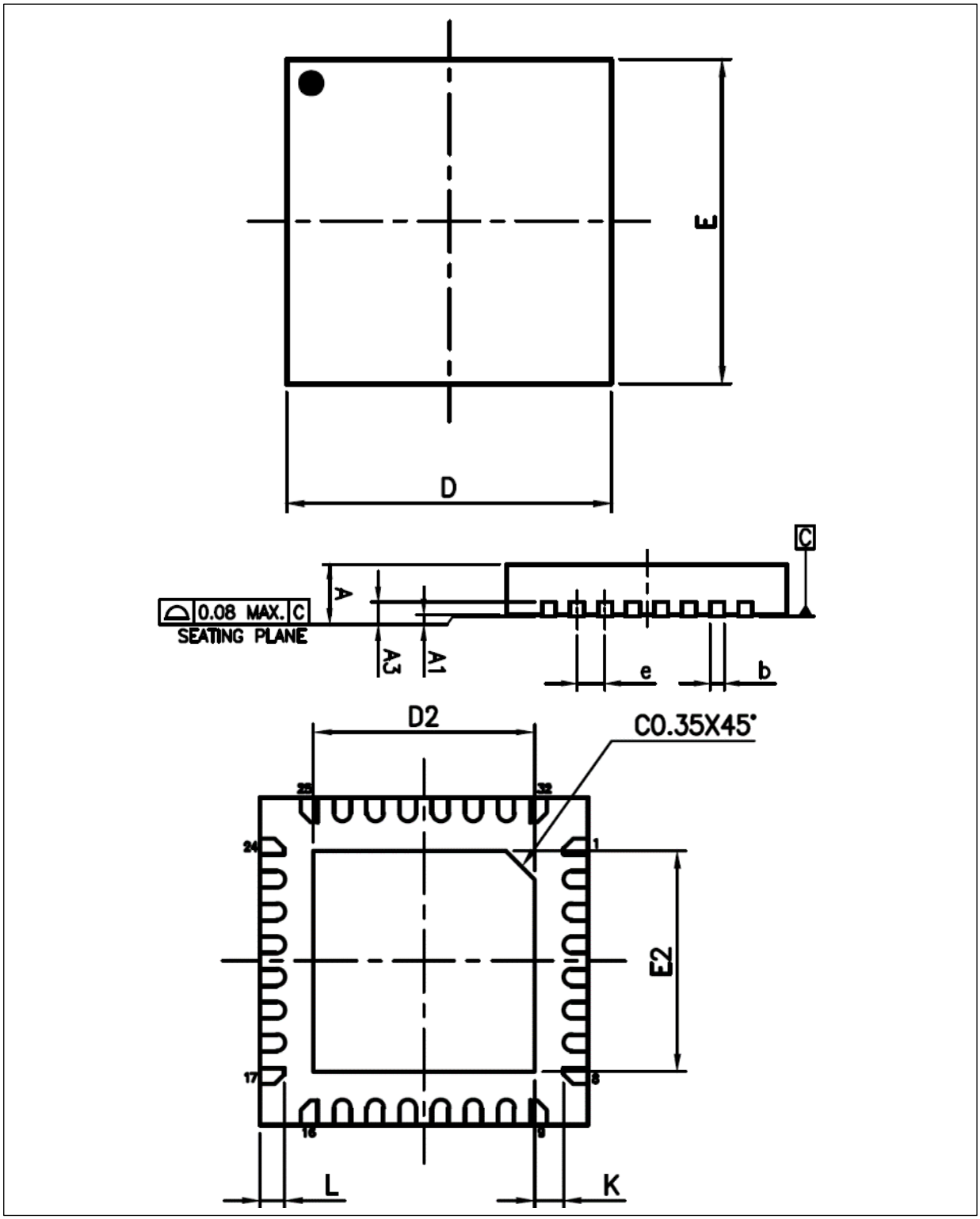
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 37. QFN32 – 5 x 5 mm marking example (package top view)



7.4 QFN32 – 4 x 4 mm package information

Figure 38. QFN32 – 4 x 4 mm 32 pin fine-pitch quad flat package outline



(1) Drawing is not in scale.

Table 49. QFN32 – 4 x 4 mm 32 pin fine-pitch quad flat package mechanical data

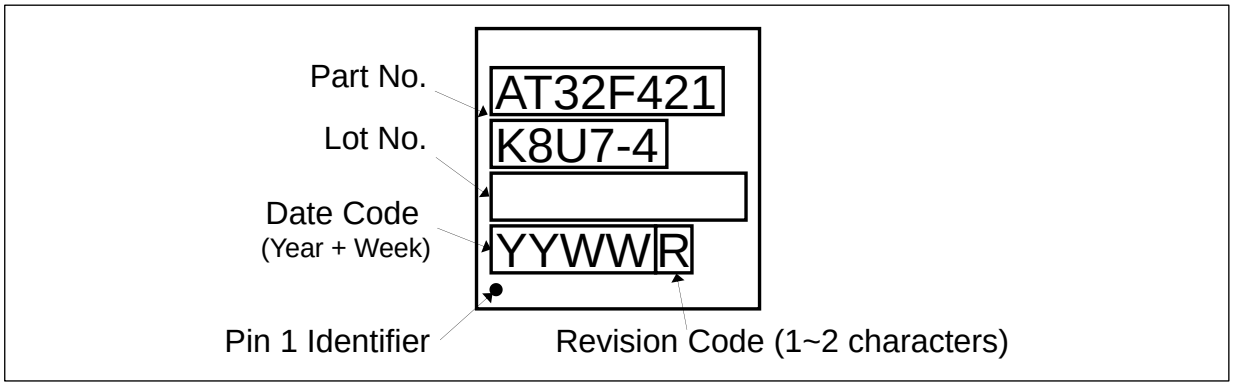
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	4.00 BSC.			0.157 BSC.		
D2	2.65	2.70	2.75	0.104	0.106	0.108
E	4.00 BSC.			0.157 BSC.		
E2	2.65	2.70	2.75	0.104	0.106	0.108
e	0.40 BSC.			0.016 BSC.		
K	0.20	-	-	0.008	-	-
L	0.25	0.30	0.35	0.010	0.012	0.014

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for QFN32 – 4 x 4 mm

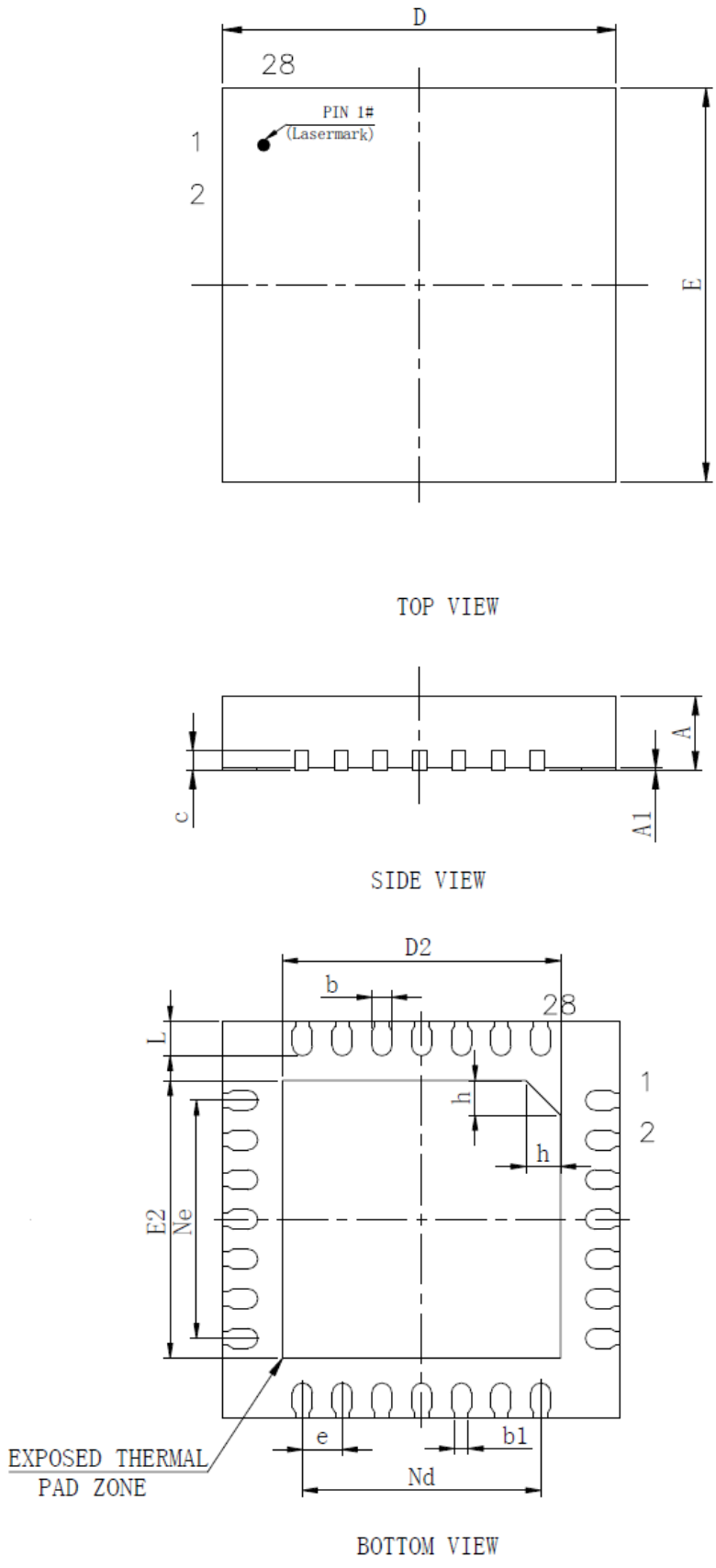
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. QFN32 – 4 x 4 mm marking example (package top view)



7.5 QFN28 – 4 x 4 mm package information

Figure 40. QFN28 – 4 x 4 mm 28 pin fine-pitch quad flat package outline



(1) Drawing is not in scale.

Table 50. QFN28 – 4 x 4 mm 28 pin fine-pitch quad flat package mechanical data

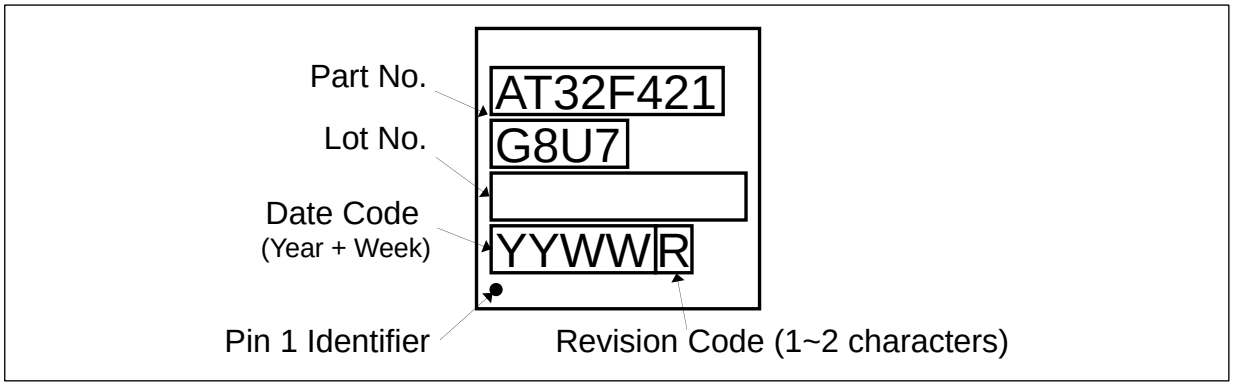
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.18	0.20	0.25	0.007	0.008	0.010
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.70	2.80	2.90	0.106	0.110	0.114
e	0.40 BSC.			0.016 BSC.		
Ne	2.40 BSC.			0.094 BSC.		
Nd	2.40 BSC.			0.094 BSC.		
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.70	2.80	2.90	0.106	0.110	0.114
L	0.30	0.35	0.40	0.012	0.014	0.016
h	0.30	0.35	0.40	0.012	0.014	0.016

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for QFN28 – 4 x 4 mm

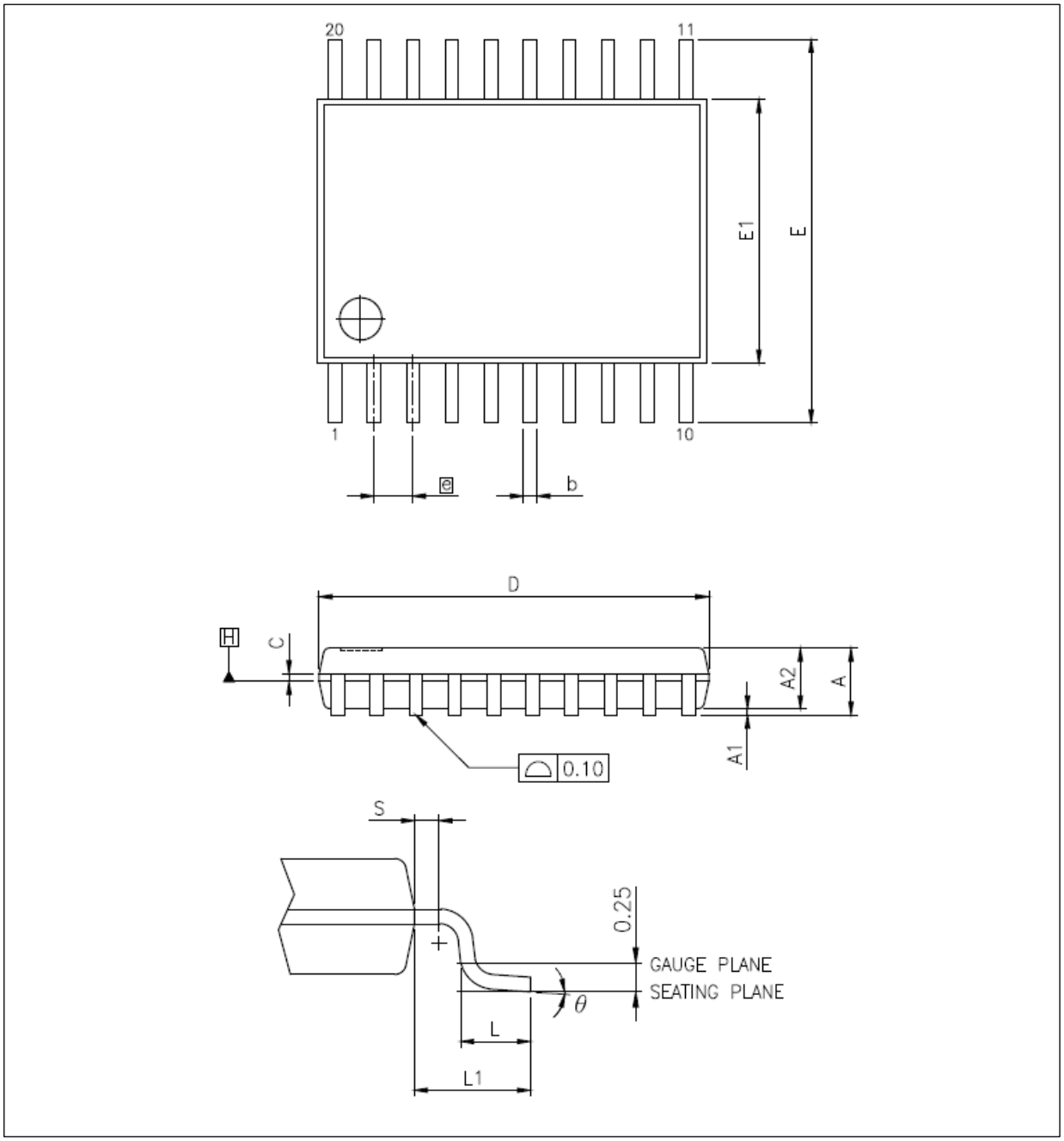
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 41. QFN28 – 4 x 4 mm marking example (package top view)



7.6 TSSOP20 – 6.5 x 4.4 mm package information

Figure 42. TSSOP20 – 6.5 x 4.4 mm 20 pin thin-shrink small outline package outline



(1) Drawing is not in scale.

Table 51. TSSOP20 – 6.5 x 4.4 mm 20 pin thin-shrink small outline package mechanical data

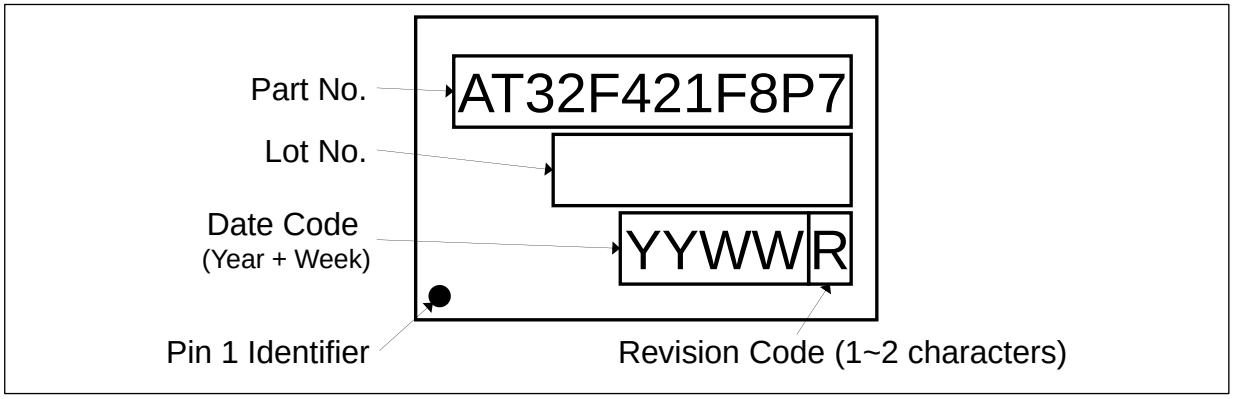
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-	0.30	0.007	-	0.012
C	0.09	-	0.20	0.004	-	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.40 BSC.			0.252 BSC.		
e	0.65 BSC.			0.026 BSC.		
L1	1.00 REF.			0.039 REF.		
L	0.50	0.60	0.75	0.020	0.024	0.030
S	0.20	-	-	0.008	-	-
Θ	0°	-	8°	0°	-	8°

(1) Values in inches are converted from mm and rounded to 3 decimal digits.

Device marking for TSSOP20 – 6.5 x 4.4 mm

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. TSSOP20 – 6.5 x 4.4 mm marking example (package top view)



7.7 Thermal characteristics

The maximum chip junction temperature ($T_j$max) must never exceed the values given in *Table 9*. The maximum chip-junction temperature, $T_j$max, in degrees Celsius, may be calculated using the following equation:

$$T_j\text{max} = T_a\text{max} + (P_d\text{max} \times \Theta_{JA})$$

Where:

- $T_a$max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_d$max is the sum of P_{INT}max and $P_{I/O}$max ($P_d$max = P_{INT}max + $P_{I/O}$max),
- P_{INT}max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins where:

$$P_{I/O}\text{max} = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

Taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 52. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 – 7 × 7 mm / 0.5 mm pitch	87.0	°C/W
	Thermal resistance junction-ambient LQFP32 – 7 × 7 mm / 0.8 mm pitch	82.4	
	Thermal resistance junction-ambient QFN32 – 5 × 5 mm / 0.5 mm pitch	39.8	
	Thermal resistance junction-ambient QFN32 – 4 × 4 mm / 0.4 mm pitch	44.8	
	Thermal resistance junction-ambient QFN28 – 4 × 4 mm / 0.4 mm pitch	44.8	
	Thermal resistance junction-ambient TSSOP20 – 6.5 × 4.4 mm / 0.65 mm pitch	103.0	

8 Part numbering

Table 53. AT32F421 ordering information scheme

Example: AT32 F 4 2 1 K 8 U 7 -4

Product family

AT32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4

Product series

2 = Value line

Product application

1 = Basic series

Pin count

C = 48 pins

K = 32 pins

G = 28 pins

F = 20 pins

Internal Flash memory size

4 = 16 KBytes of the Flash memory

6 = 32 KBytes of the Flash memory

8 = 64 KBytes of the Flash memory

Package

T = LQFP

U = QFN

P = TSSOP

Temperature range

7 = -40 °C to +105 °C

Package details

-4 = QFN32 - 4 x 4 mm

Blank = other packages

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Artery sales office.

9 Revision history

Table 54. Document revision history

Date	Version	Change
2020.8.17	1.00	Initial release.
2020.9.16	1.01	1. Corrected the maximum frequency of APB1 and APB2 as 120 MHz in *Figure 1*, *Table 9*, and *Table 19*. 2. Modifed conditons and the maxmum values of the SPI clock frequencyin *Table 38*. 3. Added the EFT result as 3/A (2 kV) in *Table 30*. 4. Added note (4) of *Table 5* to describe the software suggestions for PA11 and PA12 on QFN28 package. 5. Corrected the HSI 48 MHz block in *Figure 2*.
2021.7.1	1.02	1. Updated details of COMP V_{offset} in *Table 44*. 2. Updated details of temperature sensor T_L in *Table 45*. 3. Added LQFP48 package mechanical D, D1, E, E1 Min. and Max. in *Table 46*.

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