based onARM®32bitCortex™-M4microcontroller with16Kbyte to64Kbyte flash, sLib,10a timer,1indivualADC,1indivualComparators,7communication interface

Function

- **kernel:ARM®32bitCortex™-M4 CPU**
  - Highest120 MHzoperating frequency, with a memory protection unit (MPU), built-in single-cycle multiplication and hardware division
  - haveDSPInstruction Set
- **memory**
  - 16Kbyte to64KBytes of Flash Program/Data Memory
  - 4Kbytes of system memory as a bootloader (Bootloader), can be configured as a general user program and data area at one time
  - sLib: Set the specified main storage area as the execution code security library area, the code in this area can only be called but not read
  - 8 Kbyte to16KbyteSRAM **CRC**
- **computing unit**
- **Reset and Power Management**
  - 2.4to3.6volt power supply andI/Opin
  - Power-on/Power-off reset (POR/PDR)
  - Programmable Voltage Monitor (PVD)
  - Low Power Modes: Sleep, Shutdown, Standby,4indivualWKUP Pin to wake up from standby mode
  - support5indivual32bit backing register **clock**
- **management**
  - 4to25 MHzcrystal oscillator
  - Built-in factory-tuned48 MHz RCoscillator (25°Creach1 %precision,-40°Cto +105°Creach2 % precision)
  - PLLsFlexible configuration31to500multiplier and1to15Frequency division factor
  - Built-in with calibration40 kHz RCoscillator
  - with calibration function32 kHzcrystal
- oscillator **up to39a quickI/O**
  - All can be mapped to external interrupt
  - Almost allI/OTolerable5VInput voltage
  - all fastI/O, register access speed is the highestf_{AHB}
- **5aisleDMAcontroller**
- **1indivual12bit2 MSPS A/Dconverter, up to15external input channels**
- **1a comparator with5external input channels and1internal reference voltage**
- **up to10timer**
  - 1indivual16bit7Channel Advanced Timer, with6aislePWMoutput with deadband control and emergency stop
  - up to5indivual16bit timers, each with up to4one for input capture/output compare/PWMor pulse counting channels and incremental encoder inputs
  - 1indivual16bit basic timer
  - 2Watchdog timers (independent and windowed)
  - System tick timer:twenty fourbit down counter
- **ERTC: EnhancedRTC, with alarm clock, sub-second resolution, and hardware calendar**
- **up to7communication interface**
  - 2indivualI^2Cinterface (supportSMBus/PMBus)
  - 2indivualUSARTinterface; supports master synchronizationSPI and modem control; withISO7816interface,LIN,IrDAability
  - 2indivualSPIinterface(50Mbit/s),2can be reused as I^2S interface
  - infrared emitter
- **Serial Wire Debug (SWD)interface**
- **96bit chip unique code (UID)**
- **temperature range:-40to +105°C**
- **encapsulation**
  - LQFP48 7 x 7mm
  - LQFP32 7 x 7mm
  - QFN32 5 x 5mm
  - QFN32 4 x 4mm
  - QFN28 4 x 4mm
  - TSSOP20 6.5 x 4.4mm

surface1.selection list

flash memory	model
64Kbyte	AT32F421C8T7, AT32F421K8T7, AT32F421K8U7, AT32F421K8U7-4, AT32F421G8U7, AT32F421F8P7
32Kbyte	AT32F421C6T7, AT32F421K6T7, AT32F421K6U7, AT32F421K6U7-4, AT32F421G6U7, AT32F421F6P7
16Kbyte	AT32F421C4T7, AT32F421K4T7, AT32F421K4U7, AT32F421K4U7-4, AT32F421G4U7, AT32F421F4P7

Table of contents

table directory

Figure catalog

1 introduce

This article givesAT32F421series ordering information and device mechanical characteristics.

AT32F421series data sheet, must be combined withAT32F421Series Reference Manual read together. Information on programming, erasing, and protecting Flash memory is also available atAT32F421Series Reference Manual obtained from.

relatedCortex-M4For core information, please refer toCortex-M4Technical Reference Manual, available atARMcompany website download: http://infocenter.arm.com

2 Specifications

AT32F421series microcontrollers using high-performanceARM®Cortex™-M4 32bitRISCcore, operating at a maximum frequency of120 MHz,Cortex™-M4The kernel has a set ofDSPinstructions and a Memory Protection Unit (MPU).

AT32F421series built-in high-speed embedded memory (up to64Kbytes of flash memory and16KbyteSRAM), the rich enhancementI/O port and connect to twoAPB peripherals on the bus. The built-in memory can set any range of program area subject tosLibprotection, and become a safe library area for executing code.

Device contains1indivual12bitADC,1an analog comparator,5general16bit timer, and1advanced timers, also includes standard and advanced communication interfaces: up to2indivualI²Cinterface,2indivualSPIinterface (multiplexed asI²Sinterface),2indivualUSARTinterface, and1an infrared emitter.

AT32F421series work on-40°Cto +105°Ctemperature range, supply voltage2.4Vto3.6V, power saving mode guarantees low power consumption application requirements.

AT32F421family of microcontroller offerings including from20foot to48feet6Different packaging forms; according to different packaging forms, its members are completely compatible pin-to-pin, software and function are also compatible, only the peripheral configuration in the device is not the same. A basic introduction of all peripherals in this series is given below.

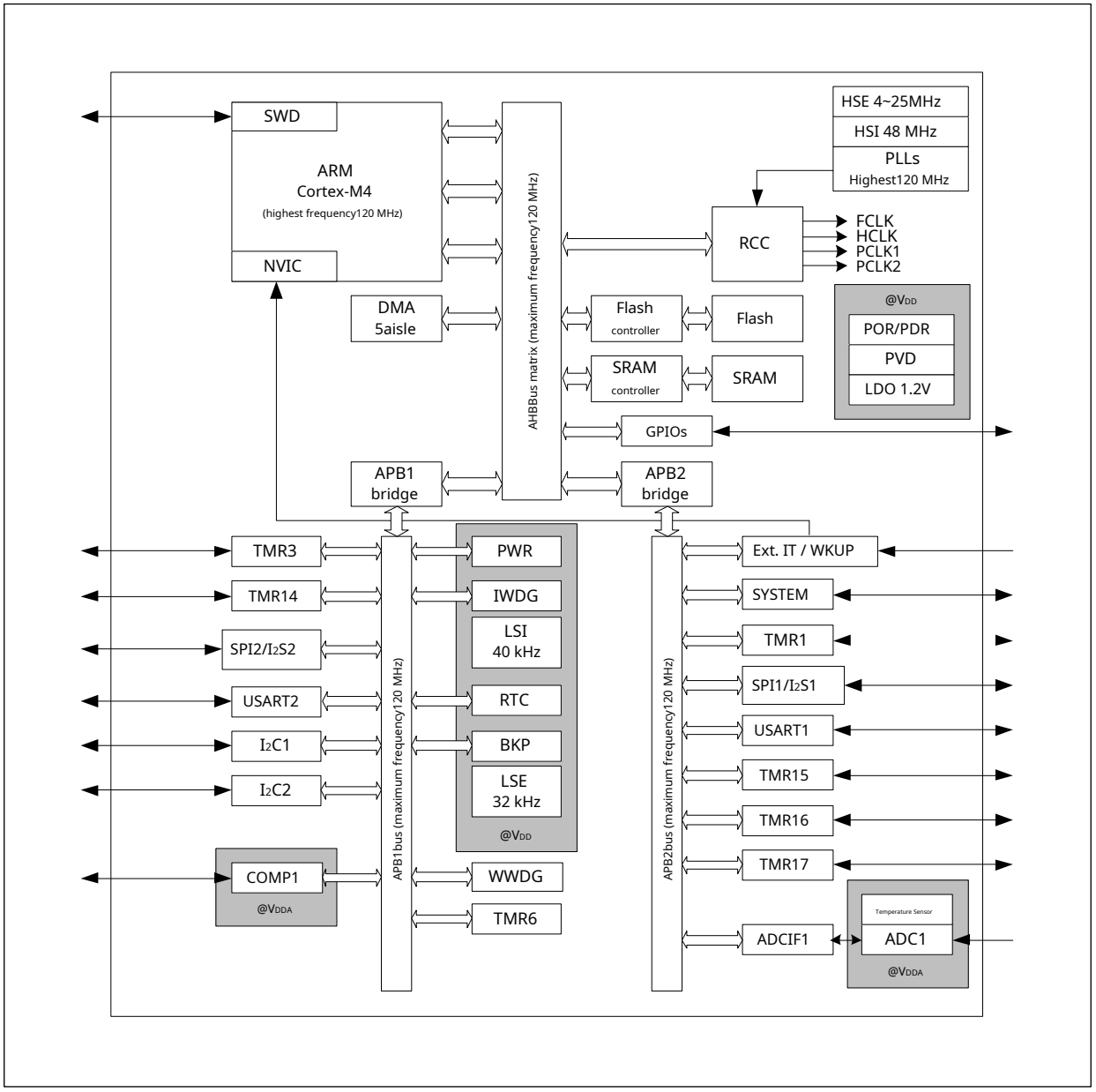
surface2. AT32F421Family Device Features and Configurations

model		AT32F421xxP7			AT32F421xxU7			AT32F421xxU7-4			AT32F421xxU7			AT32F421xxT7			AT32F421xxT7		
		F4	F6	F8	G4	G6	G8	K4	K6	K8	K4	K6	K8	K4	K6	K8	C4	C6	C8
frequency(MHz)		120																	
Flash (Kbyte)		16	32	64	16	32	64	16	32	64	16	32	64	16	32	64	16	32	64
SRAM(Kbyte)		8	16	16	8	16	16	8	16	16	8	16	16	8	16	16	8	16	16
timer	advanced	1			1			1			1			1			1		
	16bit generic	5			5			5			5			5			5		
	basic	1			1			1			1			1			1		
	SysTick	1			1			1			1			1			1		
	IWDG	1			1			1			1			1			1		
	WWDG	1			1			1			1			1			1		
	ERTC	1			1			1			1			1			1		
Communication Interface	I_2C	2			2			2			2			2			2		
	SPI/I_2S	1/1(1)			2/2			2/2			2/2			2/2			2/2		
	USART+UART	1+1(2)			2+0			2+0			2+0			2+0			2+0		
	infrared emitter	1			1			1			1			1			1		
simulation	12bitADCconverter/	1			1			1			1			1			1		
	Number of external channels	9			10			11			11			10			15		
	Comparators	1			1			1			1			1			1		
GPIOs		15			twenty three			27			27			25			39		
Operating temperature		- 40°Cto +105°C																	
Package form		TSSOP20 6.5 x 4.4 mm			QFN28 4 x 4 mm			QFN32 4 x 4 mm			QFN32 5 x 5mm			LQFP32 7 x 7 mm			LQFP48 7 x 7 mm		

(1)existTSSOP20on the packageonly supportSPI1.

(2)existTSSOP20on the packageUSART2All pins are reserved;USART1onlyTXandRXfeet, so onlyUARTuse.

picture1. AT32F421Series functional block diagram



3 Functional Overview

3.1 ARM®Cortex™-M4,WithDSPinstruction

ARM Cortex™-M4is the latest generation of embeddedARMprocessor, which implementsMCUThe need to provide a low-cost platform, reduced pin count, reduced system power consumption, while providing excellent computing performance and advanced interrupt system response.

ARM Cortex™-M4The processor is a32bitRISCprocessor, with excellent code efficiency, employs the usual8bit and16bit device memory space to playARM®High performance of the kernel.

The processor supports a set ofDSPinstructions that enable efficient signal processing and complex algorithm execution.

AT32F421series and allARMTools and software are compatible.

*picture1*is the functional block diagram of this series of products.

Note: Cortex™-M4kernel withCortex™-M3The kernel is binary compatible.

3.2 memory

3.2.1flash memory

Built-in Gundam64KBytes of flash memory for storing programs and data. The built-in memory can specify any range of program area to besLib Protection, it becomes a safe library area that can only execute code that cannot be read.sLibIt is designed based on protecting the code security of the solution provider and taking into account the convenience of its customers for secondary development.

on-chip otherwise4Kbytes of system memory, the bootloader (Bootloader) are stored in it. If the user does not need to use the boot loader, the system memory can be configured as a general user program and data area at one time.

3.2.2Memory Protection Unit (MPU)

Memory Protection Unit (MPU) for managementCPUAccess to memory that prevents one task from accidentally corrupting memory or resources used by another active task. This store is organized as a maximum of8protected areas, which in turn can be subdivided into up to8a sub-area. The size of the protected area can be32bytes to the entire4Gbyte.

If there is some critical or critical code in the application that must be protected from erroneous behavior by other tasks, thenMPUEspecially useful. it usually consists ofRTOS(real-time operating system) management. If the program accesses a memory location that isMPUprohibited, thenRTOSIt can be detected and acted upon. existRTOSIn the environment, the kernel can be dynamically updated based on the executing processMPUzone settings.

MPUis optional and can be bypassed if not required by the application.

3.2.3built-inSRAM

Gundam16Kbyte embeddedSRAM,CPUCan be accessed (read/write) with zero wait cycles.

3.3 Cyclic Redundancy Check (CRC) computing unit

CRC(cyclic redundancy check) calculation unit using a fixed polynomial generator from a32bit data word to generate aCRC code. In many applications, based onCRCThe technique is used to verify the consistency of data transmission or storage. according toEN/IEC60335-1 These techniques provide a means of detecting errors in flash memory as specified in the standard.CRCComputational units help to calculate the software's signature during runtime and compare this signature with a reference signature generated at link time and stored in a given memory unit.

3.4 Interrupts and events

3.4.1Nested Vectored Interrupt Controller (NVIC)

AT32F421The series products have built-in nested vector interrupt controller, which can manage16priority, processingCortex-M4most cores28 maskable interrupt channels and16interrupt line.

- Tightly coupledNVICCan achieve low-latency interrupt response processing
- interrupt vector entry address directly into the kernel
- Tightly coupledNVICinterface
- Allows early handling of interrupts
- Handle late arriving higher priority interrupts
- Support interrupt tail link function
- Automatically save processor state
- Automatic recovery on return from interrupt without additional instruction overhead

This module provides flexible interrupt management functions with minimal interrupt latency.

3.4.2External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains20An edge detector for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge trigger, falling edge trigger, or both edge triggers), and can be masked individually; there is a pending register to maintain the status of all interrupt requests.EXTIcan detect pulse widths smaller than the internalAHBthe clock cycle. The external interrupt line has a maximum of16root, available from as many as39generalI/Oport to select the connection.

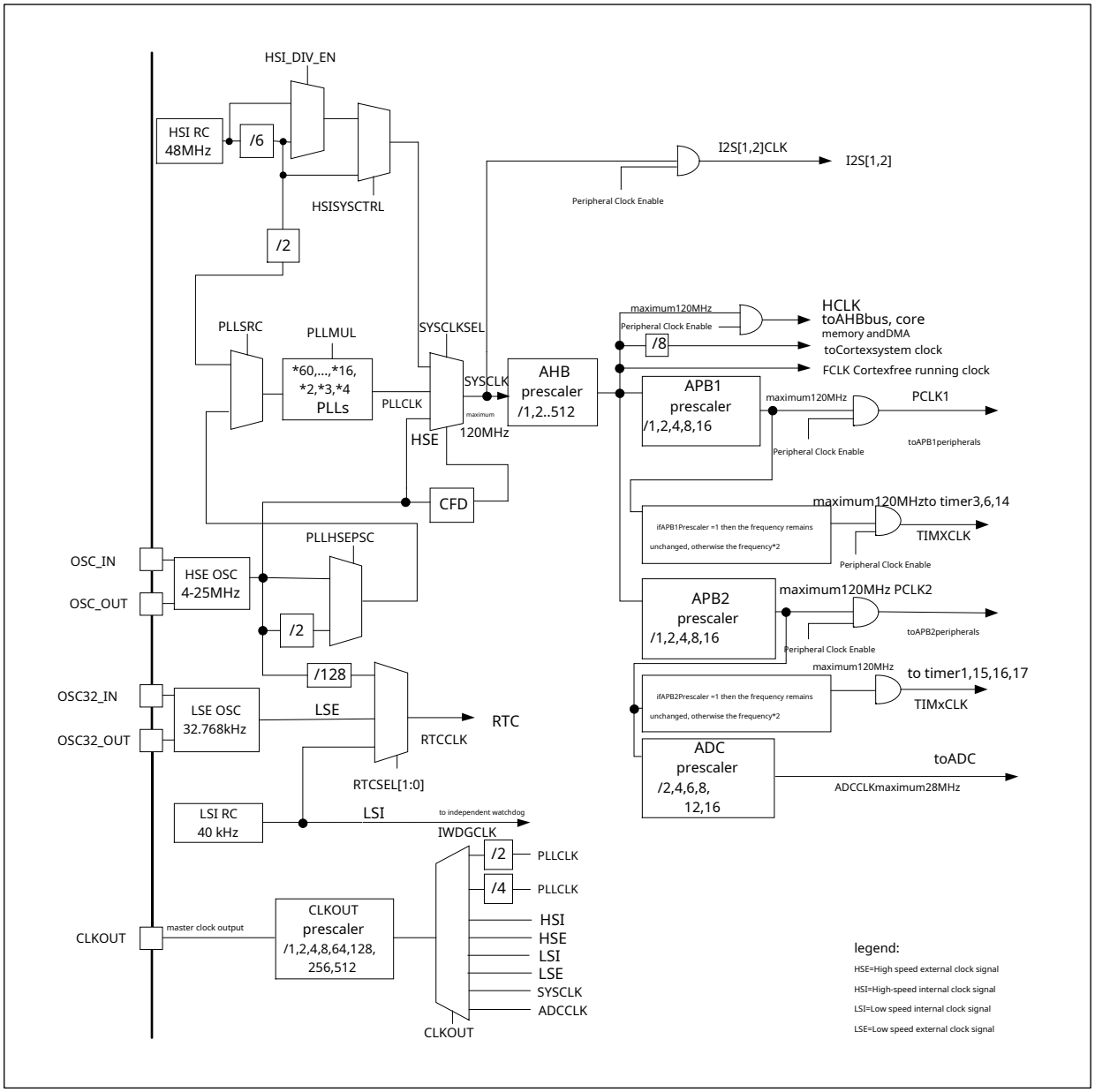
3.5 clock and start

The selection of the system clock is performed at startup, and the internal48MHzofRCoscillator(HSI)through6After frequency division (8 MHz) was selected as the defaultCPUclock, followed by an optional external, fail-safe4~25MHzclock(HSE);When the external clock failure is detected, it will be isolated and the system will automatically switch to the internalRCoscillator(HSI), if the interrupt is enabled, the software can receive the corresponding interrupt. Likewise, when required, thePLLsClock complete interrupt management (eg when an indirectly used external oscillator fails).

Multiple prescalers are used to configureAHBFrequency of,APB(APB1andAPB2)area.AHBandAPBThe highest frequency of120 MHz.

refer to*picture2*The clock driver block diagram.

picture2.clock tree



3.6 boot mode

At startup, passBOOT0pin and user select bytenBOOT1Bit settings can select one of three boot modes:

- boot from user flash memory;
- boot from system memory;
- from the insideSRAMstart up.

boot loader (Bootloader) are stored in the system memory and can be accessed byUSART1orUSART2Reprogram the flash memory. *surface3*Provides a bootloader (Bootloader)rightAT32F421pin configuration.

surface3.boot loader (Bootloader) of the pin configuration

peripherals	Corresponding pin
USART1	PA9:USART1_TX PA10:USART1_RX
USART2	PA2:USART2_TX PA3:USART2_RX

3.7 power management

3.7.1Power supply scheme

- V_{DD}= 2.4~3.6V:passV_{DD}Pin isI/Opin,ERTC,external32 kHzOscillator, backup registers, and internal voltage regulator.
- V_{DDA}= 2.4~3.6V:passV_{DDA}Pin isA/Dconverter andCOMPComparator power supply.V_{DDA}andV_{SSA}must be connected toV_{DD}andV_{SS}.

For details on how to connect the power pins, see*picture11*power supply scheme.

3.7.2power monitor

This product integrates a power-on reset (POR)/ Brownout Reset (PDR) circuit, which is always active to ensure that the device does not operate at a voltage lower than2.4Vcan work normally; whenV_{DD}below the specified threshold ($V_{POR/PDR}$), puts the device in a reset state without the use of an external reset circuit.

There is also a programmable voltage monitor (PVD), which monitorsV_{DD}powered and withV_{PVD}Threshold comparison, whenV_{DD}below or above V_{PVD}When the threshold is interrupted, the interrupt handler can issue a warning message or transfer the microcontroller into a safe mode.PVDThe function needs to be enabled by software. about$V_{POR/PDR}$andV_{PVD}The value reference*surface11*and*surface12*.

3.7.3Regulator

The regulator has three modes of operation: Master Mode (MR), low power mode (LPR), and shutdown mode

- main mode (MR) for normal run operation andCPUshutdown mode; low
- power mode (LPR)Can be used asCPUshutdown mode;
- Shutdown mode is used forCPUStandby mode: the output of the voltage regulator is in a high-impedance state, the power supply of the core circuit is cut off, and the voltage regulator is in a state of zero consumption. (but registers andSRAMwill be lost.)

The voltage regulator is always active after reset, and the high-impedance output is turned off in standby mode.

3.7.4low power mode

AT32F421The family of products supports three low-power modes, which can achieve the best balance between requiring low power consumption, short startup time and multiple wake-up events.

- sleep mode

  In sleep mode, onlyCPUStop working, all peripherals keep running and can wake up on interrupt/eventCPU.
- shutdown mode

  Low power consumption can be achieved in shutdown mode while maintainingSRAMand register contents. at this time,1.2VAll clocks in the domain are stopped,PLLs,HSIoscillator, andHSEThe crystal oscillator is also turned off. It is also possible to place the regulator in normal mode (MR) or low power mode (LPR), in which the low power mode can also lower the output voltage of the voltage regulator to further reduce power consumption. can be configured by eitherEXTIsignal to wake up the microcontroller from shutdown mode,EXTIsignal can be16externalI/Oone of the mouth,PVDOutput,ERTCalarm/intrusion detection/time stamp events, orCOMPwake-up signal. standby mode
-

  The lowest power consumption is achieved in standby mode. At this time, the internal voltage regulator is turned off, so the entire internal1.2VPart of the power supply was cut off.PLLs,HSIofRCoscillator andHSEThe crystal oscillator is also turned off. After entering standby mode,SRAMand register contents will disappear, butRTCThe contents of domain registers and backup registers are still preserved, and the standby circuit still works.

occurNRSTexternal reset signal on theIWDGreset,wxyaA rising edge on the pin, or triggerERTCAlarm/Intrusion Detection/Timestamp event, device exit from Standby mode.

Note: When entering shutdown or standby mode, theERTC,IWDGand the corresponding clock will not be stopped.

3.8 Direct Memory Access Controller (DMA)

5Channel commonDMACan manage storage-to-storage, device-to-storage, and storage-to-device data transfers.

DMAThe controller supports the management of the ring buffer without intervention by user code when the controller reaches the end of the buffer.

Each channel has dedicated hardwareDMArequest logic, while each channel can be triggered by software. The length of the transfer, the source address and the destination address of the transfer can all be set individually by software.

DMAAvailable for major peripherals:SPI,I2S,I2C,USART, all timersTMRx(Apart fromTMR14),andADC.

3.9 Enhanced Real Time Clock (ERTC) and backup registers after

Fallback domains include:

- Enhanced Real Time Clock (ERTC)
- 5indivual32bit backing register

Enhanced Real Time Clock (ERTC) is an independentBCDTimer/Counter. It supports the following functions:

- The calendar has seconds, minutes, hours (12ortwenty fourhour format), day of week, day, month, year in the formatBCD(binary coded decimal).
- Provides subsecond values in binary format.
- Automatically adjusts the number of days per month to28,29(leap year),30,still31sky.
- Programmable alarm clock has the ability to wake up from stop and standby mode.
- run-time correction1arrive32767indivualERTCclock pulse. This can be used toERTCsynchronized with the master clock. The digital calibration
- circuit has1 ppmresolution to compensate for the inaccuracy of the quartz crystal. The tamper detect pin has a programmable filter. When a
- tamper event is detected,MCUWake up from stop and standby mode.
- The timestamp feature can be used to save calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. When a timestamp event is detected,MCUWake up from stop and standby mode.
- Reference Clock Detection: Allows use of a more accurate second clock source (50or60Hz) to increase the accuracy of the calendar.

The alarm clock register is used to generate an alarm at a specific time, and the calendar fields can be individually masked to compare alarms.

20bit prescaler for the time reference clock. By default, it is configured from32.768 kHzclock generation1The time base in seconds.

The backing register is32bit register, used to store20bytes of user application data. The backup registers are not reset on system reset, nor on device wake-up from Standby mode.

other32Bit registers also contain programmable alarm subseconds, seconds, minutes, hours, day of the week, and date.

ERTCThe clock source can be:

- 32.768 kHzexternal crystal, resonator, or oscillator (LSE); internal
- low powerRCoscillator (LSI), the typical frequency is40 kHz; High-
- speed external clock (HSE)of32crossover.

3.10Timers and Watchdogs

AT32F421The series includes the most1an advanced timer,5an ordinary timer,1a basic timer, and2a watchdog timer, and1A system tick timer.

The table below compares the functionality of the different timers:

surface4.Timer Function Comparison

timer type	timer	counter Resolution	counter type	Prescaler coefficient	produceDMAask	capture/compare channel	complementary output
advanced	TMR1	16bit	increment, decrement, increment/decrement	1~65536between any integer of	have	4	3
universal	TMR3	16bit	increment, decrement, increment/decrement	1~65536between any integer of	have	4	none
	TMR14	16bit	increment	1~65536between any integer of	none	1	none
	TMR15	16bit	increment	1~65536between any integer of	have	2	1
	TMR16 TMR17	16bit	increment	1~65536between any integer of	have	1	1
basic	TMR6	16bit	increment	1~65536between any integer of	have	none	none

3.10.1Advanced Timer (TMR1)

An Advanced Timer (TMR1) can be viewed as assigning to6three-phasePWMgenerator with complementaryPWMoutput, which can also be used as a complete general-purpose timer. Four independent channels can be used for:

- input capture
- output compare
- with full modulation capability (0~100%)ofPWMGeneration (Edge or Center Aligned Mode) Single
- Pulse Mode Output

In debug mode, the counters can be frozen whilePWMoutputs are disabled, turning off the switches controlled by those outputs.

Many features of Advanced Timer are related to general-purposeTMRThe timers are the same, and the internal structure is the same, so the advanced timer can cooperate with the general-purpose timer through the timer link function to provide synchronization or event link function.

3.10.2General purpose timer (TMR3,TMR14,TMR15,TMR16,andTMR17)

AT32F421series products, built-in up to5A general-purpose timer that can run synchronously. Every general purpose timer can be used to generate PWMoutput, or as a simple time reference.

- **TMR3**

  TMR3is based on a16bit dynamic loading up/down counters and a16bit prescaler. This timer is available in the largest package configuration4independent channels, each of which can be used for input capture, output compare,PWMand single pulse mode output.

TMR3It can also work with advanced timers through the timer chaining function to provide synchronization or event chaining functions.TMR3can be used to generatePWMoutput.TMR3It can also process signals from incremental encoders, and can also process1to3Digital output of a Hall sensor.

In debug mode, the counters can be frozen.TMR3independentDMArequest mechanism.

- **TMR14**

The timer is based on a16bit autoload up counter, a16bit prescaler and1independent channels, each of which can be used for input capture, output compare,PWMand single-pulse mode output, which can be synchronized with a full-featured general-purpose timer or used as a simple timer.

In debug mode, the counters can be frozen.

- **TMR15,TMR16,andTMR17**

These three general-purpose timers have16bit auto-reload incrementing counter and16bit prescaler.TMR15have2channels and1a complementary channel,TMR16andTMR17have1channels and1a complementary channel. All channels are available for input capture/output compare, PWMor single pulse mode output.

These timers can work together through timer chaining to provide synchronization or event chaining.

In debug mode, the counters can be frozen. These timers have independentDMARequest generation mechanism.

3.10.3Basic Timer (TMR6)

This timer is used as a general16bit time base counter.

3.10.4Independent Watchdog (IWDG)

The independent watchdog is based on a8bit prescaler and a12bit down counter, which consists of an internal independent40 kHzof RCThe oscillator provides the clock; since thisRCThe oscillator is independent of the main clock, so it can run in shutdown and standby modes. It can be used as a watchdog to reset the entire system when a problem occurs, or as a free timer to provide timeout management for applications. It can be configured as a software or hardware enabled watchdog by selecting bytes. In debug mode, the counters can be frozen.

3.10.5window watchdog (WWDG)

The window watchdog is based on a free-running7Bit down counter. It can be used as a watchdog to reset the entire system when a problem occurs. it consists ofAPB1Clock driven with early warning interrupt function. In debug mode, the counters can be frozen.

3.10.6System Tick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a general-purpose down counter. It has the following properties:

- twenty fourbit down counter
- auto reload function
- When the counter is0, a maskable system interrupt is generated
- Programmable Clock Source (HCLKorHCLK/8)

3.11Inter-IC bus (I2C)

2indivualI2CBus interface, able to work in multi-master mode or slave mode, supports standard mode (up to100 kbit/s) and fast mode (maximum400 kbit/s).I2CThe bus frequency can be increased up to1 MHz. For a more complete and detailed solution, you can contact the nearest Yateli sales office for technical support.

I2Cinterface support7bit or10bit addressable,7Bit slave mode supports dual slave address addressing. built in hardwareCRCGenerator/Checker.

they can useDMAoperate and supportSMBusbus2.0Version/PMBusbus.

3.12Universal Synchronous/Asynchronous Transceiver (USART)

AT32F421series products, the built-in2a Universal Synchronous/Asynchronous Transceiver (USART1andUSART2).

this2indivualUSARTThe interface provides asynchronous communication, supportIrDA SIR ENDECTransport codec, multiprocessor communication mode, master synchronous communication, single-wire half-duplex communication mode, andLINMaster/slave functionality.2indivualUSARTinterface with hardwareCTSandRTSSignal Management, Compatibility ISO7816smart card mode.2indivualUSARTinterface can be usedDMAoperate.

2indivualUSARTInterface communication rate can reach7.5megabits per second.

3.13Serial Peripheral Interface (SPI)/internal integrated audio interface (I2S)

2indivualSPIInterface, in slave or master mode, full-duplex and half-duplex communication speed up to50megabits per second.3bit prescaler can generate8 1 main mode frequency, configurable as per frame8bit or16bit. hardwareCRCGenerate/verify support for basicSDCard,MMCmode, and SDHCmodel.

2standardI2Sinterface (withSPImultiplexing) can work in master or slave mode, which2An interface can be configured as16bit,twenty fourbit, or32 Bit transmission, can also be configured as input or output channel, supports audio sampling frequency from8 kHzarrive192 kHz. as eitherI2SThe interface is configured in master mode, and its master clock can be256times the sampling frequency output to an externalDACorCODEC(decoder).

allSPIinterface can be usedDMAoperate.

3.14Infrared Emitter (IR)

AT32F421device provides an IR emitter solution. The solution is based onTMR16,USART1,orUSART2and TMR17internal connection between.TMR17used to provide the carrier frequency,TMR16,USART1,orUSART2Provides the main signal to send. Infrared output signal atPB9orPA13available on .

In order to generate an IR remote control signal, it must be properly configuredTMR16aisle1andTMR17aisle1to generate the correct waveform. all standardsIRBoth pulse modulation modes are available by programming the two timer output compare channels.

3.15GPIO (GPIOs)

eachGPIOsAll pins can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down), or multiplexed peripheral function ports. mostGPIOsPins are shared with digital or analog multiplexed peripherals.

in case of need,I/OThe peripheral function of the pin can be locked by a specific operation to avoid theI/OA register has performed an unexpected write operation.

3.16Analog/Digital Converter (ADC)

AT32F421series of products, built-in1indivual12bit analog/digital converter (ADC), sharing up to15external channels and3internal (temperature sensor, internal voltage reference, andV_{SSA}) channels, single-shot or scan conversions can be implemented. In scan mode, conversions on a selected set of analog inputs are performed automatically.

ADCcan useDMAoperate.

The analog watchdog function allows very precise monitoring of one, multiple or all selected channels, and an interrupt will be generated when the monitored signal exceeds a preset threshold.

by the general purpose timer (TMRx) and Advanced Timer (TMR1) can be cascaded internally to theADCThe start trigger and injection trigger, the application can make theADCConversions are synchronized with the clock.

3.16.1Temperature Sensor

The temperature sensor produces a voltage that varies linearly with temperatureV_{SENSE}, the conversion range is2.4 V ≤ V_{DDA}≤ 3.6Vbetween. The temperature sensor is internally connected to theADC_IN16On the input channel of the sensor, it is used to convert the output of the sensor into a digital value.

3.16.2internal reference voltage (V_{REFINT})

internal reference voltage(V_{REFINT})forADCand comparator provides a regulated voltage output.V_{REFINT}Internally connected toADC_IN17 on the input channel for theV_{REFINT}The output of is converted to a numeric value.

3.17Comparators(COMP)

AT32F421The device contains a rail-to-rail comparator(COMP), with programmable reference voltage (internal or external), hysteresis and speed, selectable output polarity, output function with blanking, and glitch filter.

The reference voltage can be one of the following:

- externalI/O
- internal reference voltage(V_{REFINT})or its submultiples(1/4,1/2,3/4). Please refer to*surface13*to obtain the value and accuracy of the internal reference voltage.

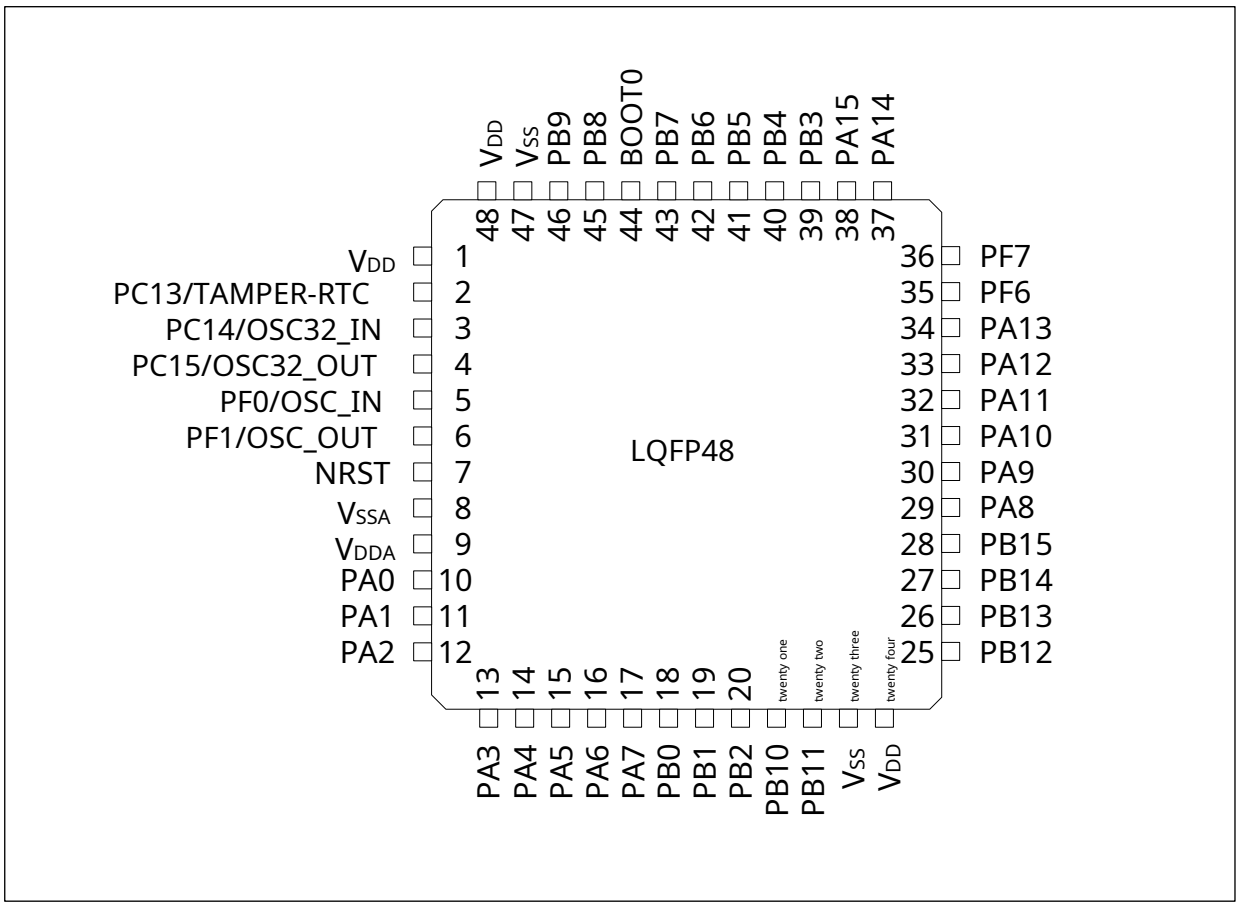
The comparator can wake up from stop mode, and can also generate interrupt and disconnect for the timer.

3.18Serial Wire Debug Port (SW-DP)

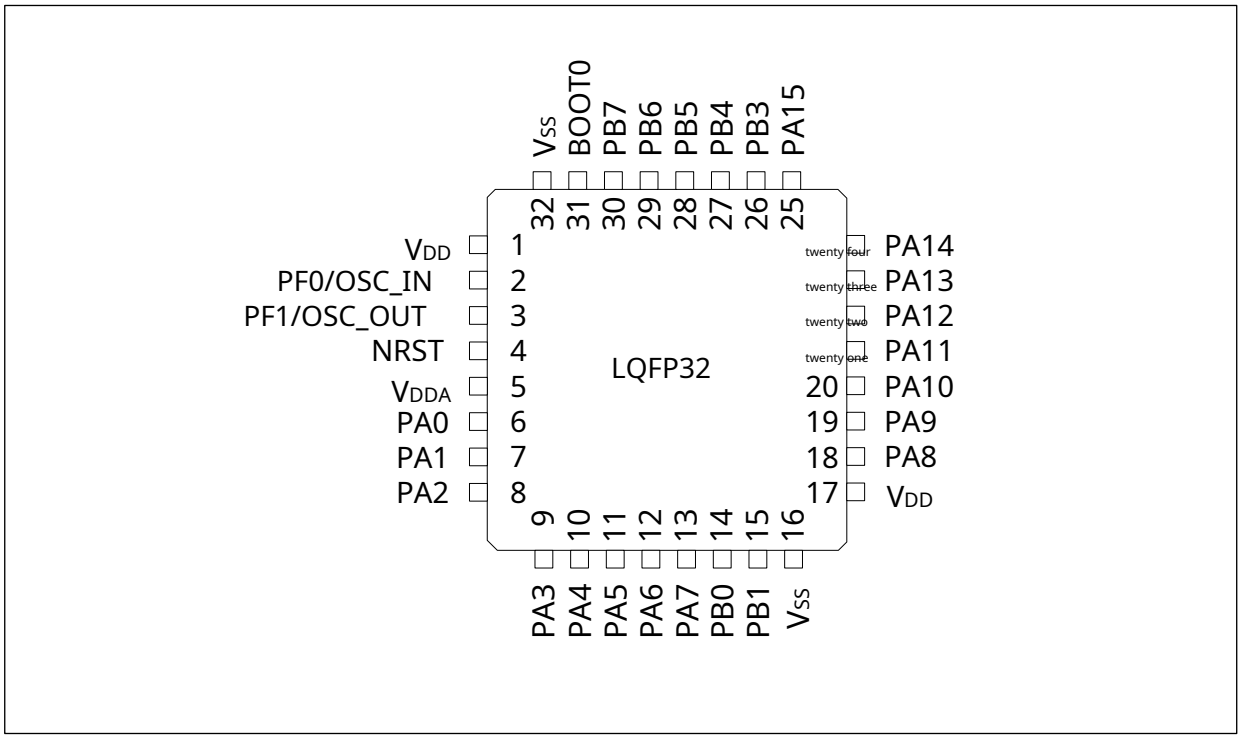
embeddedARMofSW-DPInterface, this is a serial line debugging interface, which can realize the connection of the serial line debugging interface to the target, and realize the programming and debugging of the target.

4 pin definition

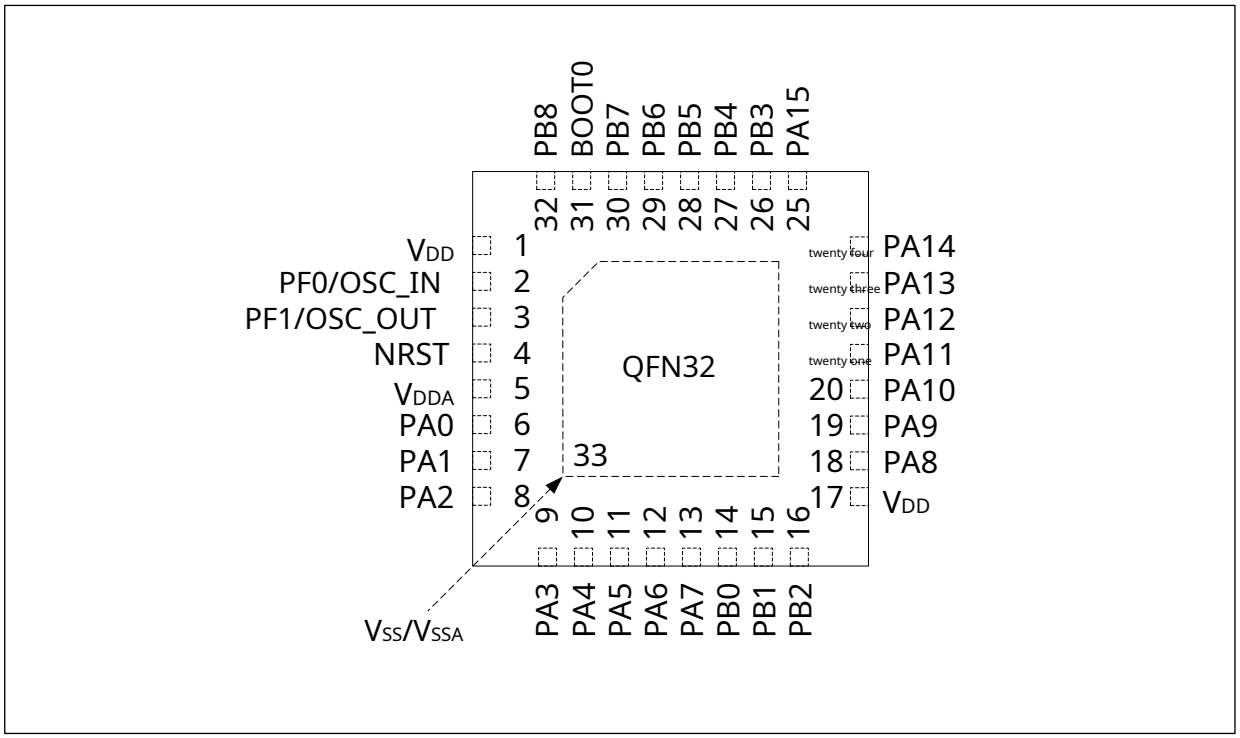
picture3. AT32F421seriesLQFP48pin distribution



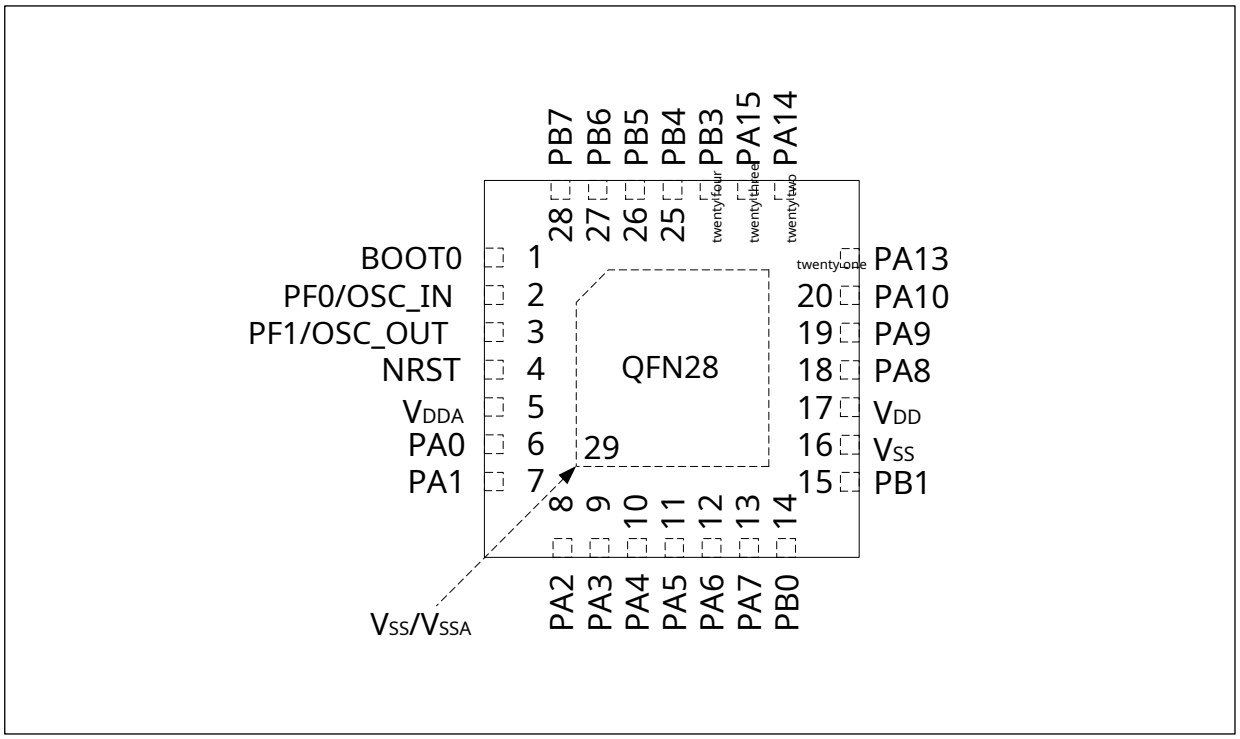
picture4. AT32F421seriesLQFP32pin distribution



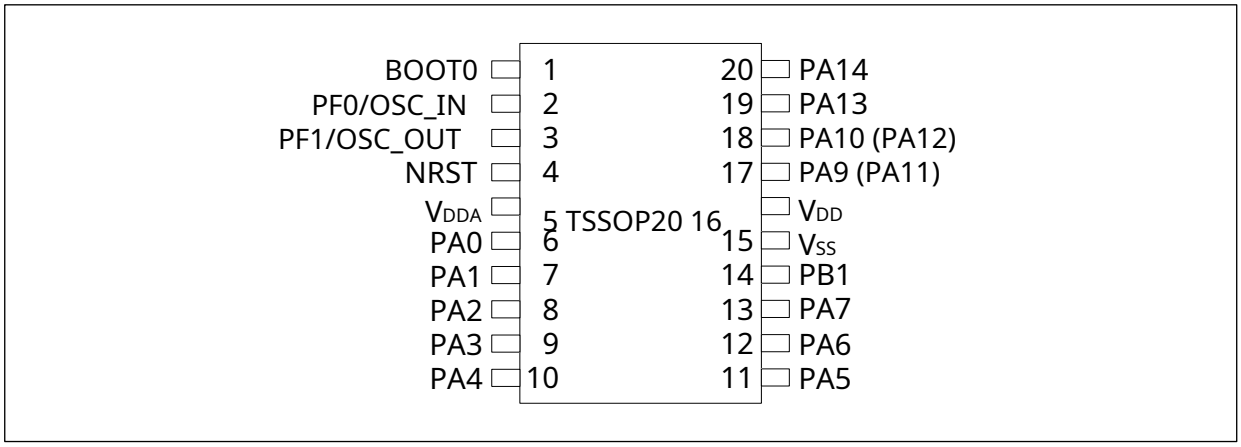
picture5. AT32F421seriesQFN32pin distribution



picture6. AT32F421seriesQFN28pin distribution



picture7. AT32F421seriesTSSOP20pin distribution



The table below isAT32F421Series pin definition, "-" indicates that there is no such pin under the corresponding package.

surface5. AT32F421Series pin definition

pin number					pin name (Function after reset)	pin type(1)	I/Ostructure(2)	multiplexing function	Additional features
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
- -	1 1	1			V_{DD}	S	-	digital power	
-	-	-	-	2	PC13	I/O	FT	-	TAMPER-RTC/WKUP2
-	-	-	-	3	PC14/OSC32_IN (PC14)	I/O	TC	-	OSC32_IN
-	-	-	-	4	PC15/OSC32_OUT (PC15)	I/O	TC	-	OSC32_OUT
2	2	2	2	5	PF0/OSC_IN (PF0)	I/O	TC	I2C1_SDA	OSC_IN
3	3	3	3	6	PF1 / OSC_OUT (PF1)	I/O	TC	I2C1_SCL	OSC_OUT
4	4	4	4	7	NRST	I/O	R	Device reset input/internal reset output (active low)	
-	-	-	-	8	V_{SSA}/V_{REF-}	S	-	Analog Ground / Negative Reference Voltage	
5	5	5	5	9	V_{DDA}/V_{REF+}	S	-	Analog Supply / Positive Reference Voltage	
6	6	6	6	10	PA0	I/O	FTa	TMR1_ETR / USART2_CTS / I2C2_SCL / COMP_OUT	ADC_IN0 / COMP_INP2 / COMP_INM6 / WKUP1
7	7	7	7	11	PA1	I/O	FTa	TMR15_CH1N/USART2_RTS/ I2C2_SDA / EVENTOUT	ADC_IN1 / COMP_INP1
8	8	8	8	12	PA2	I/O	FTa	TMR15_CH1 / USART2_TX	ADC_IN2 / COMP2_INM7
9	9	9	9	13	PA3	I/O	FTa	TMR15_CH2/USART2_RX/ I2S2_MCK	ADC_IN3
10	10	10	10	14	PA4	I/O	FTa	TMR14_CH1/USART2_CK/ SPI1_NSS / I2S1_WS	ADC_IN4/ COMP_INM4
11	11	11	11	15	PA5	I/O	FTa	SPI1_SCK / I2S1_CK	ADC_IN5 / COMP_INP0 / COMP_INM5
12	12	12	12	16	PA6	I/O	FTa	TMR1_BKIN/TMR3_CH1/ TMR16_CH1/SPI1_MISO/ I2S1_MCK / I2S2_MCK / COMP_OUT / EVENTOUT	ADC_IN6
13	13	13	13	17	PA7	I/O	FTa	TMR1_CH1N/TMR3_CH2/ TMR14_CH1/TMR17_CH1/ SPI1_MOSI/I2S1_SD/ EVENTOUT	ADC_IN7
-	14	14	14	18	PB0	I/O	FTa	TMR1_CH2N/TMR3_CH3/ USART2_RX/I2S1_MCK/ EVENTOUT	ADC_IN8
14	15	15	15	19	PB1	I/O	FTa	TMR1_CH3N/TMR3_CH4/ TMR14_CH1 / SPI2_SCK / I2S2_CK	ADC_IN9
-	-	16	-	20	PB2	I/O	FTa	TMR3_ETR	ADC_IN10

pin number					pin name (Function after reset)	pin type(1)	I/Ostructure(2)	multiplexing function	Additional features
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
-	-	-	twenty one		PB10	I/O	FT	SPI2_SCK/I2S2_CK/ I2C2_SCL	-
-	-	-	-	twenty two	PB11	I/O	FT	I2C2_SDA / EVENTOUT	-
15	16	-	16	twenty three	V_{SS}	S	-	digitally	
16	17	17	17	twenty four	V_{DD}	S	-	digital power	
-	-	-	-	25	PB12	I/O	FTa	TMR1_BKIN / TMR15_BKIN / SPI2_NSS / I2S2_WS / I2C2_SMBA / EVENTOUT	ADC_IN11
-	-	-	-	26	PB13	I/O	FTa	TMR1_CH1N / SPI2_SCK/I2S2_CK/ I2C2_SCL	ADC_IN12
-	-	-	-	27	PB14	I/O	FTa	TMR1_CH2N/TMR15_CH1/ SPI2_MISO/I2S2_MCK/ I2C2_SDA	ADC_IN13
-	-	-	-	28	PB15	I/O	FTa	TMR1_CH3N / TMR15_CH2/TMR15_CH1N/ SPI2_MOSI/I2S2_SD	ADC_IN14 / RTC_REFIN / WKUP7
-	18	18	18	29	PA8	I/O	FT	TMR1_CH1 / USART1_CK / UART2_TX / I2C2_SCL / CLKOUT / EVENTOUT	-
17	19	19	19	30	PA9	I/O	FT	TMR1_CH2/TMR15_BKIN/ USART1_TX / I2C1_SCL/I2C2_SMBA/ CLKOUT	-
18	20	20	20	31	PA10	I/O	FT	TMR1_CH3 / TMR17_BKIN / USART1_RX / I2C1_SDA	-
17(3)	-(4)	twenty one	twenty one	32	PA11	I/O	FT	TMR1_CH4/USART1_CTS/ I2C1_SMBA / I2C2_SCL / COMP_OUT / EVENTOUT	-
18(3)	-(4)	twenty two	twenty two	33	PA12	I/O	FT	TMR1_ETR / USART1_RTS / I2C2_SDA / EVENTOUT	-
19	twenty one	twenty three	twenty three	34	PA13 (SWDIO(5))	I/O	FT	PA13/IR_OUT/ SPI2_MISO/I2S2_MCK	-
-	-	-	-	35	PF6	I/O	FT	I2C2_SCL	-
-	-	-	-	36	PF7	I/O	FT	I2C2_SDA	-
20	twenty two	twenty four	twenty four	37	PA14 (SWCLK(5))	I/O	FT	PA14/USART2_TX/ SPI2_MOSI/I2S2_SD	-
-	twenty three	25	25	38	PA15	I/O	FT	USART2_RX / SPI1_NSS/I2S1_WS/ SPI2_NSS/I2S2_WS/ EVENTOUT	-
-	twenty four	26	26	39	PB3	I/O	FT	SPI1_SCK / I2S1_CK / SPI2_SCK / I2S2_CK / EVENTOUT	-
-	25	27	27	40	PB4	I/O	FT	TMR3_CH1/TMR17_BKIN/ SPI1_MISO / I2S1_MCK / SPI2_MISO / I2S2_MCK / I2C2_SDA / EVENTOUT	-

pin number					pin name (Function after reset)	pin type(1)	I/Ostructure(2)	multiplexing function	Additional features
TSSOP20	QFN28	QFN32	LQFP32	LQFP48					
-	26	28	28	41	PB5	I/O	FT	TMR3_CH2/TMR16_BKIN/ SPI1_MOSI/I2S1_SD/ SPI2_MOSI/I2S2_SD/ I2C1_SMBA	WKUP6
-	27	29	29	42	PB6	I/O	FT	TMR16_CH1N/USART1_TX/ I2S1_MCK / I2C1_SCL	-
-	28	30	30	43	PB7	I/O	FT	TMR17_CH1N/USART1_RX/ I2C1_SDA	-
1	1	31	31	44	BOOT0	I	B	Boot mode selection0	
-	-	32	-	45	PB8	I/O	FT	TMR16_CH1/I2C1_SCL	
-	-	-	-	46	PB9	I/O	FT	TMR17_CH1/IR_OUT/ SPI2_NSS/I2S2_WS/ I2S1_MCK/I2C1_SDA/ EVENTOUT	
-	-	-	32	47	V_{SS}	S	-	digitally	
-	-	-	-	48	V_{DD}	S	-	digital power	
-	29	33	-	-	EPAD (V_{SS}/V_{SSA})	S	-	Digital Ground/ Analog Ground	

(1) I =enter,O =output,S =power supply.

(2) TC =standard level,FT =generally5Vlevel tolerance,FTa =with analog function5Vlevel tolerance,R =Bidirectional reset pin with built-in weak pull-up resistor,B = Dedicated with built-in weak pull-down resistorBOOT0pin.FTaWhen the pin is set as input floating, input pull-up, or input pull-down, it has5VLevel tolerance; when set to analog mode, no5V Level tolerance characteristics, at this time the input level must be less thanVDD + 0.3V.

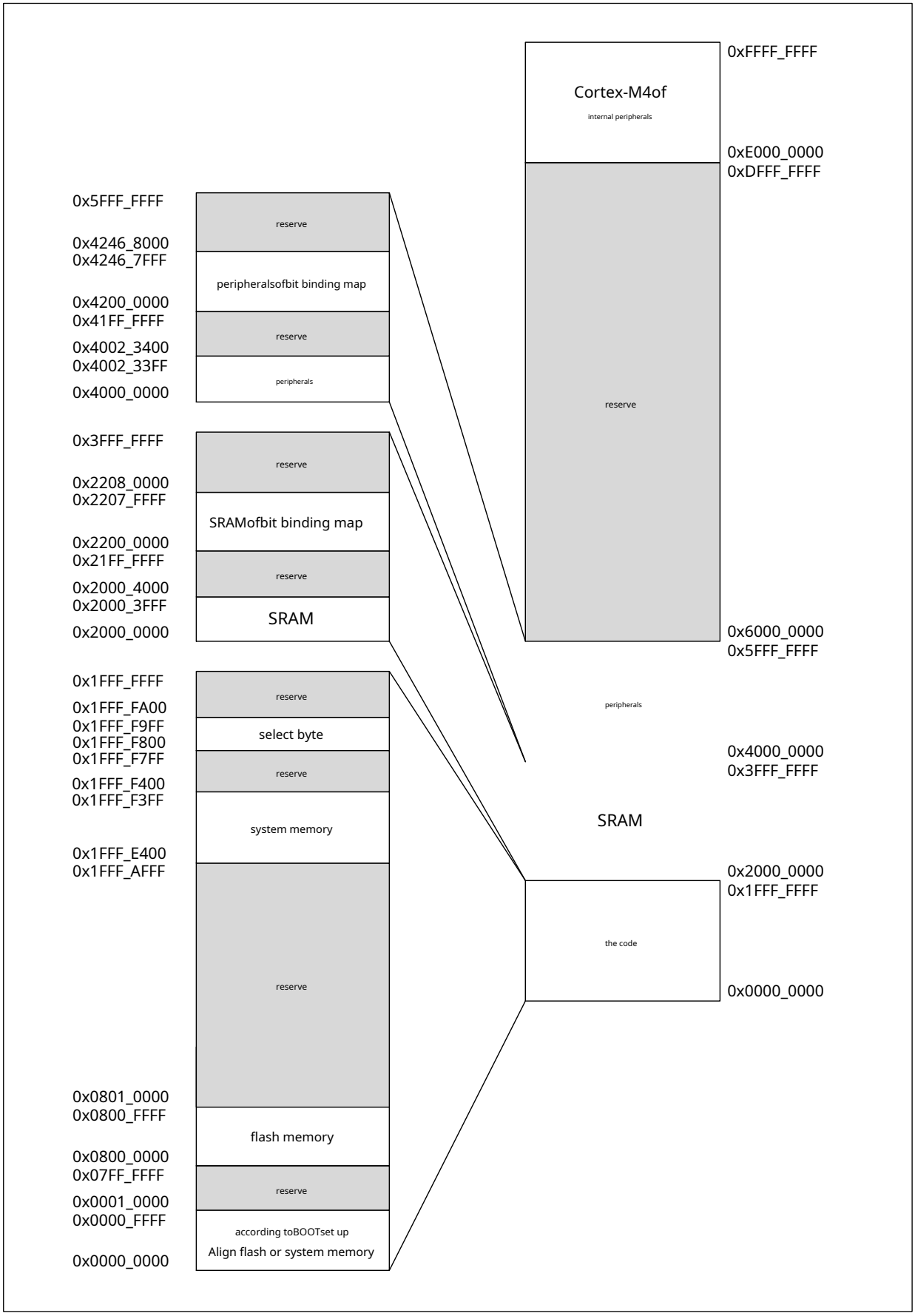
(3)existTSSOP20Package supportPA11/PA12and its multiplexing functions replace the original through software remappingPA9/PA10and its reuse function.

(4)existQFN28package, even ifPA11andPA12Not available on the package, they should be treated as unused pins. Hardware will not force them to a fixed level, it is recommended that software set them to a fixed level or analog mode to prevent leakage.

(5)After reset,PA13/PA14pins are configured as alternate functionSWDIO/SWCLK,at this timeSWDIOpins with internal pull-up resistors andSWCLKThe pin's internal pull-down resistor is turned on.

5 memory image

picture8.memory map



6 electrical characteristics

6.1 Test Conditions

Unless otherwise specified, all voltages are inV_{SS}as the benchmark.

6.1.1Minimum and maximum values

Unless otherwise specified, in the production line at ambient temperatureT_A= 25°CandT_A= $T_a$maxTests performed under ($T_a$maxmatch the selected temperature range), all minimum and maximum values are guaranteed under worst-case ambient temperature, supply voltage, and clock frequency conditions.

Notes below each table represent data obtained through comprehensive evaluation, design simulations, and/or process characterization and will not be tested in production line.

6.1.2typical value

Unless otherwise stated, typical data are based onT_A= 25°CandV_{DD}= 3.3V. These data are for design guidance only and not tested.

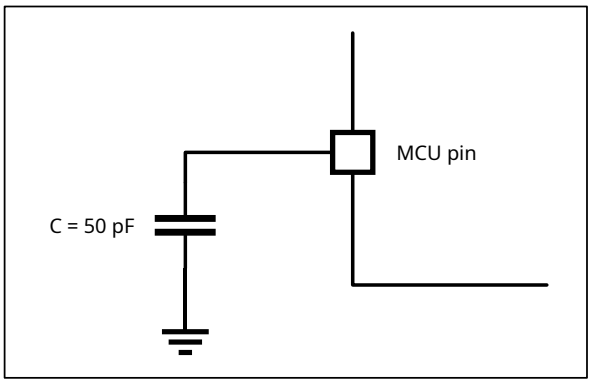
6.1.3typical curve

Unless otherwise stated, typical curves are for design guidance only and are not tested.

6.1.4load capacitance

The load conditions when measuring pin parameters are shown in*picture9*middle.

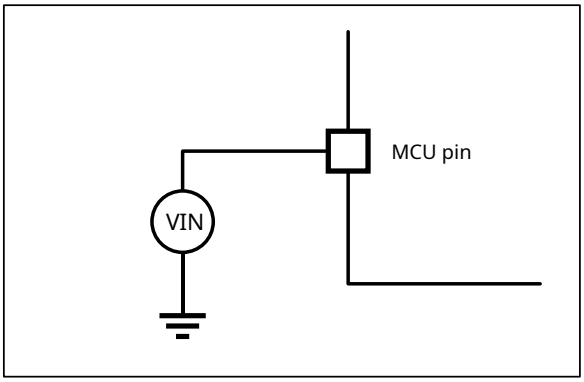
picture9.The load condition of the pin



6.1.5pin input voltage

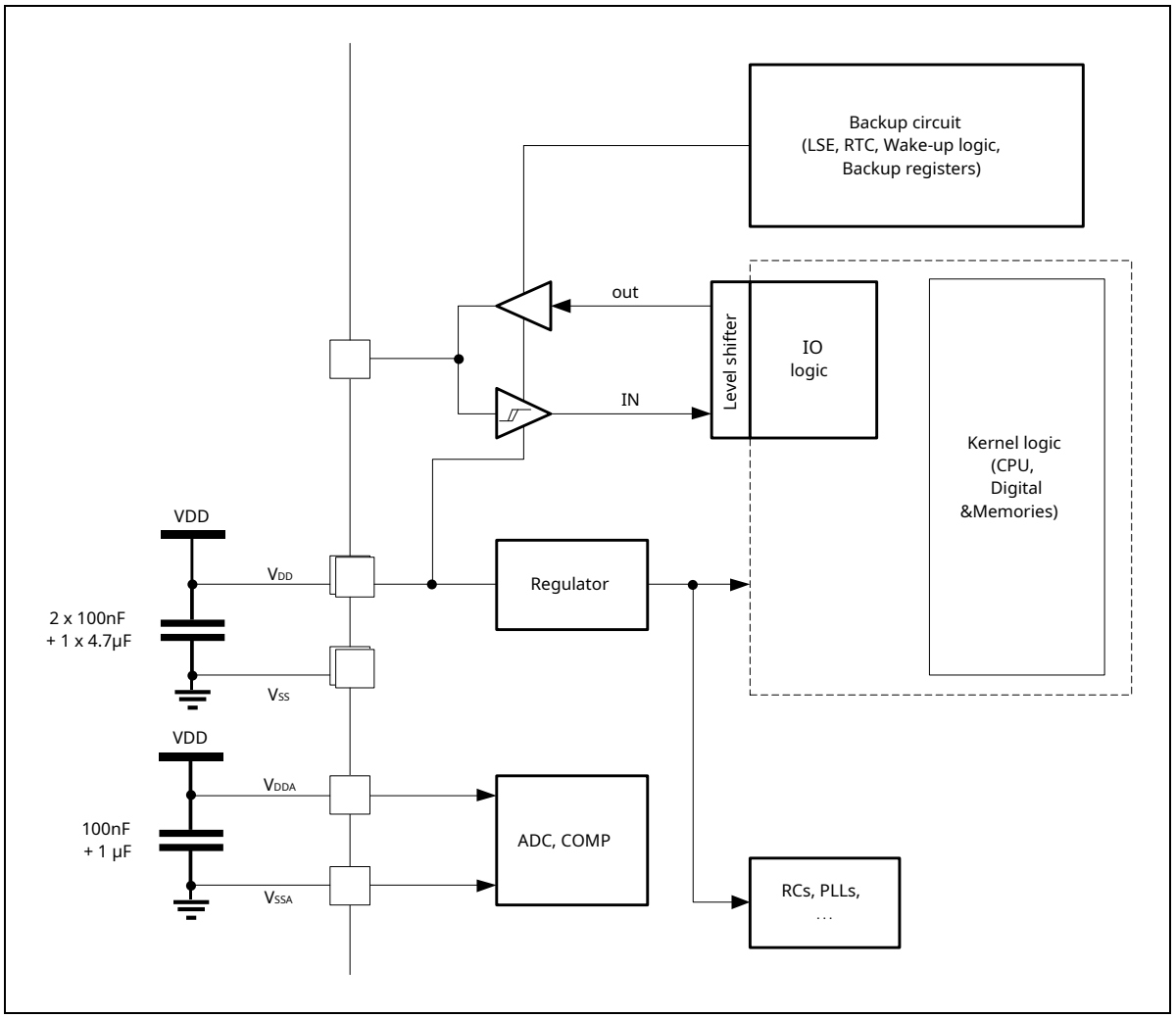
The input voltage at the pin is measured as shown in the*picture10*middle.

picture10.pin input voltage



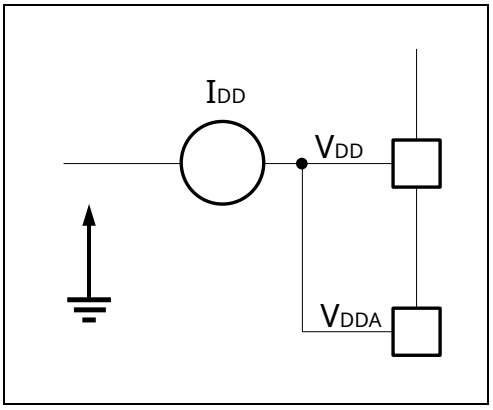
6.1.6Power supply scheme

picture11.Power supply scheme



6.1.7Current consumption measurement

picture12.Current Consumption Measurement Solution



6.2 Absolute Maximum Ratings

Loads applied to the device in excess of those listed in the "Absolute Maximum Ratings" (*surface6*,*surface7*,*surface8*), may cause permanent damage to the device. The maximum load that can be tolerated here is only given, and it does not mean that the functional operation of the device under this condition is correct. The long-term operation of the device under the maximum value will affect the reliability of the device.

surface6.Voltage characteristics

symbol	describe	minimum value	maximum value	unit
V_{DD}-V_{SS}	External mains supply voltage (includesV_{DDA}andV_{DD})(1)	- 0.3	4.0	V
V_{IN}	existFTThe input voltage on the pin	V_{SS}-0.3	6.0	
	existFTaThe input voltage on the pin, the pin is set to input floating, input pull-up, or input pull-down mode			
	existTCThe input voltage on the pin	V_{SS}-0.3	4.0	
	existFTaThe input voltage on the pin, the pin is set to analog mode			
$\lvert\Delta V_{DDx}\rvert$	Voltage difference between different supply pins	-	50	mV
$\lvert V_{SSx}$-$V_{SS}\rvert$	The voltage difference between different ground pins	-	50	

(1)All power supplies (V_{DD},V_{DDA}) and land (V_{SS},V_{SSA}) pins must always be connected to an external power supply within the allowable range.

surface7.Current characteristics

symbol	describe	maximum value	unit
I_{VDD}	External mains supply voltage (includesV_{DDA}andV_{DD})(1)	150	mA
I_{VSS}	go throughV_{SS}The total current of the ground wire (outgoing current)(1)	150	
I_{IO}	arbitrarilyI/Oand the output sink current on the CONTROL pin	25	
	arbitrarilyI/Oand the output current on the CONTROL pin	- 25	

(1)All power supplies (V_{DD},V_{DDA}) and land (V_{SS},V_{SSA}) pins must always be connected to an external power supply within the allowable range.

surface8.temperature characteristics

symbol	describe	value	unit
T_{STG}	storage temperature range	- 60 ~ +150	°C
T_J	maximum junction temperature	125	

6.3 working conditions

6.3.1general working conditions

surface9.general working conditions

symbol	parameter	condition	minimum value	maximum value	unit
f_{HCLK}	internalAHBClock frequency	-	0	120	MHz
f_{PCLK1}	internalAPB1Clock frequency	-	0	120	MHz
f_{PCLK2}	internalAPB2Clock frequency	-	0	120	MHz
V_{DD}	Standard working voltage	-	2.4	3.6	V
V_{DDA}(1)	Analog part operating voltage	must be withV_{DD}(1)same	2.4	3.6	V
$P_{D.}$	Power Dissipation:T_A= 105°C	LQFP48 (7 x 7 mm)	-	230	mW
		LQFP32 (7 x 7mm)	-	243	
		QFN32 (5x5mm)	-	503	
		QFN32 (4x4mm)	-	446	
		QFN28 (4x4mm)	-	446	
		TSSOP20 (6.5 x 4.4mm)	-	194	
T_A	ambient temperature	-	- 40	105	°C

(1)It is recommended to use the same power supply asV_{DD}andV_{DDA}power supply, during power-up and normal operation, theV_{DD}andV_{DDA}A maximum of300mVdifference.

6.3.2Operating Conditions During Power-Up and Power-Down

The parameters given in the table below are based on*surface9*Tested at ambient temperature listed.

surface10.Operating Conditions During Power-Up and Power-Down

symbol	parameter	condition	minimum value	maximum value	unit
t_{VDD}	V_{DD}rate of ascent	-	0	∞	ms/V
	V_{DD}rate of descent		20	∞	μs/V

6.3.3Built-in reset and power control block features

The parameters given in the table below are based on*surface9*listed ambient temperature andV_{DD}Tested under supply voltage.

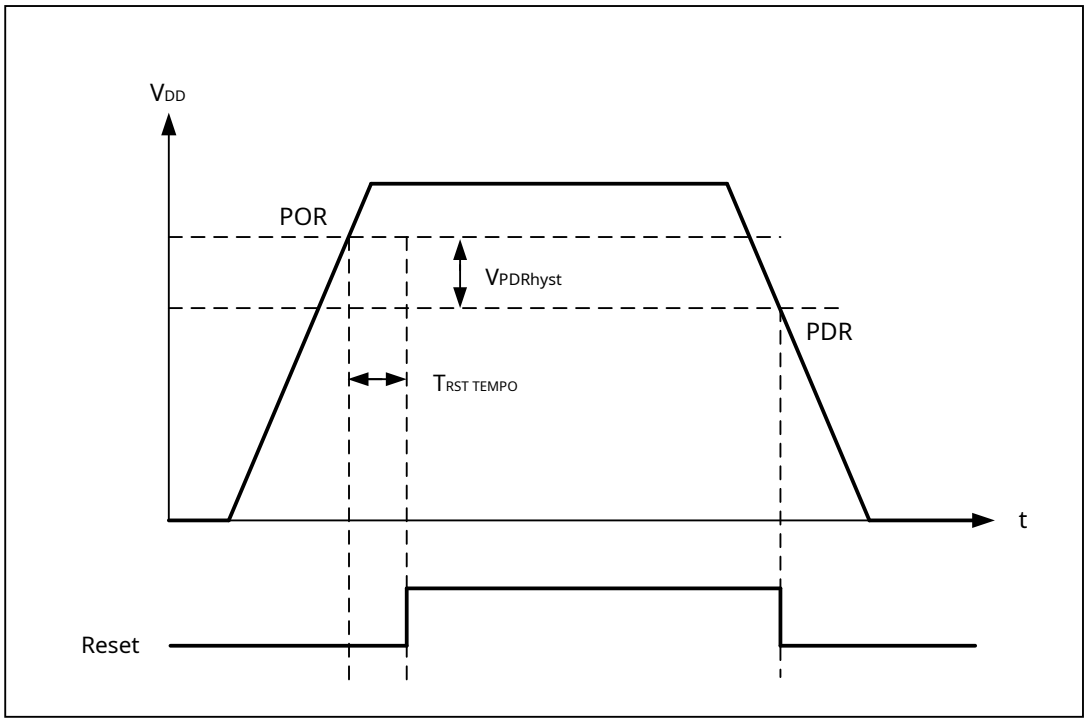
surface11.Embedded Reset and Power Control Block Features

symbol	parameter	condition	minimum value	typical value	maximum value	unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	falling edge	1.62(1)	1.88	2.16(2)	V
		rising edge	1.73(2)	2.06	2.4	V
$V_{PDRhyst}$ (2)	PDRhysteresis	-	-	180	-	mV
$T_{RST TEMPO}$(2)	Reset duration:V_{DD}higher than$V_{POR}$and lasts longer than$T_{RST TEMPO}$backCPUstart operation	-	-	4.5	-	ms

(1)The characteristics of the product are guaranteed by design to the minimum value$V_{POR/PDR}$.

(2)Guaranteed by design, not tested in production.

picture13.Waveform diagram of power-on reset and power-off reset



surface12.Programmable Voltage Detector Features

symbol	parameter	condition	minimum value	typical value	maximum value	unit
V_{PVD1}	PVDthreshold1(PLS[2:0] = 001)	rising edge(1)	2.19	2.28	2.37	V
		falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVDthreshold2(PLS[2:0] = 010)	rising edge	2.28	2.38	2.48	V
		falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVDthreshold3(PLS[2:0] = 011)	rising edge	2.38	2.48	2.58	V
		falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVDthreshold4(PLS[2:0] = 100)	rising edge	2.47	2.58	2.69	V
		falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVDthreshold5(PLS[2:0] = 101)	rising edge	2.57	2.68	2.79	V
		falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVDthreshold6(PLS[2:0] = 110)	rising edge	2.66	2.78	2.9	V
		falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVDthreshold7(PLS[2:0] = 111)	rising edge	2.76	2.88	3	V
		falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$ (2)	PVDhysteresis	-	-	100	-	mV
I_{DD} (PVD)	PVDcurrent consumption	-	-	20	30(2)	μA

(1) PLS[2:0] = 001level may be lower than theV_{PDR}not available.

(2)Guaranteed by design, not tested in production.

6.3.4Built-in reference voltage

The parameters given in the table below are based on*surface9*listed ambient temperature andV_{DD}Tested under supply voltage.

surface13.Built-in reference voltage

symbol	parameter	condition	minimum value	typical value	maximum value	unit
V_{REFINT}	Built-in reference voltage	-	1.17	1.20	1.23	V
$T_{S\_vrefint}$ (1)	When reading the internal reference voltage,ADCThe sampling time of	-	-	5.1	17.1(2)	μs
T_{Coeff} (2)	Temperature Coefficient	-	- 120	-	120	ppm/°C

(1)The shortest sample time is obtained by looping through the application multiple times.

(2)Guaranteed by design, not tested in production.

6.3.5Supply Current Characteristics

Current consumption is a composite indicator of various parameters and factors, including operating voltage, ambient temperature,I/Opin loading, product software configuration, operating frequency,I/OThe flip rate of the foot, and the code executed, etc.

For the description of the measurement method of current consumption, see*picture12*.

Typical Current Consumption

The microcontroller is subjected to the following conditions:

- allI/Opins are in analog mode.
- Flash memory access time varies withf_{HCLK}frequency adjustment (0 ~ 32MHzwhen0waiting period,33 ~ 64MHzwhen1 waiting period,65 ~ 96MHzwhen2waiting period, more than96 MHzwhen3waiting period).
- The instruction prefetch function is enabled (reminder: this parameter must be set before setting the clock and bus frequency division).
- ambient temperature andV_{DD}The supply voltage complies with*surface9*.
- f_{PCLK1}= f_{HCLK},f_{PCLK2}= f_{HCLK},f_{ADCCLK}= f_{PCLK2}/8.

surface14.Typical current consumption in run mode

symbol	parameter	condition	f_{HCLK}	typical value(1)		unit
				Enable all peripherals	turn off all peripherals	
I_{DD}	in run mode supply current	external clock(2)	120 MHz	16.7	11.3	mA
			108MHz	15.2	10.3	
			72MHz	10.5	7.19	
			48MHz	7.62	5.44	
			36 MHz	5.98	4.34	
			24 MHz	4.65	3.54	
			16 MHz	3.45	2.71	
			8 MHz	1.96	1.57	
			4 MHz	1.50	1.30	
			2 MHz	1.27	1.16	
			1 MHz	1.16	1.10	
			500 kHz	1.10	1.07	
			125 kHz	1.06	1.04	
		run at high speed insideRCoscillator (HSI)	120 MHz	16.7	11.3	mA
			108MHz	15.1	10.3	
			72MHz	10.4	7.14	
			48MHz	7.52	5.38	
			36 MHz	5.88	4.27	
			24 MHz	4.53	3.47	
			16 MHz	3.34	2.63	
			8 MHz	1.83	1.48	
			4 MHz	1.37	1.20	
			2 MHz	1.15	1.06	
			1 MHz	1.03	0.99	
			500 kHz	0.97	0.95	
			125 kHz	0.93	0.93	

(1)Typical values are inT_A= 25°C,V_{DD}= 3.3VWhen the test is obtained.

(2)The external clock is8 MHz,whenf_{HCLK}> 8 MHzenabled whenPLLs.

surface15.Typical current consumption in sleep mode

symbol	parameter	condition	f_{HCLK}	typical value(1)		unit
				Enable all peripherals	turn off all peripherals	
I_{DD}	in sleep mode supply current	external clock(2)	120 MHz	12.2	4.99	mA
			108MHz	11.1	4.59	
			72MHz	7.76	3.38	
			48MHz	5.81	2.89	
			36 MHz	4.60	2.42	
			24 MHz	3.70	2.25	
			16 MHz	2.80	1.83	
			8 MHz	1.60	1.11	
			4 MHz	1.30	1.05	
			2 MHz	1.15	1.02	
			1 MHz	1.07	1.00	
			500 kHz	1.03	0.99	
			125 kHz	1.00	0.98	
		run at high speed insideRCoscillator (HSI)	120 MHz	12.1	4.88	mA
			108MHz	11.0	4.47	
			72MHz	7.65	3.27	
			48MHz	5.70	2.78	
			36 MHz	4.49	2.30	
			24 MHz	3.59	2.13	
			16 MHz	2.68	1.71	
			8 MHz	1.47	0.98	
			4 MHz	1.17	0.93	
			2 MHz	1.02	0.89	
			1 MHz	0.94	0.88	
			500 kHz	0.90	0.87	
			125 kHz	0.87	0.86	

(1)Typical values are inT_A= 25°C,V_{DD}= 3.3VWhen the test is obtained.

(2)The external clock is8 MHz,whenf_{HCLK}> 8 MHzenabled whenPLLs.

Maximum current consumption

The microcontroller is subjected to the following conditions:

- allI/Opins are in analog mode.
- Flash memory access time varies withf_{HCLK}frequency adjustment (0 ~ 32MHzwhen0waiting period,33 ~ 64MHzwhen1 waiting period,65 ~ 96MHzwhen2waiting period, more than96 MHzwhen3waiting period).
- The instruction prefetch function is enabled (reminder: this parameter must be set before setting the clock and bus frequency division) .
- When turning on a peripheral:f_{PCLK1}= f_{HCLK},f_{PCLK2}= f_{HCLK},f_{ADCCLK}= f_{PCLK2}/8.

*surface16*and*surface17*The parameters given are at ambient temperature andV_{DD}The supply voltage complies with*surface9*The conditional test is obtained.

surface16.Maximum current consumption in run mode

symbol	parameter	condition	f_{HCLK}	maximum value(1)		unit
				T_A= 85°C	T_A= 105°C	
I_{DD}	Supply current in run mode	external clock(2)Enable all peripherals	120 MHz	18.9	20.7	mA
			108MHz	17.3	19.1	
			72MHz	12.6	14.4	
			48MHz	9.69	11.5	
			36 MHz	8.04	9.81	
			24 MHz	6.69	8.45	
			16 MHz	5.49	7.24	
			8 MHz	3.99	5.73	
		external clock(2)turn off all peripherals	120 MHz	13.5	15.2	mA
			108MHz	12.4	14.2	
			72MHz	9.29	11.0	
			48MHz	7.52	9.26	
			36 MHz	6.41	8.14	
			24 MHz	5.60	7.33	
			16 MHz	4.76	6.49	
			8 MHz	3.61	5.35	

(1)Derived from comprehensive evaluation, not tested in production.

(2)The external clock is8 MHz,whenf_{HCLK}> 8 MHzenabled whenPLLs.

surface17.Maximum Current Consumption in Sleep Mode

symbol	parameter	condition	f_{HCLK}	maximum value(1)		unit
				T_A= 85°C	T_A= 105°C	
I_{DD}	Supply Current in Sleep Mode	external clock(2)Enable all peripherals	120 MHz	14.4	16.1	mA
			108MHz	13.3	15.0	
			72MHz	9.85	11.6	
			48MHz	7.89	9.58	
			36 MHz	6.69	8.36	
			24 MHz	5.79	7.45	
			16 MHz	4.88	6.53	
			8 MHz	3.68	5.31	
		external clock(2)turn off all peripherals	120 MHz	7.06	8.70	mA
			108MHz	6.66	8.30	
			72MHz	5.45	7.09	
			48MHz	4.96	6.57	
			36 MHz	4.48	6.12	
			24 MHz	4.31	5.93	
			16 MHz	3.89	5.53	
			8 MHz	3.18	4.81	

(1)Derived from comprehensive evaluation, not tested in production.

(2)The external clock is8 MHz,whenf_{HCLK}> 8 MHzenabled whenPLLs.

surface18.Typical and Maximum Current Consumption in Shutdown and Standby Modes

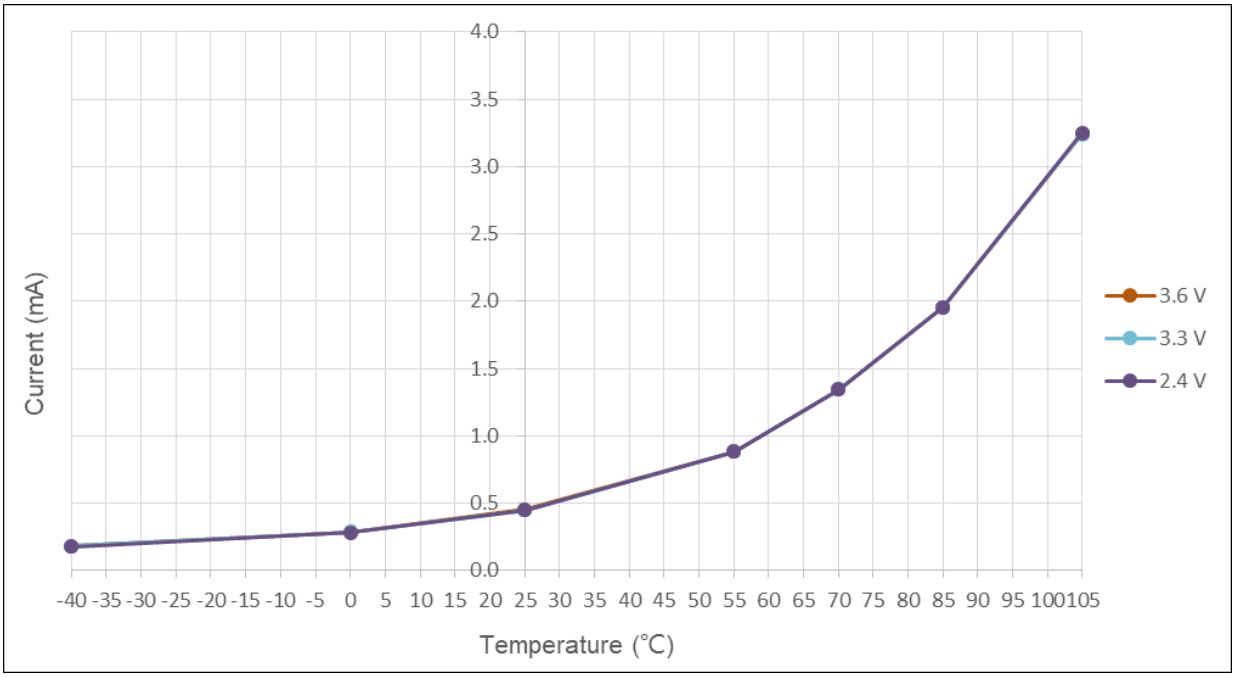
symbol	parameter	condition	typical value(1)		maximum value(2)		unit
			V_{DD}= 2.4V	V_{DD}= 3.3V	T_A= 85°C	T_A= 105°C	
I_{DD}	in stop mode supply current (3)	regulator is in run mode, the high-speed internal RCoscillators and high-speed external oscillators at in shutdown state (no independent watchdog)	445	450	4100	6750	μA
		The regulator is in low power mode and the LPDS1Set as1, high-speed internalRC Oscillator and High Speed External Oscillator are off Closed state (no independent watchdog)	205	210	2000	3315	
	in standby mode supply current	low speed external oscillator andRTCis off state	2.4	3.6	5.9	7.6	μA
		low speed external oscillator andRTCis on state	3.2	5.1	7.2	9.2	

(1)Typical values are inT_A= 25°CThe next test is obtained.

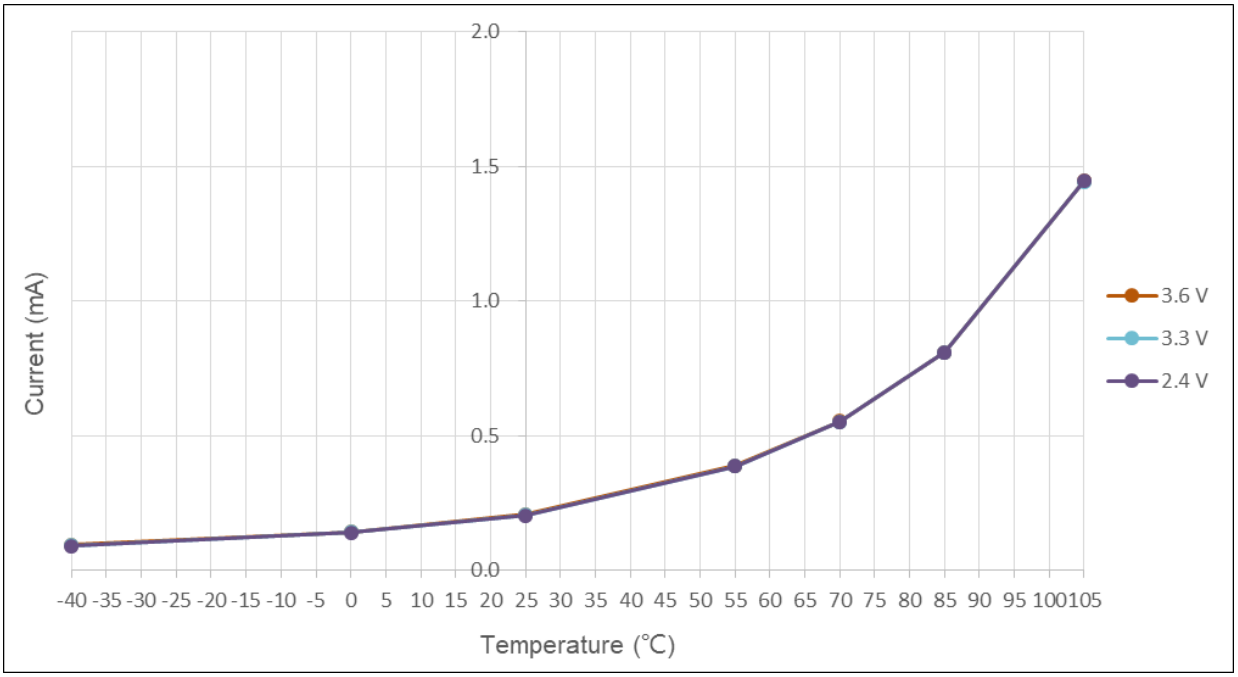
(2)Derived from comprehensive evaluation, not tested in production.

(3)Before entering stop modeRCC_AHBEN[4] (FLASHEN)must be set to1, otherwise the typical value will generate an additional approx.50μApower consumption.

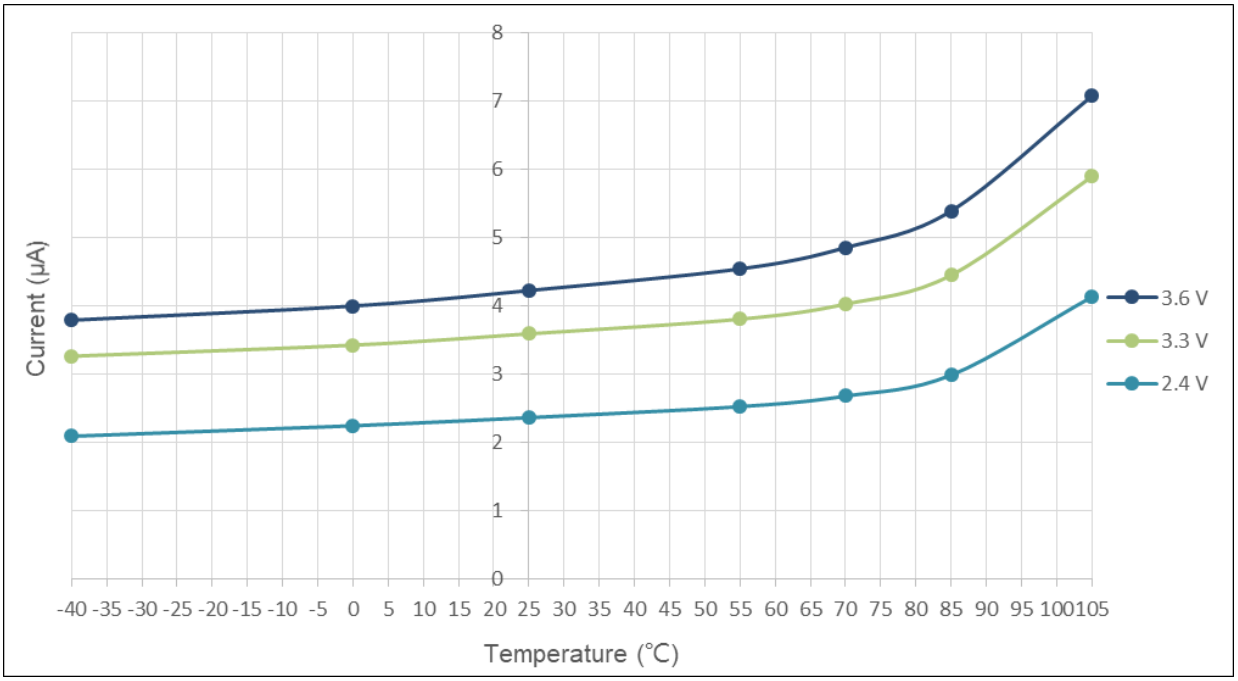
picture14.When the regulator is in run mode, the typical current consumption in stop mode varies betweenV_{DD}time versus temperature



picture15.When the regulator is in low-power mode, the typical current consumption in shutdown mode varies betweenV_{DD}time versus temperature



picture16.Typical current consumption in standby mode at differentV_{DD}time versus temperature



Built-in Peripheral Current Consumption

The current consumption of the built-in peripherals is listed in*surface19*, the operating conditions of the microcontroller are as follows:

- allI/Opins are in analog mode.
- All peripherals are turned off unless otherwise noted.
- The values given are calculated by measuring the current consumption
  - Turn off clocks to all peripherals
  - Turn on the clock of only one peripheral
- ambient temperature andV_{DD}The supply voltage conditions are listed in the*surface9*.

surface19.Current Consumption of Built-in Peripherals

built-in peripherals		typical value	unit
AHB(up to120 MHz)	DMA1	2.15	μA/MHz
	SRAM	1.06	
	Flash	12.08	
	GPIOA	0.50	
	GPIOB	0.50	
	GPIOC	0.50	
	GPIOF	0.50	
	CRC	0.70	
APB1(up to120 MHz)	TMR3	6.29	
	TMR6	0.49	
	TMR14	2.28	
	SPI2/I^2S2	2.26	
	USART2	2.11	
	I^2C1	1.71	
	I^2C2	1.68	
	WWDG	0.20	
	PWR	0.39	
APB2(up to120 MHz)	SYSCFG/COMP	0.29	
	SPI1/I^2S1	2.03	
	USART1	2.12	
	TMR1	7.68	
	TMR15	4.65	
	TMR16	3.19	
	TMR17	3.41	
	ADC1	5.17	
	ACC	0.95	

6.3.6External Clock Source Characteristics

High-speed external user clock generated by external oscillator source

In bypass mode,HSEOscillator off, input pins are standardGPIOs.

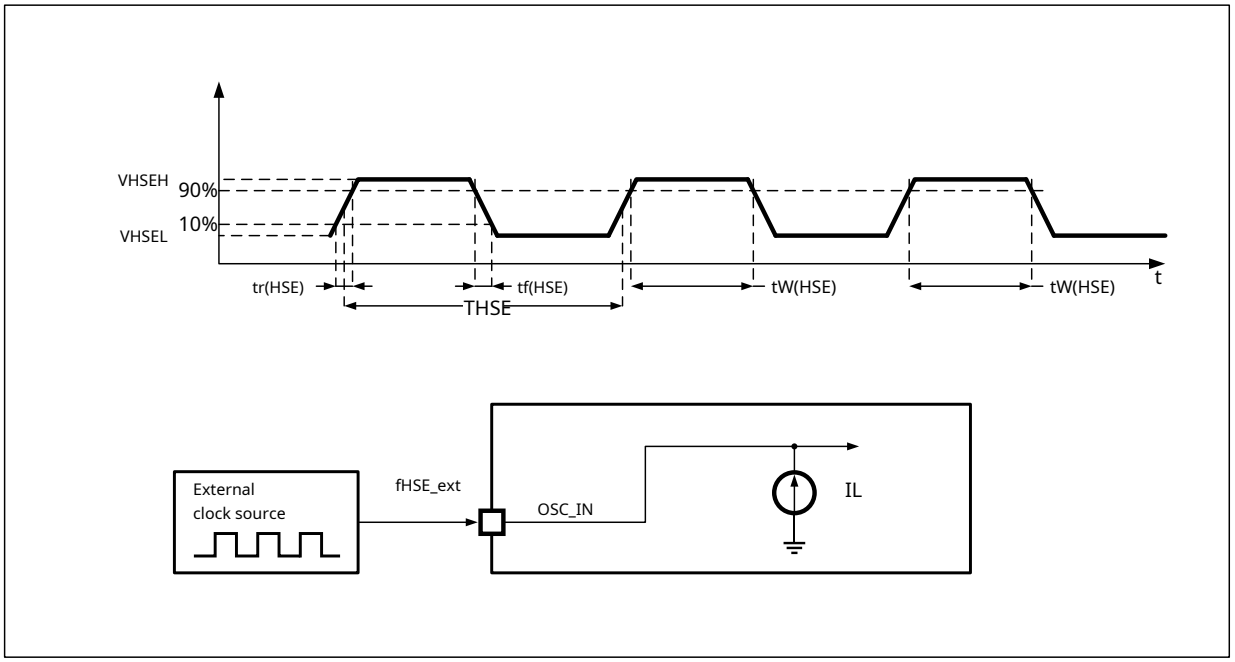
The external clock signal must take into account the first*6.3.13*In the chapterI/Ocharacteristic. However, the suggested clock input waveform is shown in*picture17*middle.

surface20.High-Speed External User Clock Features

symbol	parameter(1)	condition	minimum value	typical value	maximum value	unit
f_{HSE_ext}	User external clock frequency	-	1	8	25	MHz
V_{HSEH}	OSC_INInput pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_INInput pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_INhigh or low time		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_INrise or fall time		-	-	20	
$DuCy_{(HSE)}$	duty cycle	-	45	-	55	%
I_L	OSC_ININput leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1)Guaranteed by design, not tested in production.

picture17.AC Timing Diagram for External High Speed Clock Source



Low-speed external user clock from external oscillator source

In bypass mode,LSEOscillator off, input pins are standardGPIOs.

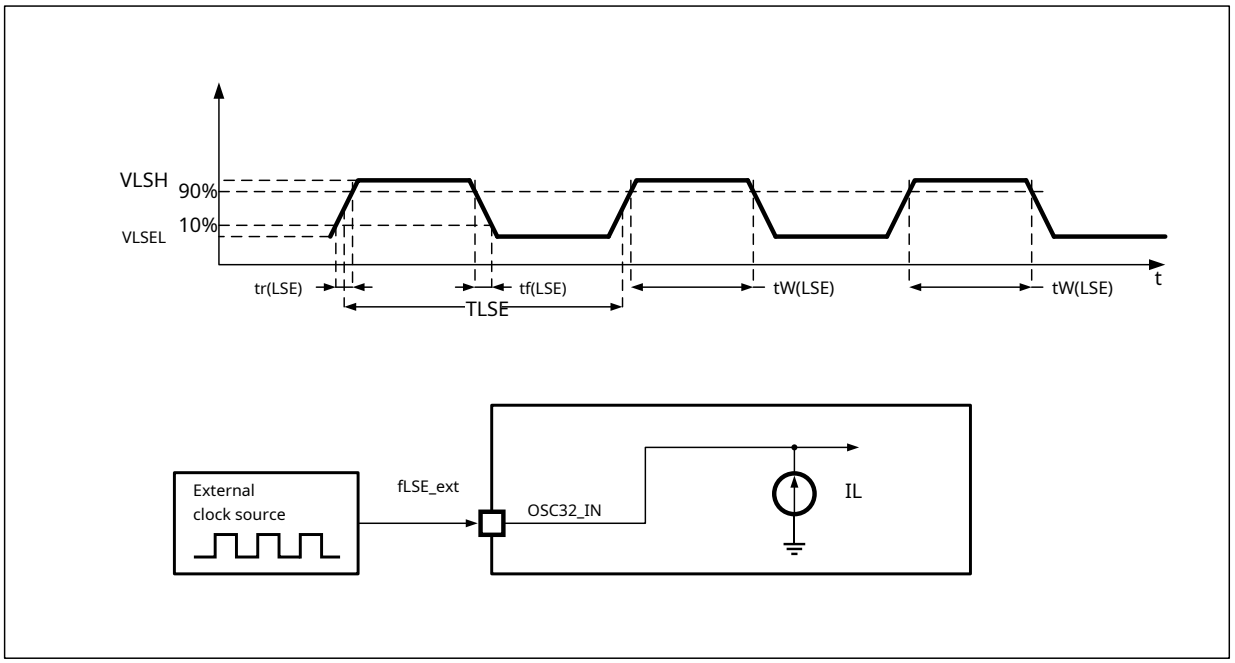
The external clock signal must take into account the first*6.3.13*In the chapterI/Ocharacteristic. However, the suggested clock input waveform is shown in*picture18*middle.

surfacetwenty one.Low-Speed External User Clock Characteristics

symbol	parameter(1)	condition	minimum value	typical value	maximum value	unit
f_{LSE_ext}	User external clock frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_INInput pin high level voltage	-	0.7V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_INInput pin low level voltage	-	V_{SS}	-	0.3V_{DD}	V
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_INhigh or low time	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_INrise or fall time	-	-	-	50	ns
$DuCy_{(LSE)}$	duty cycle	-	30	-	70	%
I_L	OSC32_ININput leakage current	$V_{SS}\leq V_{IN}\leq V_{DD}$	-	-	±1	μA

(1)Guaranteed by design, not tested in production.

picture18.AC Timing Diagram for External Low Speed Clock Source



High-speed external clock from crystal/ceramic resonator

High speed external clock (HSE) can use a4~25MHzOscillators constructed from crystal/ceramic resonators are produced. The information given in this section is based on comprehensive characterization results using typical external components listed in the table below. In the application, the resonator and load capacitors must be placed as close as possible to the pins of the oscillator to minimize output distortion and settling time during start-up. For detailed parameters (frequency, package, accuracy, etc.) of crystal resonators, please consult the corresponding manufacturers.

surface22. HSE 4~25 MHzOscillator Characteristics(1)(2)

symbol	parameter	condition	minimum value	typical value	maximum value	unit
f_{OSC_IN}	oscillator frequency	-	4	8	25	MHz
$t_{SU(HSE)}$ (3)	Start Time	$V_{DD}$is stable	-	2	-	ms

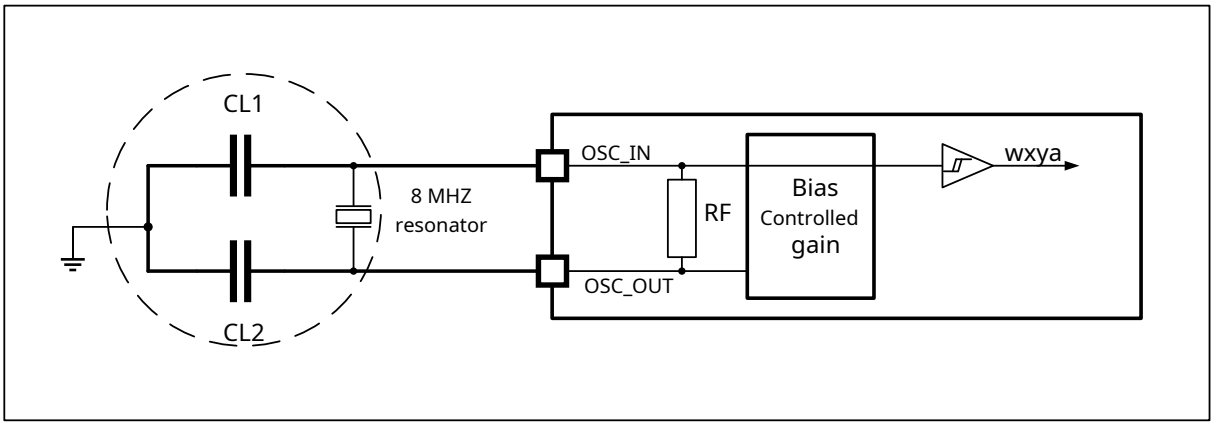
(1)The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2)Derived from comprehensive evaluation, not tested in production.

(3) $t_{SU(HSE)}$is the start-up time and is the slave software enableHSEstart measuring until a stable8 MHzOscillate this time. This value is measured on a standard crystal resonator and may vary widely depending on the crystal manufacturer.

forC_{L1}andC_{L2}, it is recommended to use a high-quality, designed for high-frequency applications (typical value)5pF~25pFBetween the ceramic capacitors, and select a crystal or resonator that meets the requirements. usuallyC_{L1}andC_{L2}have the same parameters. Crystal manufacturers usually start withC_{L1}andC_{L2}The serial combination of gives the parameters of the load capacitance. in selectionC_{L1}andC_{L2}hour,PCBandMCUThe capacitive reactance of the pin should be taken into account (you can roughly compare the pin with thePCBboard capacitance by10pFestimate).

picture19.use8MHzTypical Applications of Crystals



Low-speed external clock generated by crystal oscillator

Low Speed External Clock (LSE) can use a32.768 kHzOscillators composed of crystal oscillators are generated. The information given in this section is based on comprehensive characterization results using typical external components listed in the table below. In the application, the crystal and load capacitors must be placed as close as possible to the pins of the crystal to minimize output distortion and settling time at start-up. For detailed parameters of the crystal oscillator (frequency, package, precision, etc.), please consult the corresponding manufacturer.

surface23. LSEOscillator Characteristics (f_{LSE}= 32.768 kHz)(1)(2)

symbol	parameter	condition	minimum value	typical value	maximum value	unit
$t_{SU(LSE)}$	Start Time	$V_{DD}$is stable	-	180	-	ms

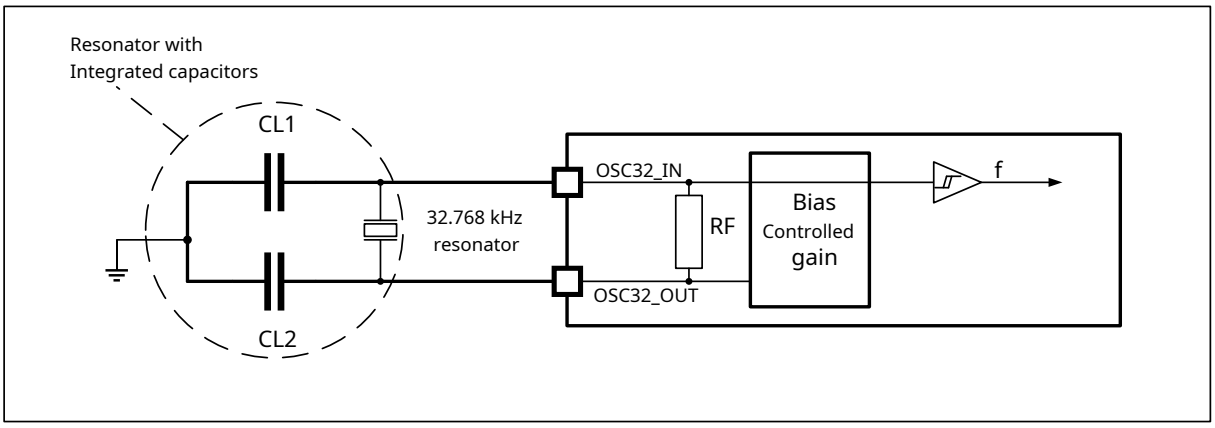
(1)The characteristic parameters of the resonator are given by the crystal manufacturer.

(2)Derived from comprehensive evaluation, not tested in production.

forC_{L1}andC_{L2}, it is recommended to use high quality5pF~15pFBetween the ceramic capacitors, and select a crystal or resonator that meets the requirements. usuallyC_{L1}andC_{L2}have the same parameters. Crystal manufacturers usually start withC_{L1}andC_{L2}The serial combination of gives the parameters of the load capacitance.

load capacitanceC_LCalculated by the following formula:$C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$,in$C_{stray}$is the capacitance of the pin andPCBboard or PCB associated capacitance, its typical value is between2 pFto7 pFbetween.

picture20.use32.768 kHzTypical Applications of Crystals



Note: *OSC32_INandOSC32_OUTNo external resistors are required between and are prohibited from being added.*

6.3.7Internal Clock Source Characteristics

The characteristic parameters given in the following table are the operating environment temperature and supply voltage conforming to*surface9*conditions are measured. Curves provided are based on characterization results, not production tested.

High-speed internal (HSI)RCoscillator

surface24. HSIOscillator Characteristics(1)

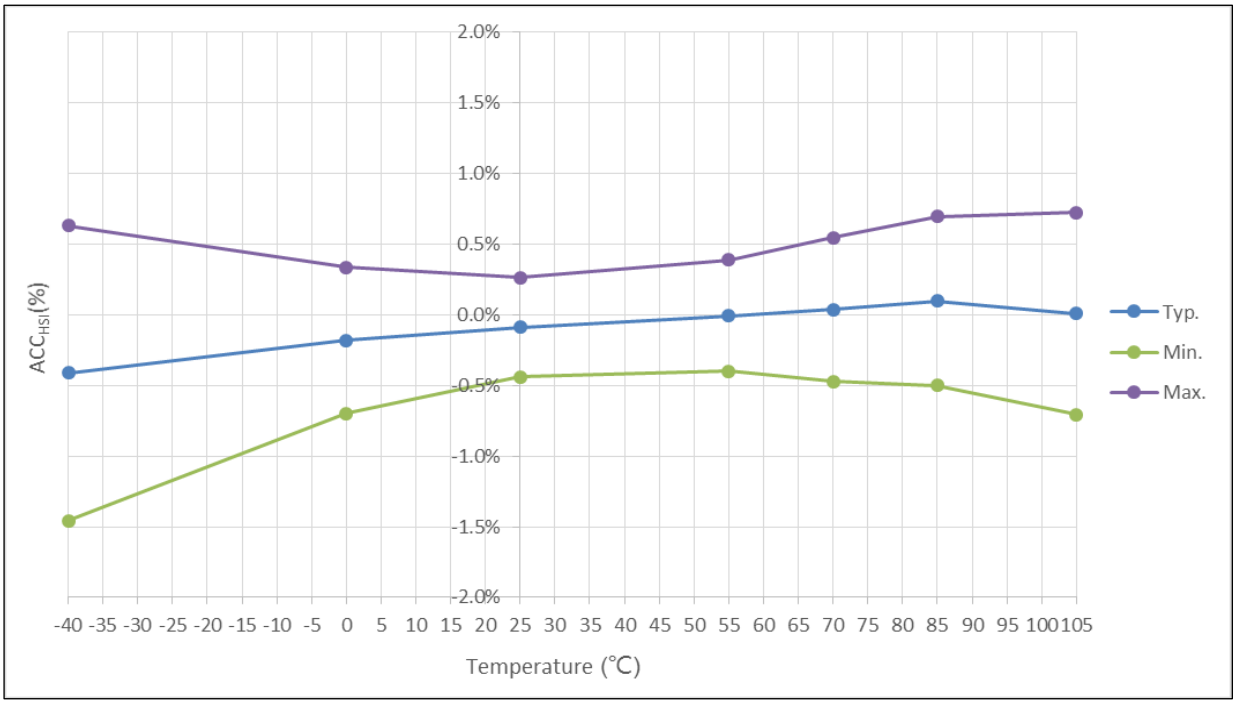
symbol	parameter	condition		minimum value	typical value	maximum value	unit
f_{HSI}	frequency	-		-	48	-	MHz
DuCy(HSI)	duty cycle	-		45	-	55	%
ACC_{HSI}	HSIOscillator Accuracy	registerRCC_CTRL calibration		-	-	1(2)	%
		factory calibration(3)	T_A= -40 ~ 105°C	- 2	-	1.5	%
			T_A= -40 ~ 85°C	- 2	-	1.2	%
			T_A= 0 ~ 70°C	- 1.5	-	1.2	%
			T_A= 25°C	- 1	-	1	%
$t_{SU(HSI)}$(3)	HSIOscillator start-up time	-		-	10	12	μs
$I_{DD(HSI)}$(3)	HSIOscillator Power Consumption	-		-	220	290	μA

(1) V_{DD}= 3.3V,T_A= -40~105°C, unless otherwise specified.

(2)Guaranteed by design, not tested in production.

(3)Derived from comprehensive evaluation, not tested in production.

picture21. HSIOscillator Accuracy vs. Temperature



low speed internal (LSI)RCoscillator

surface25.LSIOscillator Characteristics(1)

symbol	parameter	condition	minimum value	typical value	maximum value	unit
f_{LSI}(2)	frequency	-	25	35	45	kHz

(1) V_{DD}= 3.3V,T_A= -40~105°C, unless otherwise specified.

(2)Derived from comprehensive evaluation, not tested in production.

6.3.8Low Power Mode Wake Up Time

The wake-up times listed in the table below are at a system clock ofHSI RCThe wake-up phase of the oscillator is measured as the delay between the wake-up event and the execution of the first user instruction. The clock source used on wake-up currently depends on the current operating mode:

- Shutdown or Standby Mode: The clock source isHSI RCOscillator sleep
- mode: clock source is the clock used when entering sleep mode

All times are using ambient temperature and supply voltage in compliance with*surface9*conditions are measured.

surface26.Wake-up time for low-power modes

symbol	parameter	typical value	unit
tWUSLEEP	wake up from sleep mode	3.3	μs
tWUSTOP	Wake-up from shutdown (regulator in run mode)	380	μs
	Wake up from shutdown (regulator in low power mode)	450	
tWUSTDBY	Wake up from standby mode	1250	μs

6.3.9 PLLscharacteristic

The parameters listed in the table below are the operating environment temperature and supply voltage*surface9*conditions are measured.

surface27. PLLscharacteristic

symbol	parameter	minimum value	typical value	maximum value(1)	unit
f_{PLL_IN}	PLLsinput clock(2)	2	8	16	MHz
	PLLsInput Clock Duty Cycle	40	-	60	%
f_{PLL_OUT}	PLLsMultiplied output clock	16	-	120	MHz
t_{LOCK}	PLLsphase lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1)Derived from comprehensive evaluation, not tested in production.

(2)Care needs to be taken to use the correct multiplication factor so that according toPLLsThe input clock frequency makes$f_{PLL_OUT}$is within the allowable range.

6.3.10memory characteristics

Unless otherwise specified,*surface28*The characteristic parameters given in are based onT_A= -40to105°Cconditions are measured.

surface28.Flash memory characteristics

symbol	parameter	condition	minimum value	typical value	maximum value(1)	unit
T_{PROG}	programming time	T_A= -40 ~ 105°C	-	40	60	μs
t_{ERASE}	page erase time	T_A= -40 ~ 105°C	-	6.4	8	ms
t_{ME}	chip erase time	T_A= -40 ~ 105°C	-	8	10	ms
I_{DD}	programming current	write mode,V_{DD}= 3.3V,f_{HCLK}= 8 MHz, T_A= 25°C	-	1.95	-	mA
		erase mode,V_{DD}= 3.3V,f_{HCLK}= 8 MHz T_A=, 25°C	-	1.62	-	

(1)Guaranteed by design, not tested in production.

surface29.Flash Memory Lifetime and Data Retention

symbol	parameter	condition	minimum value(1)	typical value	maximum value	unit
N_{END}	Lifespan (erasing times)	T_A= -40 ~ 105°C	100	-	-	thousand times
t_{RET}	Data retention period	T_A= 105°C	10	-	-	Year

(2)Guaranteed by design, not tested in production.

6.3.11 EMCcharacteristic

Sensitivity testing is performed on a sample basis during the comprehensive evaluation of the product.

FeatureEMS(electromagnetic susceptibility)

- **EFT:**existVDDandVSSon through a47 µFand two100nFThe capacitor applies a burst of transient voltages (forward and reverse) until a functional error occurs. This test meetsIEC 61000-4-4standard.

surface30.EMScharacteristic

symbol	parameter	condition	level/type
VEFT	existVDDandVSSon through a47 µFand two100nF Transient bursts imposed by the capacitance of the voltage limit	VDD= 3.3V,LQFP48,TA= +25°C, fHCLK= 120 MHz. conform toIEC 61000-4-4	3/A
		VDD= 3.3V,LQFP48,TA= +25°C, fHCLK= 72 MHz. conform toIEC 61000-4-4	(2kV)

Design robust software to avoid noise issues

performed at the device levelEMCThe evaluation and optimization are carried out in a typical application environment. It should be noted that, okayEMCPerformance is closely related to user application and specific software.

Therefore, users are advised to implement the softwareEMCoptimized, and performed withEMCrelevant certification tests.

software advice

The software process must include the control of program run-away, such as:

- Corrupted Program Counter
- unexpected reset
- Critical data is corrupted (control registers, etc....)

Tests before certification

Many common failures (unintended resets and program counter corruption) can be detected manually in theNRSTIntroduce a low level on the crystal pin or introduce a continuous1second low level and reproduce.

6.3.12electrical sensitivity

Based on three different tests (ESD,LU), using a specific measurement method, the chip is subjected to a stress test to determine its performance in terms of electrical susceptibility.

electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse after a second interval) was applied to all pins of all samples, and the size of the sample was related to the number of power supply pins on the chip (3piecex(n+1) supply pin). This test meetsJS-001-2017/JS-002-2014 standard.

surface31. ESDabsolute maximum

symbol	parameter	condition	type	maximum value(1)	unit
$V_{ESD(HBM)}$	Electrostatic Discharge Voltage (Human Body Model)	T_A= +25°C,conform toJS-001-2017	3A	6000	V
$V_{ESD (CDM)}$	Electrostatic discharge voltage (charging device model)	T_A= +25°C,conform toJS-002-2014	III	1000	

(1)Derived from comprehensive evaluation, not tested in production.

static latch

To evaluate latch-up performance, the6samples2A complementary static latch-up test:

- For each supply pin, provide a supply voltage exceeding the limit.
- at each input, output and configurableI/OInject current on the pin.

This test meetsEIA/JESD78EIntegrated Circuit Latch Standard.

surface32.electrical sensitivity

symbol	parameter	condition	level/type
LU	static latch class	T_A= +105°C,conform toEIA/JESD78E	IIkindA (200mA)

6.3.13 GPIOscharacteristic

General purpose input/output characteristics

Unless otherwise specified, the parameters listed in the table below are based on*surface9*conditions are measured. allI/Oports are compatibleCMOSandTTL.

surface33. I/Ostatic characteristics

symbol	parameter	condition	minimum value	typical value	maximum value	unit
V_{IL}	I/OPin input low level voltage	-	- 0.3	-	0.28*V_{DD}+ 0.1	V
V_{IH}	TC I/OPin input high level voltage	-	0.31*V_{DD}+ 0.8	-	V_{DD}+ 0.3	V
	FTa I/OPin input high level voltage	simulation mode				
	FT I/OPin input high level voltage	-		-	5.5	
	FTa I/OPin input high level voltage	Input floating, input on pull, or input pull-down				
V_{hys}	TC I/Opin Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
	FTandFTa I/Opin Schmitt trigger voltage hysteresis(1)		5%V_{DD}	-	-	-
I_{lkg}	Input Float Mode Leakage Current(2)	V_{SS}≤V_{IN}≤V_{DD} TC I/Ofoot	-	-	±1	μA
		V_{SS}≤V_{IN}≤ 5.5V FT andFTa I/Ofoot	-	-	±1	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}= V_{SS}	65	80	130	kΩ
R_{PD}	Weak pull-down equivalent resistance(3)	V_{IN}= V_{DD}	65	70	130	kΩ
C_{IO}	I/OPin Capacitance	-	-	9	-	pF

(1)Hysteresis voltage for Schmitt trigger switching levels. Derived from comprehensive evaluation, not tested in production.

(2)The leakage current may be higher than the maximum value if there is reverse current flowing in adjacent pins.

(3) BOOT0The pin weak pull-down resistor cannot be disabled.

allI/Oports areCMOSandTTLCompatible (no software configuration required), their characteristics take into account the most stringentCMOScraft or TTL parameter.

output drive current

In the user application,I/OThe number of pins must ensure that the drive current cannot exceed*6.2*The absolute maximum ratings given in section:

- allI/Oport fromV_{DD}on the sum of the currents obtained, plusMCUexistV_{DD}The maximum operating current drawn on the absolute maximum rating must not be exceededI_{VDD}(see*surface7*).
- allI/Oport absorbs and from theV_{SS}The sum of the currents flowing out, plusMCUexistV_{SS}The maximum operating current that flows out of the above, cannot exceed the absolute maximum ratingI_{VSS}(see*surface7*).

The output voltage

Unless otherwise specified, the parameters listed in the table below are based on ambient temperature andV_{DD}The supply voltage complies with*surface9*conditions are measured. allI/O ports are compatibleCMOSandTTLof.

surface34.Output Voltage Characteristics

symbol	parameter	condition	minimum value	maximum value	unit
Moderate current push/sink capability					
V_{OL}	output low level	CMOSport,I_{IO}= 4 mA 2.7	-	0.4	V
V_{Oh}	output high level	V ≤ V_{DD}≤ 3.6V	V_{DD}-0.4	-	
V_{OL}	output low level	TTLport,I_{IO}= 2 mA 2.7	-	0.4	V
V_{Oh}	output high level	V ≤ V_{DD}≤ 3.6V	2.4	-	
V_{OL}	output low level	I_{IO}= 9 mA	-	1.3	V
V_{Oh}	output high level	2.7 V ≤ V_{DD}≤ 3.6V	V_{DD}-1.3	-	
V_{OL}	output low level	I_{IO}= 4 mA	-	0.4	V
V_{Oh}	output high level	2.4 V ≤ V_{DD}< 2.7V	V_{DD}-0.4	-	
High current push/sink capability					
V_{OL}	output low level	CMOSport,I_{IO}= 6 mA 2.7	-	0.4	V
V_{Oh}	output high level	V ≤ V_{DD}≤ 3.6V	V_{DD}-0.4	-	
V_{OL}	output low level	TTLport,I_{IO}= 5 mA 2.7	-	0.4	V
V_{Oh}	output high level	V ≤ V_{DD}≤ 3.6V	2.4	-	
V_{OL}	output low level	I_{IO}= 18mA	-	1.3	V
V_{Oh}	output high level	2.7 V ≤ V_{DD}≤ 3.6V	V_{DD}-1.3	-	
V_{OL}	output low level	I_{IO}= 8mA	-	0.4	V
V_{Oh}	output high level	2.4 V ≤ V_{DD}< 2.7V	V_{DD}-0.4	-	
Very high current push/sink capability					
V_{OL}	output low level	CMOSport,I_{IO}= 15 mA 2.7	-	0.4	V
V_{Oh}	output high level	V ≤ V_{DD}≤ 3.6V	V_{DD}-0.4	-	
V_{OL}	output low level	TTLport,I_{IO}= 12 mA 2.7	-	0.4	V
V_{Oh}	output high level	V ≤ V_{DD}≤ 3.6V	2.4	-	
V_{OL}	output low level	I_{IO}= 36mA	-	1.3	V
V_{Oh}	output high level	2.7 V ≤ V_{DD}≤ 3.6V	V_{DD}-1.3	-	
V_{OL}	output low level	I_{IO}= 18mA	-	0.4	V
V_{Oh}	output high level	2.4 V ≤ V_{DD}< 2.7V	V_{DD}-0.4	-	

(1)Derived from comprehensive evaluation, not tested in production.

Input AC Characteristics

The definition and values of the input AC characteristics are given in the table below.

Unless otherwise specified, the parameters listed in the table below are based on the ambient temperature and power supply voltage*surface9*conditions are measured.

surface35.Input AC Characteristics

symbol	parameter	minimum value	maximum value	unit
tEXTIpw	EXTIThe controller detects the pulse width of the external signal	10	-	ns

6.3.14 NRSTsPin Characteristics

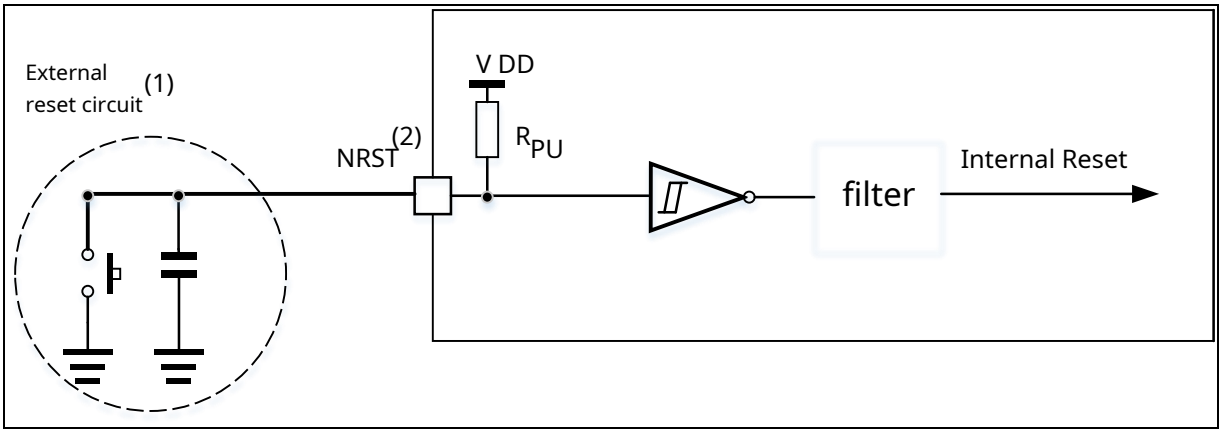
NRSTpin input driver usingCMOSprocess, which connects a pull-up resistor that cannot be disconnected,R_{PU}(see table below). Unless otherwise specified, the parameters listed in the table below are based on the ambient temperature and power supply voltage*surface9*conditions are measured.

surface36. NRSTPin Characteristics

symbol	parameter	condition	minimum value	typical value	maximum value	unit
$V_{IL(NRST)}$ (1)	NRSTInput low level voltage	-	- 0.3	-	0.72	V
$V_{IH(NRST)}$ (1)	NRSTInput high level voltage	-	2	-	V_{DD}+ 0.3	
$V_{hys(NRST)}$	NRSTSchmitt Trigger Voltage Hysteresis	-	-	400	-	mV
R_{PU}	Weak pull-up equivalent resistance	V_{IN}= V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$ (1)	NRSTinput filter pulse	-	-	29	40	μs
$V_{NF (NRST)}$ (1)	NRSTInput unfiltered pulse	-	80	52	-	μs

(1)Guaranteed by design, not tested in production.

picturetwenty two.suggestedNRSTpin protection



(1)The reset network is to prevent parasitic resets.

(2)The user must guaranteeNRSTThe potential of the pin can be lower than*surface36*the largest listed in$V_{IL(NRST)}$below, otherwiseMCUCan't get reset.

6.3.15 TMRsTimer Features

The parameters listed in the table below are guaranteed by design.

For input and output alternate function pins (output compare, input capture, external clock,PWMoutput), see*6.3.13 GPIOs characteristic*.

surface37. TMRx(1)characteristic

symbol	parameter	condition	minimum value	maximum value	unit
$t_{res(TMR)}$	timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$= 120 MHz	8.3	-	ns
f_{EXT}	CH1toCH4external clock frequency of the timer	-	0	$f_{TMRxCLK}$/2	MHz
		$f_{TMRxCLK}$= 120 MHz	0	60	

(1) TMRxis a generic name that stands forTMR1,TMR3,TMR6,andTMR14~17.

6.3.16Communication Interface

I2CInterface Features

SDAandSCL I/OSatisfaction of requirements is subject to the following restrictions:SDAandSCLNot a "true" open-drain pin, when configured as an open-drain output, the pin andV_{DD}betweenPMOSThe tube is closed, but is still there. For input and output alternate function pins (SDAandSCL) for details of the characteristics, see*6.3.13 GPIOscharacteristic*.

I2CThe bus interface supports standard mode (up to100 kbit/s) and fast mode (maximum400 kbit/s).I2CThe bus frequency can be increased up to1 MHz. For a more complete and detailed solution, you can contact the nearest Yateli sales office for technical support.

SPI-I2SInterface Features

Unless otherwise specified,*surface38*listedSPIparameters and*surface39*listedI2Sparameter is the ambient temperature used,f_{PCLKx}frequency andV_{DD}The supply voltage complies with*surface9*conditions are measured.

For input and output alternate function pins (SPIofNSS,SCK,MOSI,MISO,I2SofWS,CK,SD) for details of the characteristics, see*6.3.13 GPIOscharacteristic*.

surface38. SPIcharacteristic

symbol	parameter	condition		minimum value	maximum value	unit
f_{SCK} $(1/t_{c(SCK)})$(1)	SPIClock frequency(2)	main mode	V_{DD}= 3.3 V, T_A= 25°C	-	50	MHz
			V_{DD}= 3.3 V, T_A= 105°C	-	40	
			V_{DD}= 2.4 V, T_A= 105°C	-	36	
		slave mode		-	f_{PCLK}/2	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPIClock Rise and Fall Times	Load Capacitance:C = 15pF		-	6	ns
$t_{su(NSS)}$ (1)	NSSbuild time	slave mode		4t_{PCLK}	-	ns
$t_{h(NSS)}$ (1)	NSShold time	slave mode		2t_{PCLK}+ 10	-	ns
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCKhigh and low times	master mode,f_{PCLK}= 120 MHz, prescaler factor =4		t_{PCLK}/twenty two	t_{PCLK}/2 + 1	ns
$t_{su(MI)}$(1)	Data input setup time	main mode		4	-	ns
$t_{su(SI)}$ (1)		slave mode		5	-	
$t_{h(MI)}$ (1)	Data input hold time	main mode		4	-	ns
$t_{h(SI)}$ (1)		slave mode		5	-	
$t_{a(SO)}$ (1)(3)	Data Out Access Time	from the schema,f_{PCLK}= 20 MHz		0	3t_{PCLK}	ns
$t_{dis(SO)}$ (1)(4)	Data output inhibit time	slave mode		0	18	ns
$t_{v(SO)}$ (1)	Data output effective time	Slave mode (after enable edge)		-	22.5	ns
$t_{v(MO)}$ (1)	Data output effective time	Master mode (after enable edge)		-	6	ns
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)		11.5	-	ns
$t_{h(MO)}$ (1)		Master mode (after enable edge)		2	-	

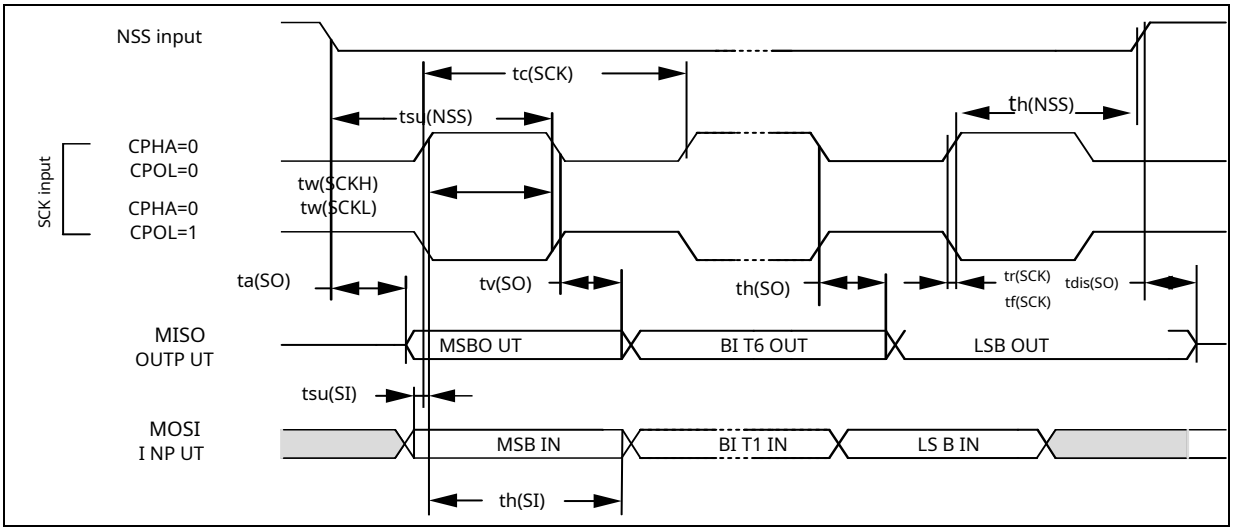
(1)Derived from comprehensive evaluation, not tested in production.

(2)The maximum clock frequency varies with the device andPCBLayout is highly dependent. For a more complete and detailed solution, you can contact the nearest Yateli sales office for technical support.

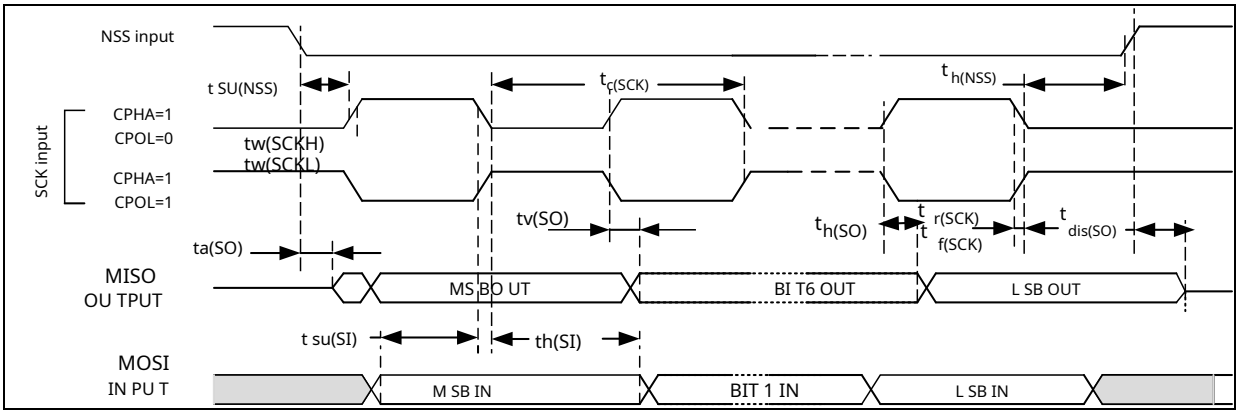
(3)The minimum value indicates the minimum time to drive the output, and the maximum value indicates the maximum time to get the data correctly.

(4)The minimum value indicates the minimum time to turn off the output, and the maximum value indicates the maximum time to put the data line in a high-impedance state.

picture23. SPITiming Diagram – Slave Mode andCPHA = 0

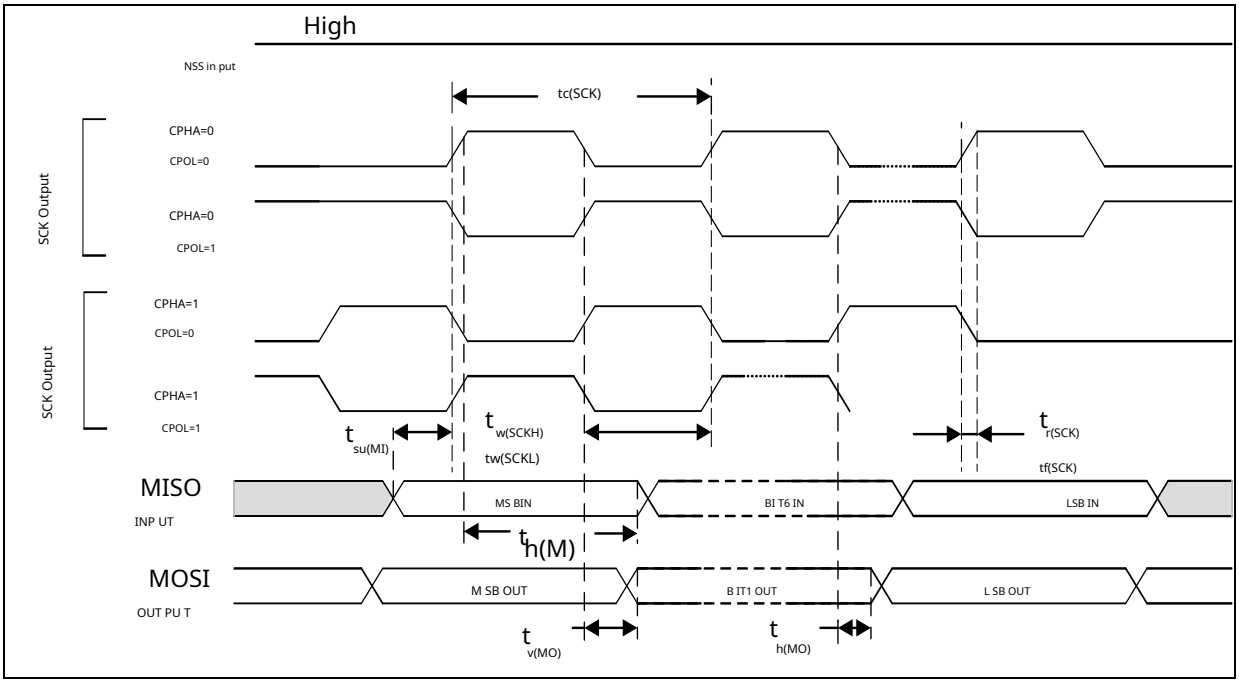


picture24. SPITiming Diagram – Slave Mode andCPHA = 1(1)



(1)The measurement point is set atCMOSLevel:0.3V_{DD}and0.7V_{DD}.

picture25. SPITiming Diagram – Master Mode(1)



(1)The measurement point is set atCMOSLevel:0.3V_{DD}and0.7V_{DD}.

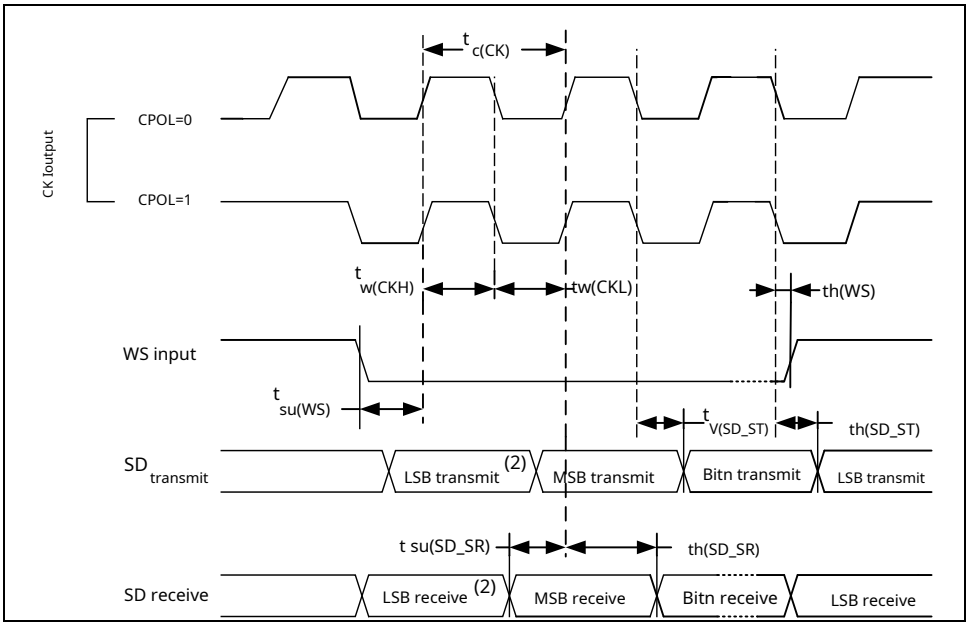
surface39.I2Scharacteristic

symbol	parameter	condition	minimum value	maximum value	unit
f_{CK} $1/t_{c(CK)}$	I2SClock frequency	Master Mode (Source:16bits, audio:48 kHz)	1.522	1.525	MHz
		slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I2SClock Rise and Fall Times	Load Capacitance:C = 15pF	-	12	ns
$t_{v(WS)}$ (1)	WSEffective time	main mode	2	-	
$t_{h(WS)}$ (1)	WShold time	main mode	2	-	
$t_{su(WS)}$(1)	WSbuild time	slave mode	7	-	
$t_{h(WS)}$ (1)	WShold time	slave mode	0	-	
$t_{w(CKH)}$(1)	CKhigh and low times	master mode,f_{PCLK}= 16 MHz, audio:48 kHz	306	-	
$t_{w(CKL)}$(1)			312	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	master receiver	6	-	
$t_{su(SD\_SR)}$(1)		from the receiver	2	-	
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	master receiver	4	-	
$t_{h(SD\_SR)}$ (1)(2)		from the receiver	0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output effective time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	13	-	
$t_{v(SD\_MT)}$ (1)(2)	Data output effective time	Master Transmitter (after enable edge)	-	4	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master Transmitter (after enable edge)	0	-	

(1)Derived from design simulation and/or synthesis evaluation, not tested in production.

(2)depends onf_{PCLK}. For example, iff_{PCLK}= 8 MHz,butt_{PCLK}= 1/f_{PCLK}= 125ns.

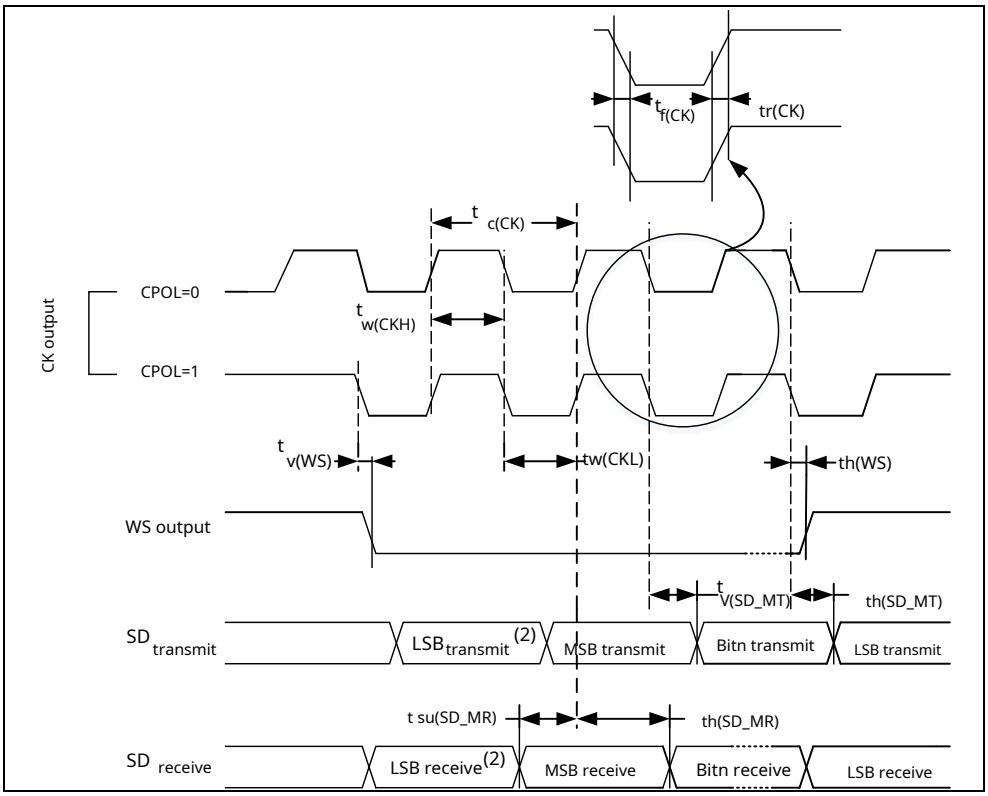
picture26.I2SSlave Mode Timing Diagram (Philipsprotocol)(1)



(1)The measurement point is set atCMOSLevel:0.3V_{DD}and0.7V_{DD}.

(2)The lowest bit of the previous byte is sent/received. There is no sending/receiving of this lowest bit before the first byte.

picture27.I2SMaster Mode Timing Diagram (Philipsprotocol)(1)



(1)The measurement point is set atCMOSLevel:0.3V_{DD}and0.7V_{DD}.

(2)The lowest bit of the previous byte is sent/received. There is no sending/receiving of this lowest bit before the first byte.

6.3.17 12bitADCcharacteristic

Unless otherwise specified, the parameters in the table below are used in accordance with*surface9*conditions of ambient temperature,f_{PCLK2}frequency andV_{DDA}The supply voltage is measured.

Note: *It is recommended to perform a calibration every time the power is turned on.*

surface40. ADCscharacteristic

symbol	parameter	condition	minimum value	typical value	maximum value	unit
V_{DDA}	supply voltage	-	2.4	-	3.6	V
I_{DDA}	existV_{DDA}The current on the input pin	-	-	480(1)	560	μA
f_{ADC}	ADCClock frequency	-	0.6	-	28	MHz
f_S(2)	sampling rate	-	0.05	-	2	MHz
f_{TRIG} (2)	External trigger frequency	f_{ADC}= 28 MHz	-	-	1.65	MHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0(V_{REF-}internally connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-	see*surface41*and*surface42*			Ω
C_{ADC} (2)	Internal sample and hold capacitor	-	-	8.5	13	pF
t_{CAL}(2)	calibration time	f_{ADC}= 28 MHz	6.61			μs
		-	185			$1/f_{ADC}$
$t_{(a)}$	Injection Triggered Conversion Latency	f_{ADC}= 28 MHz	-	-	107	ns
		-	-	-	3(4)	$1/f_{ADC}$
$t_{(a)r}$	Normal Trigger Conversion Latency	f_{ADC}= 28 MHz	-	-	71.4	μs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	sampling time	f_{ADC}= 28 MHz	0.053	-	8.55	μs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	power on time	-	42			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC}= 28 MHz	0.5	-	9	μs
		-	14~252(samplingt_S+step by step12.5)			$1/f_{ADC}$

(1)Guaranteed by comprehensive evaluation, not tested in production.

(2)Guaranteed by design, not tested in production.

(3)V_{REF+}internally connected toV_{DDA},V_{REF-}internally connected toV_{SSA}.

(4)For an external trigger, the*surface40*Add a delay to the listed delay1/f_{PCLK2}.

*surface41*and*surface42*Determine the maximum external impedance such that the error can be less than1 LSB.

surface41. f_{ADC}= 14 MHzwhen the maximumR_{AIN} (1)

Ts(cycle)	ts(μthe s)	maximumR_{AIN}(kΩ)
1.5	0.11	0.35
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

(1)Guaranteed by design.

surface42. f_{ADC}= 28 MHzwhen the maximumR AIN(1)

Ts(cycle)	ts(μthe s)	maximumR_{AIN}(kΩ)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

(1)Guaranteed by design.

surface43. ADCsprecision(1)(2)

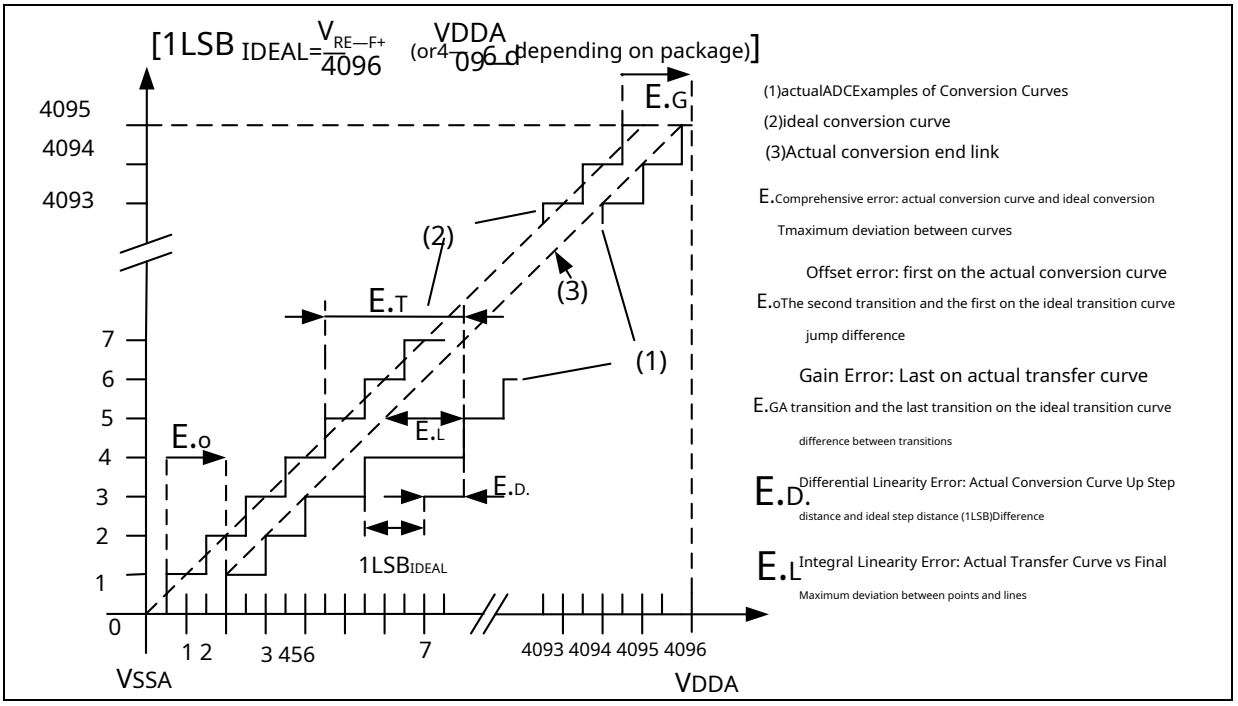
symbol	parameter	Test Conditions	typical value	maximum value(3)	unit
ET	Comprehensive error	fPCLK2= 56 MHz, fADC= 28 MHz,RAIN< 10 kΩ, VDDA= 3.0~3.6V,TA= 25°C	+ 2	+ 3.5	LSB
EO	offset error		+ 1	+ 2.5	
EG	gain error		+ 1.5	+ 3	
ED	Differential Linearity Error		±0.7	±1	
EL	Integral Linearity Error		±0.8	±1.5	
ET	Comprehensive error	fPCLK2= 56 MHz, fADC= 28 MHz,RAIN< 10 kΩ, VDDA= 2.4~3.6V	±2	+ 4	LSB
EO	offset error		+ 1	+ 3	
EG	gain error		+ 1.5	+ 3.5	
ED	Differential Linearity Error		±0.6	+1.5/-1	
EL	Integral Linearity Error		±1	±2.5	

(1) ADCThe DC accuracy values are measured after internal calibration.

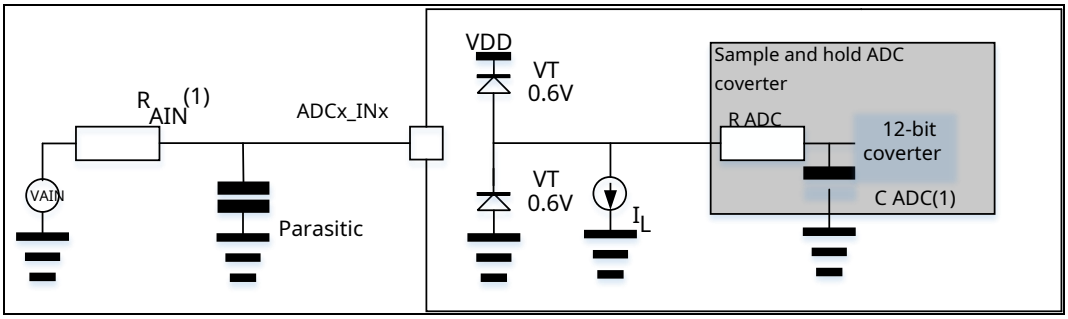
(2) ADCsAccuracy vs. Reverse Injection Current: Injecting reverse current on any standard analog input pin needs to be avoided as this can significantly degrade the accuracy of the conversion being performed on another analog input pin. It is recommended to add a Schottky diode (between pin and ground) on standard analog pins that may cause reverse injection current.

(3)Guaranteed by comprehensive evaluation, not tested in production.

picture28. ADCsAccuracy characteristics



picture29.useADCTypical Connection Diagram



(1)relatedRAINandCADCvalue, see*surface40*.

(2)CparasiticexpressPCB(with soldering andPCBlayout quality) versus the parasitic capacitance on the pad (approximately7 pF). largerCparasiticThe numerical value will reduce the precision of the conversion, the solution is to reduce thefADC.

PCBdesign advice

Should be as*picture11*Perform power supply decoupling as shown in .100nFThe capacitors should be ceramic type(high quality), should be placed as close as possible to the chip.

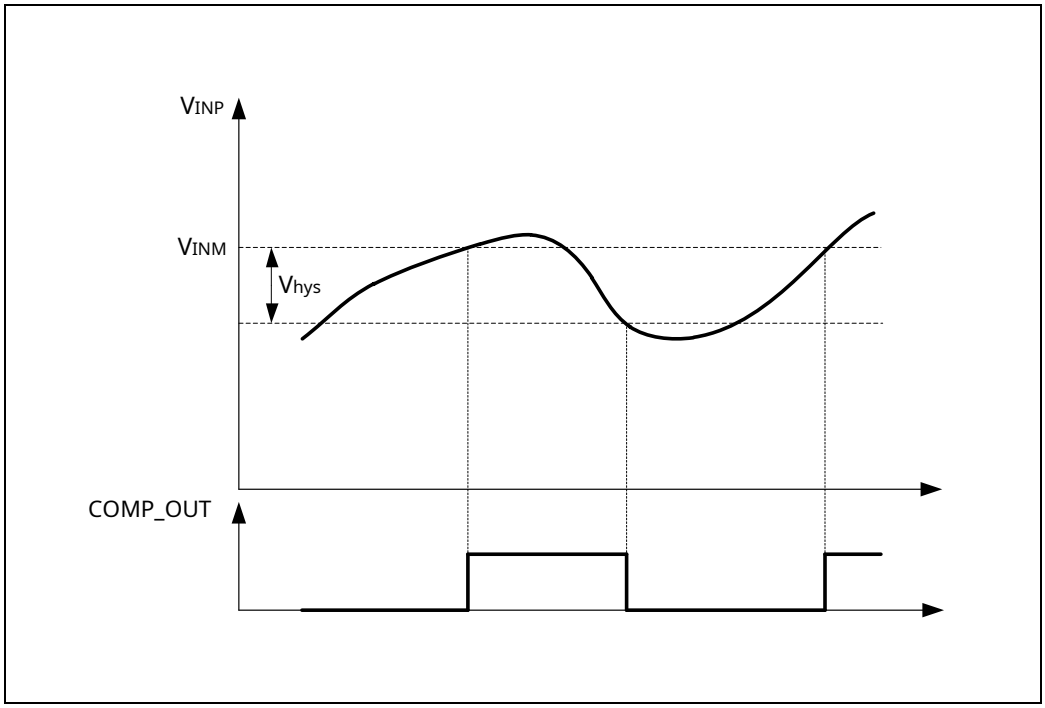
6.3.18Comparator Characteristics

surface44.Comparator Characteristics

symbol	parameter	condition	minimum value(1)	typical value	maximum value(1)	unit
V_{DDA}	supply voltage	-	2.4	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
t_{START}	Start Time	high speed mode	-	1.0	3.5	μs
		medium speed mode	-	2.8	5	
		low power mode	-	8	13	
		Ultra Low Power Mode	-	12	18	
$t_{D.}$	200mVstepper,100mV overloaded propagation delay	high speed mode	-	40	100	ns
		medium speed mode	-	240	320	
		low power mode	-	500	820	
		Ultra Low Power Mode	-	800	1800	
V_{offset}	shift error voltage	-	-	±4	±15	mV
V_{hys}	hysteresis voltage	no hysteresis	-	0	1	mV
		low hysteresis	5	8	17	
		medium hysteresis	10	18	37	
		high hysteresis	18	38	70	
I_{DDA}	existV_{DDA}The current on the input pin	high speed mode	-	40	61	μA
		medium speed mode	-	9.7	13.9	
		low power mode	-	3.2	4.7	
		Ultra Low Power Mode	-	1.9	2.8	

(1)Guaranteed by comprehensive evaluation, not tested in production.

picture30.Comparator Hysteresis Diagram



6.3.19Temperature Sensor Characteristics

surface45.Temperature Sensor Characteristics

symbol	parameter	minimum value	typical value	maximum value	unit
T_L(1)	V_{SENSE}Linearity with respect to temperature	-	±1	±2	o C
Avg_Slope(1)(2)	mean slope	- 4.17	- 4.30	- 4.44	mV/°C
V_{25}(1)(2)	exist25°Cvoltage at	1.22	1.28	1.34	V
t_{START} (3)	build time	-	-	100	μs
T_{S_temp} (3)(4)	When reading the temperature,ADCsampling time	-	8.6	17.1	μs

(1)Guaranteed by comprehensive evaluation, not tested in production.

(2)The output voltage of the temperature sensor changes linearly with the temperature. Due to the change of the production process, the offset of the temperature change curve will be different on different chips (the difference is at most50°C). Internal temperature sensors are better suited for detecting changes in temperature rather than measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor should be used.

(3)Guaranteed by design, not tested in production.

(4)Short sample times can be determined by the application through multiple loops.

Use the following formula to find the temperature:

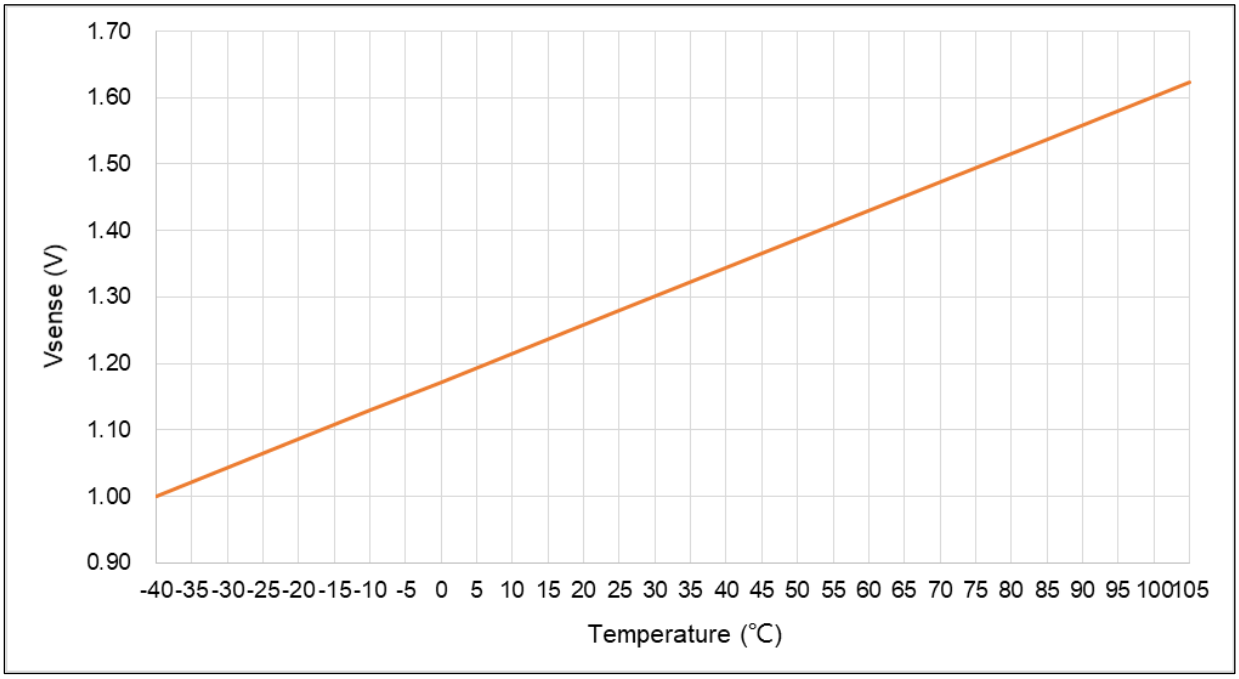
temperature(°C) = {(V_{25}–V_{SENSE}) / Avg_Slope} + 25

here:

V_{25} =V_{SENSE}exist25°Cwhen the value

Avg_Slope= temperature andV_{SENSE}The average slope of the curve (in units ofmV/°C)

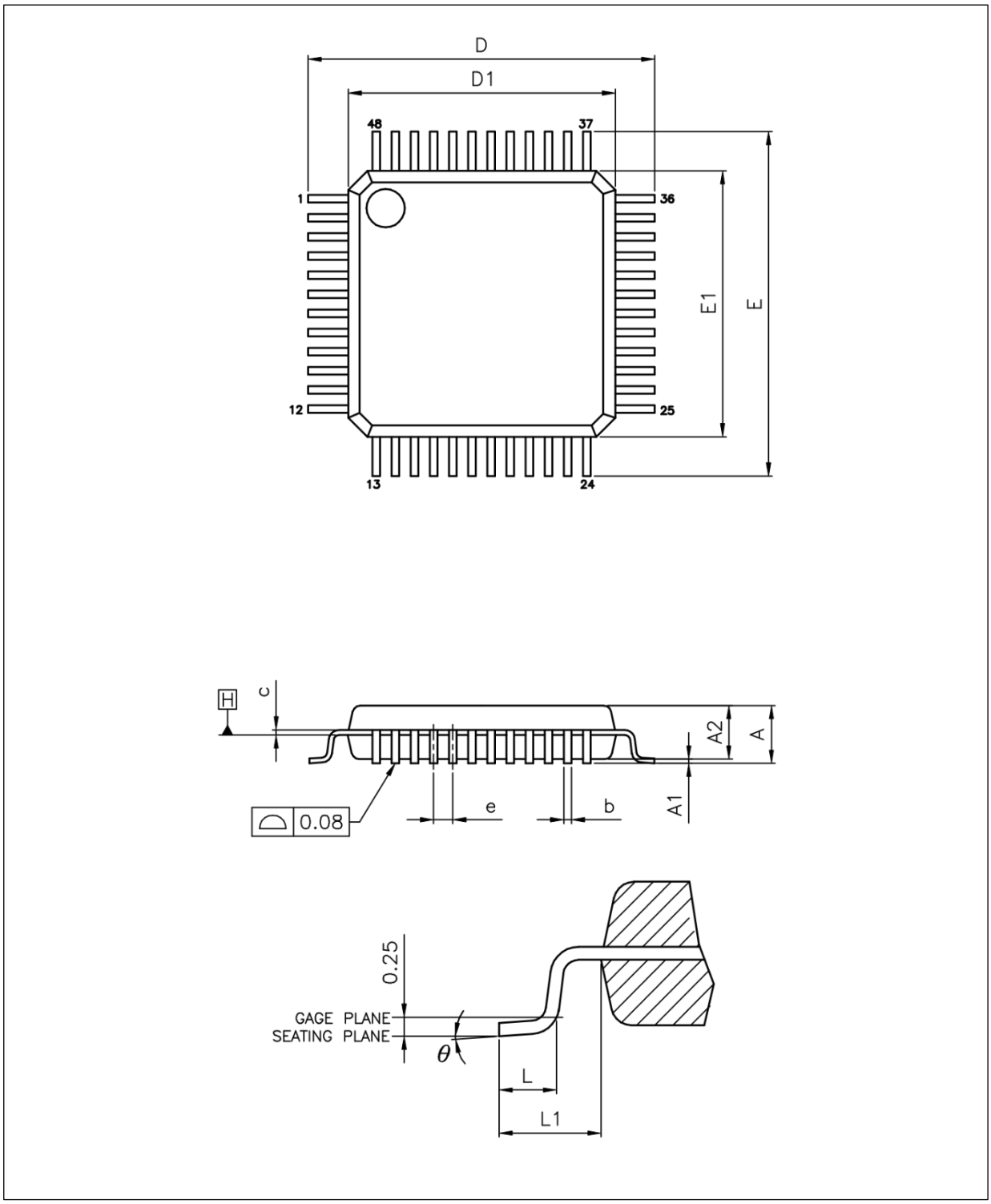
picture31.V_{SENSE}Ideal curve for temperature



7 Package Features

7.1 LQFP48 – 7 x 7 mmencapsulated data

picture32. LQFP48 – 7 x 7 mm 48Lead Thin Quad Flat Package Diagram



(1)Figures are not drawn to scale.

surface46. LQFP48 – 7 x 7 mm 48Leaded Thin Quad Flat Pack Mechanical Data

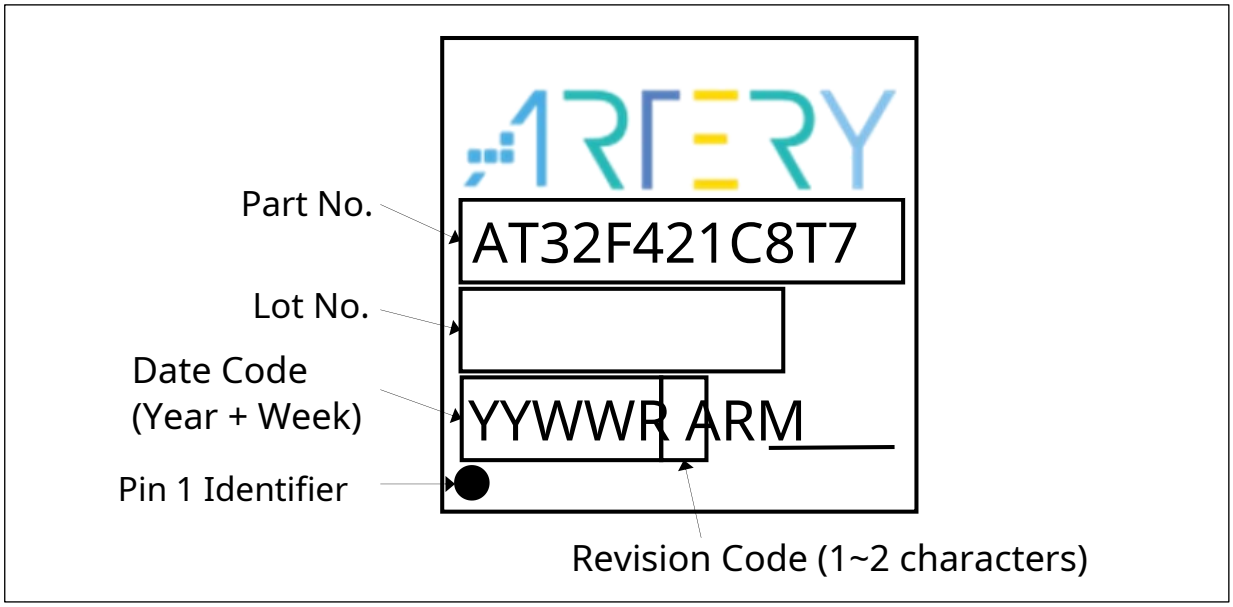
label	mm			inch(1)		
	minimum value	typical value	maximum value	minimum value	typical value	maximum value
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	-	0.20	0.004	-	0.008
D.	9.00 BSC.			0.345 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E.	9.00 BSC.			0.345 BSC.		
E1	7.00 BSC.			0.276 BSC.		
e	0.50 BSC.			0.020 BSC.		
Θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

(1)Inch values are based on mm data according to3It is obtained by rounding to decimal precision conversion.

LQFP48 – 7 x 7 mequipment marking The image below is a top marking orientation with pin1

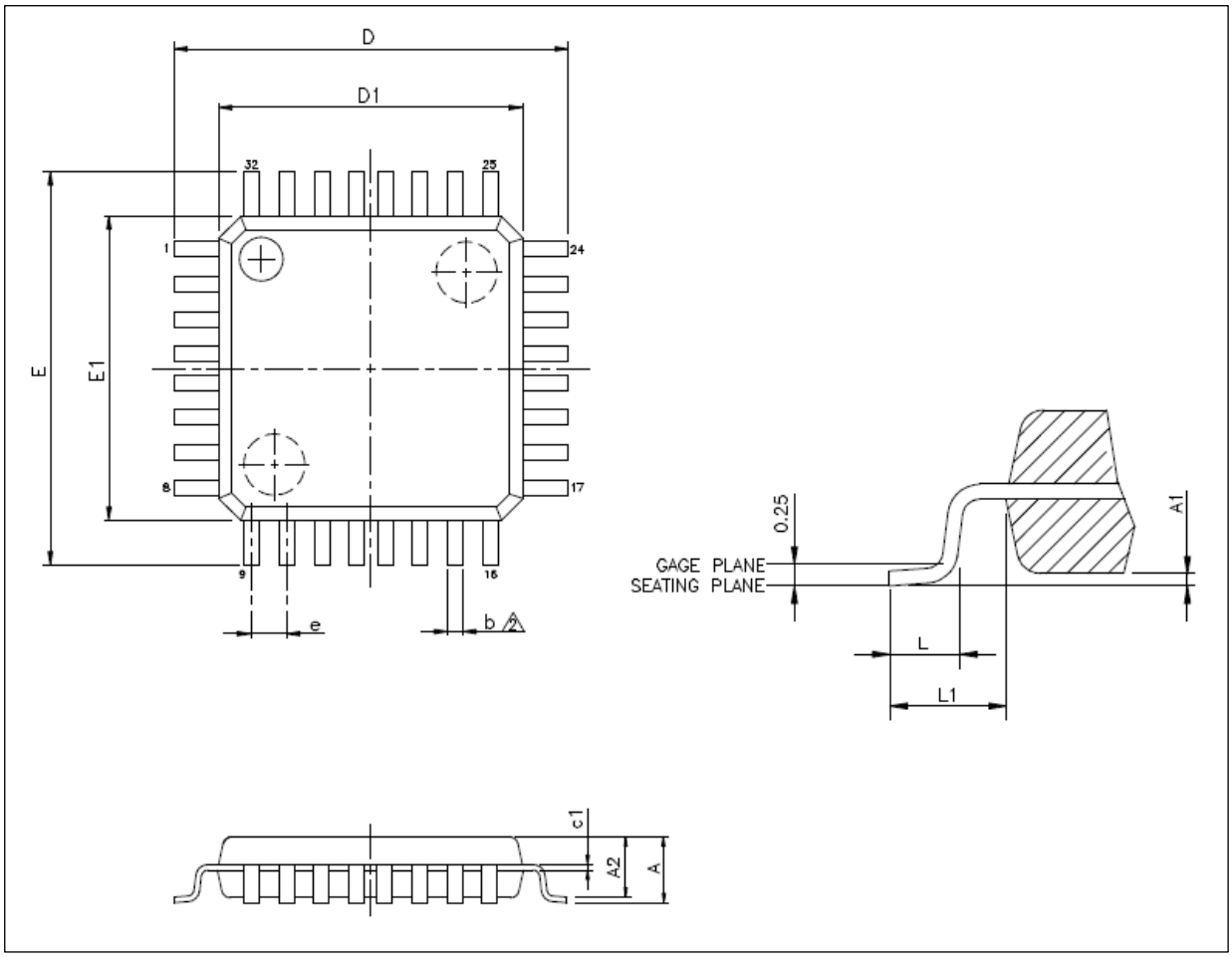
Examples of identifying marker locations

picture33. LQFP48 – 7 x 7 mmMarking (Package Top View)



7.2 LQFP32 – 7 x 7 mmencapsulated data

picture34. LQFP32 – 7 x 7 mm 32Lead Thin Quad Flat Package Diagram



(1)Figures are not drawn to scale.

surface47. LQFP32 – 7 x 7 mm 32Leaded Thin Quad Flat Pack Mechanical Data

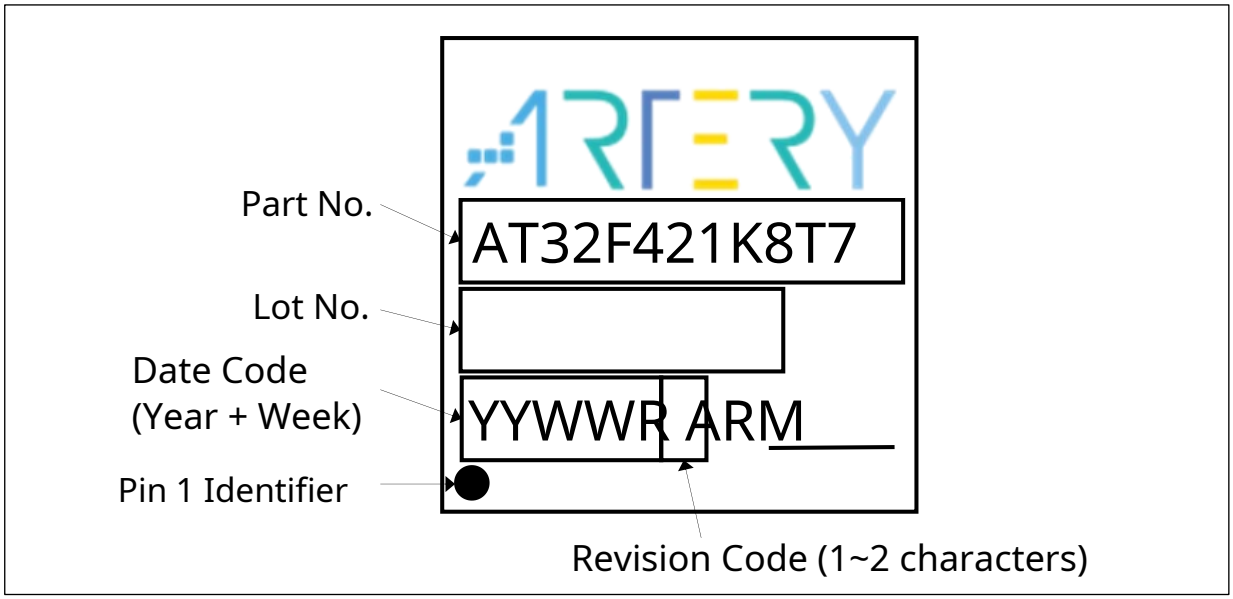
label	mm			inch(1)		
	minimum value	typical value	maximum value	minimum value	typical value	maximum value
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	-	1.45	0.053	-	0.057
b	0.30	-	0.45	0.012	-	0.018
c	0.09	-	0.16	0.004	-	0.006
D.	9.00 BSC.			0.345 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E.	9.00 BSC.			0.345 BSC.		
E1	7.00 BSC.			0.276 BSC.		
e	0.80 BSC.			0.031 BSC.		
L	0.45	-	0.75	0.018	-	0.030
L1	1.00 REF.			0.039 REF.		

(1)Inch values are based on mm data according to3It is obtained by rounding to decimal precision conversion.

LQFP32 – 7 x 7 mequipment marking The image below is a top marking orientation with pin1

Examples of identifying marker locations

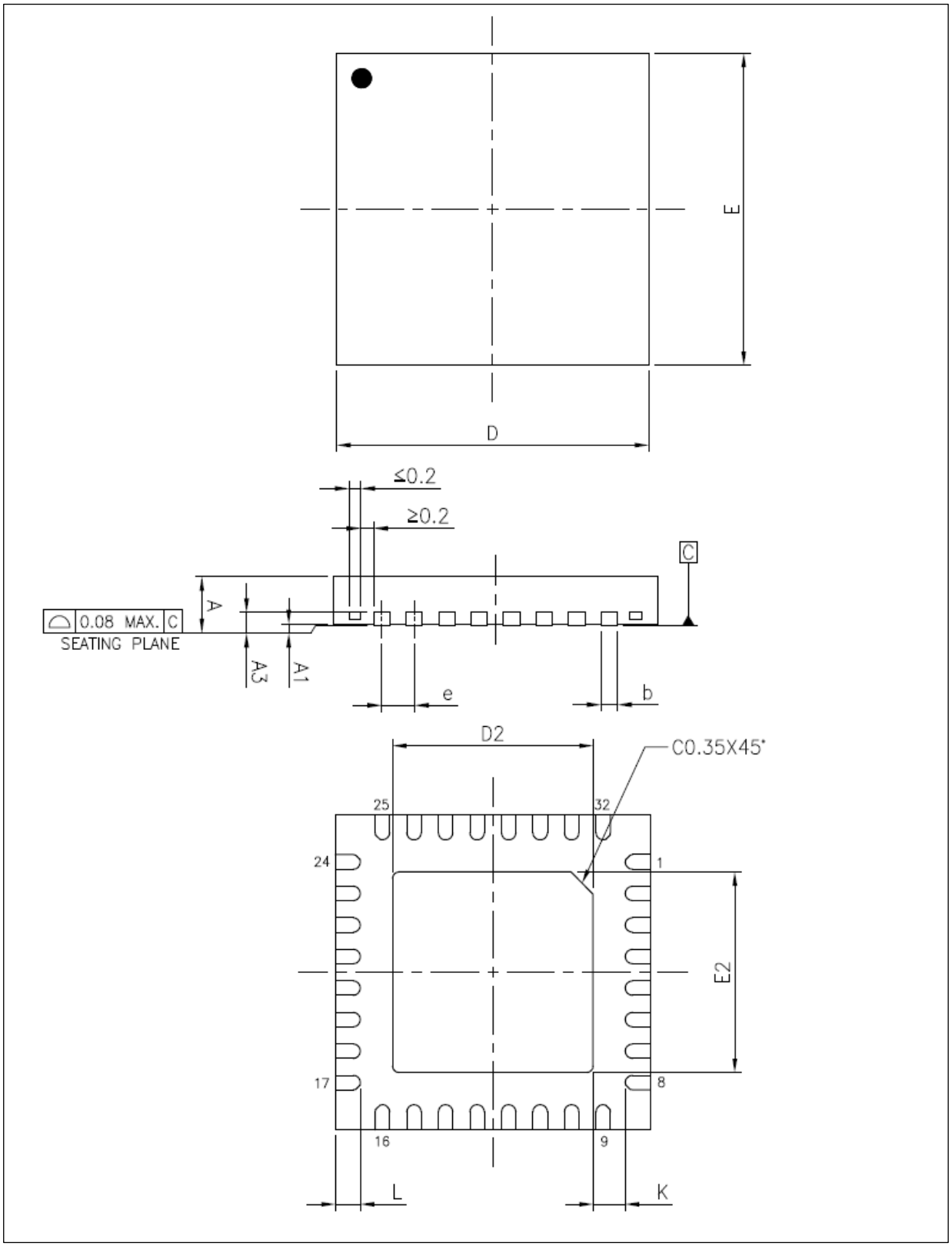
picture35. LQFP32 – 7 x 7 mmMarking (Package Top View)



7.3 QF

encapsulated data

FN32 – 5 x 5 mm 32Pinned Quad Flat No Leads Package Drawing



(1)Figures are not drawn to scale.

surface48. QFN32 – 5 x 5 mm 32Leaded Quad Flat No Lead Package Mechanical Data

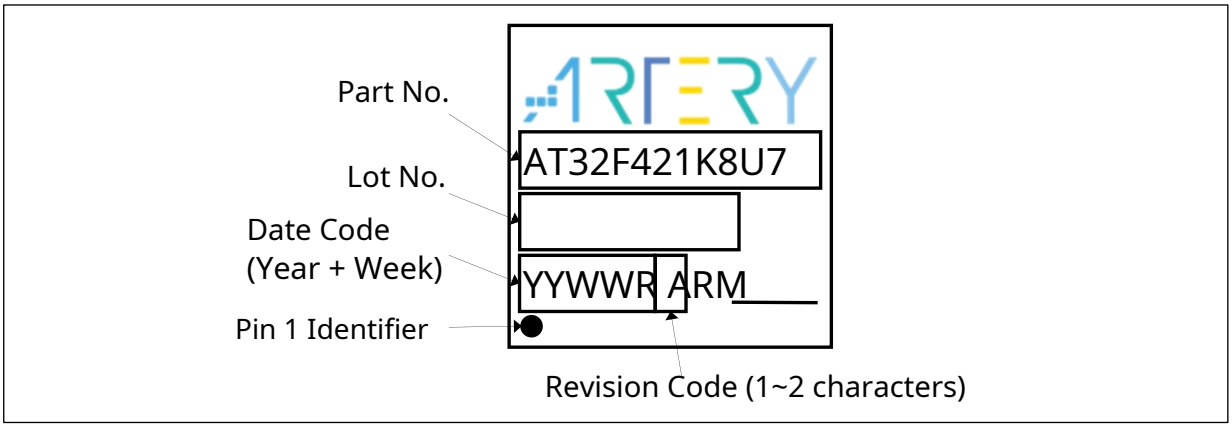
label	mm			inch(1)		
	minimum value	typical value	maximum value	minimum value	typical value	maximum value
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D.	5.00 BSC.			0.197 BSC.		
D2	3.20	3.25	3.30	0.126	0.128	0.130
E.	5.00 BSC.			0.197 BSC.		
E2	3.20	3.25	3.30	0.126	0.128	0.130
e	0.50 BSC.			0.020 BSC.		
K	0.20	-	-	0.008	-	-
L	0.35	0.40	0.45	0.014	0.016	0.018

(1)Inch values are based on mm data according to3It is obtained by rounding to decimal precision conversion.

QFN32 – 5 x 5 mmequipment marking The image below is a top marking orientation with pin1

Examples of identifying marker locations

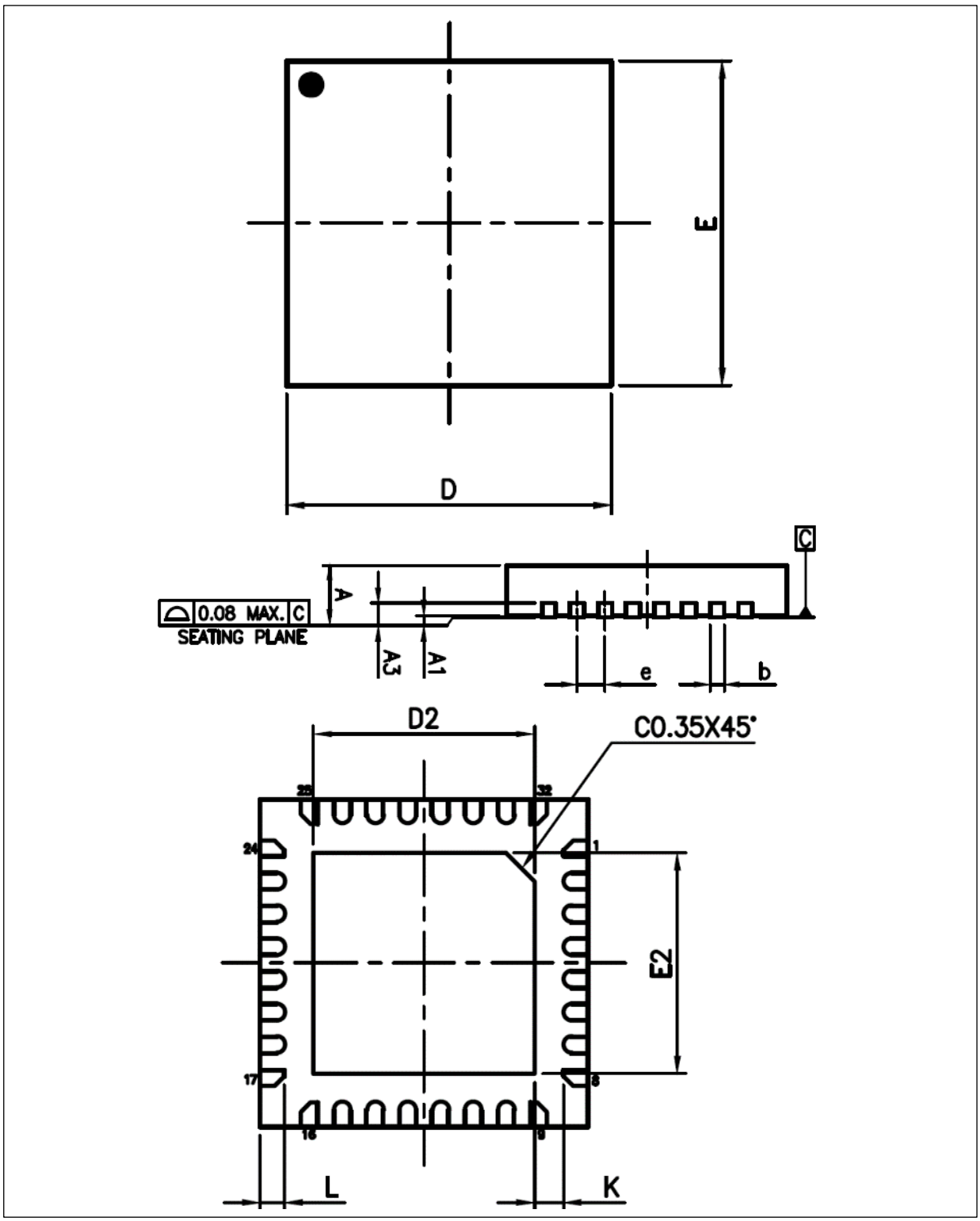
picture37. QFN32 – 5 x 5 mmMarking (Package Top View)



7.4 QFN32-4

encapsulated data

32 – 4 x 4 mm 32Pinned Quad Flat No Leads Package Drawing



(1)Figures are not drawn to scale.

surface49. QFN32 – 4 x 4 mm 32Leaded Quad Flat No Lead Package Mechanical Data

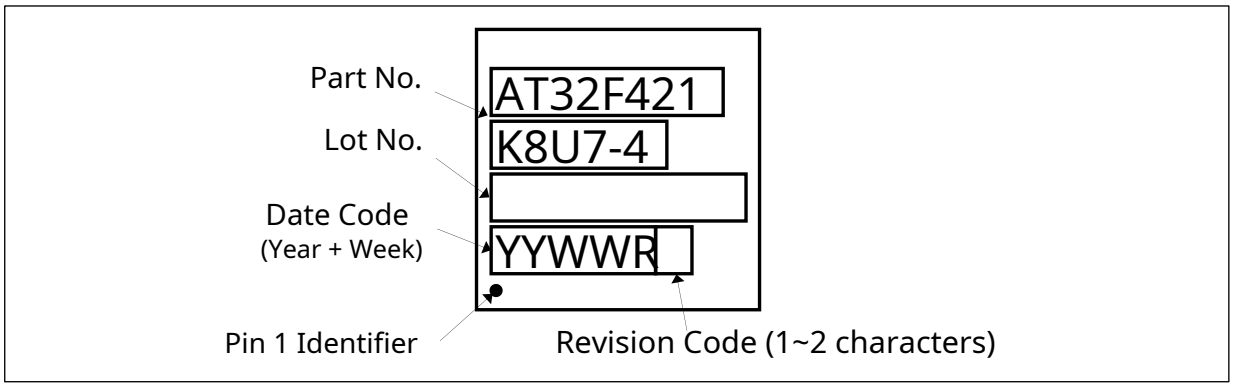
label	mm			inch(1)		
	minimum value	typical value	maximum value	minimum value	typical value	maximum value
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D.	4.00 BSC.			0.157 BSC.		
D2	2.65	2.70	2.75	0.104	0.106	0.108
E.	4.00 BSC.			0.157 BSC.		
E2	2.65	2.70	2.75	0.104	0.106	0.108
e	0.40 BSC.			0.016 BSC.		
K	0.20	-	-	0.008	-	-
L	0.25	0.30	0.35	0.010	0.012	0.014

(1)Inch values are based on mm data according to3It is obtained by rounding to decimal precision conversion.

QFN32 – 4x4mmequipment marking The image below is a top marking orientation with pin1

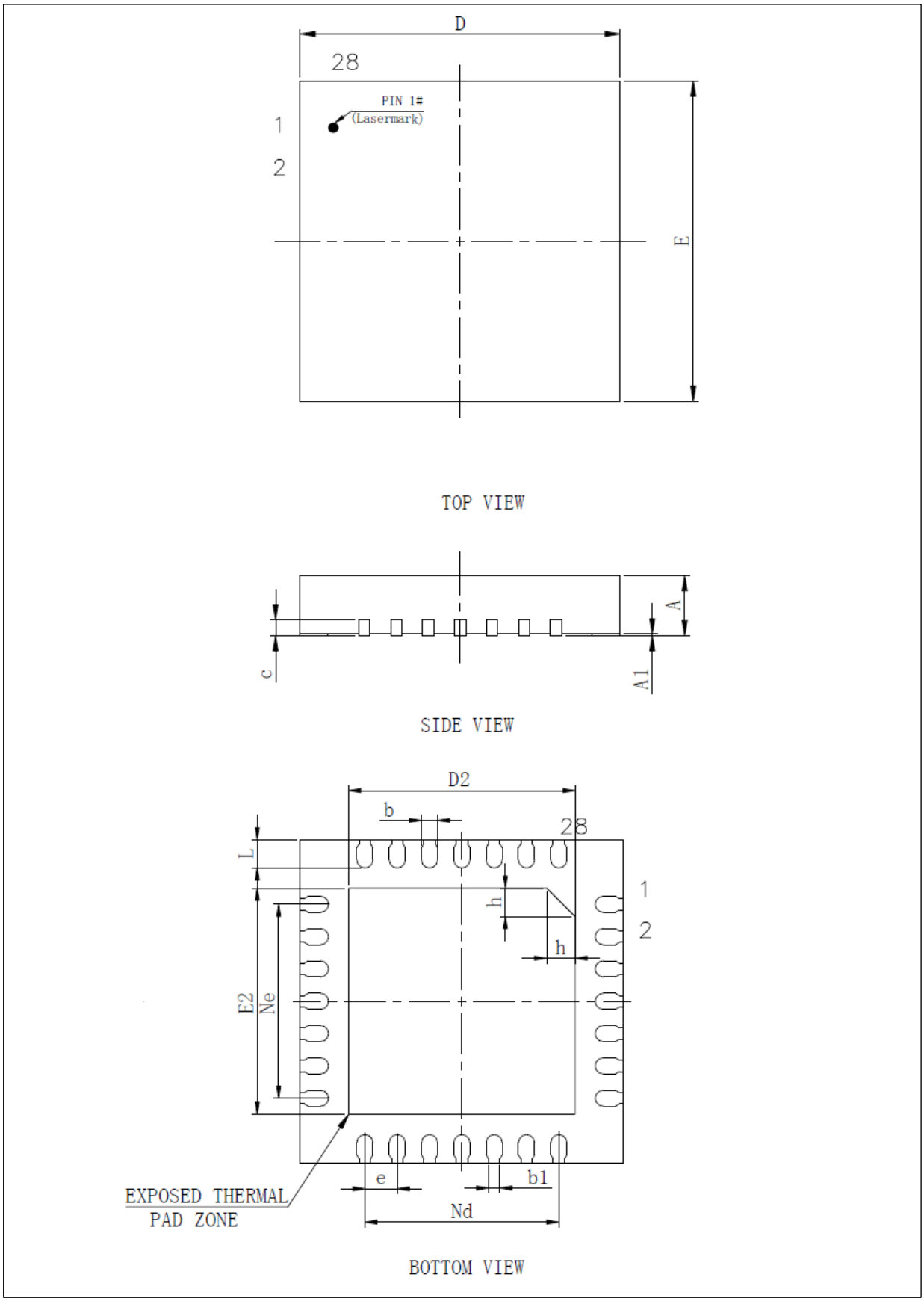
Examples of identifying marker locations

picture39. QFN32 – 4 x 4mmMarking (Package Top View)



7.5 QFN28 – 4 x 4 mmencapsulated data

picture40. QFN28 – 4 x 4 mm 28Pinned Quad Flat No Leads Package Drawing



(1)Figures are not drawn to scale.

surface50. QFN28 – 4 x 4 mm 28Leaded Quad Flat No Lead Package Mechanical Data

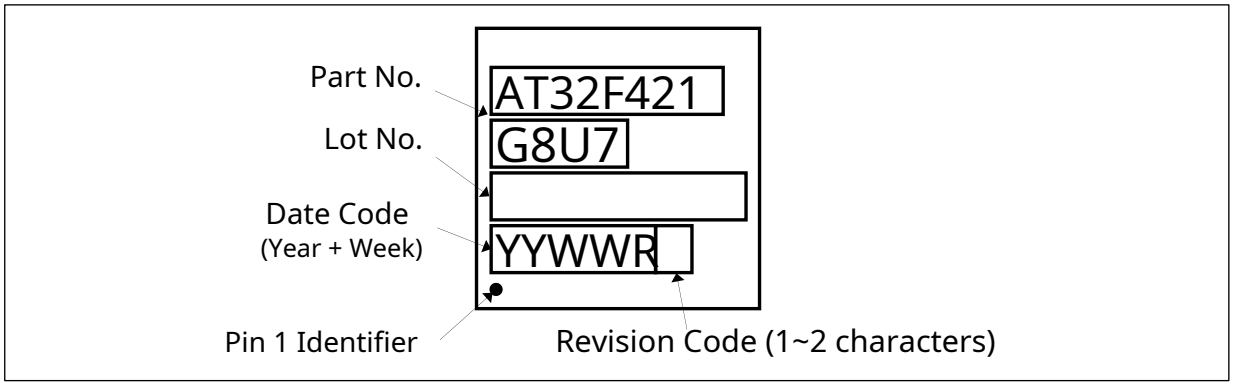
label	mm			inch(1)		
	minimum value	typical value	maximum value	minimum value	typical value	maximum value
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.18	0.20	0.25	0.007	0.008	0.010
D.	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.70	2.80	2.90	0.106	0.110	0.114
e	0.40 BSC.			0.016 BSC.		
Ne	2.40 BSc.			0.094 BSC.		
Nd	2.40 BSc.			0.094 BSC.		
E.	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.70	2.80	2.90	0.106	0.110	0.114
L	0.30	0.35	0.40	0.012	0.014	0.016
h	0.30	0.35	0.40	0.012	0.014	0.016

(1)Inch values are based on mm data according to3It is obtained by rounding to decimal precision conversion.

QFN28 – 4x4mmequipment marking The image below is a top marking orientation with pin1

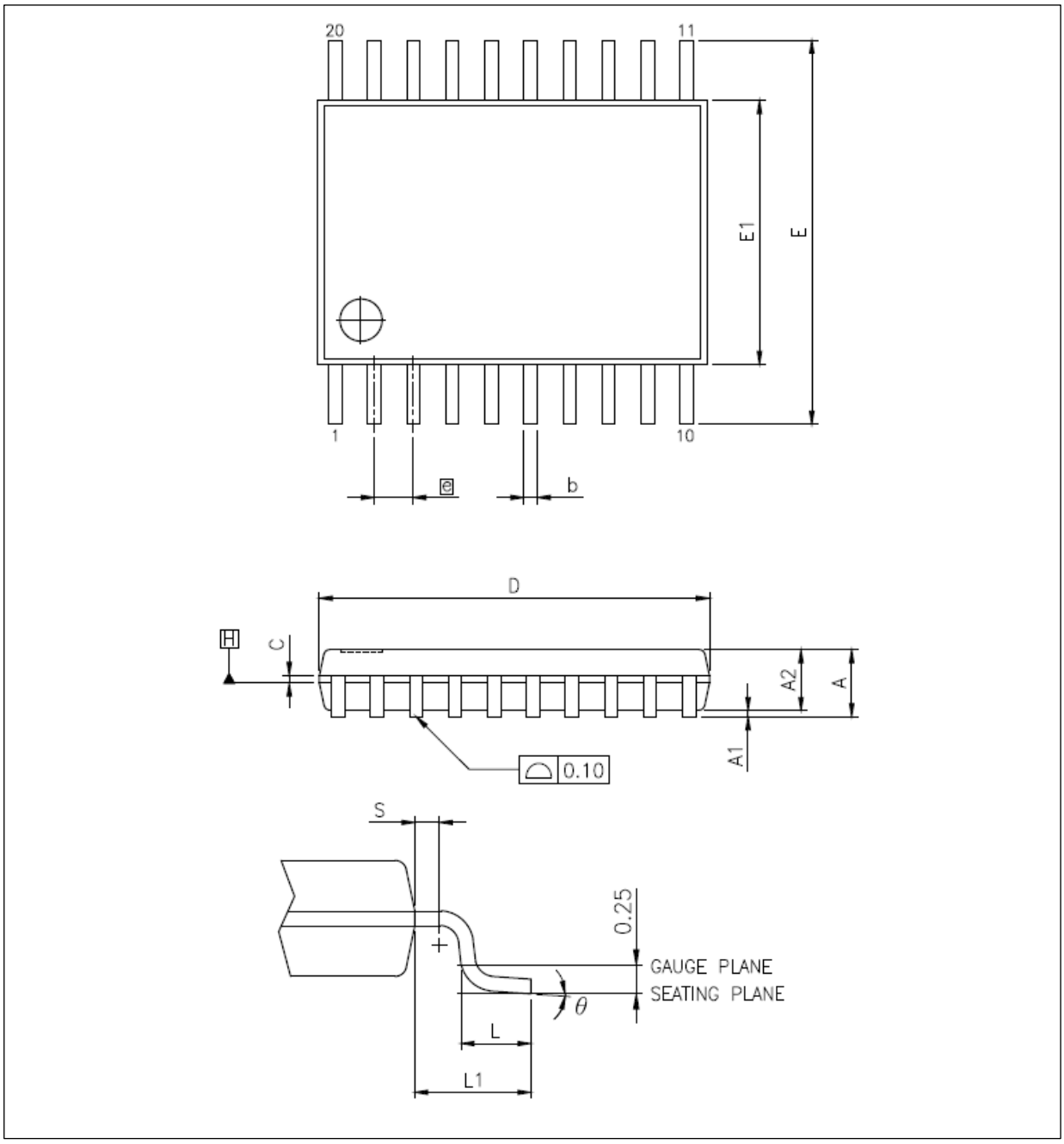
Examples of identifying marker locations

picture41. QFN28 – 4 x 4mmMarking (Package Top View)



7.6 TSSOP20 – 6.5 x 4.4 mmencapsulated data

picture42. TSSOP20 – 6.5 x 4.4 mm 20Pin thin and compact small size package diagram



(1)Figures are not drawn to scale.

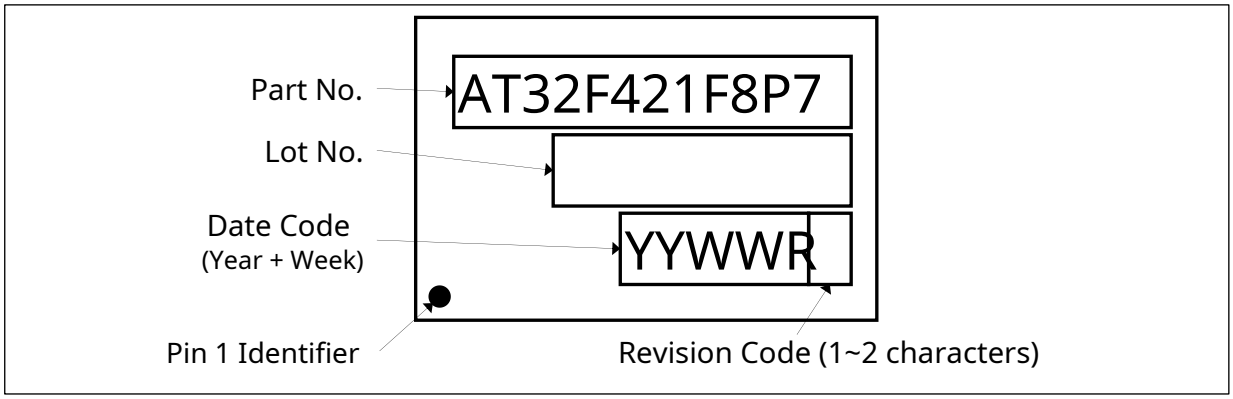
surface51. TSSOP20 – 6.5 x 4.4 mm 20Lead Thin Shrink Small Size Package Mechanical Data

label	mm			inch(1)		
	minimum value	typical value	maximum value	minimum value	typical value	maximum value
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-	0.30	0.007	-	0.012
C	0.09	-	0.20	0.004	-	0.008
D.	6.40	6.50	6.60	0.252	0.256	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E.	6.40 BSc.			0.252 BSC.		
e	0.65 BSC.			0.026 BSC.		
L1	1.00 REF.			0.039 REF.		
L	0.50	0.60	0.75	0.020	0.024	0.030
S	0.20	-	-	0.008	-	-
Θ	0°	-	8°	0°	-	8°

(1)Inch values are based on mm data according to3It is obtained by rounding to decimal precision conversion.

TSSOP20 – 6.5 x 4.4mmequipment marking The image below is a top marking orientation with pin1Examples of identifying marker locations

picture43. TSSOP20 – 6.5 x 4.4 mmMarking (Package Top View)



7.7 thermal properties

The maximum junction temperature of the chip ($T_J$max) must not exceed*surface9*The range of values given. The maximum junction temperature of the chip ($T_J$max) in Celsius

In degrees, it can be calculated with the following formula:

$$T_J max = T_A max + (P_D max \times \Theta_{JA})$$

in:

-$T_A$maxis the maximum ambient temperature, with°Cexpress,

- $\Theta_{JA}$is the junction-to-ambient thermal impedance of the package, with°C/Wmark,

-$P_D$maxyesP_{INT}maxand$P_{I/O}$maxand ($P_D max = P_{INT} max + P_{I/O} max$),

-P_{INT}maxyesI_{DD}andV_{DD}The product of , in watts (Watt) represents the maximum internal power consumption of the chip.

$P_{I/O}$maxis the maximum power dissipation of all output pins:

$$P_{I/O} max = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{Oh}) \times I_{Oh}),$$

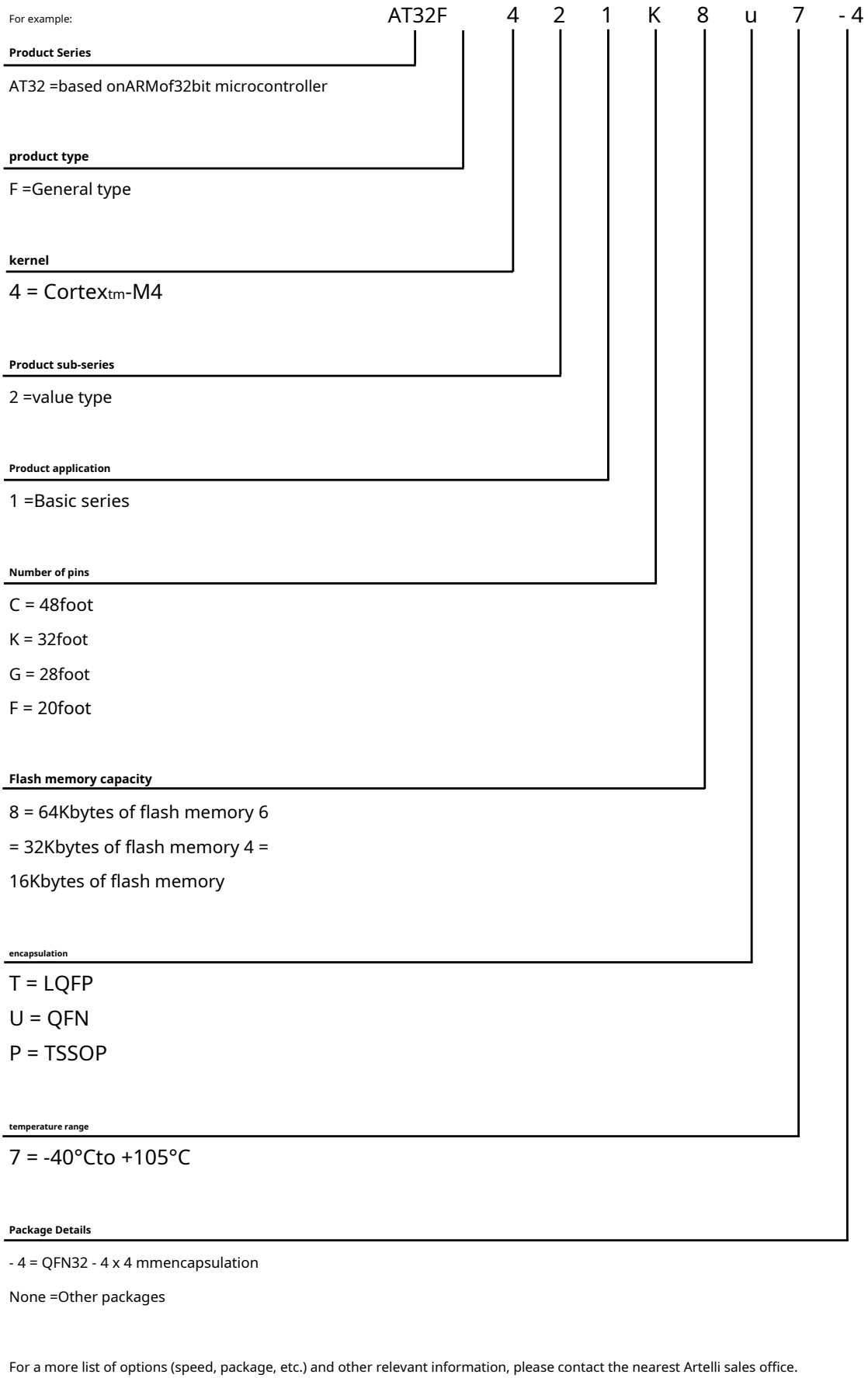
considered in the applicationI/Oon low and high on the actualV_{OL}/ I_{OL}andV_{Oh}/ I_{Oh}.

surface52.Package Thermal Characteristics

symbol	parameter	value	unit
Θ_{JA}	Thermal Impedance Junction to Ambient –LQFP48 – 7 × 7 mm / 0.5 mmspacing	87.0	°C/W
	Thermal Impedance Junction to Ambient –LQFP32 – 7 × 7 mm / 0.8 mmspacing	82.4	
	Thermal Impedance Junction to Ambient –QFN32 – 5 × 5 mm / 0.5 mmspacing	39.8	
	Thermal Impedance Junction to Ambient –QFN32 – 4 × 4 mm / 0.4 mmspacing	44.8	
	Thermal Impedance Junction to Ambient –QFN28 – 4 × 4 mm / 0.4 mmspacing	44.8	
	Thermal Impedance Junction to Ambient –TSSOP20 – 6.5 × 4.4 mm / 0.65 mmspacing	103.0	

8 order code

surface53. AT32F421Series Order Code Information Diagram



For a more list of options (speed, package, etc.) and other relevant information, please contact the nearest Artelli sales office.

9 version history

surface54.Document Version History

date	Version	change
2020.8.17	1.00	original version
2020.9.16	1.01	1.fixpicture1,surface9,andsurface19middleAPB1andAPB2The maximum frequency of120 MHz 2.Revisesurface38middleSPIConditions and maximum values of clock frequency 3.Addsurface30EFTThe test result is3/A (2kV) 4.Addsurface5footnote (4)illustrateQFN28encapsulationPA11andPA12Recommendations for software settings 5.fixpicture2HSI 48 MHzBlock Diagram

IMPORTANT NOTICE - PLEASE READ CAREFULLY

The purchaser is solely responsible for the selection and use of Artly products and services described herein, and Artly disclaims any liability in connection with the selection or use of Artly products and services described herein.

Regardless of any previous representations, this document does not in any way give any express or implied authorization or license to any intellectual property rights. If any part of this document refers to any third-party products or services, shall not be deemed to be an authorization by Yatri to use such third-party products or services, or to license any intellectual property rights therein, or to be deemed to involve in any way the use of any Warranty for such third party products or services or any intellectual property rights therein.

Except as otherwise stated in Artelli's terms of sale, Artelli's use of Artelli's products and/or sold without warranty of any kind, express or implied, including but not limited to merchantability, THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE (AND ITS EQUIVALENCE UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHTS.

Yateli products are not designed or specially designed for the following purposes: (A)Applications with special requirements on safety, such as: life support, active implanted devices or requirements for product functional safety system;(B)Aeronautical applications; (c)automotive applications or automotive environments; (D)aerospace applications or aerospace environments, and/or (E)arms. Because Artellitic products are not designed for the aforementioned applications, and adopt Any unauthorized use thereof by the purchaser in the aforementioned applications, even if the purchaser has given written notice to Artelli, is at the sole risk of the purchaser and is solely responsible for compliance with all laws in such related use and regulatory requirements.

Resale of Arteli products with provisions that differ from the claims and/or technical characteristics set forth in this document will immediately result in any warranty granted by Artelli for the products or services described herein void, and shall in no way create or extend any liability of Artelli.