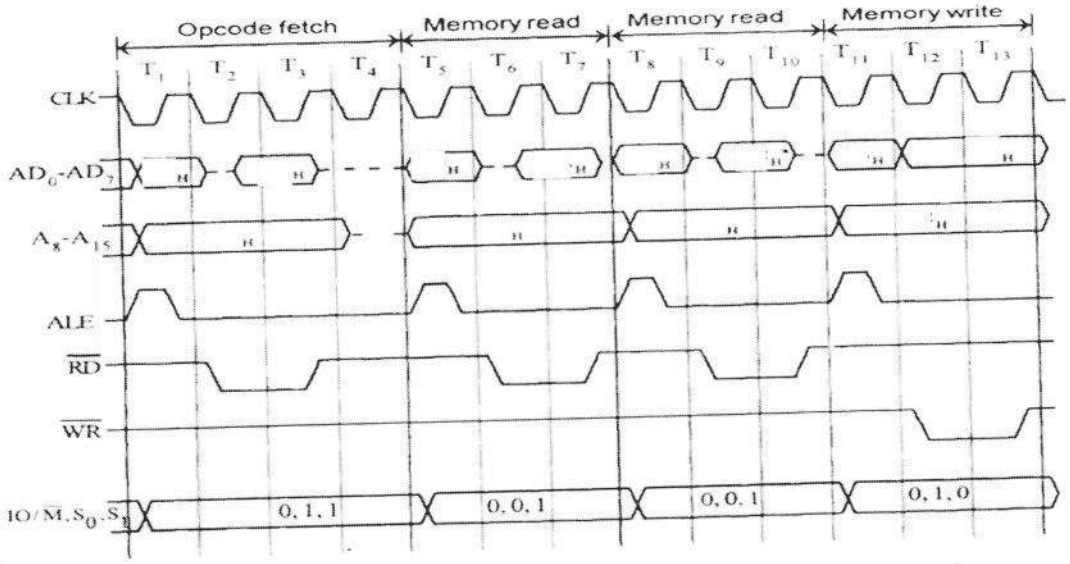
Roll no:

CS321: Midterm Examination (75 points)

Q1: Figure shows the timing diagram of STA 6100H instruction in 8085. Assuming that Accumulation contains 66_H and instruction is stored in memory starting 10FF H, which contains opcode 32H, fill the content of Address and Data bus in the timing diagram (places marked **H**). Show clearly how instruction is stored in memory and explain. Re-draw the timing diagram with answers in the answer booklet.



(5 Points)

Q2. State whether the following sentence is True or false. Give explanation

a)Reading memory from the heap is slower than reading from a local variable allocated on the stack.

b)An 8086 program which uses **lea** instructions can be translated to a functionally equivalent version which does not use any lea instructions.

c) Any two address lines, along with CS signal, determine the selection of a particular port or control register in an 8255.

d)Multiple control word determines the operating mode of 8255.

e)In an 8086 architecture pointers point to locations in memory that are multiples of 16 bits apart.

f) 8086 assembly store the return value is always in ax when a function is finished

(6x2 =12)

(g)

.data

```
count db 100
wVal  dw 2
.code
        mov bl,count
        mov ax,wVal
        mov count,al
        mov ds,45          :(a) what is content of ds
        mov al,wVal        ;(b) what is content of al
        mov ax,count       ;(c) what is content of ax
```

(4)

(h) Fill in the blanks. In an 8086 Processor, If dx = 0000h, ax = 00005h, and bx = 0002h

div bx

ax = ...? dx =.....?

If dx = 0000h, ax = 0005h, and bx = FFFEh

div bx

ax =..... ? dx =..... ?

idiv bx

ax = ...? dx = ...?

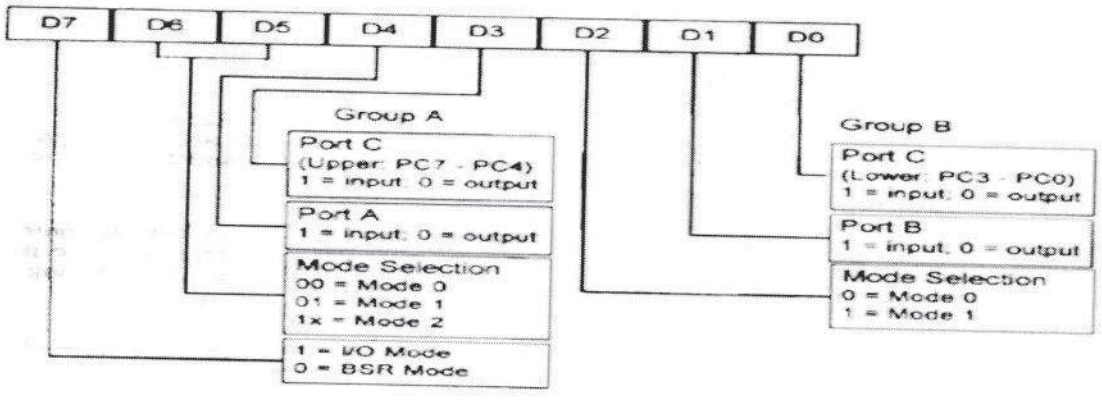
(4)

Q3: Write a 8086 program to calculate the average wage of 5 workers. Each byte represents the daily wages of a worker. Assume a person does not make more than 255 a day. The decimal data is as follows: 128, 235, 197, 91 and 48.

(5 Points)

Q4: In a given **8086** -based system, 8255 interfaced at port A address 0300H and it is an input port for monitoring the temperature. Write Assembly language instructions to monitor that port A continuously for the temperature of 100 degrees. If it reaches 100, sends it to port address B
(use appropriate control word)

(5 Points)



(b) Write an assembly language program that sends values 55H and AAH to I/O

port address 0300H (in the above system); the program toggles the bits of port address 0300H continuously in every 1s. Assume that each instruction take one cycle. The processor operates at 1 MHz. **(5 Points)**

Q5: Consider two different implementations, P1 and P2, of the same instruction set. There are different classes of instructions (A, B, C, D, and E) in the instruction set. The clock rate and CPI of each class is given below.

Machine	Clock	CPI A	CPI B	CPI C	CPI D	CPI E
P1	1 GHz	1	1	2	3	2
P2	1.5Ghz	1	2	3	4	3

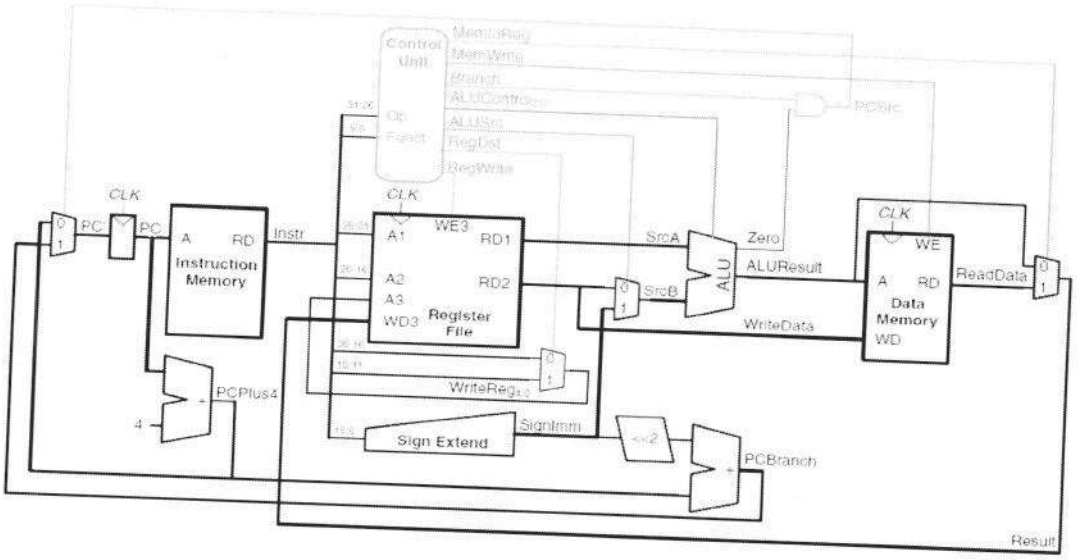
Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence. What are the peak performances of P1 and P2 expressed in instructions per second? CPI(clock per instruction). **(5 points)**

Q6: Translate the following MIPS assembly language statement into machine language.

addi $s0, $s1, 5
addi $t0,$s3, -12
lw $t2, 32($s0)
sw $s1, 4($t1)
($t0, and $s0 reg numbers are registers 8 and 16; opcodes for addi , lw, and sw respectively are 8, 35 and 43.
Give answer in hexadecimal format.

(b) The machine language an instruction is 0x2108ffff. Find the source instruction? **(10 points)**

Q7: A single-cycle MIPS processor structure is shown in Figure. We wish to add instruction **j** (jump) to the single cycle datapath . Add any necessary datapaths and control signal to the single cycle datapath of the Figure . Re-draw the answer (MIPS processor structure) in the answer sheet along with additional modification. **(10 points)**



Q8: Suppose that one of the following control signals in the single-cycle MIPS processor has a *stuck-at-0 fault*, meaning that the signal is always 0, regardless of its intended value. What instructions would malfunction? Why?

(a) *RegWrite* **(5 points)**
(b) *ALUOp1*
(c) *MemWrite*

Q9: Considering the MIPS processor structure is shown in Figure (Question 7)what would the cycle time of the machine? Delay of the individual block is given below.

(5 points)

Element	Parameter	Delay (ps)
register clk-to-Q	t_{pcq}	30
register setup	t_{setup}	20
multiplexer	t_{mux}	25
ALU	t_{ALU}	200
memory read	t_{mem}	250
register file read	t_{RFread}	150
register file setup	$t_{RFsetup}$	20