CS225: Final Examination (2019)

Max Marks: 100 (Answer all questions)

Q1: In IEEE 754 Floating Point Standard, the value of a real number can be represented in scientific binary notation as: Value = $(-1)^{sign} \times Mantissa_2 \times 2^{Exponent} = (-1)^S \times 1.M_2 \times 2^{E\text{-}bias}$ and special cases. Answer the following assuming a IEEE single precision Floating Point Standard.

I. What is the largest, finite, positive value that can be stored using a float? (give answer in 2^p-2^q form)

II. What is the smallest, positive, normalized value that can be stored using float?

III. What are the decimal values of the following floats? 0x-represents hexadecimal form)

(a) 0x80000000 (b) 0xFF94BEEF (c) 0x41180000

(5 Points)

Q2: Given three four-input Boolean functions f1(a, b, c, d) = ∑ m(1, 2, 4, 7)+ ∑ d(3), f2(a, b, c, d) = ∑ m(0, 3, 14)+ ∑ d(15), f3(a, b, c, d) = ∑ m(12, 15)

1. Implement the functions using a minimal network of 4:16 decoders and OR gates.

2. Implement the functions using a minimal network of 3:8 decoders and OR gates.

3. Implement the functions using a minimal network of 2:4 decoders and OR gates.

(10 Points)

Q3: Given a three-input Boolean function f(a, b, c) = Σ m(0, 3, 5, 7) + Σ d(6).

1. Implement the function using a minimal network of 8:1 multiplexers
2. Implement the function using a minimal network of 4:1 multiplexers.
3. Implement the function using a minimal network of 2:1 multiplexers

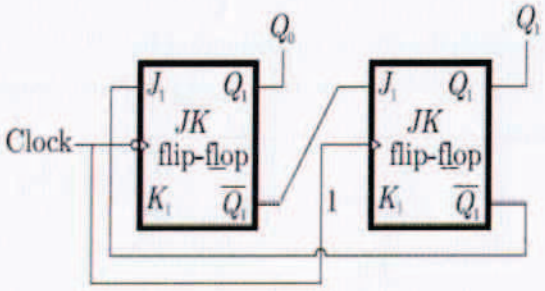
(8 Points)

Q4: Use Karnaugh map to simplify function $f\ (a, b, c, d)$ = Σm (0,4,5,10,11,13,15) + Σd (2, 8, 9, 12) . List all possible minimal sum of products expressions. Show the Boolean expressions. No need for the logic diagram. List the essential prime implicants.

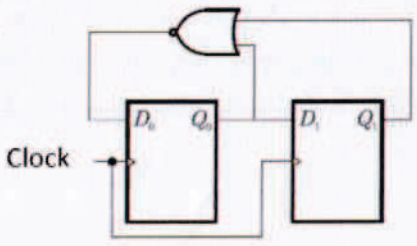
(5 Points)

Q5: Use Karnaugh map to simplify function $f(a,b,c)= \sum m(1,6)+ \sum d(2,7)$. List all possible minimal product of sums expressions. Show the Boolean expressions. No need for the logic diagram. List the essential prime implicants. **(5 points)**

Q6: Consider the following circuits involving two flip-flops. What are the counting states (*Q*0,*Q*1) for the counters shown in the figures below.



(a)

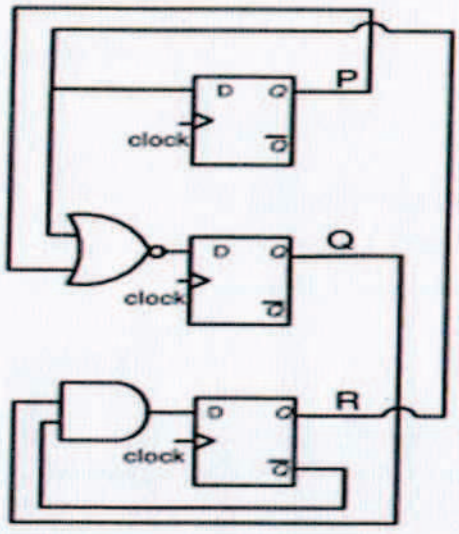


(b)

(8 points)

Q7: Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter? List the states.

(5 points)



Q8: Design a system to detect the pattern "1101" using Moore and Mealy state machine approach. The FSM produces output Y='1' when the last four Cycle input Bits are, from left to right, "1101". Compare the designs. Assume X is the 1 bit input and Y is the output

(16 Points)

Q9: (a) Design a 4 bit register with two control inputs s1 and s0, 4 data inputs I3, I2,I1, and I0 and 4 data outputs Q3, Q2, Q1, and Q0.

When s1s0=00, the register maintains its value.; When s1s0=01, the register loads $I_3I_2I_1I_0$

When s1s0=10, the register loads 0000; When s1s0=11, the register complements itself, so for example 0000 would become 1111, and 1010 would become 0101.

(b) Assume Mux is implemented using basic gates. Estimate the maximum frequency of operation of the above design. Assume the following parameters for each of flops and gates. *D flop:* t_{ccq} = 30 ps; t_{pcq} = 50 ps ; t_{setup} = 60 ps; t_{hold} = 70 ps; Gates: t_{pd} = 35 ps t_{cd} – 25 ps

(12 Points)

Q10: For the following function f(a,b,c)= $\sum$ m(0, 3, 6, 7)

(a) Build Binary Decision Tree
(b) Binary Decision Diagram for the variable order (a > b > c)

(10 Points)

Q11: A computer system has 8-bit wide data bus uses RAM chips of 4Kx1-bit capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 64 K-bytes . Show the address mapping. **(8 Points)**

Q12: State and explain Shannon Expansion Theorem. Illustrate with examples **(8 Points)**