**Design of   a half adder and a Full adder**

Aim
To familiarize logic gate packages and to verify the truth tables of these gates. Study the 74 series IC data sheets.

COMPONENTS REQUIRED:

| SL NO	COMPONENT	SPECIFICATION	QUANTITY
1.	IC	7400	1 no
		7402	1 no
		7432	1 no
		7486	1 no
		7408	1 no
		7404	1 no
2.	Resistor	330Ω, 1/4W	1 no
3.	LED		1 no
4.	Bread Board		1 no

The 7408 is a digital IC in TTL family which contains four AND gates. Every AND gate has two inputs in this dual-in-line packages. For this reason, this is called **quad two input AND gate**. Pin 14 is the supply pin. For TTL devices to work properly, the supply voltage must be between + 4.75V and + 5.25V. This is why, + 5V is the nominal supply voltage specified for TTL devices. Pin 7 is a common ground for the chip. The other pins are the input and output pins.
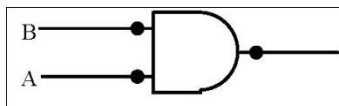
| A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate:

The OR gate performs logical addition. It can have two or more inputs but only a single output. The output assumes the logic 1 state, even if one of its inputs is in the logic 1 state. Its output assumes the logic 0 state, only when each of its input is in logic 0 state. Hence an OR gate is also called as *any* or *all* **gate**. The 7432 IC is a **quad two input OR gate**.
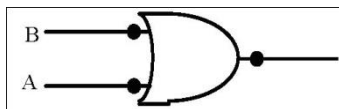
| A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate:

The NOT gate performs a basic logic function called the inversion or complementation. The purpose of the inverter is to change one logic level to the opposite level. This gate has only one input and a single output. The output of a NOT gate assumes logic 1 state when the input is a logic 0 and the output assumes the logic 0 state when the input is a logic 1. The 7404 IC is a **hex inverter**.
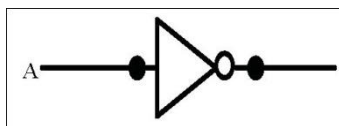
A	Y
0	1
1	0

NAND Gate:

A NOT gate following an AND gate is called a NAND gate. The output of a NAND gate is logic 0, only when each of the inputs assumes a logic 1 level. The NAND is called as a universal gate because of the basic gate can be realized using a NAND gate. The 7400 IC is a quad two input NAND gate.
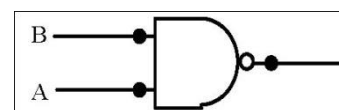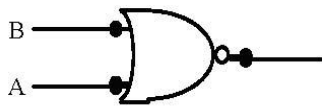

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate:

A NOT gate following an OR gate is called a NOR gate. The output is a logic 1 level only when each of its input assumes a logic 0 level. The NOR gate is also called as universal gate since each of the basic gates can be realized using the NOR gate. The 7402 IC is quad two input NOR gate.

A	B	Y

0	0	1
0	1	0
1	0	0
1	1	0

B

A

X-OR Gate:

An X-OR gate is a two input, one output logic circuit, whose output assumes a logic 1 state when one and only one of its two inputs assumes a logic 1 state. Under the conditions when both the inputs assume logic 0 states, or when both the inputs assume logic 1 state, the output assumes a logic 0 state. Since an X-OR gate produces an output 1 only when the two inputs are not equal, it is called an *inequality detector* **or** *anti-coincidence* **gate**. The output of an X-OR gate is the modulo sum of its two inputs.
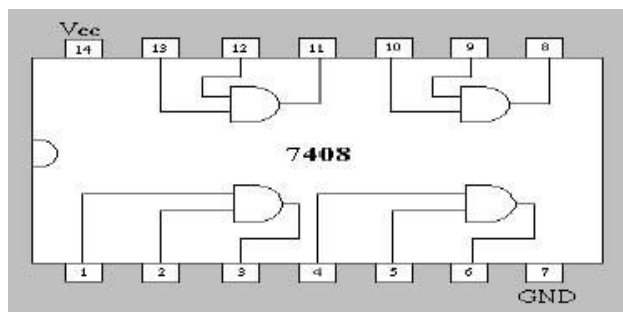
B

A
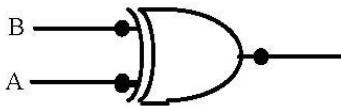
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Check all the components using multimeter.
2. Verify the dual in line package pin out of the IC before feeding the inputs.
3. Setup the circuit and observe the outputs.
4. Enter the input and the output states in the truth table corresponding to the input combinations.
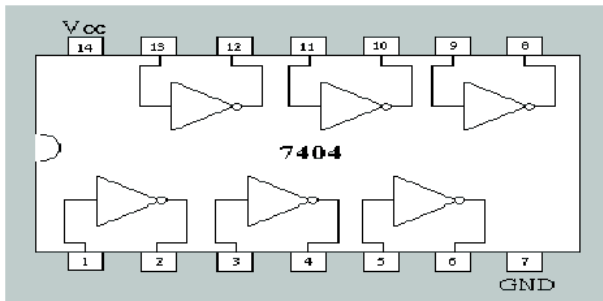
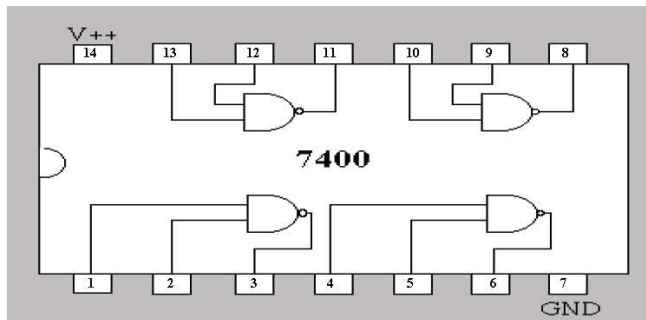## CIRCUIT DIAGRAM:

QUAD TWO INPUT AND GATE:

OBSERVATIONS

7408

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

HEX INVERTER:

A	Y
0	1
1	0

QUAD TWO INPUT NAND GATE:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

QUAD TWO INPUT OR GATE:
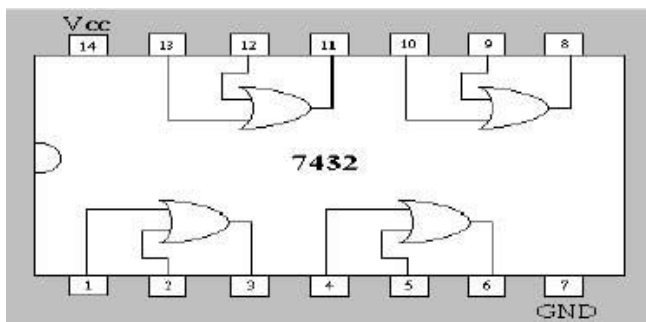
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

QUAD TWO INPUT X-OR GATE:
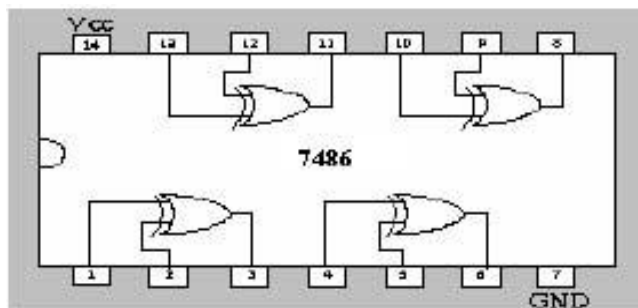
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

QUAD TWO INPUT NOR GATE:

7402 Quad 2-input NOR Gates

Vcc 4B 4A 4Y 3B 3A 3Y
14 13 12 11 10 9 8

1A 1B 1Y 2A 2B 2Y GND
1 2 3 4 5 6 7
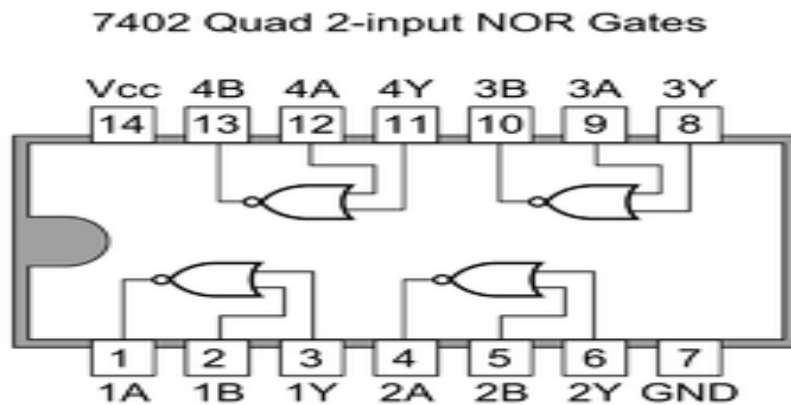
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Part 2: REALIZATION OF LOGIC GATES USING UNIVERSAL GATE (NAND GATES)

COMPONENTS REQUIRED:

SL NO	COMPONENT	SPECIFICATION	QUANTITY
1.	IC	7400	1 no
		7402	1 no
2.	Resistor	330Ω	1 no
3.	LED		1 no
4.	Bread Board		1 no

Logic circuits of any complexity can be realized by using only three logic gates **AND, OR and NOT**.But the NAND or NOR gates can also realize the logic circuits single handedly. Thus the NAND and NOR gates are therefore called the universal building blocks since the foundation of NAND or NOR alone can be used to realize all the other logic gate functions.

The NAND gate implements the NAND function, which is exactly inverted from the AND function. It should be must that, both inputs should have logic 1 signals applied to them in order to obtain the output a 'logic 0'. With either input at logic 0, the output will be held to logic 1.

The circle at the output of the NAND gate denotes the logical inversion, just as it did at the output of the inverter. This shows that it is the AND function itself that is inverted, rather

than each separate input.

As with AND, there is no limit to the number of inputs that may be applied to a NAND function, so there is no functional limit to the number of inputs a NAND gate may have. However, for practical reasons, commercial NAND gates are most commonly manufactured with 2, 3, or 4 inputs, to fit in a 14-pin or 16-pin package.

The NOR gate is an OR gate with the output inverted. Where the OR gate allows the output to be true (logic 1) if any one or more of its inputs are true, the NOR gate inverts this and forces the output to logic 0 when any input is true.

In symbols, the NOR function is designated with a plus sign (+), with an over bar over the entire expression to indicate the inversion. In logical diagrams, the symbol to the left designates the NOR gate. As expected, this is an OR gate with a circle to designate the inversion.

The NOR function can have any number of inputs, but practical commercial NOR gates are mostly limited to 2, 3, and 4 inputs, as with other gates in this class, to fit in standard IC packages.

PROCEDURE:

1. Check all the wires and components that they are in good condition.
2. Setup the circuit and feed the input bit combination.
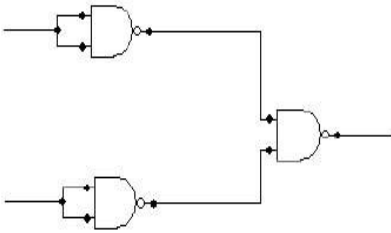3. Observe the output for corresponding input and enter it in the truth table.

CIRCUIT DIAGRAM: **OBSERVATION:**
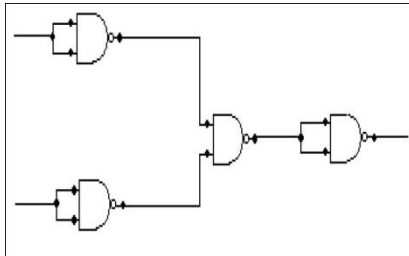
NOR GATE:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

A	B	Y

OR GATE:

0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:
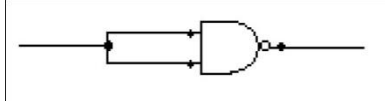
A	Y
0	1
1	0

AND GATE:
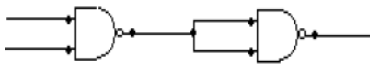
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

XOR GATE:
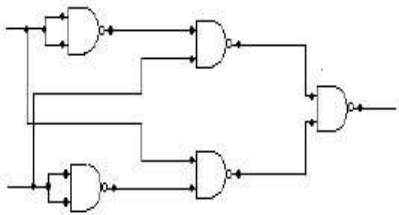
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Task for Lab3:   **(50 points)**

Design and test a half adder and a full adder using basic gates

Submission:
Show the implementation to the TAs and submit hardcopy of the design.