Flnal_Quiz_CS321_26th November 2020

Total points 36/100

Email address *

maheeth2000@gmail.com

✓ When the following code is run ; the value of fun(6) is 2/2

```
typedef struct {
   int a[2];
   double d;
} struct_t;

double fun(int i) {
   volatile struct_t s;
   s.d = 3.14;
   s.a[i] = 1073741824;
   return s.d;
}
```

- ○ 3.14
- ○ Machine Specific (random value)
- ◉ Segmentation fault ✓
- ○ None of these

✓ Consider a program, P, with 1 billion dynamic instructions,50% R-Rype, 10% each of loads and stores, and 30% branches. How long would P take to execute on a single cycle processor with a 100MHz clock? 3/3

- ○ 1s
- ○ 2s
- ◉ 10s ✓
- ○ None of the above

✓ Give answer as (XXH) 2/2

```
LXI SP, 00FF
LXI H, 0107
MVI A, 20H
SUB M
ORI 40H
ADD M
```

What will be the result in the accumulator after the last instruction is executed?

60H ✓

✗ Assuming the following dynamic instruction frequency for a program running on the single-cycle MIPS processor Add- 25%; addi- 25%; beq- 10%; lw-25%; sw- 15% In what fraction of cycles is the sign extend circuit used?? Give answer XX% ···/3

25 ✗

✗ Assuming x,y, and z are floats ; (x + y) + z = x + (y + z)? 0/1

- ○ True
- ○ False
- ◉ can not decide ✗

✓ In MIPS, Jump Register equivalent to ..... instruction X86 1/1

RET ✓

✓ 2. How many cache lines does the cache have? ? (in Part (a)). Give answers as: XX 2/2

For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

32 ✓

✓ Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. 0 0000 001 represents 1/1

- (●) 1/512 ✓
- ( ) 3/512
- ( ) 6/512
- ( ) 1/256
- ( ) Other: _____

✓ The two address lines, along with CS signal, determine the selection of a particular port or control register in an 8255. 1/1

- (●) True ✓
- ( ) False

✗ Compute the cache memory size? (in Part (a)). Give answers as: X Kbytes ···/2

For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

4 ✗

✗ On a write hit, a cache that is write-back will immediately write a value from the cache back to memory 0/2

- (●) True ✗
- ( ) False

✓ Opcode part of MIPS instruction has x bits (give answer in decimal) 1/1

6 ✓

✗ For non-pipelined processor: what is the cycle time for processor (b)? (Give answer in the format: XXXps) ···/2

The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20 ps extra for the registers between pipeline stages.

800ps ✗

✗ Consider a program, P, with 1 billion dynamic instructions,50% R-Rype, 10% each of loads and stores, and 30% branches. Assuming the multicycle processor operated at 400MHz, how long would it take to execute P? 0/3

- ○ 2.75s
- ◉ 8.75s ✗
- ○ 9.75s
- ○ 10.75s

✗ Give answer as (XXXps) ···/3

The multi-cycle has been broken down into 5 steps:
1. Hardware to support an instruction fetch
2. Hardware to support an instruction decode (i.e. a register file read)
3. Hardware to support instruction execution (i.e. the ALU)
4. Hardware to support a memory load or store
5. Hardware to support the write back of the ALU operation back to the register file

Assume that each of the above steps takes the amount of time specified in the table below.
(Fetch:305ps; Decode: 275ps; Execute:280ps; memory:305ps; Write Back:250ps)

Given the times for the datapath stages listed above, what would the *clock period* be for the entire datapath?

430ps ✗

✗ Give answer as XXXXps ···/3

The multi-cycle and pipelined datapaths have been broken down into 5 steps:
1. Hardware to support an instruction fetch
2. Hardware to support an instruction decode (i.e. a register file read)
3. Hardware to support instruction execution (i.e. the ALU)
4. Hardware to support a memory load or store
5. Hardware to support the write back of the ALU operation back to the register file

Assume that each of the above steps takes the amount of time specified in the table below.

Fetch	Decode	Execute	Memory	Write Back
305 ps	275 ps	280 ps	305 ps	250 ps

In a pipelined datapath, assuming no hazards or stalls, how many seconds will it take to execute 1 instruction?

1500ps ✗

✓ Assume variables x, f, and d are of type int, float, and double, respectively. Their values are arbitrary, except that neither f nor d equals +∞, −∞, or NaN. For the following C expression, check whether it will always be true: d > f ⇒ -f > -d 1/1

- (●) Always True ✓
- ( ) Not Always
- ( ) Can not Decide

Name *

Maheeth Reddy

✗ We use dynamic memory because storing data on the stack requires knowing the size of that data at compile time 0/2

- ○ True
- ◉ False ✗

✗ Assuming x,y, and z are unsigned and signed ints; (x + y) + z = x + (y + z)? 0/1

- ○ True
- ○ False
- ◉ can not decide ✗

✗ How many cache lines does the cache have? ? (in Part (b)). Give answer as: XX ···/2

For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

32 ✗

✓ In a x86-32 architecture pointers point to locations in memory that are multiples of 32 bits apart. This statement is 2/2

- ○ True
- ◉ False ✓

✗ Compute the cache memory size? (in Part (b)). Give answers as: X Kbytes ···/2

For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

4 ✗

✓ In MIPS, Jump And Link equivalent to ..... instruction X86 1/1

call ✓

✗ Suppose that " ALUOp1" in the single-cycleMIPS processor has a stuck-at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction? 0/1

- ○ R-type
- ○ lw
- ○ addi
- ◉ all of the above ✗

✓ In a x86-64 architecture pointers point to locations in memory that are multiples of 64 bits apart. 1/1

- ○ True
- ◉ False ✓

✓ In an 8086 Microprocessor, given that the IP = 1230H and CS = 0100H What is the physical address of the code. 2/2

- 1230H
- 1330H
- 22300
- 02230 ✓

✓ Assuming the following dynamic instruction frequency for a program running on the single-cycle MIPS processor Add- 25%; addi- 25%; beq- 10%; lw-25%; sw- 15% In what fraction of all cycles is the data memory accessed (either read or written)? Give answer XX% 2/2

40% ✓

✗ Increasing the associativity of a cache is the best way to improve the hit rate when accessing values from an array in order. 0/2

- True ✗
- False

✓ Opcode part of MIPS instruction has x bits (give answer in decimal) 1/1

6 ✓

✗ When the following code is run ; the value of fun(2) is 0/2

```
typedef struct {
   int a[2];
   double d;
} struct_t;

double fun(int i) {
   volatile struct_t s;
   s.d = 3.14;
   s.a[i] = 1073741824;
   return s.d;
}
```

- (●) 3.14 ✗
- ( ) Machine Specific (random value)
- ( ) Segmentation fault
- ( ) None of these

✓ Suppose that "RegWrite" in the single-cycleMIPS processor has a stuck-at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction? Why? 2/2

- ( ) R-type
- ( ) lw
- ( ) addi
- (●) all of the above ✓

✕ Pipelined processor: What is the cycle time for processor (a)? (Give answer in the format: XXXXps) ···/2

The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20 ps extra for the registers between pipeline stages.

0780ps ✕

✕ For pipelined processor: what is the cycle time for processor (b)? (Give answer in the format: XXXps) ···/3

The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20 ps extra for the registers between pipeline stages.

780ps ✕

✗ Suppose that " MemWrite" in the single-cycle MIPS processor has a stuck-at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction? Why? 0/1

- ○ R-type
- ○ sw
- ○ addi
- ◉ all of the above ✗

✗ What is the cache line size? (in Part (b)). 0/2

For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

- ○ 16
- ◉ 32 ✗
- ○ 64
- ○ none of these
- ○ Other: _____

✕ Who is right? 0/3

Three programmers are debating how best to write the code to transpose a matrix in a C software package that will run on a variety of different machines. The exact details of the different computers aren't known. What is known is that all of them have caches and virtual memory. The matrix is much too large to fit entirely in the caches, but it is small enough to fit in main memory, so virtual memory paging is not an issue. The array is normal C array of doubles stored in row-major order. Alice says that this code will do the best overall job:

```
for (i = 0; i < N; i++) {
        for (j = 0; j < N; j++) {
        temp = A[i][j];
        A[i][j] = A[j][i];
        A[j][i] = temp;
                }
        }
```

Bob says that this is all wrong and that the performance will be much better if it's written this way:

```
for (j = 0; j < N; j++) {
        for (i = 0; i < N; i++) {
        temp = A[i][j];
        A[i][j] = A[j][i];
        A[j][i] = temp;
                }
        }
```

Chris says it doesn't matter. The code will perform about the same either way.

Who's right?

- ○ Chris
- ◉ Alice ✕
- ○ Bob
- ○ None of them

✗ When the following code is run ; the value of fun(3) is 0/2

```
typedef struct {
   int a[2];
   double d;
} struct_t;

double fun(int i) {
   volatile struct_t s;
   s.d = 3.14;
   s.a[i] = 1073741824;
   return s.d;
}
```

- ○ 3.14
- ◉ Machine Specific (random value) ✗
- ○ Segmentation fault
- ○ None of these

✕ When the following code is run ; the value of fun(0) is ···/2

```
typedef struct {
   int a[2];
   double d;
} struct_t;

double fun(int i) {
   volatile struct_t s;
   s.d = 3.14;
   s.a[i] = 1073741824;
   return s.d;
}
```

- (●) 3.14 ✕
- ( ) Machine Specific (random value)
- ( ) Segmentation fault
- ( ) None of these

✗ When the following code is run ; the value of fun(1) is 0/2

```
typedef struct {
   int a[2];
   double d;
} struct_t;

double fun(int i) {
   volatile struct_t s;
   s.d = 3.14;
   s.a[i] = 1073741824;
   return s.d;
}
```

- (●) 3.14 ✗
- ( ) Machine Specific (random value)
- ( ) Segmentation fault
- ( ) None of these

✗ A RET instruction is equivalent to 0/1

- (●) pop sp ✗
- ( ) pop ip
- ( ) pop a
- ( ) push sp

✓ Condition: exp = 111...1; Case: exp = 111...1, frac = 000...0; This represents? 1/1

- ○ Operation that overflows
- ○ Both positive and negative
- ◉ Represents value infinity ✓
- ○ None of these
- ○ All of the above

✓ Condition: exp = 111...1; Case: exp = 111...1, frac ≠ 000...0; This represents? 1/1

- ○ Operation that overflows
- ○ Both positive and negative
- ○ Represents value infinity
- ◉ Not-a-Number (NaN) ✓
- ○ All of the above

✓ Functional Part of MIPS instruction has x bits (give answer in decimal) 1/1

6 ✓

Roll Number *

1801CS31

✓ Assume variables x, f, and d are of type int, float, and double, respectively. Their values are arbitrary, except that neither f nor d equals +∞, −∞, or NaN. For the following C expression, check whether it will always be true: x == (int)(float) x — 1/1

- ○ Always True
- ◉ Not Always ✓
- ○ Can not Decide

✓ Jump instruction has x bits for address (give answer in decimal) — 1/1

26 ✓

✗ Multiple control word determines the operating mode of 8255. — 0/1

- ◉ True ✗
- ○ False

✗ Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. 0 1110 110 represents (give answer in decimal) — …/1

224 ✗

✗ Reading memory from the heap is slower than reading from a local variable allocated on the stack. This statement is 0/2

- (●) True ✗
- ( ) False

✗ Give answer as (XXH) ···/2

The following program start at location 0100H.
LXI SP, 00FF
LXI H, 0107
MVI A, 20H
SUB M
The content of accumulator when the program counter reaches 0109H is:

20H ✗

✗ For non-pipelined processor: what is the cycle time for processor (a)? (Give answer in the format: XXXXps) ···/2

The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20 ps extra for the registers between pipeline stages.

0780ps ✗

✓ Consider a program, P, with 1 billion dynamic instructions,50% R-Rype, 10% each of loads and stores, and 30% branches. Assuming a multicycle processor where R-type instructionstake 4 cycles, loads and stores 5 cycles, and branches 3cycles, what is the CPI of P? 3/3

- ○ 2.8
- ○ 3
- ◉ 3.9 ✓
- ○ 3.8

✓ What is the cache line size? (in Part (a)) 2/2

For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

	Tag	Index	Offset
a.	31-10	9-5	4-0
b.	31-12	11-6	5-0

- ◉ 32 bytes ✓
- ○ 16 bytes
- ○ 64 bytes
- ○ None of these

✓ Assume variables x, f, and d are of type int, float, and double, respectively. Their values are arbitrary, except that neither f nor d equals +∞, −∞, or NaN. For the following C expression, check whether it will always be true: d * d >= 0.0 1/1

- (●) Always True ✓
- ( ) Not Always
- ( ) Can not Decide

✗ X86 assembly store the return value is always in ..... when a function is finished 0/2

- (●) ebx ✗
- ( ) eax
- ( ) ecx
- ( ) esp
- ( ) Other: _____

✗ Microarchitecture: Implementation of the architecture. One of the examples is 0/1

- ( ) The byte-level programs that a processor executes
- ( ) A text representation of machine code
- ( ) cache sizes and core frequency
- (●) instruction set specification ✗

✕ Give answer as (XXH) ···/4

```
1          MVI  B,87H
2          MOV  A, B
3  START:  JMP  NEXT
4          MVI  B, 00H
5          XRA  B
6          OUT  PORT 1
7          HLT
8  NEXT:   XRA  B
9          JP   START
10         OUT  PORT 2
11         HLT
```

What is the output at PORT 2

00H ✕