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CS 321: Computer Architecture

End-Semester Exam. Max Marks: 35 (70 Pt), Max Time: 180 minutes, Nov 2017

(No electronic equipment (Mobile, Calculator etc.) is allowed)

(Instructions: You must show your complete work. Marks will be awarded only based on what appears in your answer book. Please explicitly mention your assumptions, if it is essential and not given in the question.)

Answer to all Questions

1. Assume that you have the following sequence of pipelined instructions in an MIPS (5-stage: IF, ID, EX, DM, WB) processor with appropriate full forwarding architecture:

```
lw  $10, 0($7)
add $12, $9, $8
sub $11, $10, $12
```

   (a) Where will the data operands that are processed during the EX stage of the subtract (sub) instruction come from? Specify clearly through a diagram (inserting line(s)). [4]

   (b) Specify the condition(s) to detect hazard(s) so the forward to take place in this architecture. [4]

2. Let the memory stage(DM) of the above architecture is divided into two stages (M1, M2), so it has become MIPS-6 stage and appropriate full forwarding (as discussed in class) has been considered. Let you have the following sequence of pipelined instructions.

```
lw  $9, 0($7)
add $12, $9, $8
sub $11, $9, $5
```

   (a) Show how the instruction sequence would progress through this 6-stage pipeline. Draw proper line, only if forwarding helps. [7]

   (b) How many total clock cycles are required to complete this sequence of Instructions. [3]

3. (a) Assume the cache is organized in following two different approaches. Approach-1: There are more data elements per block and fewer blocks . Approach-2: there are fewer elements per block but more blocks. Note that in both the approaches cache size is same and direct mapping has been used. Answer to the point as follows (Pro, Cons, Useful for which data access type like Sequential or random or both) with proper justification, for both the approaches. [6]

   (b) In a two level memory hierarchy if the top level has an access time of 10ns and bottom level has an access time of 100ns, what is the hit rate in the top level required to result an average access time of 20ns. [4]

4. (a) Draw the hardware logic of a 4-way set associative cache of size 512KB and Byte addressable 256MB (physical address) Main memory with block of 8-bytes. Show the field size for tag, line and word. [3+3=6]

(b) Write the hexa decimal values of tag, line and word fields for the following physical address [6]

(i) 0xA68432C (ii) 0x 0C84116.

(c) Write the physical address of the last byte in the cache line containing those addresses as under.

(i) 0xA68432C (ii) 0x 0684116 [4]

5. A byte organized memory chip with 21 bit address bus is used as a building block in a larger memory organization.

(a) Calculate the capacity of the above chip. [1]
(b) If the above chip is used to build a 32 MB long word organized (32 bit word size) memory, calculate the number of chips needed and the way it is organized . [3]
(c) Specify the new Memory Address map, and the Memory Connections to the CPU for this new 32-bit word-organized memory with 21-bit address bus. Specify the address range of first memory chip. [4]

6. (a) Write an ISA program of to read one line from the Keyboard [6]

(b) Distinguish between Memory mapped I/O and Isolated I/Othe way they operate. State pro and cons. [5]

7. (a) Assume a 5 stage multicycle (IF,ID,EX, DM,WB) processor as discussed in class receives an interrupt signal while the instruction (I) is in ID stage. Explain precisely step wise the task performed showing the level of instruction and the stage. [4]

(b) Consider your PC has a mouse used with graphical user interface. For this case what would you prefer to use (Polled I/O or Interrupt driven. Justify. [3]

Good Luck