CS 321- Quiz 2

Total points 48/100

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Assume variables x, f, and d are of type int, float, and double, respectively. Their values are arbitrary, except that neither f nor d equals +∞, −∞, or NaN. For the following C expression, check whether it will always be true: (f+d)-f == d 0/1

- (●) Always True
- ( ) Not Always
- ( ) Other: _____

Q2: Assuming all initial values registers are zero, In the following snippet of code the content of DE pair after the execution is ..... (ans: XXXXH) ···/2

```
LXI B, AABBH,
MOV C,A
LXI SP,4000H
PUSH H
POP D
```

_____

QXX3: The widths of data bus(DB) and address bus(AB) of 8085 microprocessor are _____and _____ respectively.(Ans: XX and XX) 2/2

08 and 16

Q2: PUSH PSW moves content of the following register(s) to stack (use notations, A, B,C, D, E,H, L and F) 2/2

A and F

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The value of 01111 111 (give answer one of the following, x.xxx, neg infinity, pos infinity, NAN) ···/1

In 8085, the longest instruction is ..... ···/3

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The value of 01110 111 is (give answer as one of the followings: x.xxx, neg infinity, pos infinity, NAN) ···/1

..... instruction is usually placed at the end of subroutine/procedure 2/2

RET

Q2: Assuming all initial values registers are zero, In the following snippet of code the content of DE pair after the execution is ..... (ans: XXXXH) ···/2

```
LXI B, AABBH,
MOV C,A
LXI SP,4000H
PUSH B
POP D
```

Q2: CZ (Call if zero) instruction combines the functions of ..... and ..... (Ans: Mnemonic 1 and Mnemonic 2) ···/3

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The maximum posit ive De- normalised number is (Ans:0.XXXX) ···/1

The number of hardware interrupts (which require an external signal to interrupt) present in an 8085 microprocessor are 0/1

- 1
- 2
- 5
- 13
- Other: _____

QXX: HL register pair can be used as a 0/2

- Data pointer
- Memory pointer
- Stack Pointer
- option 1 and option 2
- Other: _____

Name *

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MVI B, 3EH is an example of ..... addressing mode. ···/1

_____

Q2: The content of register A after the execution of the following code is (Ans: XXH) ···/2

```
MVI A,,44
STA C00AH,
MOV C,A
LXI H,C00A
ADD M
```

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The value of 01111 101 (give answer as one of the following, x.xxx, neg infinity, pos infinity, NAN) ···/1

Qxx: In an intel 8085 microprocessor, why is READY signal used? 0/2

- ○ To indicate to user that the microprocessor is working and is ready for use
- ○ To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device
- ○ To slow down a fast peripheral device so as to communicate at the microprocessor's device
- ○ None
- ○ Other: _____

Assume variables x, f, and d are of type int, float, and double, respectively. Their values are arbitrary, except that neither f nor d equals +∞, −∞, or NaN. For the following C expression, check whether it will always be true: d*d >= 0.0 0/1

- ○ Always True
- ○ Not Always
- ○ Other:

Roll Number *

1801CS31

Q7 Nine_ints are 9-bit signed two's complement integers. Nine_floats are 9-bit floating point numbers with 4 bits for the exponent, 4 bits for the fraction, and 1 bit for the sign. Nine_floats are similar to IEEE floating point as far as layout of sign, exponent and fraction and represent special values (e.g. 0, pos and neg infinity, NAN) similar to how they are represented in 32 bit IEEE floating point. (Ans: xxx) ···/1

7. The largest positive number we can represent with **Nine_ints?**

511

Q2: To store the following snippet of code requires .....bytes of memory (XX) ···/2

```
MVI A, 33H
MVI B, 78H
ADD B
CMA
ANI 32H
```

Q2: The following five instructions were executed on an 8085 microprocessor. The Accumulator content after SUB M instruction is ..... (Ans: XXH) ···/2

```
MVI A,44H
STA C00AH,
MOV C,A
LXI H,C00AH
CMP M
SUB M
```

In 8085, on execution of .....instruction, the top of stack is loaded in Program Counter (PC). ···/2

Q5:Which one of the following addressing technique is not used in 8085 microprocessor? 1/1

- ○ Register
- ○ Immediate
- ◉ Relative
- ○ Register indirect

QXX1: In 8085 name of the 16 bit registers is 0/1

- ○ Stack pointer
- ○ Memory pointer
- ○ Stack pointer and Memory pointer
- ◉ Program counter
- ○ Other: _____

Qx: An 8085 microprocessor executes “LDA 2400H” with starting address location 1000H . While the instruction is fetched and executed, the sequence of values written at the address pins A15 – A8 is 3/3

- (●) 10H, 10H,10H
- ( ) 10H, 10H,11H
- ( ) 10H, 10H,11 H
- ( ) 10H, 00H,10H
- ( ) Other: _____

Q2: Instruction CZ (Call if zero) takes ..... T states to execute in 8085 (Ans: XX) 2/2

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CMA is an example of ..... addressing mode. …/1

Implied

In the 8085 microprocessor, the RST6 instruction transfers the program execution to the .....location (XXXXH) 2/2

0030H

MOV A, M is an example of ..... addressing mode. …/1

Register indirect

Q2: The content of register A after the execution of the following code is (Ans: XXH) 2/2

```
MVI A,,44H
STA C00AH,
MOV C,A
LXI H,C00AH
INX H
ADD M
```

44H

LDA 1050H is an example of ..... addressing mode. ···/1

Direct

Q2:The following five instructions were executed on an 8085 microprocessor. 2/2
The Accumulator value immediately after the execution of the fifth instruction is

```
MVI A, 33H
MVI B, 78H
ADD B
CMA
ANI 32H
```

- ○ 00H
- ◉ 10H
- ○ 11H
- ○ 32H

The address/data bus in 8085 is 1/1

- ◉ Multiplexed
- ○ Demultiplexed
- ○ Decoded
- ○ Encoded
- ○ Other: _____

Q2: In the following snippet of code the content of stack pointer after the execution of PUSH B instruction is (ans: XXXXH) ···/2

```
LXI B, AABBH,
MOV C,A
LXI SP,4000H
PUSH B
POP D
```

4000H

QAA: In 8085 microprocessor address line for RST3 is .....(Ans: XXXXH) 2/2

0018H

Q4 2/2

In a hypothetical 10 bit processor uses 10 bit Floating point representation and assumes the following format

1bit sign	4 bit Exponent	5 bit Mantissa

4. The minimum De-normalized number that can be represented in the system is?

- (●) 0.00048828125
- ( ) 0.0009765625
- ( ) 0.001953125
- ( ) None of these

Q2: To run the following snippet of code requires .....T states (XX) 2/2

```
LXI B, AABBH,
MOV C,A
LXI SP,4000H
PUSH B
POP D
```

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Q6: . In 8085 microprocessor system with memory mapped I/O, which of the following is true? 3/3

- ○ Devices have 8-bit address line
- ○ Devices are accessed using IN and OUT instructions
- ○ There can be maximum of 256 input devices and 256 output devices
- ◉ Arithmetic and logic operations can be directly performed with the I/O data

The flags are altered after execution of ..... instructions ···/1

every

QX: Which one of the following is not a vectored interrupt?s 0/2

- ○ TRAP
- ○ INTR
- ○ RST 7.5
- ◉ RST 3
- ○ Other:

MOV A, B is an example of ..... addressing mode. ···/1

Register

Qx: An 8085 microprocessor executes “LDA 2400H” with starting address location 1000H . While the instruction is fetched and executed, the sequence of values ALE in the first clock of every machine cycle respectively are 2/2

- [ ] 1,0,1,0
- [ ] 1,1,0,0
- [x] 1,1,1,1
- [ ] 0,1,1,1
- [ ] Other: _____

_____ Interrupt has the highest priority in 8085 microprocessor. 2/2

TRAP

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The representation for 5/8 is (give answer in binary eg: 11000001) 1/1

00110010

Qx: An 8085 microprocessor executes “STA 1234H” with starting address location 1FFEH (STA copies the contents of the Accumulator to the 16-bit address location). While the instruction is fetched and executed, the sequence of values written at the address pins A15 – A8 is 0/3

- ○ 1FH,1FH,20H,12H
- ○ 1FH,1FEH,1FH,12H
- ○ 1FH,1FH,12H,12H
- ○ 1FH,1FH,12H,20H,12H
- ◉ Other: 1FH,1FH,20H,20H

Q2: In the following snippet of code the content of stack pointer after the execution of POP D instruction is (ans: XXXXH) 2/2

```
LXI B, AABBH,
MOV C,A
LXI SP,4000H
PUSH B
POP D
```

4000H

Q2: To store the following snippet of code requires .....bytes of memory (XX) 2/2

```
LXI B, AABBH,
MOV C,A
LXI SP,4000H
PUSH B
POP D
```

09

QZZ: _____ instruction is required to rotate the content of accumulator one bit right along with carry 2/2

RAR

QQ:The cycle required to fetch and execute an instruction in a 8085 microprocessor is which one of the following? 0/1

- ○ Clock cycle
- ○ Memory cycle
- ◉ Machine cycle
- ○ Instruction cycle

Assume variables x, f, and d are of type int, float, and double, respectively.Their values are arbitrary, except that neither f nor d equals +∞, −∞, or NaN. For the following C expression, check whether it will always be true: d == (double)(float) d 1/1

- ○ Always True
- ◉ Not Always
- ○ Other: _____

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The representation for 5/8 is (give answer in decimal: -X.XX) ···/2

0.62

Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent bits, and 3 fraction bits. The minimum positive De- normalised number is (Ans:0.XXXX) ···/1

0.0019

Q2: While calling a subroutine/procedure using CALL instruction, the address of next instruction of the program is stored in..... ···/2

Q2:The following five instructions were executed on an 8085 microprocessor. The Accumulator value immediately after the execution of the fifth instruction is 2/2

```
MVI A, 33H
MVI B, 78H
ADD B
CMA
ANI 32H
```

- ○ 00H
- ◉ 10H
- ○ 11H
- ○ 32H

Qx: An 8085 microprocessor executes “LDA 2400H” with starting address location 1000H . While the instruction is fetched and executed, the sequence of values written at the address pins A7 – A0 is (opcode for LDA: 3A) 3/3

- ○ 00H,3AH,01H,00H,02H, 24H, 03H, 03H
- ○ 00H,3AH,01H,00H,02H, 20H, 03H, 00H
- ○ 00H,3AH,01H,00H,02H, 24H, 03H, 20H
- ◉ 00H,3AH,01H,00H,02H, 24H, 03H, 00H
- ○ Other: _____

QXX1: 8085 microprocessor can support _____different instructions(Ans:XX) ···/2

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Q9 : Which of the following statements for Intel 8085 is correct? 3/3

- ○ Program Counter (PC) specifies the address of the instruction last executed
- ○ PC specifies the address of the instruction being executed
- ◉ PC specifies the address of the instruction to be executed
- ○ PC specifies the number of instructions executed so far
- ○ Other: _____