Switching Theory Lab – CS226

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Lab No.: 8

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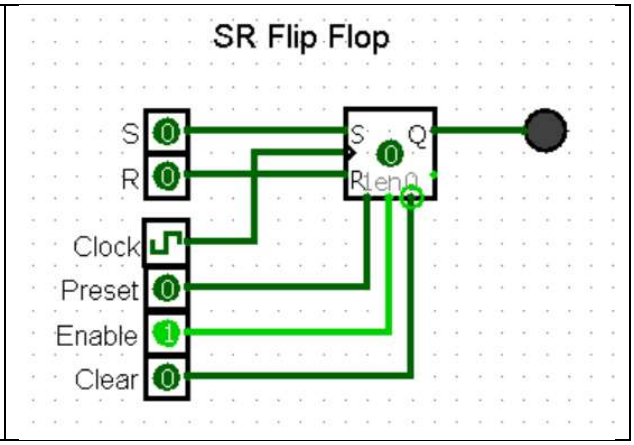
0 Ans.:

SR Flip Flop

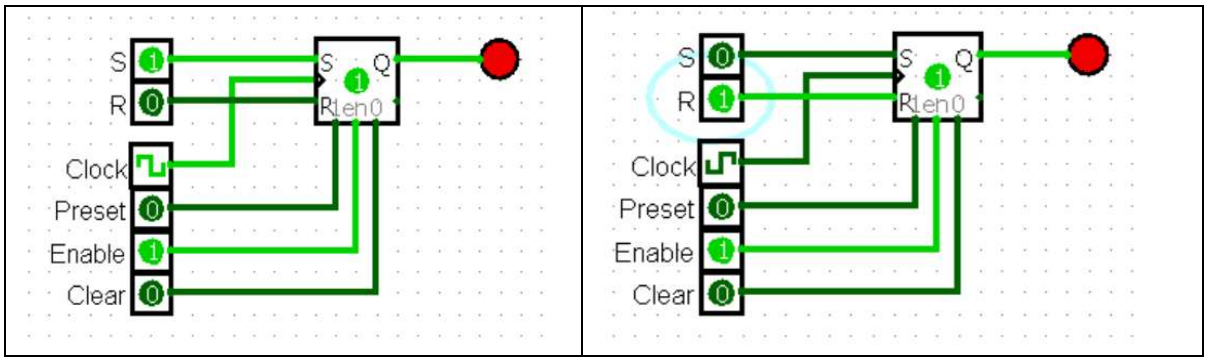
Clock	S	R	Q(t)	Q'(t)	State
0	X	X	Q(t-1)	Q'(t-1)	Memory
1	0	0	Forbidden		
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q(t-1)	Q'(t-1)	Memory

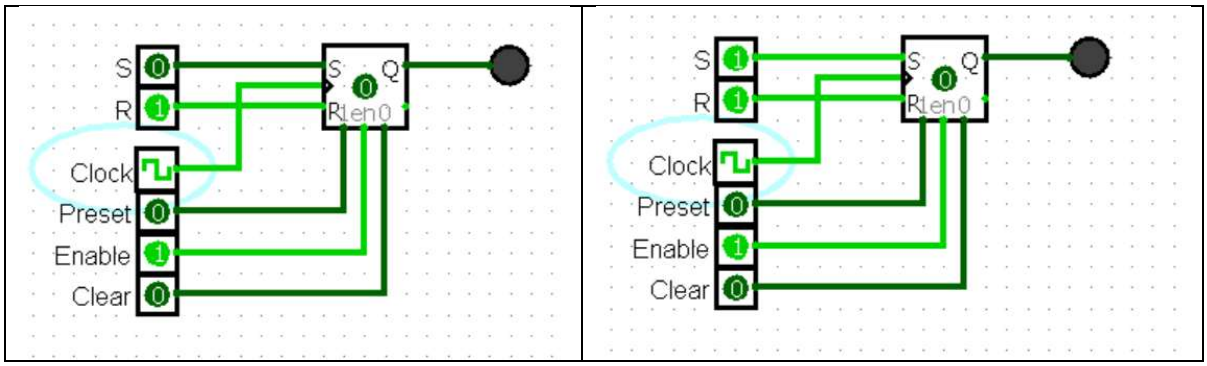
Truth Table



Test Case:

1. Set S = 1, followed by Clock = 1, notice Value stored = 1 (Set State)
2. Set Clock = 0, change S and R randomly, no change in Value stored (Memory State)
3. Set S = 0, R = 1, then Clock = 1, notice Value stored = 0 (Reset State)
4. Set Clock = 0
5. Set S = 1, R = 1, then Clock = 1, no change in Value stored (Memory State)

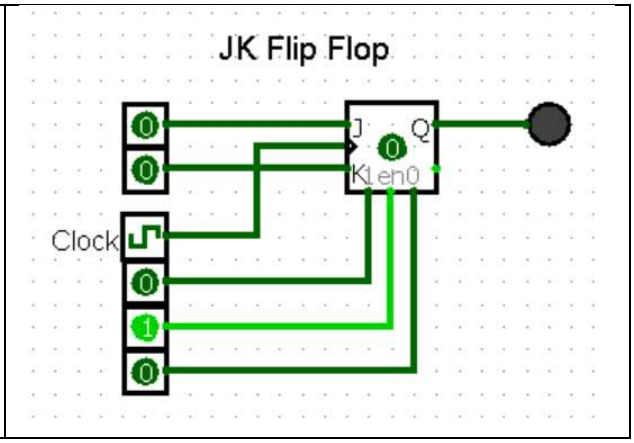




JK Flip Flop

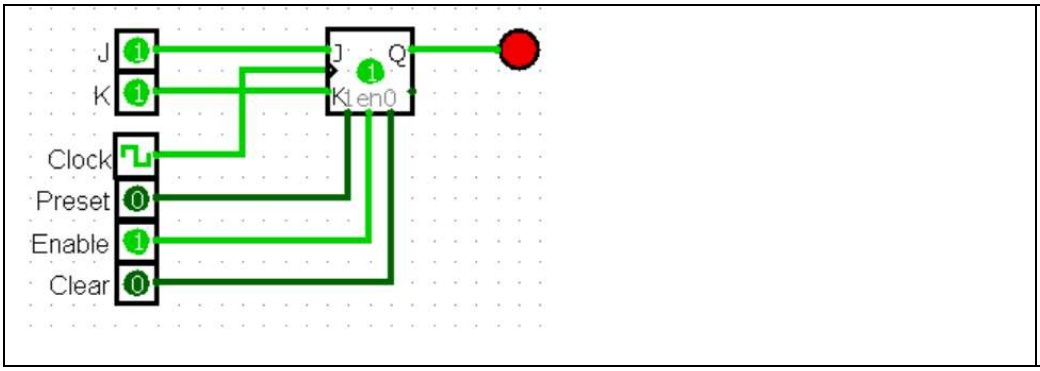
Clock	J	K	Q(t)	Q'(t)	State
0	X	X	Q(t-1)	Q'(t-1)	Memory
1	0	0	Q(t-1)	Q'(t-1)	Memory
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q'(t-1)	Q(t-1)	Toggle

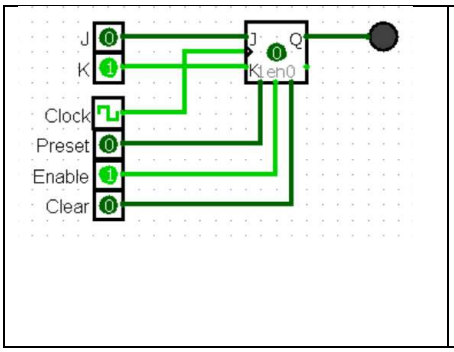
Truth Table

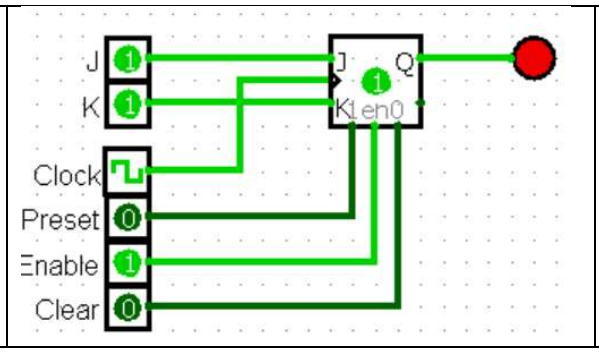


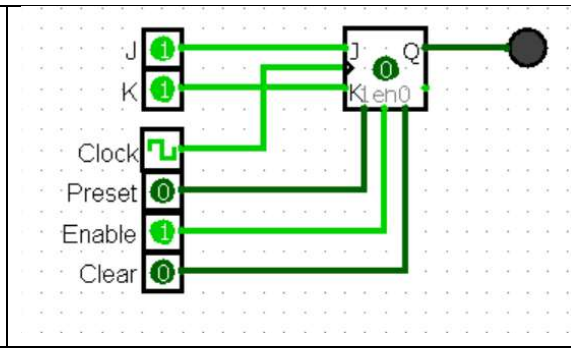
Test Case:

1. Set J = 1, K = 1 followed by Clock = 1, notice Value stored = 1 (Set State)
2. Set Clock = 0, change J and K randomly, no change in Value stored (Memory State)
3. Set J = 0, K = 1, then Clock = 1, notice Value stored = 0 (Reset State)
4. Set Clock = 0
5. Set J = 1, K = 1, and keep toggling the clock, notice value stored also toggles (Toggle State)





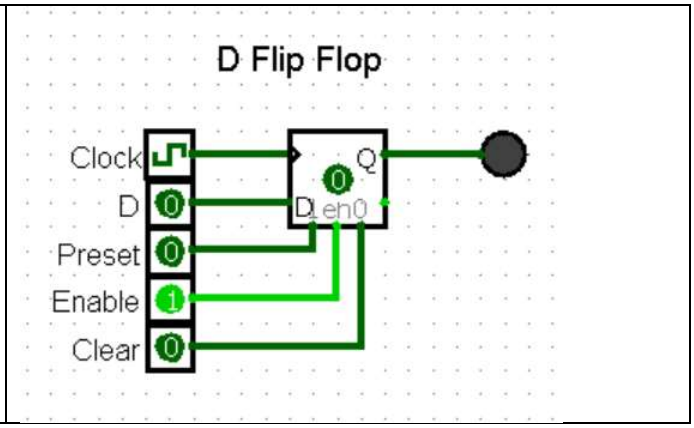




D Flip Flop

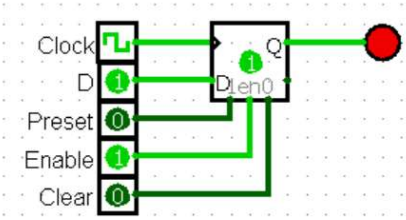
Clock	D	Q(t)	State
0	X	Q(t-1)	Memory
1	0	0	Reset
1	1	1	Set

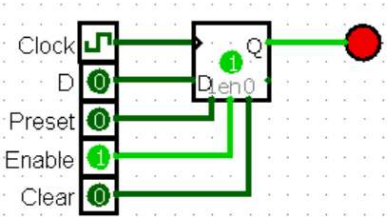
Truth Table

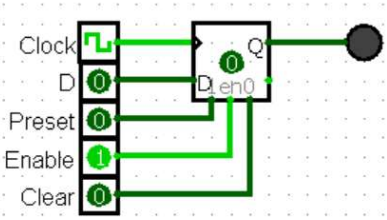


Test Case:

1. Set Clock = 1, D = 1, notice Value Stored = 1
2. Set Clock = 0, Value stored doesn't change on changing D (Memory)
3. Set D = 1, Clock = 1, notice Value Stored = 1



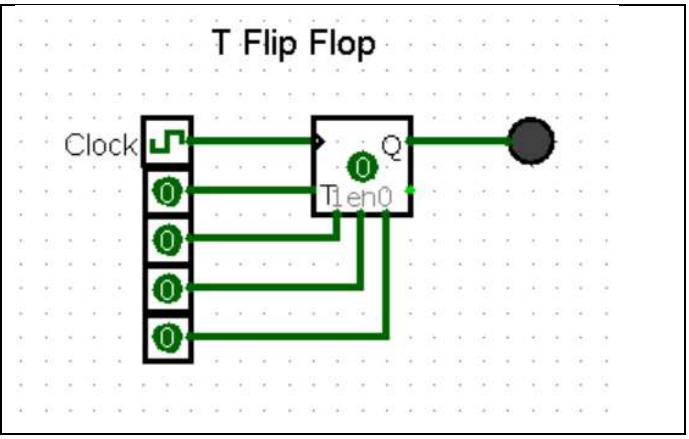




T Flip Flop

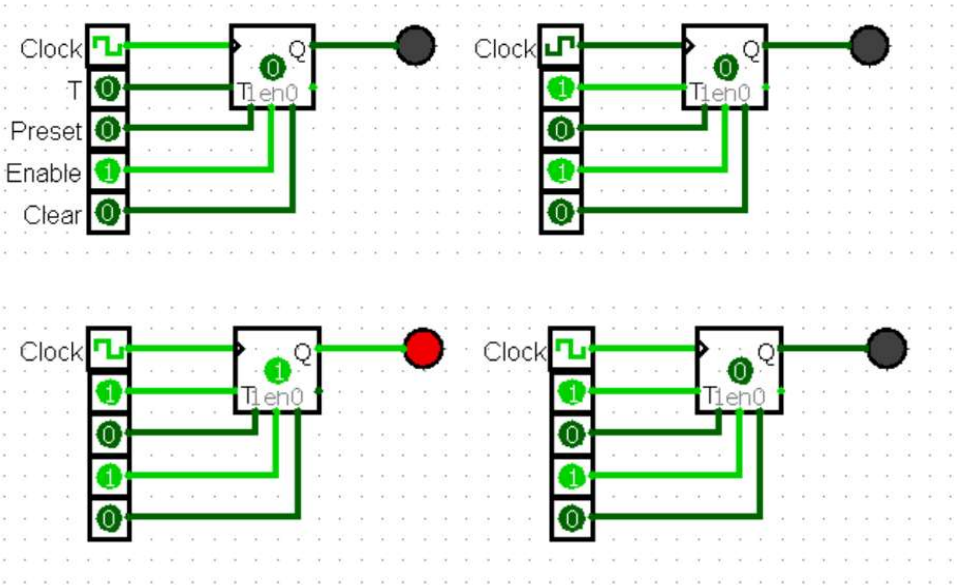
Clock	T	Q(t)	State
0	X	Q(t-1)	Memory
1	0	Q(t-1)	Memory
1	1	Q'(t-1)	Toggle

Truth Table



Test Case:

1. Set Clock = 1, T = 0, notice no change in Value Stored
2. Set Clock = 0, Value stored doesn't change on changing T (Memory)
3. Set T = 1, Clock = 1, and keep toggling the clock, notice Value stored also toggles



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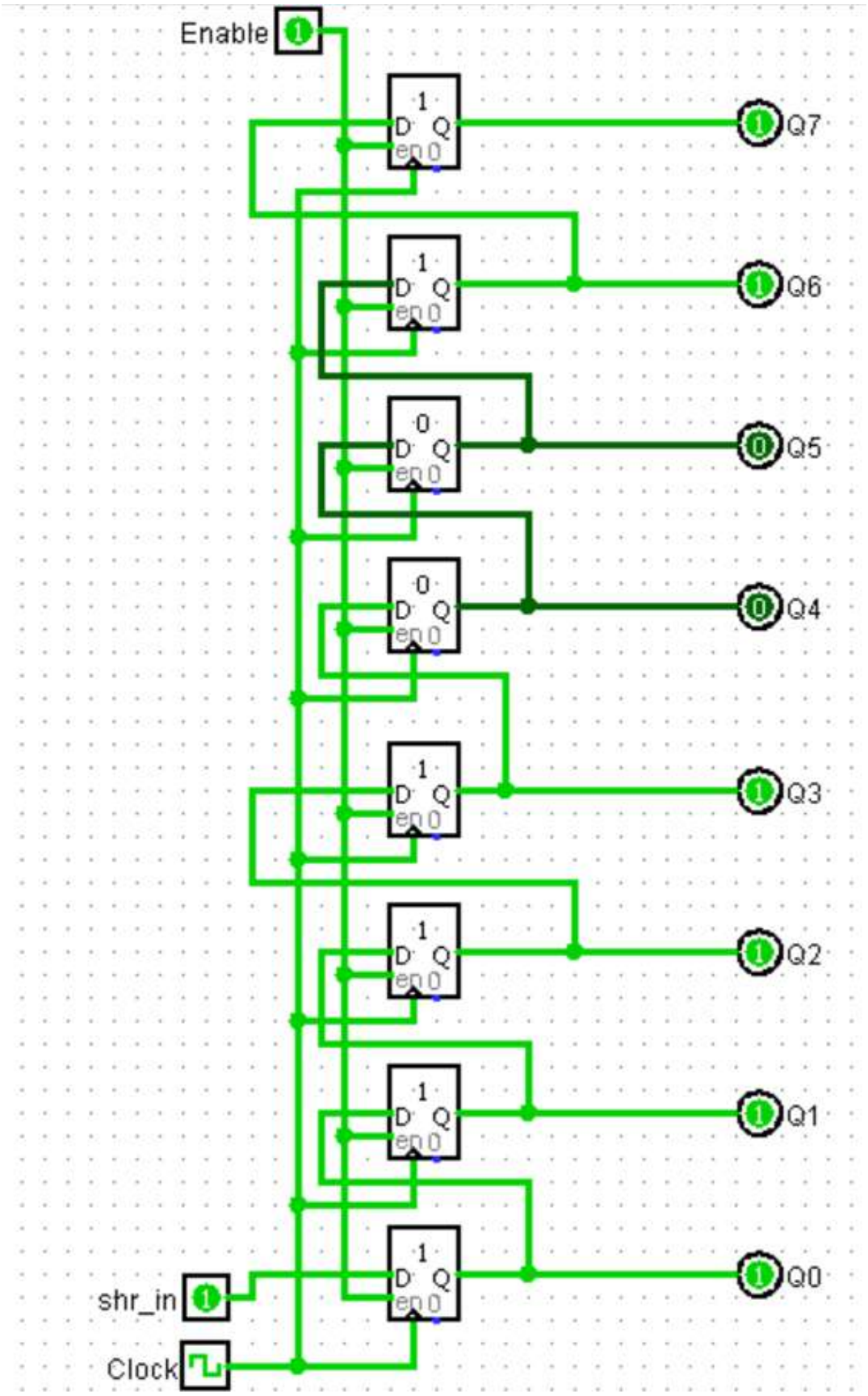
1 Ans.:

Storing D_{in} = 11001111 in 8-bit Shift Register

Screenshot taken after LSB has been input

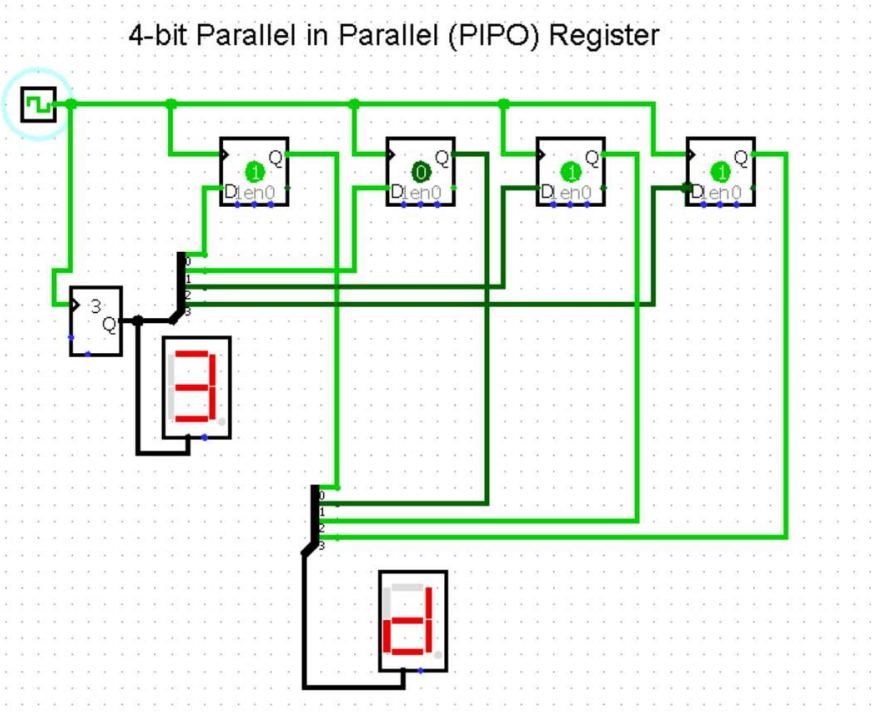
As you can see MSB is at the top-most Output Pin and LSB at bottom-most Output pin


Enable
1
D Q
en 0
Q7
Q6
0
Q5
Q4
Q3
Q2
Q1
Q0
shr_in
Clock

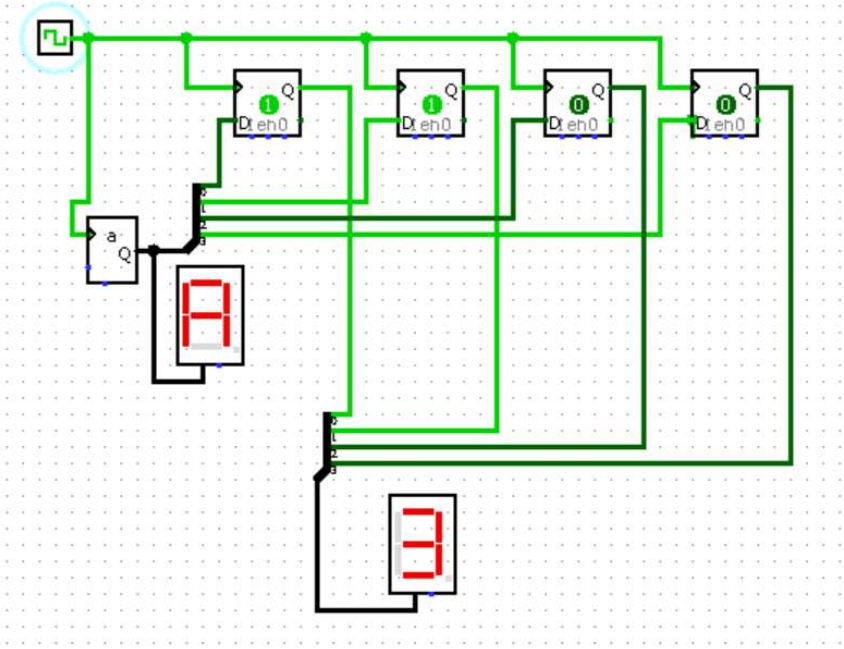
2 Ans.:

Simulated 4-bit PIPO Register:

Step 1: Input = 3 (Input has been stored)

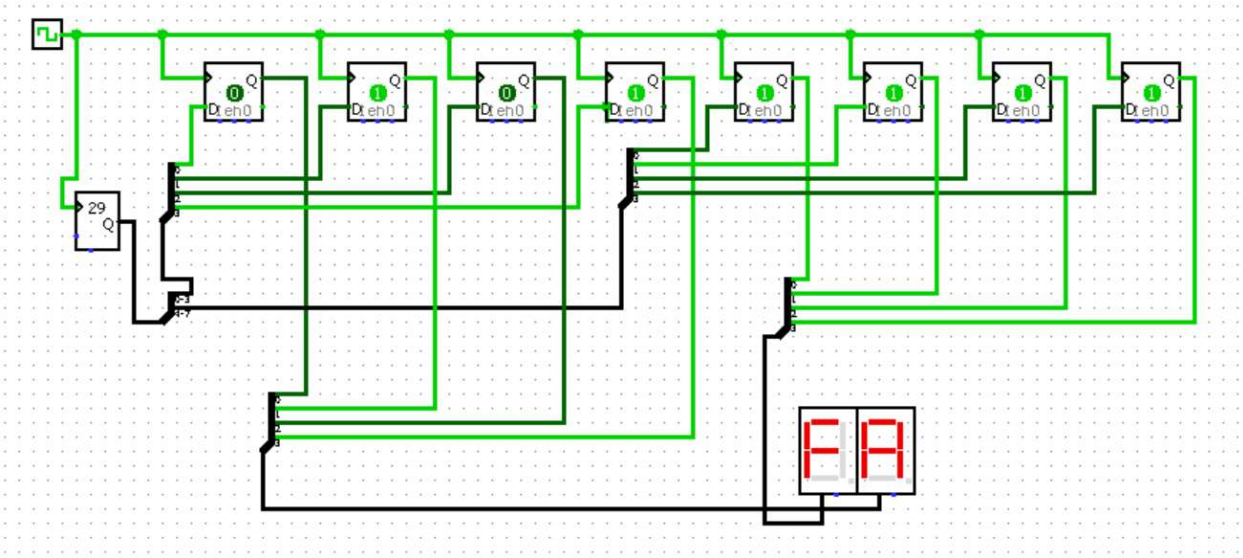


Step 2: Output = Stored Value = 3

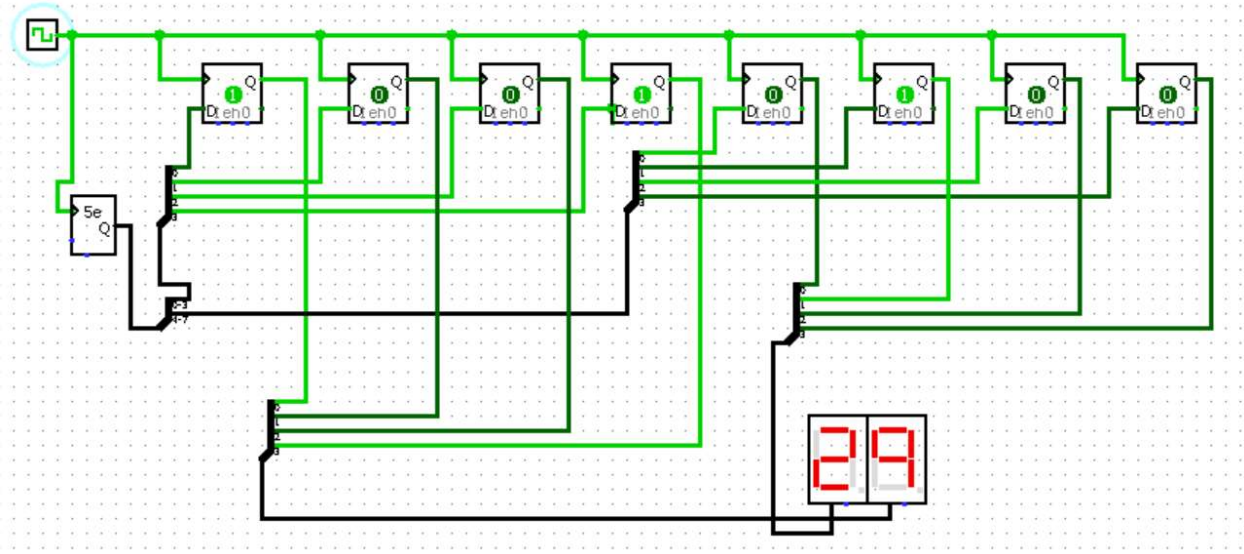


Designed an 8-bit PIPO Register:

Step 1: Input = 29 (Input has been stored)



Step 2: Output = Stored Value = 29



In case of a PIPO Register, data storage and data retrieval occur in parallel mode. In the registers shown above, each flip-flop stores an individual bit of the data appearing as its input at the instant of the first clock pulse. Also, at the same instant, the bit stored in each individual flip-flop also appears at their respective output pins. In this way, both data storage and data recovery occur at the same, single clock pulse in PIPO registers.

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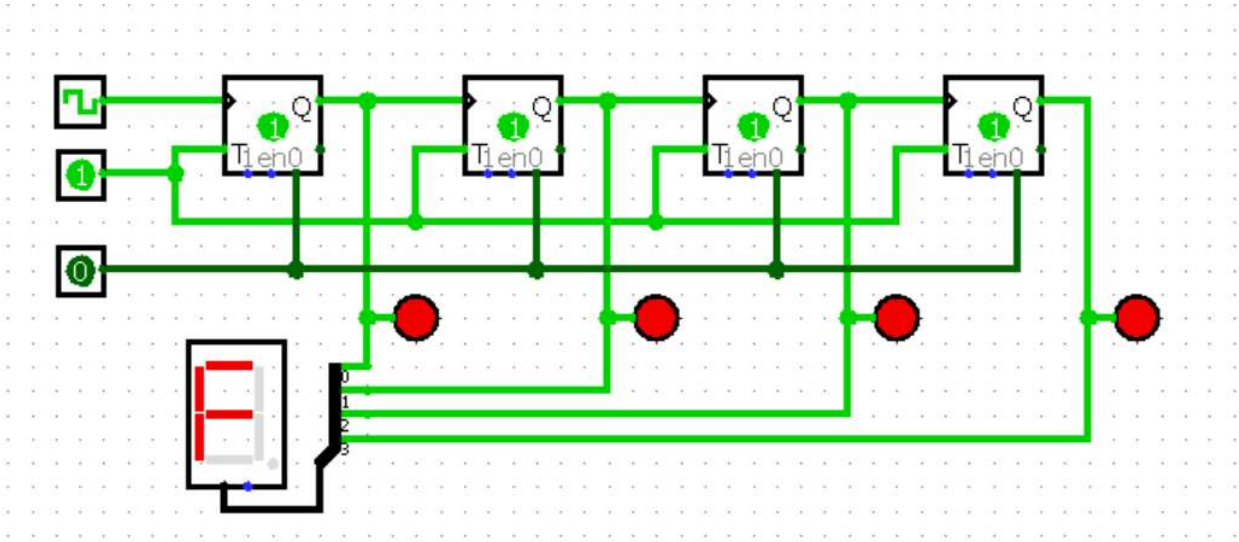
3 Ans.:

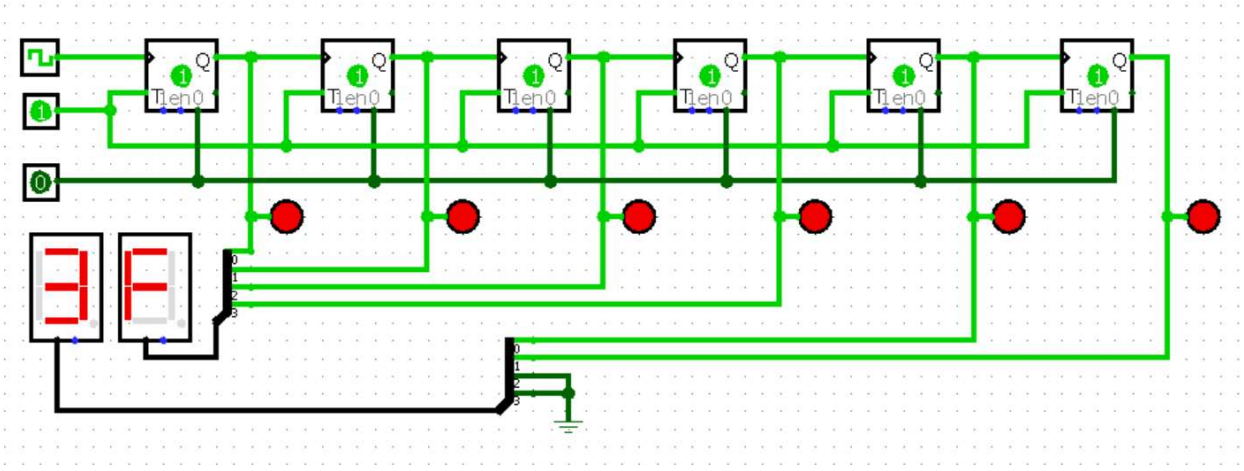
Simulated 4 – bit Counter:

Largest 4-bit Number = **15 = f** (in hexadecimal)



Simulated 6 – bit Counter:

Largest 6-bit Number = **63 = 3f** (in hexadecimal, **(3 x 16) + 15 = 63**)

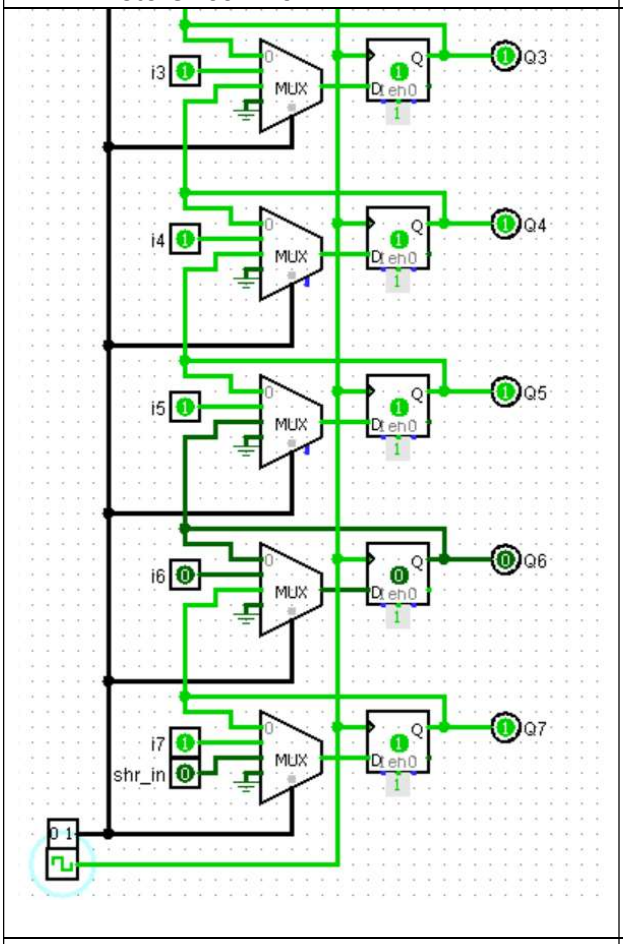
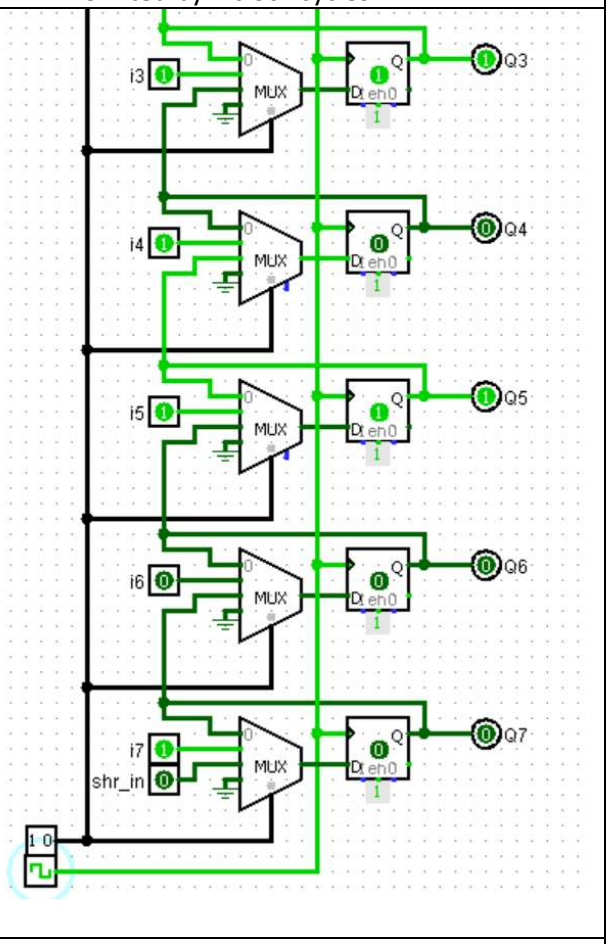


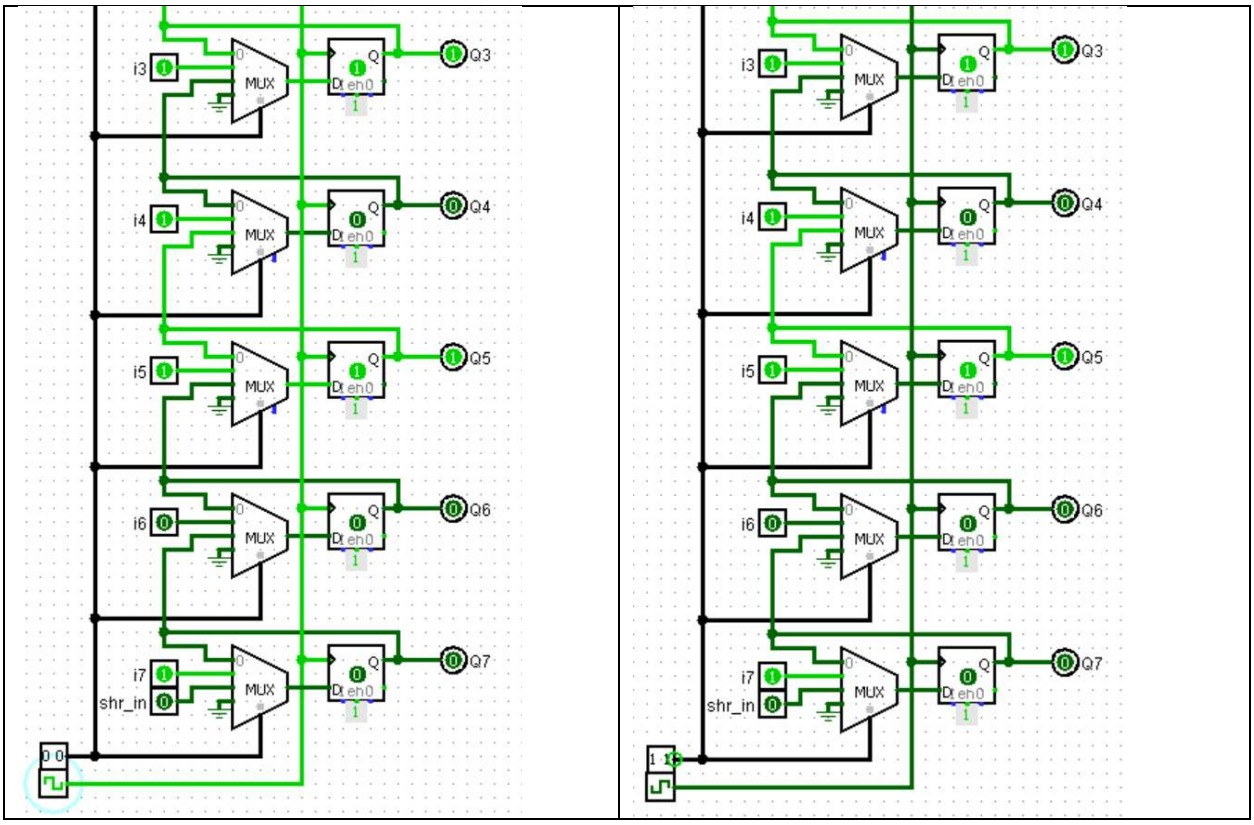
These are N-bit Counters that count from $2^N - 1$ down to 0. Consider the 4-bit Counter for simplicity. (Q_3 is stored at rightmost flip-flop). Now Q_0 is toggled for every rising clock edge. Q_1 is toggled for every Q_0 that goes from 0 to 1, otherwise remained in the previous state. Similarly, Q_2 follows Q_1 and Q_3 follows Q_2. Initial status of the flip-flops is $Q_3Q_2Q_1Q_0 = 0000$. This is decremented by one for every rising clock edge and reaches to the same value at 16^{th} rising edge of clock signal. This pattern repeats when further rising edges of clock signal are applied.

4 Ans.:

8-bit Multi-Function Shift Register:

Steps:

S1 = 0, S0 = 1 → Parallel Load	S1 = 1, S0 = 0 → Shift Right
1. Store 10011101	2. Shifted by 2 clock cycles
	
S1 = 0, S0 = 0 → Maintain Present Value	S1 = 1, S0 = 1 → Unused (Load 0's)
3. Retain 01110100	4. Clear (P.T.O)



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5 Ans.:

16x16 Register File:

Notations:

W_data is Data to be written

R_data is Data to be read

W_en is Enable input to write data

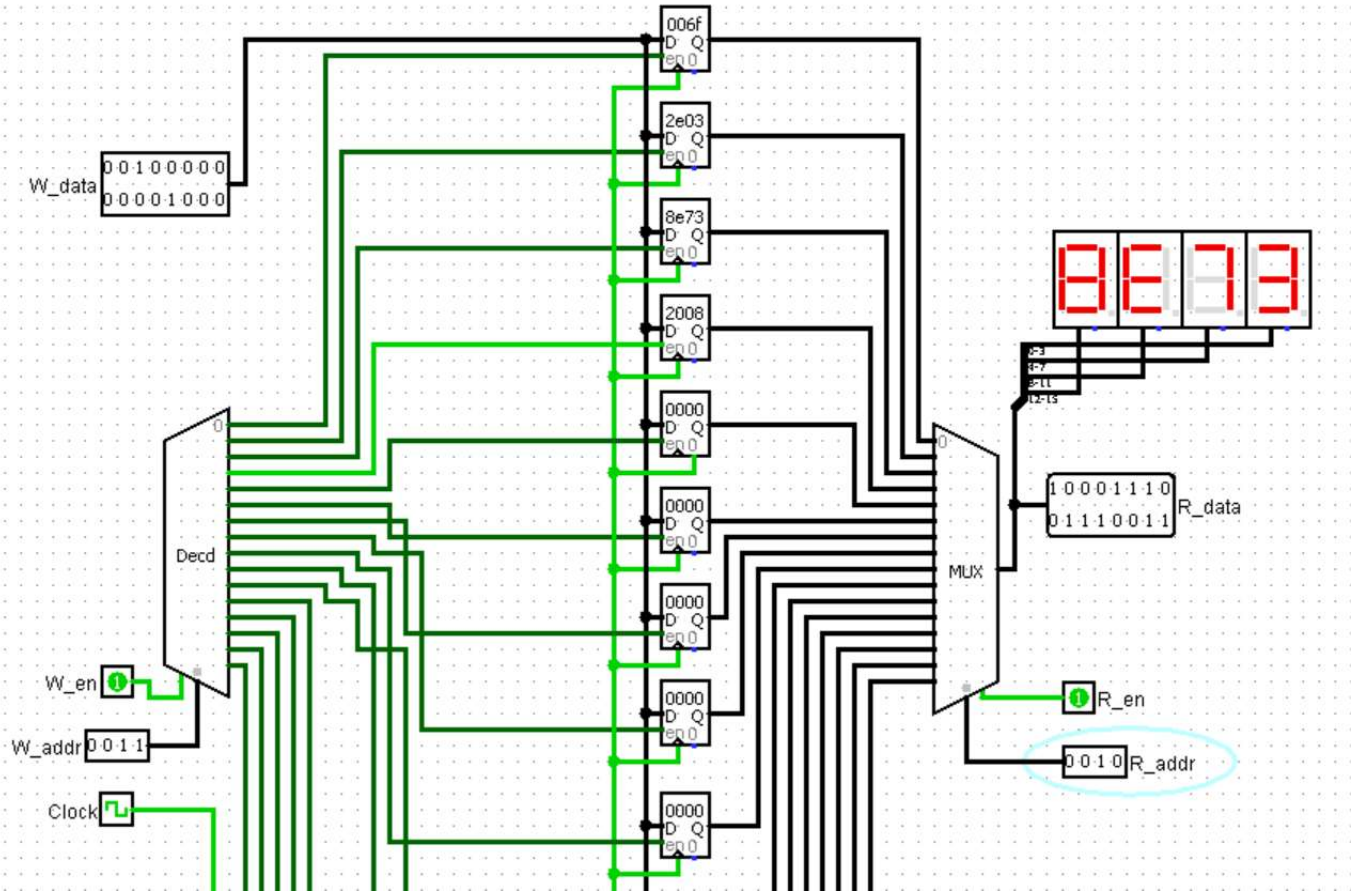
R_en is Enable input to read data

W_addr is Register location in which data should be written

R_addr is Register location from which data should be read

In the circuit diagram below, values are stored as follows,

Register Address	Data
0000	006f (DEC 111)
0001	2e03 (DEC 11779)
0010	8e73 (DEC 36467)
0011	2008 (DEC 8200)



Data = 2008 has been written in Register whose address = 0011

Data is being retrieved from Register, addr = 0010, which is displayed, 8e73,

(DEC 36467, BIN 1000 1110 0111 0011)