## Flnal\_Quiz\_CS321\_26th November 2020

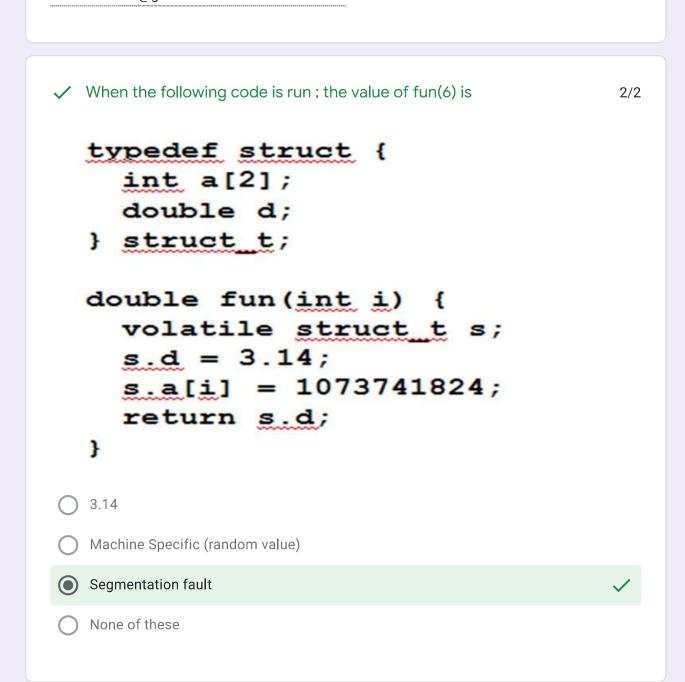
Total points 36/100 ?

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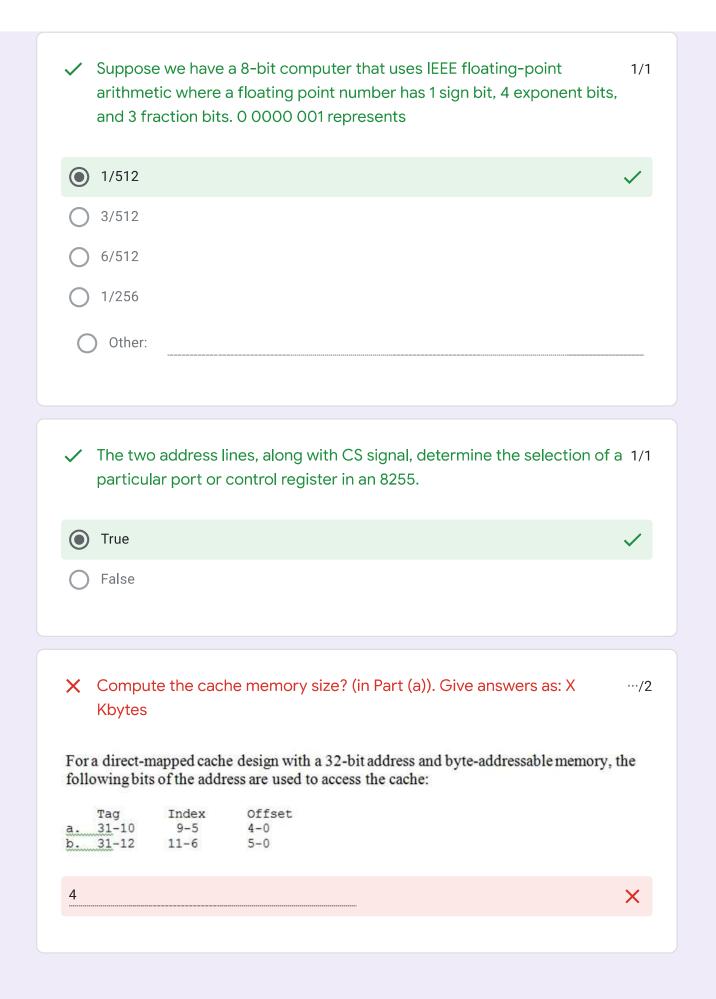
Email address \*

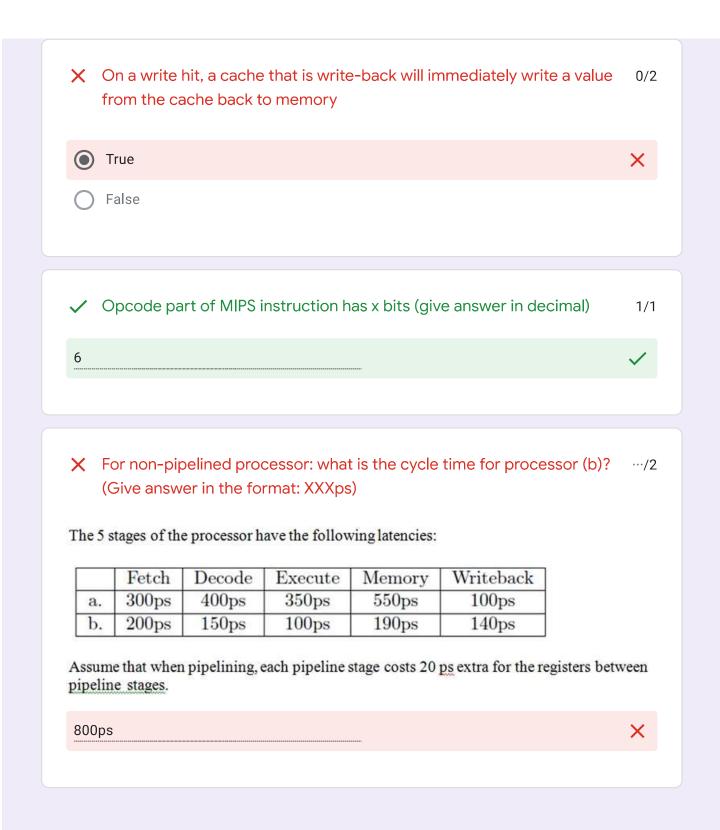
maheeth2000@gmail.com



<b>\</b>	Consider a program, P, with 1 billion dynamic instructions,50% R-Rype, 10% each of loads and stores, and 30% branches. How long would P take to execute on a single cycle processor with a 100MHz clock?	3/3
0	1s	
0	2s	
•	10s	<b>✓</b>
0	None of the above	
M SU OI AE	Give answer as (XXH)  I SP, 00FF I H, 0107 VI A, 20H IB M RI 40H DD M hat will be the result in the accumulator after the last instruction is executed	2/2 d?
601		<b>~</b>
×	Assuming the following dynamic instruction frequency for a program running on the single-cycle MIPS processor Add- 25%; addi- 25%; beq- 10%; lw-25%; sw- 15% In what fraction of cycles is the sign extend circuit used?? Give answer XX%	/3
25		×

	ing x,y, and	z are floats; $(x + y) + z = x + (y + z)$ ?	0/1
True			
False			
can not	t decide		X
✓ In MIPS	S, Jump Reç	gister equivalent to instruction X86	1/1
RET			<b>✓</b>
	many cach rs as: XX	ne lines does the cache have? ? (in Part (a)). Give	2/2
answer	rs as: XX	ne lines does the cache have? ? (in Part (a)). Give e design with a 32-bit address and byte-addressable memoress are used to access the cache:	
For a direct-following bi	mapped cach ts of the addr  Index 9-5	e design with a 32-bit address and byte-addressable memoress are used to access the cache:  Offset 4-0	





×	Consider a program, P, with 1 billion dynamic instructions,50% R-Rype, 10% each of loads and stores, and 30% branches. Assuming the multicycle processor operated at 400MHz, how long would it take to execute P?	0/3
0	2.75s	
•	8.75s	×
0	9.75s	
0	10.75s	
1. F 2. F 3. F 4. F 5. F Ass (Fe	e multi-cycle has been broken down into 5 steps: Hardware to support an instruction fetch Hardware to support an instruction decode (i.e. a register file read) Hardware to support instruction execution (i.e. the ALU) Hardware to support a memory load or store Hardware to support the write back of the ALU operation back to the register file ume that each of the above steps takes the amount of time specified in the table below. tch:305ps; Decode: 275ps; Execute:280ps; memory:305ps; Write Back:250ps) en the times for the datapath stages listed above, what would the clock period be for the eapath?	ntire
430	ps	×

The multi-cycle and pipelined datapaths have been broken down into 5 steps:

- 1. Hardware to support an instruction fetch
- 2. Hardware to support an instruction decode (i.e. a register file read)
- 3. Hardware to support instruction execution (i.e. the ALU)
- 4. Hardware to support a memory load or store
- 5. Hardware to support the write back of the ALU operation back to the register file Assume that each of the above steps takes the amount of time specified in the table below.

Fetch	Decode	Execute	Memory	Write Back
305 ps	275 ps	280 ps	305 ps	250 ps

In a pipelined datapath, assuming no hazards or stalls, how many seconds will it take to execute 1 instruction?



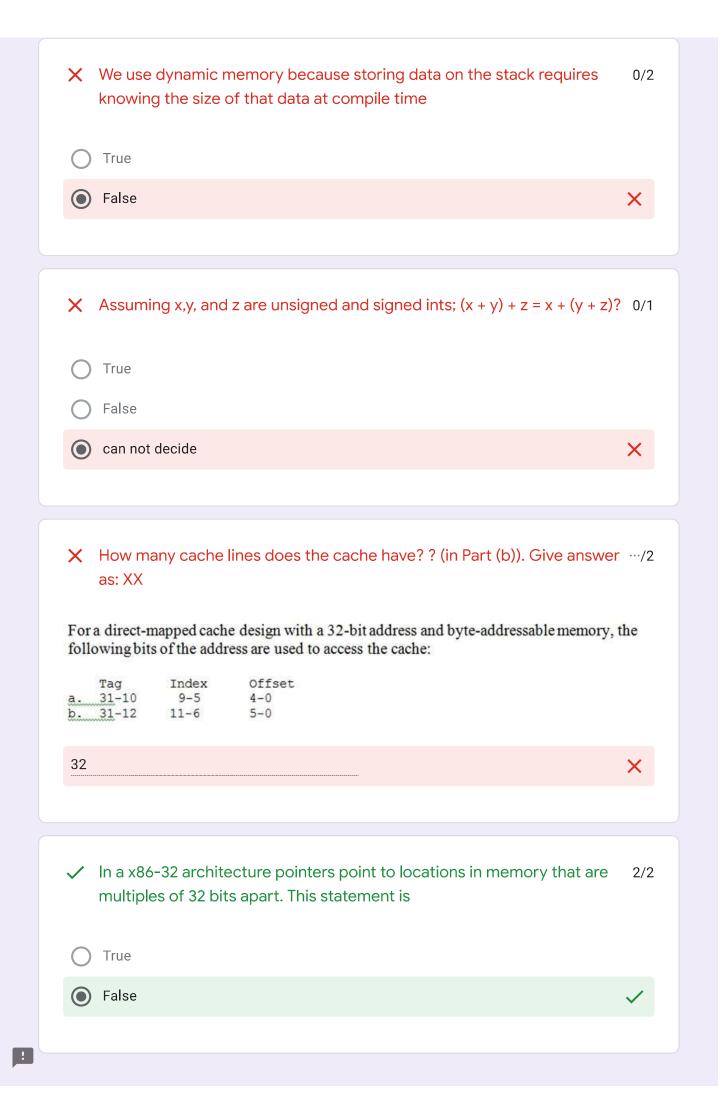
✓ Assume variables x, f, and d are of type int, float, and double, 1/1 respectively. Their values are arbitrary, except that neither f nor d equals  $+\infty$ ,  $-\infty$ , or NaN. For the following C expression, check whether it will always be true: d > f  $\Rightarrow$  -f > -d



Can not Decide

Name \*

Maheeth Reddy



×	Compute the cache memory size? (in Part (b)). Give answers as: X Kbytes	···/2
	a direct-mapped cache design with a 32-bit address and byte-addressable memory, to owing bits of the address are used to access the cache:	he
a. b.	Tag Index Offset 31-10 9-5 4-0 31-12 11-6 5-0	
4		×
<b>✓</b>	In MIPS, Jump And Link equivalent to instruction X86	1/1
call		<b>✓</b>
×	Suppose that "ALUOp1" in the single-cycleMIPS processor has a stuck- at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction?	0/1
	at-O fault, meaning that the signal is always O,regardless of its intended	0/1
	at-O fault, meaning that the signal is always O,regardless of its intended value. What instructions would malfunction?	0/1
	at-O fault, meaning that the signal is always O,regardless of its intended value. What instructions would malfunction?  R-type	0/1
	at-O fault, meaning that the signal is always O,regardless of its intended value. What instructions would malfunction?  R-type  lw	0/1
	at-O fault, meaning that the signal is always O,regardless of its intended value. What instructions would malfunction?  R-type lw addi	
	at-O fault, meaning that the signal is always O,regardless of its intended value. What instructions would malfunction?  R-type lw addi	
	at-O fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction?  R-type  Iw addi all of the above  In a x86-64 architecture pointers point to locations in memory that are	X

	In an 8086 Microprocessor, given that the IP = 1230H and CS = 0100H What is the physical address of the code.	2/2
0	1230H	
0	1330H	
$\bigcirc$	22300	
	02230	<b>✓</b>
	Assuming the following dynamic instruction frequency for a program running on the single-cycle MIPS processor Add- 25%; addi- 25%; beq-10%; lw-25%; sw- 15% In what fraction of all cycles is the data memory accessed (either read or written)? Give answer XX%	2/2
40%		<b>✓</b>
	Increasing the associativity of a cache is the best way to improve the hit rate when accessing values from an array in order.	0/2
<b>()</b>	True	×
0	False	
<b>~</b>	Opcode part of MIPS instruction has x bits (give answer in decimal)	1/1
6		<b>/</b>

X Pipelined processor: What is the cycle time for processor (a)? (Give answer in the format: XXXXps)

.../2

The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300 ps	400ps	350 ps	550 ps	$100 \mathrm{ps}$
b.	200 ps	150ps	$100 \mathrm{ps}$	190ps	140 ps

Assume that when pipelining, each pipeline stage costs 20 ps extra for the registers between pipeline stages.



X For pipelined processor: what is the cycle time for processor (b)? (Give ···/3 answer in the format: XXXps)

The 5 stages of the processor have the following latencies:

	Fetch	Decode	Execute	Memory	Writeback
a.	300 ps	400ps	350 ps	550 ps	100 ps
b.	200ps	150ps	100ps	190ps	140 ps

Assume that when pipelining, each pipeline stage costs 20 ps extra for the registers between pipeline stages.

780ps	X

	at-0 fault, n	emWrite" in the single-cycle MIPS processor has a neaning that the signal is always 0,regardless of its hat instructions would malfunction? Why?	0/1 S
R-type			
O sw			
addi			
all of th	ne above		×
For a direct-	mapped cache	line size? (in Part (b)).  e design with a 32-bit address and byte-addressable memoress are used to access the cache:	0/2 ory, the
8 <u>00</u> (2000)			
Tag a. 31-10 b. 31-12	Index 9-5 11-6	Offset 4-0 5-0	
a. 31-10	9-5	4-0	
a. 31-10 b. 31-12	9-5	4-0	×
a. 31-10 b. 31-12	9-5	4-0	×
a. 31-10 b. 31-12	9-5 11-6	4-0	×
a. 31-10 b. 31-12	9-5 11-6	4-0	×

X Who is right?

Three programmers are debating how best to write the code to transpose a matrix in a C software package that will run on a variety of different machines. The exact details of the different computers aren't known. What is known is that all of them have caches and virtual memory. The matrix is much too large to fit entirely in the caches, but it is small enough to fit in main memory, so virtual memory paging is not an issue. The array is normal C array of doubles stored in row-major order. Alice says that this code will do the best overall job:

```
for (i = 0; i < N; i++) {
    for (j = 0; j < N; j++) {
    temp = A[i][j];
    A[i][j] = A[j][i];
    A[j][i] = temp;
    }
}
```

Bob says that this is all wrong and that the performance will be much better if it's written this way:

```
for (j = 0; j < N; j++) {
    for (j = 0; j < N; j++) {
        temp = A[i][j];
    A[i][j] = A[j][i];
    A[j][i] = temp;
    }
}
```

Chris says it doesn't matter. The code will perform about the same either way.

Who's right?

Chris







None of them

```
X When the following code is run; the value of fun(3) is
```

0/2

```
typedef struct {
  int a[2];
  double d;
} struct t;

double fun(int i) {
  volatile struct t s;
  s.d = 3.14;
  s.a[i] = 1073741824;
  return s.d;
}
```

- 3.14
- Machine Specific (random value)
- Segmentation fault
- None of these

```
X When the following code is run; the value of fun(0) is
```

```
.../2
```

X

```
typedef struct {
  int a[2];
  double d;
} struct t;

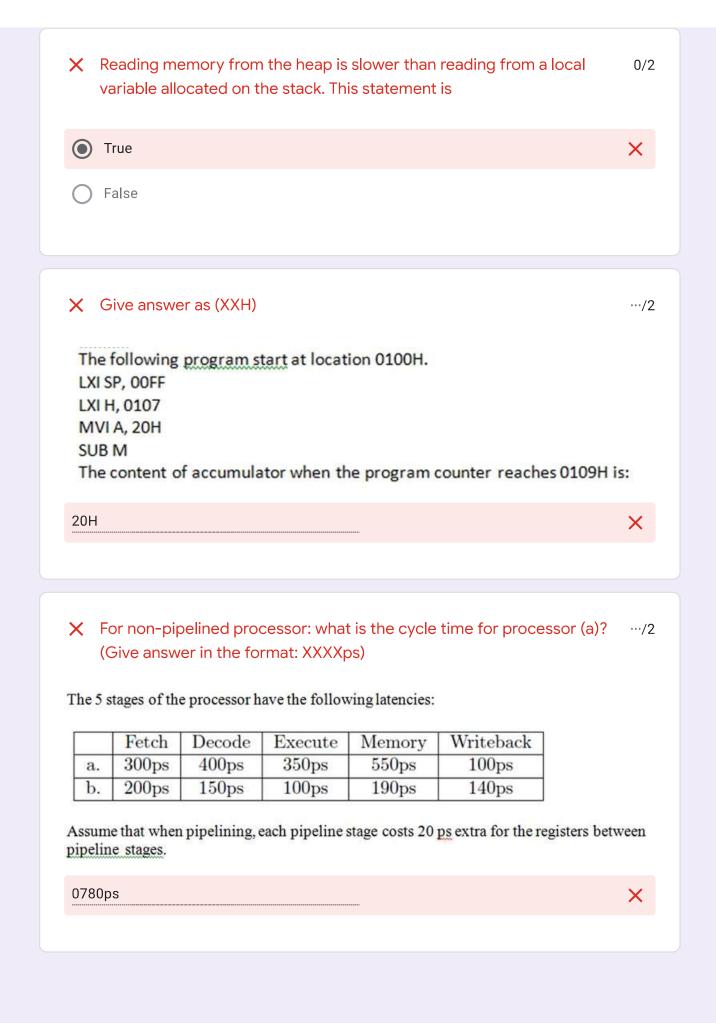
double fun(int i) {
  volatile struct t s;
  s.d = 3.14;
  s.a[i] = 1073741824;
  return s.d;
}
```

- 3.14
- Machine Specific (random value)
- Segmentation fault
- None of these

```
X When the following code is run; the value of fun(1) is
                                                0/2
  typedef struct {
     int a[2];
     double d;
   } struct t;
  double fun(int i) {
     volatile struct t s;
     s.d = 3.14;
     s.a[i] = 1073741824;
     return s.d;
   }
                                               X
3.14
  Machine Specific (random value)
  Segmentation fault
  None of these
X A RET instruction is equivalent to
                                                0/1
pop sp
  pop ip
  pop a
  push sp
```

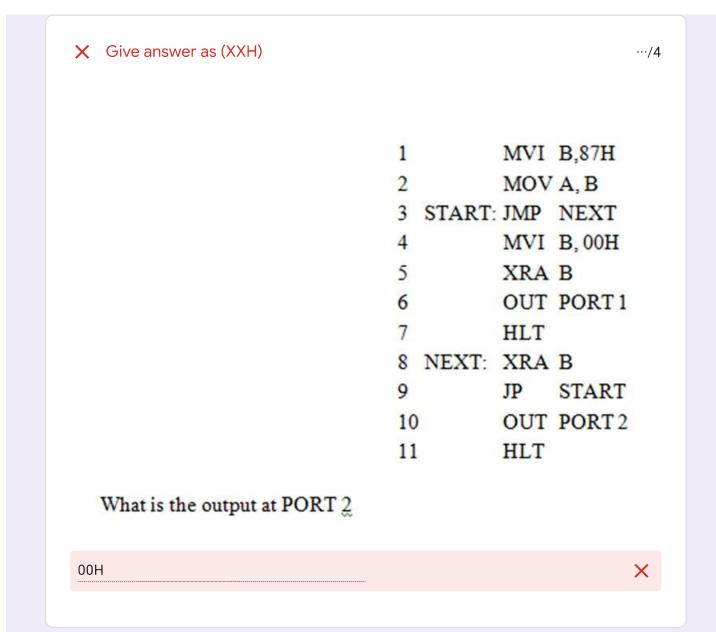
✓ Condition: exp = 1111; Case: exp = 1111, frac = 0000; This represents? 1/1
Operation that overflows
Both positive and negative
Represents value infinity
None of these
All of the above
Condition: exp = 1111; Case: exp = 1111, frac ≠ 0000; This represents? 1/1
Operation that overflows
Both positive and negative
Represents value infinity
Not-a-Number (NaN)
All of the above
✓ Functional Part of MIPS instruction has x bits (give answer in decimal) 1/1
6
Roll Number *
1801CS31

✓ Assume variables x, f, and d are of type int, float, and double, respectively. Their values are arbitrary, except that neither f nor d ec $+\infty$ , $-\infty$ , or NaN. For the following C expression, check whether it will always be true: x == (int)(float) x	1/1 Juals
Always True	
Not Always	<b>✓</b>
Can not Decide	
✓ Jump instruction has x bits for address (give answer in decimal)	1/1
26	<b>✓</b>
X Multiple control word determines the operating mode of 8255.	0/1
True	×
O False	
Suppose we have a 8-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 4 exponent be and 3 fraction bits. 0 1110 110 represents (give answer in decimal)	···/1 pits,
224	×



1 F	Consider a program, P, with 1 billion dynamic instructions,50% R-Rype, 3/0% each of loads and stores, and 30% branches. Assuming a multicycle processor where R-type instructionstake 4 cycles, loads and stores 5 cycles, and branches 3cycles, what is the CPI of P?	/3	
	2.8		
	3		
	3.9		
	3.8		
	✓ What is the cache line size? (in Part (a)) 2/2 For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache: Tag Index Offset a 31-10 9-5 4-0		
For a follow	direct-mapped cache design with a 32-bit address and byte-addressable memory, the ving bits of the address are used to access the cache:  Tag Index Offset	/2	
For a follow	direct-mapped cache design with a 32-bit address and byte-addressable memory, the ving bits of the address are used to access the cache:	/2	
For a follow	direct-mapped cache design with a 32-bit address and byte-addressable memory, the ving bits of the address are used to access the cache:  lag Index Offset 11-10 9-5 4-0	/2	
For a follow	direct-mapped cache design with a 32-bit address and byte-addressable memory, the ving bits of the address are used to access the cache:  lag Index Offset 1-10 9-5 4-0 1-12 11-6 5-0	/2	
For a follow	direct-mapped cache design with a 32-bit address and byte-addressable memory, the ving bits of the address are used to access the cache:    ag	/2	

<ul><li>•</li></ul>	Always True	
0		<b>✓</b>
	Not Always	
0	Can not Decide	
	X86 assembly store the return value is always in when a function is finished	1 0/2
•	ebx	×
0	eax	
$\bigcirc$	есх	
$\bigcirc$	esp	
C	Other:	
	Microarchitecture: Implementation of the architecture. One of the examples is	0/1
0	The byte-level programs that a processor executes	
$\bigcirc$	A text representation of machine code	
0	cache sizes and core frequency	
	instruction set specification	×



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