PH401 – Introduction to Nanomaterials

Mid-Semester Examination

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Ans 1:

Why does no engineering below nm scale?

We have no engineering below nm scale because:

a) The materials are not observable beyond nanometre scale. So, it is not difficult for engineering at that scale.

b) In the nanometer scale, materials do not exist in groups but as single atoms or in plasma state. Since there is no reliability on the existence of atoms we cannot carry out engineering in this case.

What is the meaning of 14nm technology?

14nm technology refers to the MOSFET technology that was introduced by Intel as a successor to their earlier 22nm technology. This technology further advances the scaling of transistors in accordance with Moore's Law. The value 14nm does not actually represent the size of the transistor but the fabrication technology used to manufacture them. Eariler the gate pitch of the transistor was same as its fabrication value but this has changed now. The 14nm technology has 42nm pitch size and more transistor density. The fin sizes of the FinFET tranistors fins are thinner taller and fewer in number (per transistor) as compared to the earlier 22nm technology. Hence, 14nm technology is more advanced as it accomodates more transistors in a smaller space, thus increasing the performance and power efficiency.

Specialities/Advantages of 14nm scaling:

1. 52nm interconnect pitch provides better than normal interconnect scaling
2. Taller and thinner fins for increased drive and current performance
3. Reduced number of fins for improved density and lower capacitance.
4. Provide improved performance and leakage

What are the challenges the industries face to handle the 14nm technology?

1. Additional design constraints and new sources of variability associated with the non-planar transistor structure.
2. Computational Lithography and the need for double patterning at the 14nm node will drive up the complexity and difficulty of the physical design implementation, pushing designs towards more uniform and regular structures instead of customized ones.
3. The tradeoff for that is that wafer costs continue to rise from generation to generation, as double patterning requires additional time and ever-finer tools that drive up the cost of production. The end result is that while Intel's cost per

transistor is not decreasing as quickly as the area per transistor, the cost is still decreasing and significantly.

Can one go beyond 14nm to develop technology?

The answer is **YES**. We can go beyond 14nm but the extent to which we can go is very less and gets saturated very soon due to the following reasons:

1. Complex machinery and high costs are involed in manufacturing and patterning. Also, the scope for error is very less, making the production very difficult.
2. The technology may not be cost-effective for the customers and hence they may not buy it.

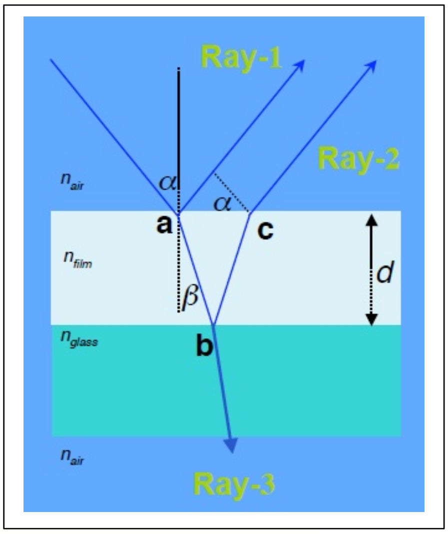
Why did Moore's law fail?

In present day, Moore's law has become saturated and is no longer as meaningful as it used to be. The industry has reached its peak of scaling down nodes or transistors upto the 5nm level. And going beyond this means that we will near the size of a single Silicon atom which obviously cannot serve as a transistor. So, Moore's law fails because we cannot scale down transistors beyond a point.

Ans 2:

What will be the thickness of MgF_2 on spectacle glass for appearing it as yellow (λ=5893 Å)?

If constructive interference occurs at the wavelength 5893 Å, then the spectacle glass will appear as yellow in colour.



We know, $n_{air} = 1$, $n_f = 1.4$ and $n_{glass} = 1.5$

We can observe that $\underline{n_{air} < n_f < n_{glass}}$

So constructive interference will occur if,

$$2n_f d = m\lambda$$

We need to find d, thickness of the film

Substituting given values,

$$2 \times 1.4 \times d = m \times 5893 \times 10^{-10}$$

$$\Rightarrow d = m \times \frac{5893 \times 10^{-10}}{2.8}$$

$$\Rightarrow d = m \times 0.21\ \mu m$$

Where m = 1,2,3,....

For the thinnest film possible, m = 1 $\Rightarrow$ d = 0.21 μm

Therefore the smallest possible thickness of the film is 0.21 μm. Other possible thicknesses are 0.42 μm, 0.63 μm, 0.84 μm....

Which technique will be better to get a high-quality view (explain and justify your answer).

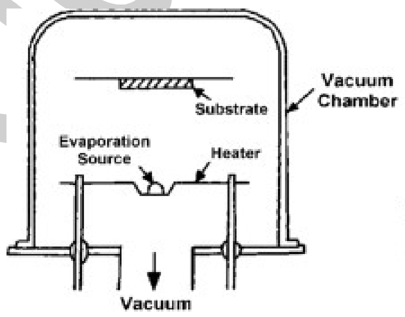
Pulse Layer Deposition (PLD) technique will be better to get a high-quality view because:

- The laser induced expulsion in PLD produces a film with the same stoichiometry as the target, especially in the case of multi-element materials. But in Thermal Evaporation, the stoichiometry is greatly influenced by the vapour pressures of elements in the target material.
- We have control over the film growth rate. It is a versatile method.
- It has a fast deposition rate and is cost effective, clean, scalable. It is compatible with oxygen and other inert gases.

Explain the principle of the pulse laser deposition (PLD)/thermal evaporation system.

Principle of Thermal Evaporation:

- Thermal Evaporation is a physical vapour deposition technique.
- It consists of evaporating solid metal or other material samples under high vacuum (10^{-6} torr or 1.3×10^{-4} Pa) inside vacuum chamber. This produces some vapour pressure.
- The evaporated material is then condensed on the substrate to form the thin film.
- This process is also called **vacuum deposition**.
- Heat is produced by electrical resistance.
- If nanoclusters are formed during the evaporation process, it is top down.
- If atoms or molecules are formed during the evaporation process that recombine to form a thin layer without any chemical reaction, it is a crossover technique.
- It is used to deposit metals such as silver, aluminum for OLEDS, solar cells etc.

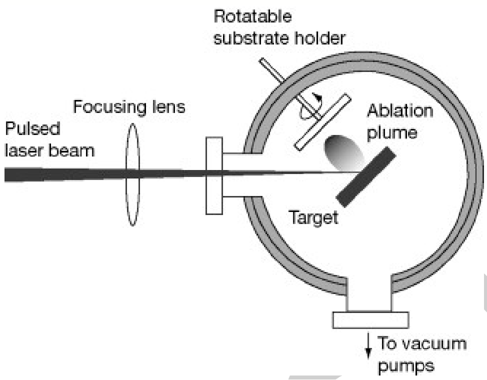


Thermal Evaporation by Electrical Resistance

Principle of Pulse Laser Deposition:

- Pulsed laser deposition (PLD) is a physical vapour deposition technique.
- In PLD, a high power pulsed laser beam is focused to strike a target of the desired composition.

- The material is then vaporized and deposited as a thin film on a substrate facing the target.
- This process is carried out in either ultra high vacuum or in the presence of a background gas (for e.g., oxygen is used when oxide films should be deposited).
- Electromagnetic energy is converted into electronic excitation and then into thermal/mechanical energy to cause ablation.



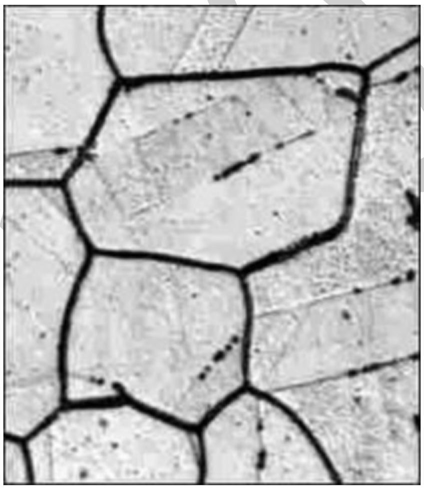
Pulse Laser Deposition

Ans 3:

Differences:

Macro Grain: The grain size or shape is visible to an naked eye

Micro Grain: The grain size is very small and only visible using a microscope after etching



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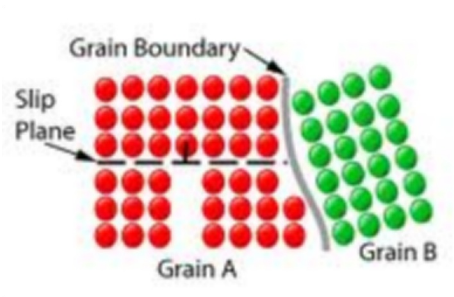

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- Macro grain are bigger than micro grains
- To view micro grains several process like polishing, etching has to be carried out

Importance of Microstructure:

- With the help of microstructure of various metals we can find the change the physical properties like strength, hardness, ductility, etc..
- If we study the microstructure of the product we can improve it according to our requirements

Ball Milling is more stronger than Melt Casting because:
After ball milling, the hot press will make the grains smaller. So, strain hardening will occur due to which the steel rod can carry more stress. In other words, Ball milling will contain more micro-grains and micro-grains help in strengthening the material. But in case of casting the grains formed will be larger and hence the strength will also be less.

Ans 4:

Find the decrease of critical diameter NdFeB if an engineer has increased its saturation magnetization from 70 emu/g to 100 emu/g without changing its crystal symmetry and magnetic anisotropy.

Since, the engineer has not changed its symmetry and magnetic anisotropy. So, according to the formula,

$$r_c = \frac{9[AK_u]^{\frac{1}{2}}}{\mu_0 M_s^2}$$

Here, r_c → critical size below which particle exists as single domain
M_s → saturation magnetism.

Therefore, r_c at 70 emu/g is

$$[r_c]_{70} = \frac{9[AK_u]^{\frac{1}{2}}}{\mu_0[70]^2}\ [\mathbf{eqn(1)}]$$

and r_c at 100 emu/g is

$$[r_c]_{100} = \frac{9[AK_u]^{\frac{1}{2}}}{\mu_0[100]^2}\ [\mathbf{eqn(2)}]$$

After dividing eqn (1) by eqn(2),

$$\frac{[r_c]_{70}}{[r_c]_{100}} = \frac{[100]^2}{[70]^2}$$

$$\Longrightarrow [r_c]_{100} = 0.49\ [r_c]_{70}$$

If $[D_c]_{70}$ and $[D_c]_{100}$ represent the corresponding diameter of the radii, then

$$\Longrightarrow [D_c]_{100} = 0.49\ [D_c]_{70}$$

∴ Decrease in Critical Diameter is

$$\Delta D_c = [D_c]_{70} - [D_c]_{100} = [D_c]_{70} - 0.49[D_c]_{70} = 0.51[D_c]_{70}$$

In terms of percentage, it is 51%

So, there is a 51% decrease of Critical Diameter NdFeB if its saturation magnetization is increased from 70 emu/g to 100 emu/g without changing its crystal symmetry and magnetic anisotropy.

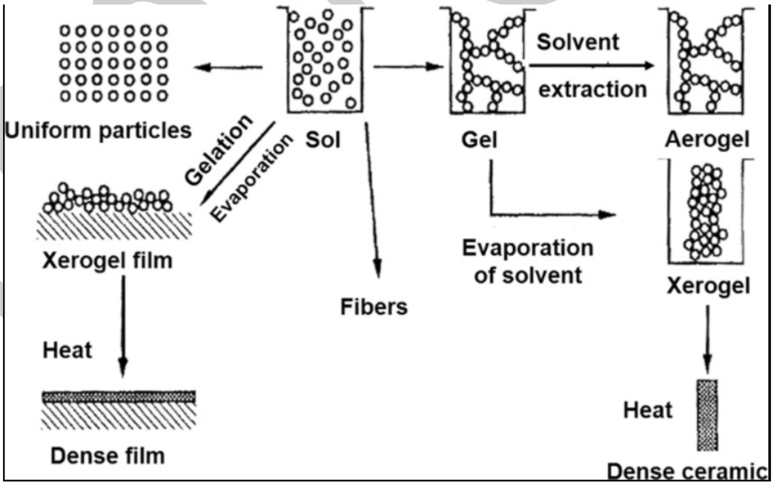
Suggest a method to make a high-quality thin film of such a permanent magnet and explain its (thin film deposition) process.

We can use **Sol-Gel Deposition** method to make high quality thin film of such permanent magnets for industrial applications.

Using Sol-Gel Deposition, we can produce a large quantity of nanosized material with modeled and controlled particle size, morphology, orientation and crystal structure as well as optimized physical and chemical properties.

This applies to the fabrication of the metal oxides thin films including chemical reactions, nucleation, growth and ageing, as an aqueous thin-film processing method (aqueous chemical growth). Tuning the thermodynamic and kinetics of nucleation, growth and ageing, and the precipitation conditions provides a simple and efficient control of particle size and its distribution. Requirement of minimum surface energy drives nanoparticles to develop spherical morphology.

The low-cost technique consists of heating aqueous solution of metal salt on complex at given pH and temperature [< 100^0C] in a closed bottle including substrates. Organic solvents as surfactants can also be used with disadvantages of safety hazards, toxicity and purity of deposited film. For example, coatings of crystalline nanoparticles of various textures have been grown with magnetite [Fe_3O_4], hematite [Fe_2O_3], CrO_3, Cr_2O_3, Mn_2O_4, ZnO or RuO_2.



Sol-gel Deposition

Ans 5:

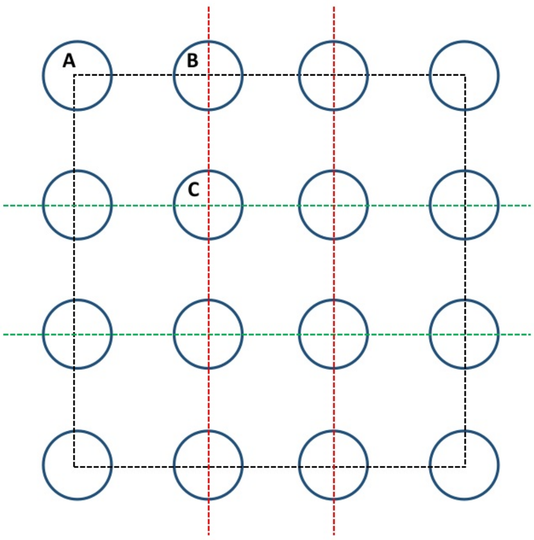
What is the importance of the surface-to-volume ratio in nanotechnology?

Surface Area to Volume ratio has a significant effect on the properties of Nanomaterials. Nanomaterials have a relatively larger surface area when compared to the volume of the same material. Within nanomaterials we can see that lesser the size, the higher is the surface to volume ratio. For a single shell nanomaterial 92% of the atoms are surface atoms. This has a huge impact on the different properties of the nanomaterials. Due to the presence of more atoms on the surface, nanomaterials are more chemically active as they have more surface electrons. This phenomenon is particularly useful in applications of nanomaterials in chemical catalytic reactions where surface area of contact is very important.

What is the magic number in nanoscience for a simple cubic (SC) crystal structure?

Magic Number for Simple Cubic Crystal (SCC) structure:

Let us say, we have n=3 layers. Then we will have an arrangement on the surface as shown in the figure below. Here, A, B and C are the different kinds of atoms which are possible on the surface of the SCC crystal. We now calculate the number of types of A,B,C atoms in terms of n and Magic Number for Simple Cubic Crystal (SCC) structure.



Group A: We can see 4 atoms of type A in this figure. We have 6 such sides in a cube and each atom of type A is shared by 3 edges. Hence, we will have a total of

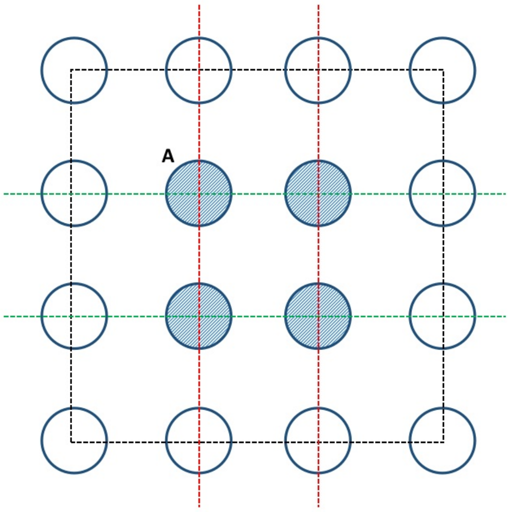
$\frac{4}{3} \times 6 = 8 \text{ atoms}$

Group B: There are 8 atoms of group B in this figure. These 8 atoms are shared among two faces and there are 6 faces in a cube. So we have total number of atom count = $\frac{8}{2} \times 6 = 24$. We have these atoms at the intersection of the middle lines with the edges. Since, each edge has (n-1) middle lines and there are 12 edges, multiplying by the number of edges we have 12(n-1) atoms.

Group C: In case of 3 layers, we can see that we will have 4 × 6 = 24 Group C atoms (since there are 4 on every face and there are 6 faces). Generalizing this concept, we see that C atoms occur (n-1)^2 times i.e. the number of times of intersection of the middle lines. Considering 6 faces we have totally $6(\mathrm{n}-1)^2$ Group C atoms

So, Total Number of Surface Atoms
= Sum of Number of Surface Atoms of Groups A,B,C = 8 + 12(n-1) + $6(n-1)^2$ = $6n^2 + 2$
Therefore, **Total Number of Surface Atoms is ($6n^2 + 2$)**

Calculating the bulk atoms:

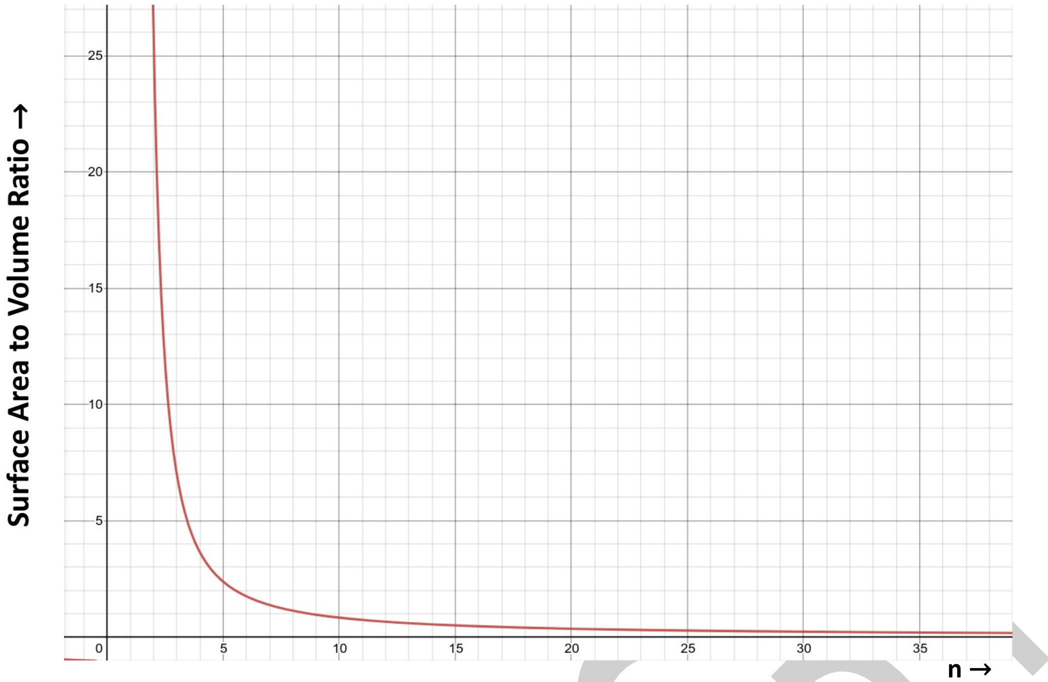


We will have only atoms of type A in the bulk atoms. We see that there are 4 atoms for n=3 case. On generalizing, we will have $(n-1)^2$ atoms as these atoms are on the intersection of the lines in the middle and there are (n-1) such intersections. Since, (n-1) such layers are possible, the total number of atoms of type A is $(n-1)^3$.

Hence, the Magic Number for SCC = surface atoms + bulk atoms = $6n^2 + 2 + (n-1)^3$.

Therefore, **Magic Number for SCC =** $(n-1)^3 + 6n^2 + 2$

Surface to volume ratio = $\dfrac{6n^2 + 2}{(n-1)^3}$



Graph of Surface Area to Volume Ratio against Particle Size

Ans 6:

Explain the steps of the Lithography (Visible/UltraViolet/X-ray/Electron) method for making nanodevices.

Nanolithography is the branch of nanotechnology concerned with the study and application of the nanofabrication of nanometer-scale structures, meaning nanopatterning with at least one lateral dimension between the size of an individual atom and approximately 100 nm. Nanolithography is used e.g. during the nanofabrication of leading-edge semiconductor integrated circuits (nanocircuitry), for nanoelectromechanical systems (NEMS) or for almost any other fundamental application across various scientific disciplines in nanoresearch.

This technology is suitable for the nanofabrication of various semiconductor Integrated Circuits (ICs), NEMS and for various applications in research. The modification in semiconductor chips at the nano-scale (in the range of 10^{-9} meter) is also possible.

There are many techniques through which micro/nanopatterning could be possible. They are:

- Photolithography
- X-ray lithography
- Electron beam lithography
- Ultra-violet lithography

<u>Steps of Nanolithography</u>:

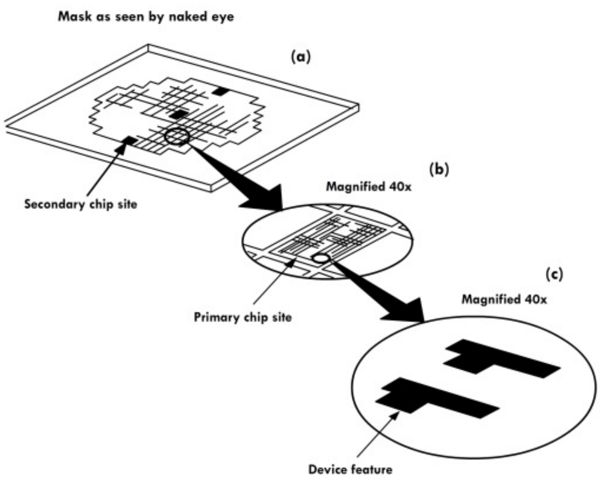
For lithography processing, a hard copy of the pattern has to be first generated. This is called a reticle or mask.

The design on the mask has to be transferred to the wafer, as shown in figure 1. The transfer can be 1:1 (i.e. with no reduction in size) but usually the size is reduced so that the pattern is transferred to a smaller region on the wafer. This is done by using suitable lens to demagnify the pattern.

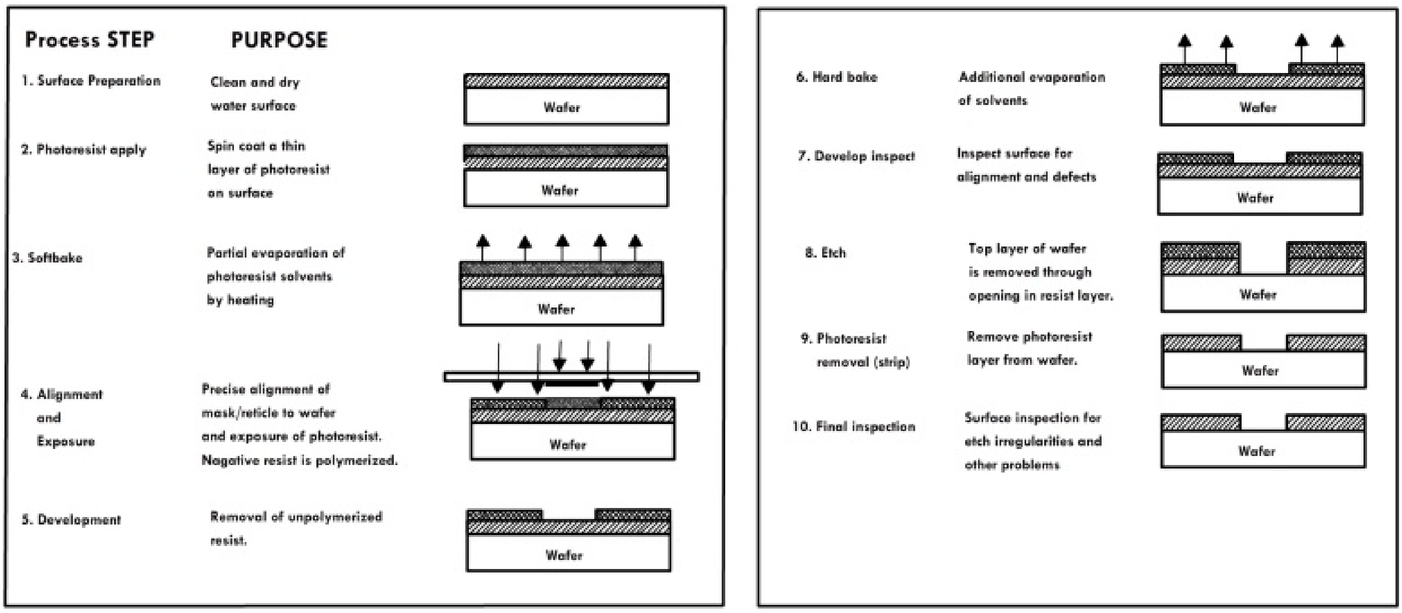
Lithography can be broadly divided into two stages, each of which consists of several steps:

1. First, the pattern is transferred to a photoresist layer on the wafer. Photoresist is a light sensitive material whose properties change on exposure to light of specified wavelength. This process is called developing. The pattern formed in this step is temporary and can be removed easily. This is especially important if the pattern is not properly alignment with the wafer or with any existing patterns on the wafer, improper registry.
2. The transfer of the pattern takes place from the photoresist to the wafer. Exposed wafer surfaces can be etched (removal of material) or layers deposited on it. Dopant materials can also be added to sections of the wafer through the pattern. This stage is final and it is very hard to remove the formed patterns without causing damage to the underlying wafer. The overall lithography process is summarized in figure 2.

After the pattern is formed on the photoresist and the wafer surface is exposed (developing process) the exposed wafer surface is etched. It is also possible to deposit material on the exposed surface.



<u>Figure 1</u>: Typical IC fabrication process showing the different features on the die with increasing magnification from (a) - (c). A mask can be made of many chips, each chip will also have a variety of device features. These patterns will be transferred to the wafer during lithography.



<u>Figure 2</u>: Overview of the lithography process. Lithography is used to remove material (etching) from the wafer surface by selectively exposing part of it in this figure.

How does it differ from the nanoimprint method?

- Lithography uses an optical approach to create patterns. But Nanoimprint method creates patterns through the use of photons or electrons to modify the chemical and physical properties of the resist.
- The resolution achieved by conventional Lithography is limited by light diffraction or beam scattering. But Nanoimprint relies on direct mechanical deformation of the resist and can therefore achieve higher resolutions.
- Since, the resolution of Nanoimprint mainly depends on the minimum template feature size that can be fabricated, it can produce sub-10 nm features over a large area with high throughput and low cost. This is not the case with Lithography techniques.
- Lithography is costlier as it requires expensive equipment, clean room conditions, high-vacuum conditions. Nanoimprint produces extremely clear circuit diagrams and has lesser chip failure rates, hence making it costeffective for industrialization.

Which method is cost-effective for industrialization?

- **Nanoimprint method is cost-effective for industrialization**
- <u>Reason</u>: Due to the reasons stated above, we can see Nanoimprint is capable of patterning with high resolution, high fidelity, high throughput, and low cost. That makes it cost-effective for industrialiaztion.

What is/are the advantage/s of electron lithography over nanoimprint?

Advantages of Electron Lithography over Nanoimprint are:

- Can write smaller features than X-ray lithography and photolithography
- The pattern is written directly to the wafer.
- Used to develop specialized devices and prototype devices
- Fast turn-around time
- This employs a beam of electrons instead of photons

THE END