Computer Architecture Lab – CS322

Name: M. Maheeth Reddy	**Roll No.**: 1801CS31	**Date**: 31 October 2020

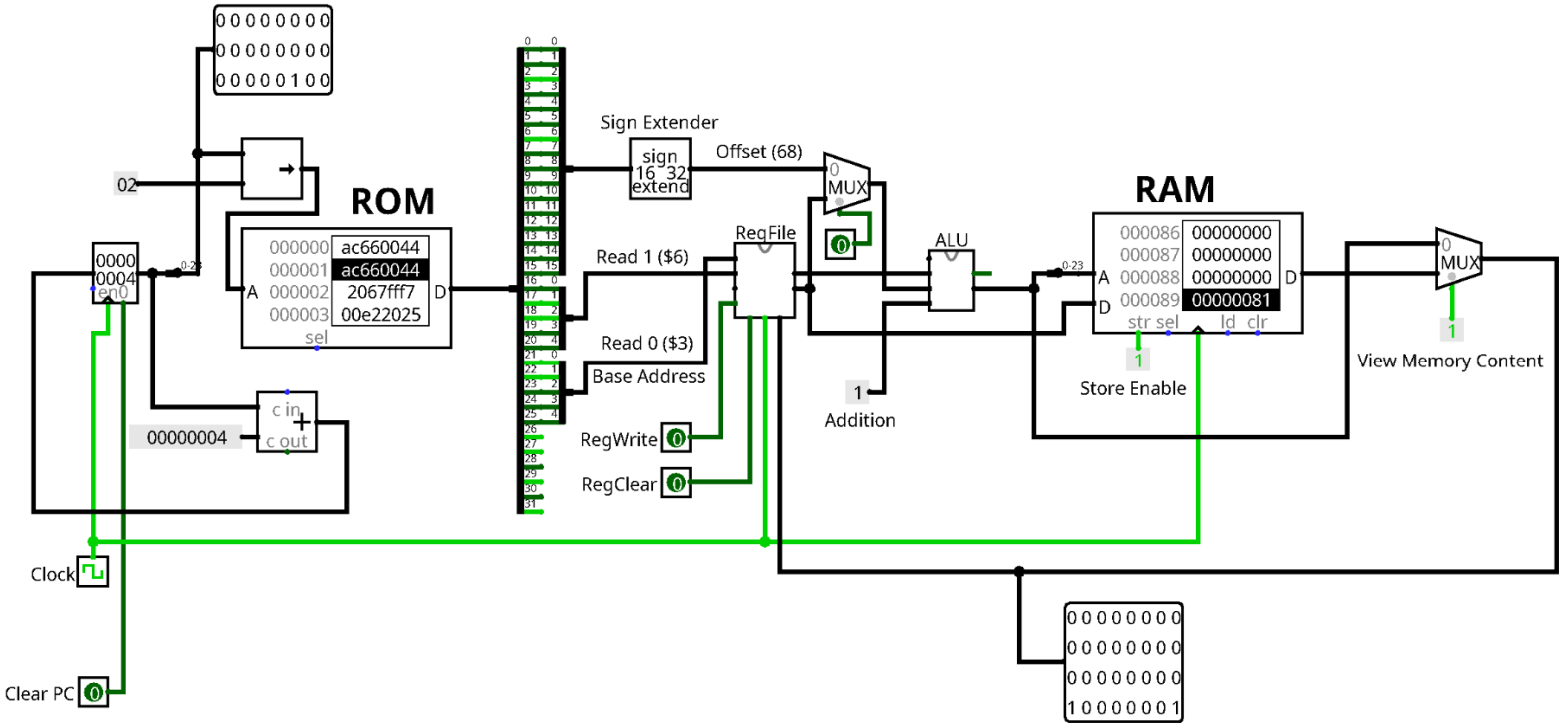
Lab 7 – Implement a RISC Single Cycle Processor

Task 1:

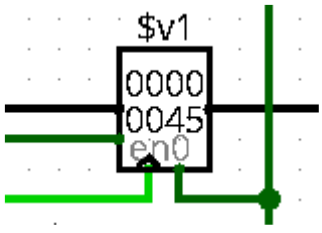
(a)

Instruction	Encoding
sw $6, 68($3)	0x**ac660044**

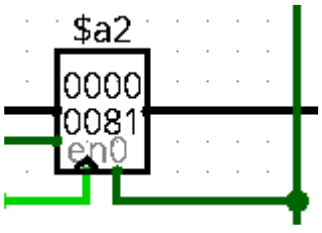
Implementation (File: 1801CS31_Lab7_1.circ)



Contents of $3 before execution



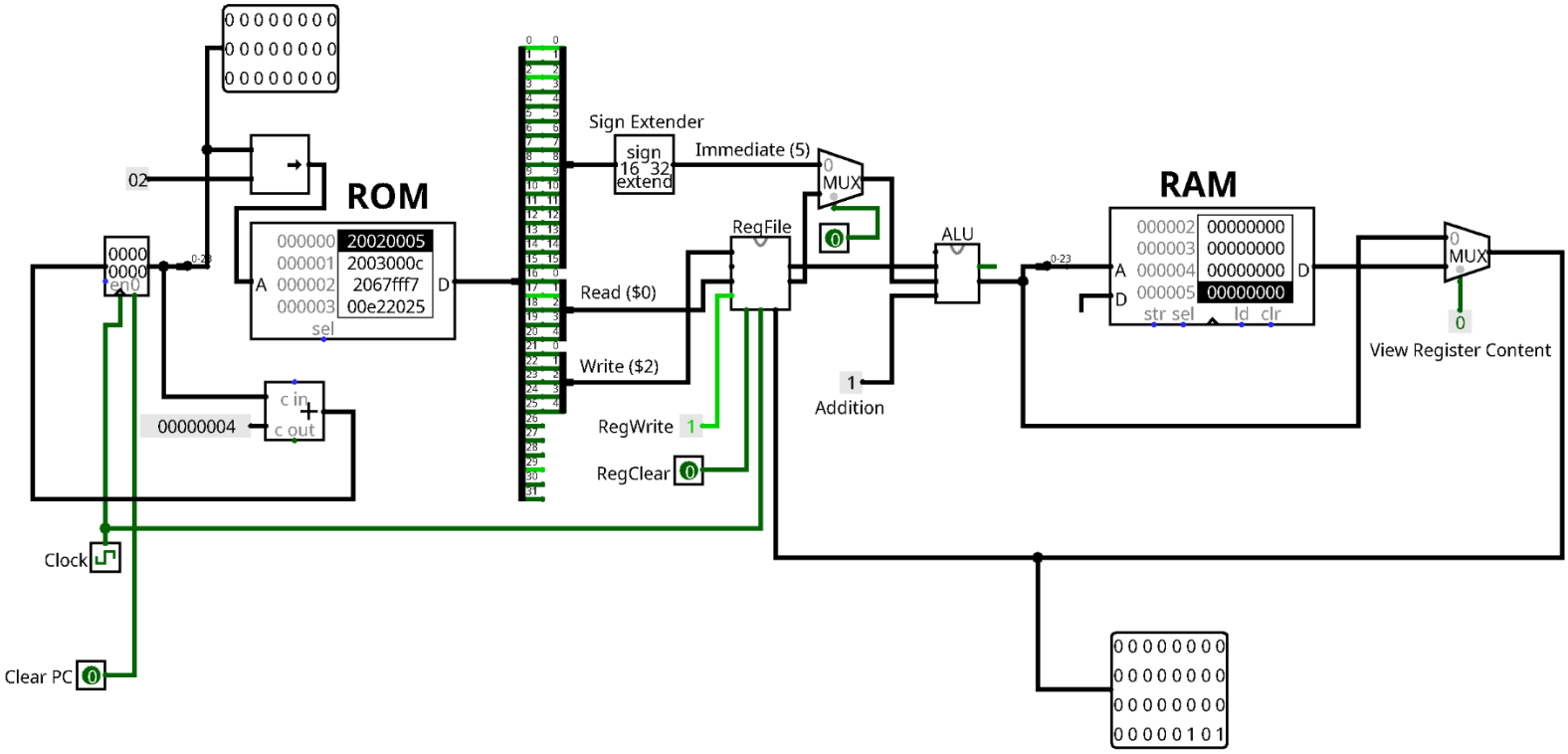
Contents of $6 before execution



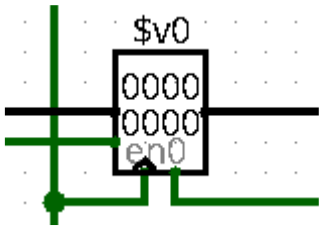
(b)

Instruction	Encoding
addi, $2, $0, 5	0x**20020005**

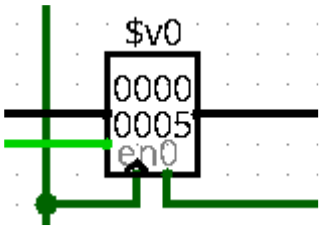
Implementation (File: 1801CS31_Lab7_2.circ)



Contents of $2 before execution



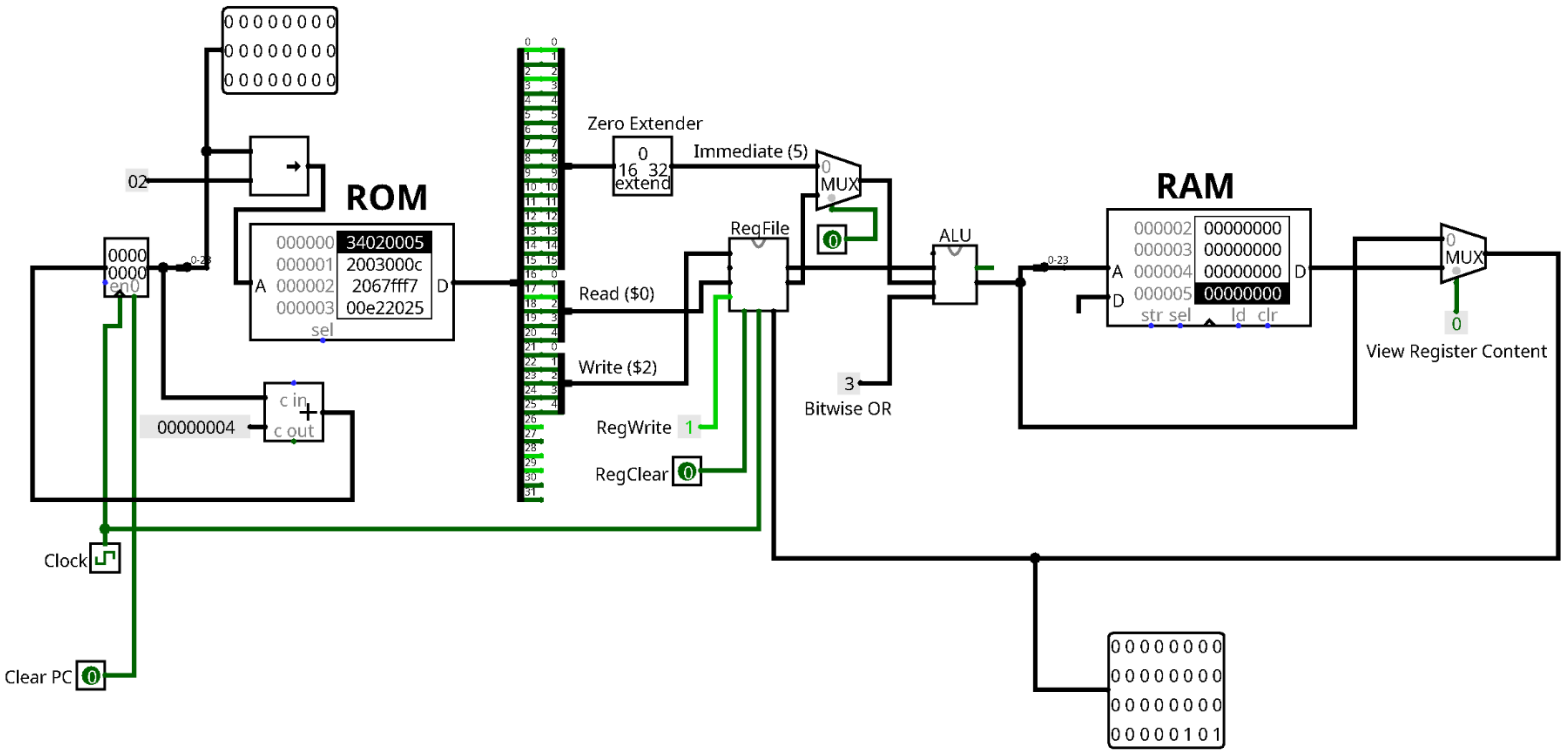
Contents of $2 after execution



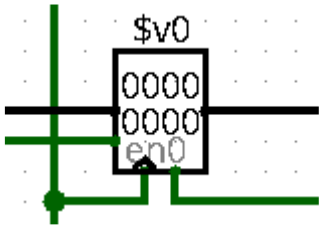
(c)

Instruction	Encoding
ori $2, $0, 5	0x**34020005**

Implementation (File: 1801CS31_Lab7_3.circ)



Contents of $2 before execution



Contents of $2 after execution