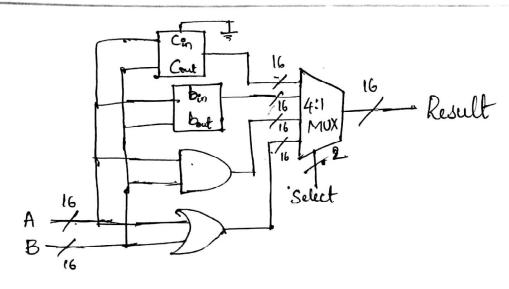
Logic Diagram Value 1 RA1 0000 16×16 ALU regester file RA 2 0 0 0 0 16) Value 2 WA 0000 16

12



RA1, RA2 - read addresses

NA is write adobress

Data\_in - data to be written

sel - select line for 2:1 MUX, decides by storing Data in or sum of numbers.

Clock is Clock

sug Doute - inables vosite mode

sug Read - enables read mode

regClear - when = 1, clears all stored values in register file

ALU - performs Addition, Subtraction, bitwise AND, bitwise OR over 16-bit inputs

- Olim: 1) To store 10 numbers in registers 1 to 10
  - @ Compute their sum & write result in another regreter

## Procedure:

Consider the numbers to be stored are:

1, 2, 4, 8, 16,

32, 64, 128, 256, 512

- (1) Set WA to 0001, Data-in to DEC 1.
- 2) Let neg Drite to 1. Toggle the Clock.

  DEC 1 is stored in register and address 0001
- (3) Keep repeating 'step 122 till all desired numbers are stored
- (4) Set reglière to 0. Now all the numbers are stored.
- (5) Set RA2 to 1011 (from 0001 to 1010, numbers are stoud) Set WA to 1011, sel to 1
- 6 Set regionite to 1. Set regRead to 0
- 9 Set RAI to 0001. Toggle the clock
- (B) Repeat step 7 for RA1 from 0010 to 1010. (B)
  Finally sum of all numbers is stored at register 1011