Quiz-3_CS321-4thNovember2020

Total points 33/50

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✓ Global variables are accessed using the global pointer ($gp), which is initialized to 1/1

- 300080000
- 200080000
- 10000000
- 700080000
- (●) 100080000 ✓

✓ Opcode part of MIPS instruction has x bits (give answer in decimal) 2/2

6 ✓

✓ Assembler turns the assembly language code into an object file containing machine language code. Assuming two pass assembly process. In First pass 1/1

- ○ assembler assigns and instruction addresses
- ○ finds all the symbols
- ○ Identifies labels and global variable names
- ◉ All of the above ✓

✗ Select from the following examples which meets architecture design principles: simplicity favors regularity 0/1

- ○ Each instruction has a 6-bit opcode
- ○ MIPS has only 3 instruction formats (R-Type, I-Type, J-Type).
- ◉ Each instruction format has the same number and order of operands ✗
- ○ Each instruction is the same size, making decoding hardware simple
- ○ All of the above

Correct answer

- ◉ All of the above

✓ Which of the following is/ are pseudo-instructions (select all that apply) 1/1

- ◉ li ✓
- ○ ori
- ○ blt
- ○ addi

✗ Consider memory storage of a 32-bit word stored at memory word 42 in a byte addressable memory. What are the byte addresses that memory word 42 spans? (give answer in hex eg. XX, XX,XX,XX). ···/2

A8,A9,AA,AB ✗

Correct answer

A8, A9, AA,AB

✓ The dynamic data segment holds the stack and the heap ($sp), in MIPS $sp is initialized to 1/1

- 300080000
- 200080000
- 10008000
- 0x700080000
- FFFFFFC ✓
- Other:

✗ In MIPS, Frame pointer register is (give answer in decimal) ···/2

28 ✗

Correct answer

30

✓ Consider memory storage of a 32-bit word stored at memory word 42 in a byte addressable memory. What is the byte address of memory word 42? (give answer in hex eg. XX). 2/2

A8 ✓

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✓ Assembler turns the assembly language code into an object file containing machine language code. Assuming two pass assembly process. In second pass 3/3

- ○ assembler assigns and instruction addresses
- ○ finds all the symbols
- ○ Identifies labels and global variable names
- ◉ produces the machine language code ✓
- ○ All of the above

✗ 16 bit address can load word within the range of 0/1

- (●) 2^17 ✗
- ( ) 2^16
- ( ) 2^14
- ( ) 2^15

Correct answer

- (●) 2^15

✗ In MIPS, Jump Register equivalent to ..... instruction X86 ···/2

jmp ✗

Correct answers

RET

RETURN

return

✗ Suppose that " ALUOp1" in the single-cycleMIPS processor has a stuck-at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction? Why? 0/3

- ○ R-type
- ○ lw
- ○ addi
- ◉ all of the above ✗

Correct answer

- ◉ R-type

✓ operating system loads a program by reading the text segment of the executable file from a storage device (usually the hard disk) into the segment of memory. 2/2

- ○ data
- ◉ text ✓
- ○ stack
- ○ heap

✓ identify MIPS pseudoinstruction 1/1

- ○ beq
- ○ ori
- ◉ move ✓
- ○ jmp

✓ Registers that used for Values for Function Results and Expression Evaluation 1/1

- ○ 1-2
- ◉ 2-3 ✓
- ○ 4-5
- ○ 6-7

✓ In MIPS, stack pointer register is (give answer in decimal) 2/2

29 ✓

✓ Select the odd one out 1/1

- ○ IA-32
- ○ MIPS
- ○ SPARC
- ○ PowerPC
- ◉ ESP-32 ✓

✓ Consider following instructions. addi $s0, $0, 73; sw $t1, -7($t2); sub $t1, $s7, $s2. Which instructions from the list are I-type instructions? 1/1

- 2-3
- 1-2 ✓
- 1-3

✓ In MIPS, Jump And Link equivalent to ..... instruction X86 2/2

call ✓

✓ Functional Part of MIPS instruction has x bits (give answer in decimal) 2/2

6 ✓

✓ Opcode part of MIPS instruction has x bits (give answer in decimal) 2/2

6 ✓

✓ MIPS architecture defines an optional floating-point coprocessor,known as coprocessor 1. There are X even-numbered registers are used to specify double-precision operations 1/1

- ○ 32
- ◉ 16 ✓
- ○ 64
- ○ 8

✓ NOP instruction can implemented using 1/1

- ○ add
- ○ sub
- ○ or
- ◉ all of the above ✓

✗ Select from the following examples which meets architecture design principles: Make the common case fast 0/1

- ○ Registers make the access to most recently accessed variables fast
- ◉ The RISC (reduced instruction set computer) architecture, makes the common/ simple instructions fast because the computer must handle only a small number of simple instructions ✗
- ○ Most instructions require all 32 bits of an instruction, so all instructions are 32 bits. The instruction size is chosen to make the common instructions fast.
- ○ All of the above

Correct answer

- ◉ All of the above

✗ Suppose that " MemWrite" in the single-cycle MIPS processor has a stuck-at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction? Why? 0/2

- ○ R-type
- ○ sw
- ○ addi
- ◉ all of the above ✗

Correct answer

- ◉ sw

✗ Which of the following statements best describes the use of the rt field by the MIPs sw instruction 0/1

- (●) The contents of the rt register are added to the signed 16-bit constant and used as a memory address ✗
- ( ) The contents of the rt register are added to 4 times the signed 16-bit immediate field and used as a memory address
- ( ) The contents of rt are stored into memory
- ( ) The contents of the memory location with the address pointed to by rt are stored in memory
- ( ) The 5-bit value encoded in the rt field is stored in memory

Correct answer

- (●) The contents of rt are stored into memory

✗ text segment stores the machine language program. It is large enough to accommodate almost X MB of code 0/2

- ( ) 1024
- (●) 128 ✗
- ( ) 512
- ( ) 256
- ( ) Other: .....

Correct answer

- (●) 256

✓ Jump instruction has x bits for address (give answer in decimal) 2/2

26 ✓

✓ Suppose that "RegWrite" in the single-cycleMIPS processor has a stuck-at-0 fault, meaning that the signal is always 0,regardless of its intended value. What instructions would malfunction? Why? 2/2

- ○ R-type
- ○ lw
- ○ addi
- ◉ all of the above ✓

✓ Opcode part of MIPS instruction has x bits (give answer in decimal) 2/2

6 ✓

Name *

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