CS225: Final Examination

Max Marks: 100 Time: 3 Hours

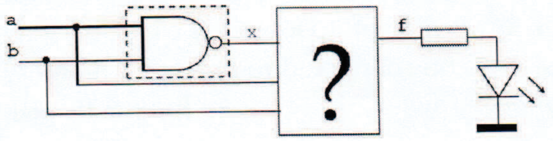
Q1: (a) Suppose we have a 7-bit computer that uses IEEE floating-point arithmetic where a floating point number has 1 sign bit, 3 exponent bits, and 3 fraction bits. For each of the following, write the binary value and the corresponding decimal value of the 7-bit floating point number that is the closest available representation of the requested number. If rounding is necessary use round-to-nearest. Give the decimal values either as whole numbers or fractions. The first line is filled in for you.

Number	Binary	Decimal
0	0 000 000	0.0
-0.125		
Smallest positive normalized number		
Largest positive number < ∞∞		
-3.1		
12.25		

(b) Represent the following numbers using signed and 2's complement representations (assume a 16 bit computer) (i) 224 (ii) -65 **[points (5 +5)]**

Q2: Implement the following function using CMOS logic F= ((x + y)z)'

(b) Design a simplified circuit that verifies the logical operation of a NAND gate. f = '1' (LED ON) if the NAND gate does NOT work properly. Assumption: when the NAND gate is not working, it generates 1's instead of 0's and vice versa.



[points (3 +7)]

Q3: Design a BCD counter via a Finite State Machine (FSM): The counter has the following features

- Count:0,1,2,3,4,5,6.7,8,9,0,1,2 ....
- Reset: Initializes the count to 0
- Output 'z' becomes '1' when count is 9.
  (a) Provide the state diagram and excitation table. Is this a Moore or Mealy Machine
  (b) Sketch the circuit (simplify your circuit using K-Maps) **[points (4+6)]**

Q4: **(a)** Design a single bit magnitude comparator that has two outputs, a greater than or equal to output (gte) and a less than or equal to output (lte).

(b)Using (a) design a 4 bit ripple carry style magnitude comparator that has two outputs GTE and LTE. Assume two inputs A= a3a2a1a0; B=b3b2b1b0. Modify block in (a) if necessary.

(c) Show a modified block schematic of the above design to pass the greater number to the output (use appropriate extra functional block if necessary)

[points (2 +5+3)]

Q5: (a) Design a 4 bit register with two control inputs s1 and s0, 4 data inputs I3, I2,I1, and I0 and 4 data outputs Q3, Q2, Q1, and Q0.

When s1s0=00, the register maintains its value.; When s1s0=01, the register loads $I_3I_2I_1I_0$
When s1s0=10, the register loads 0000; When s1s0=11, the register complements itself, so for example 0000 would become 1111, and 1010 would become 0101.

(b) Assume Mux is implemented using basic gates. Estimate the maximum frequency of operation of the above design. Assume the following parameters for each of flops and gates. *D flop:* t_{ccq} = 30 ps; t_{pcq} = 50 ps ; t_{setup} = 60 ps;t_{hold} = 70 ps; Gates: t_{pd} = 35 ps t_{cd} = 25 ps

[points (5+5)]

Q6: (a) Design a 4 bit 2' Complement Adder/Subtraction circuits using full adders and extra logic. (b)Assuming delay of the gates is 1ns compute addition delay and subtraction delay.

(c) How will you identify overflow in the addition/subtraction? Show the circuit?

(points (4+3+3)

Q7: Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms.

$A(x, y, z) = \sum(1, 3, 5, 6)$
$B(x, y, z) = \sum (0, 1, 6, 7)$
$C(x, y, z) = \sum (3, 5)$
$D(x, y, z) = \sum (1, 2, 4, 5, 7)$

[points (2 +5+3)]

Q8: (a) Compare SRAM, DRAM, and FLASH Memory structures?

(b) A computer system has 8-bit wide data bus uses RAM chips of 4096 x 1-bit capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 16 K-bytes . Show the address mapping for each row ? **[points (6 +4)]**

Q9: (a) Given F(x,y,z)= $x \oplus y \oplus z$

Implement F using (a) 8:1 MUX , (b) using a 4:1 Mux only (c) using 2:1 Muxes only (d) Using a Look up table (LUT)

(b) State and explain Shannon Expansion Theorem. Illustrate with examples **([points (4 +6)]**

Q10: Design a 5 bit array Multiplier (Assume A= a4a3a2a1a0; B=b4b3b2b1b0) . Compute the maximum frequency of operation assuming a gate delay 1ns for basic gates **[points (5+5)]**