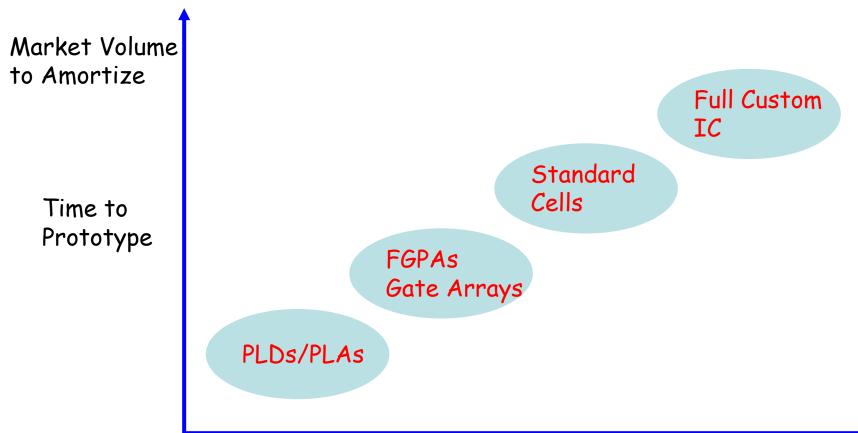
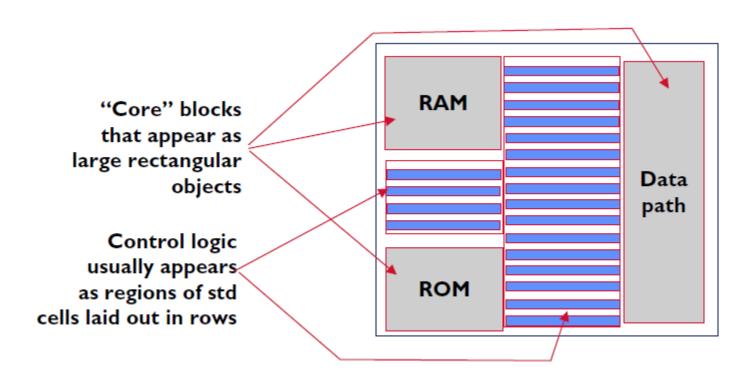
FPGA - Field Programmable Gate Array

Alternative Technologies for IC Implementation

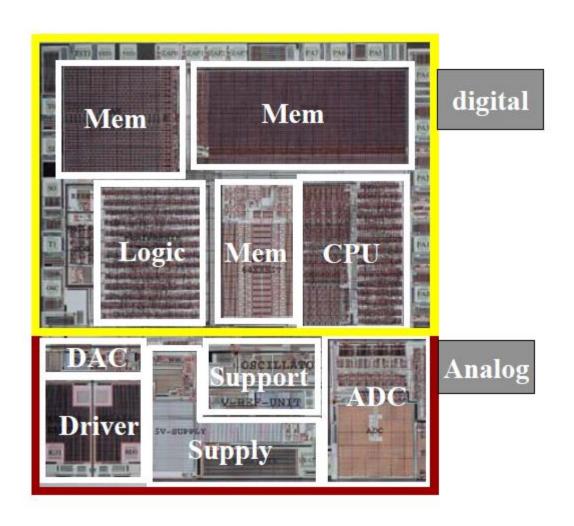


Nonrecurring engineering cost Process Complexity Density, speed, complexity

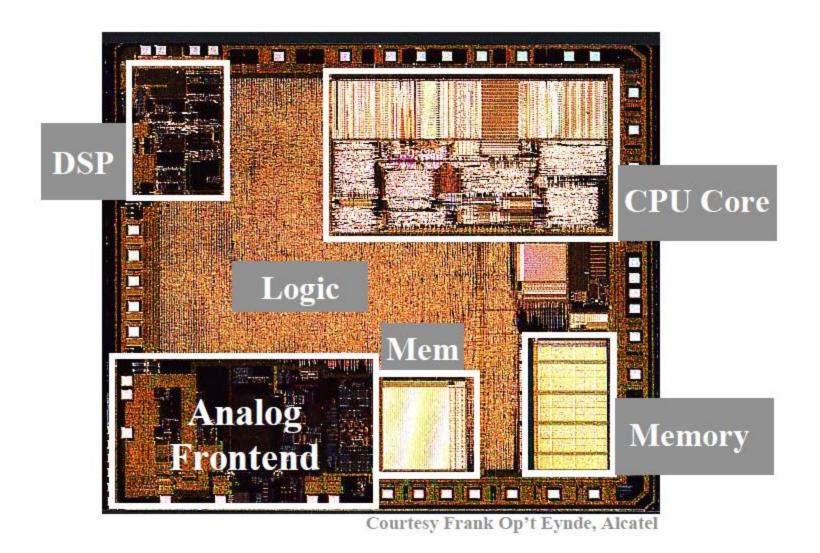
System on Chip



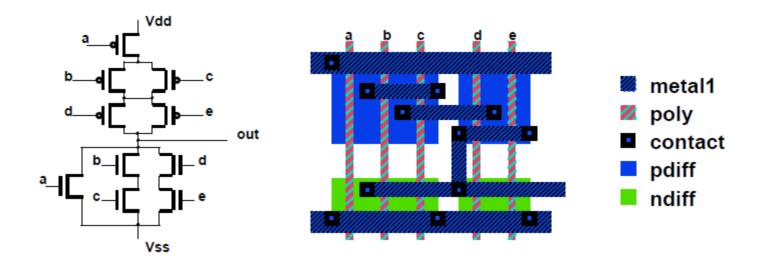
System on chip – example(automotive)



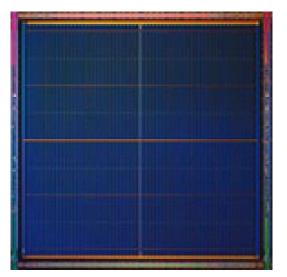
System on chip -example(Telecom)

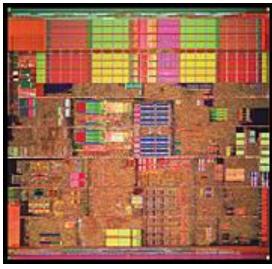


Full custom- for Implementation



Die Photos: Vertex vs. Pentium IV





- FGPA Vertex chip looks remarkably well structured
 - Very dense, very regular structure
- Full Custom Pentium chip somewhat more random in structure
 - Large on-chip memories (caches) are visible

Review

x_2	x_1	x_0	$F(x_2, x_1, x_0)$
0	0	0	0 = F(0,0,0)
0	0	1	1 = F(0,0,1)
0	1	0	0 = F(0,1,0)
0	1	1	0 = F(0,1,1)
1	0	0	1 = F(1,0,0)
1	0	1	1 = F(1,0,1)
1	1	0	1 = F(1,1,0)
1	1	1	0 = F(1,1,1)

Shannon showed that the logic expression for the above F can be obtained by the following expansion

$$F(x_2, x_1, x_0) = \overline{x_2} \cdot \overline{x_1} \cdot \overline{x_0} \cdot F(0, 0, 0) + \overline{x_2} \cdot \overline{x_1} \cdot x_0 \cdot F(0, 0, 1) + \overline{x_2} \cdot x_1 \cdot \overline{x_0} \cdot F(0, 1, 0)$$

$$+ \overline{x_2} \cdot x_1 \cdot x_0 \cdot F(0, 1, 1) + x_2 \cdot \overline{x_1} \cdot \overline{x_0} \cdot F(1, 0, 0) + x_2 \cdot \overline{x_1} \cdot x_0 \cdot F(1, 0, 1)$$

$$+ x_2 \cdot x_1 \cdot \overline{x_0} \cdot F(1, 1, 0) + x_2 \cdot x_1 \cdot x_0 \cdot F(1, 1, 1)$$

$$F(x_2, x_1, x_0) = \overline{x_2} \cdot \overline{x_1} \cdot x_0 + x_2 \cdot \overline{x_1} \cdot \overline{x_0} \cdot + x_2 \cdot \overline{x_1} \cdot x_0 \cdot + x_2 \cdot x_1 \cdot \overline{x_0} = \sum m(1, 4, 5, 6)$$

POS form

$$F(x_{2}, x_{1}, x_{0}) = (x_{2} + x_{1} + x_{0} + F(0, 0, 0)) \cdot (x_{2} + x_{1} + \overline{x_{0}} + F(0, 0, 1)) \cdot (x_{2} + \overline{x_{1}} + x_{0} + F(0, 1, 0)) \cdot (x_{2} + \overline{x_{1}} + \overline{x_{0}} + F(0, 1, 1)) \cdot (\overline{x_{2}} + x_{1} + x_{0} + F(1, 0, 0)) \cdot (\overline{x_{2}} + x_{1} + \overline{x_{0}} + F(1, 0, 1)) \cdot (\overline{x_{2}} + \overline{x_{1}} + x_{0} + F(1, 1, 0)) \cdot (\overline{x_{2}} + \overline{x_{1}} + \overline{x_{0}} + F(1, 1, 1))$$

$$F(x_2, x_1, x_0) = (x_2 + x_1 + x_0) \cdot (x_2 + \overline{x_1} + x_0) \cdot (x_2 + \overline{x_1} + \overline{x_0}) \cdot (\overline{x_2} + \overline{x_1} + \overline{x_0}) = \prod M(0, 2, 3, 7)$$

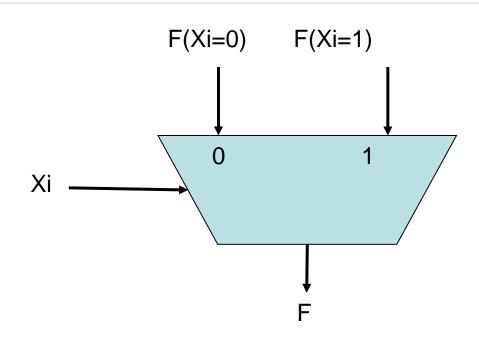
- C. E. Shannon, "A Symbolic Analysis of Relay and Switching Circuits," *Trans. AIEE*, vol. 57, pp. 713-723, 1938.
- Consider:
 - Boolean variables, X1, X2, ..., Xn
 - Boolean function, F(X1, X2, ..., Xn)
- Then $F = X_i F(Xi=1) + X_i' F(Xi=0)$
- Where
 - X_i' is complement of X_i
 - Cofactors, F(Xi=j) = F(X1, X2, ..., Xi=j, ..., Xn), j = 0 or 1

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Theorem

(1)
$$F = Xi \cdot F(Xi=1) + Xi' \cdot F(Xi=0) \forall i=1,2,3,...n$$

(2)
$$F = (Xi + F(Xi=0)) \cdot (Xi' + F(Xi=1)) \quad \forall i=1,2,3,...n$$



Example

$$f(a,b,c,d) = ab + b'cd + acd$$

$$f(a,1,c,d) \stackrel{b=1}{=} a + acd = \underbrace{a + acd}_{covering} = a$$

$$f(a,0,c,d) \stackrel{b=0}{=} cd + acd = \underbrace{cd + acd}_{covering} = cd$$

$$f(a,b,c,d) = b \cdot f(a,1,c,d) + b' \cdot f(a,0,c,d) \text{ Shannon's expansion}$$

$$= b \cdot a + b' \cdot cd$$

$$= ab + b'cd$$

Example-POS

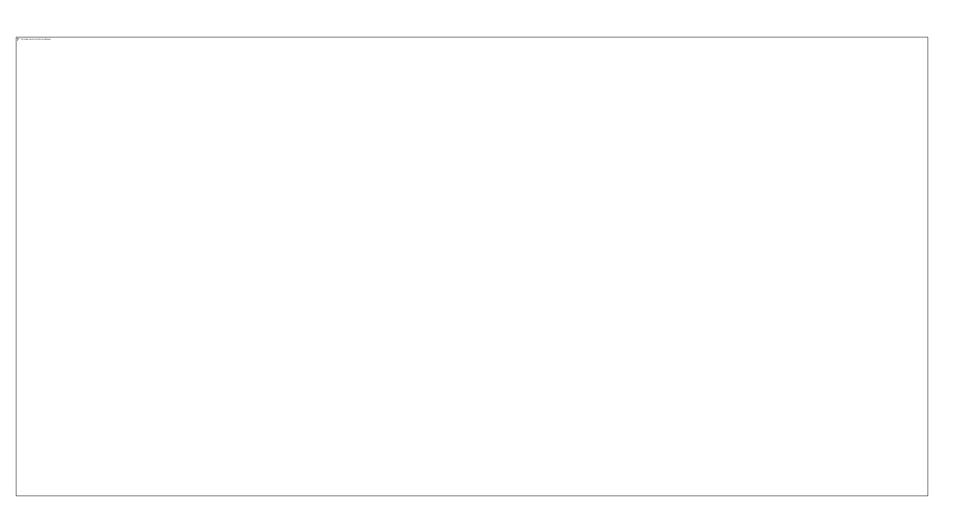
$$f(a,b,c,d) = (a+b+c)(a'+d)(b+c+d)$$

$$f(1,b,c,d) \stackrel{a=1}{=} (1+b+c)(0+d)(b+c+d) = \underbrace{(d)(a+c+d)}_{covering} = d$$

$$f(0,b,c,d) \stackrel{a=0}{=} (0+b+c)(1+d)(a+c+d) = \underbrace{(b+c)(b+c+d)}_{covering} = (b+c)$$

$$f(a,b,c,d) = (a+f(0,b,c,d))(a'+f(1,b,c,d)) \text{ Shannon's expansion}$$

$$= (a+b+c)(a'+d)$$



More examples

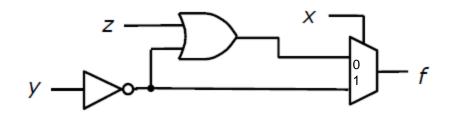
X	У	z	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

$$f=x'y'z'+x'y'z+x'yz+xy'z'+xy'z$$

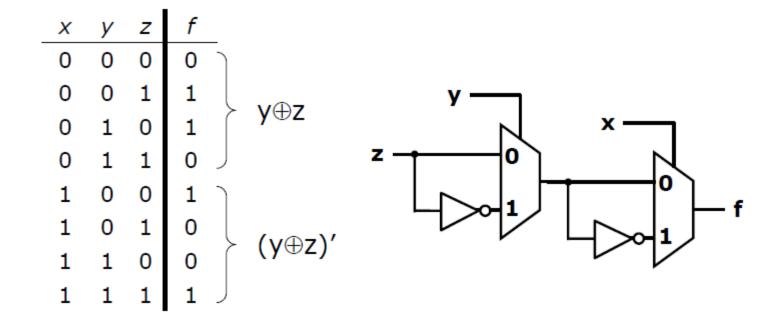
choose x as the expansion variable

$$f=x'(y'z'+y'z+yz)+x(y'z'+y'z)$$

$$f=x'(y'+z)+x(y')$$

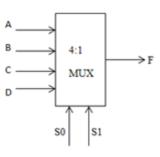


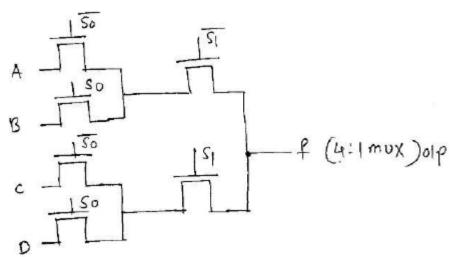
More examples



MUX implementation

S1	S0	F
0	0	Α
0	1	В
1	0	С
1	1	D





MUX implementation

