Indian Institute of Technology Patna
Department of Electrical Engineering

EE101 - Electrical Sciences
Autumn - 2014
End Sem Exam
26 November 2014

There are 5 problems. $(5 \times 10 = 50)$

1. Consider a two stage common emitter amplifier circuit shown in Figure 1. $V_{CC} = 9$ V, $R_1 = 100$ kΩ, $R_2 = 47$ kΩ, $R_E = 3.9$ kΩ, $R_C = 6.8$ kΩ , $R_S = 5$ kΩ, $R_L = 2$ kΩ and $\beta = 100$. Assume $V_{BE} = 0.7$ V.

   (a) Draw the small signal model of a complete circuit. **(5 points)**

   (b) Determine the gains $A_1 = \frac{v_{o1}}{v_i}$ and $A_2 = \frac{v_{o2}}{v_{o1}}$. **(4 points)**

   (c) What is the overall gain? **(1 point)**

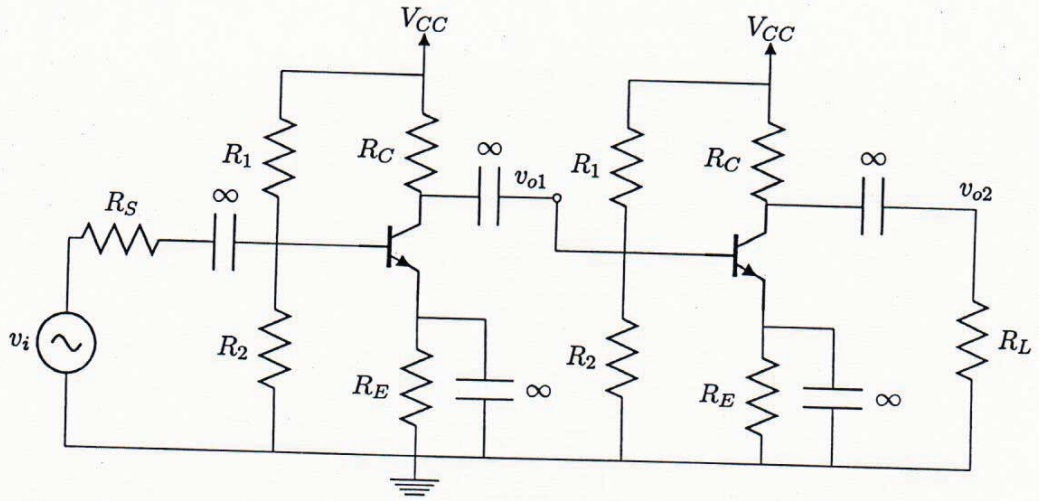


Figure 1

2. Consider the op-amp circuit shown in Figure 2. It consists of a resistor and a nonlinear element N whose $i - v$ characteristics is

$$i_N = \begin{cases} K v_N^2; & v_N \geq 0 \\ 0; & v_N < 0 \end{cases}$$

where $K = \frac{1}{2}\left(\frac{\text{Amp}}{\text{Volt}^2}\right)$. Assume the op-amp is ideal.

   (a) Find v_O if $v_I = 4$ V. **(5 points)**

   (b) If $v_I = 4 + 0.001\sin(\omega t)$ V, the output voltage v_O can be represented as $v_O = V_O + v_o$. Draw the small signal model. **(3 points)**

   (c) Find the small signal gain $A = \frac{v_o}{v_i}$. **(2 points)**

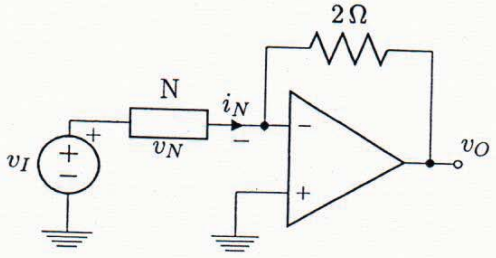


Figure 2

3. Consider the op-amp circuit shown in Figure 3. Assume the circuit is in sinusoidal steady state and the op-amp is ideal. If $v_i(t) = V_I \sin(\omega t)$ is applied, the output $v_o(t)$ will be of the form $v_o(t) = V_O \sin(\omega t + \phi)$.

(a) Determine V_O and ϕ in terms of V_I, R, C_1, C_2 and ω. **(6 points)**

(b) Find $A = \left|\frac{V_O}{V_I}\right|$ and plot A Vs ω. **(3 points)**

(c) Identify the type of filter. **(1 point)**

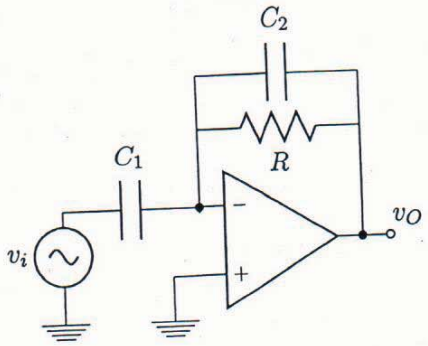


Figure 3

4. Given the truth table for the logic function F:

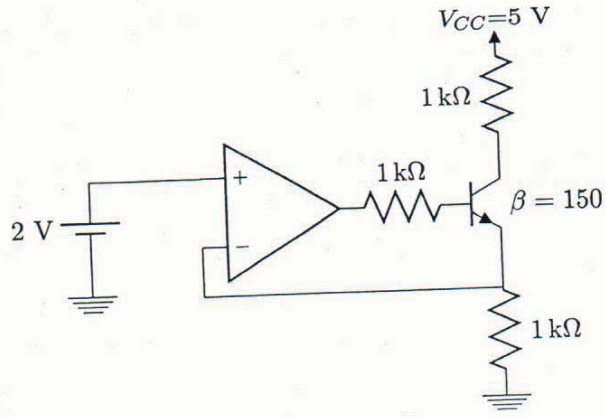
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(a) Write the sum of products (SOP) expression. **(2 points)**

(b) Find the minimum SOP expression. **(4 points)**

(c) Implement the minimum SOP using only NAND gates. **(4 points)**

5. (a) Identify the mode of operation of BJT in the following circuit. **(5 points)**



(b) Design a logic circuit to operate a lamp using two switches for the following condition. The lamp should not glow when both the switches are ON and OFF. Implement the circuit using only NOR gates. **(5 points)**