Roll:_____

CS 321: Computer Architecture

Mid-Semester Exam. Max Marks: 35 (52 Pt), Max Time: 120 minutes, Sept 2017

(No electronic equipment (Mobile, Calculator etc.) is allowed)

(**Instructions:** You must show your complete work. Marks will be awarded only based on what appears in your answer book. Please explicitly mention your assumptions, if it is essential and not given in the question.)

Answer to all Questions

1. Consider two different implementations, P1 and P2, of the same instruction set. There are four different classes of instructions (Arithmetic, Logic, Jump, Load, Store) in the instruction set. The clock rate and CPI of each class is given below. [3+3+4]

Processor	Clock Rate	CPI for Arithmetic	CPI for Logic	CPI for Jump	CPI for Load	CPI for Store
P1	1.0	2	1	2	3	3
P2	1.5	1	1	2	4	4

   (a) Assume that peak performance is defined as the fastest rate that a computer can execute any instruction sequence. What are the peak performances (Execution time) of P1 and P2 expressed in instructions per second?
   (b) If the number of instructions executed in a certain benchmark program is divided equally among the classes of instructions except for class Arithmetic, which occurs twice as often as each of the others: Which processor is faster? How much faster is it?
   (c) The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would be the performance achieved by the new processor P1 (P1_new) on the benchmark?

2. (a) Explain (with an example) how a 4-bit ALU can detect arithmetic overflow when adding two numbers. [3]

   (b) Depict the I type instruction format for MIPS processor showing the length of each field. [3]

   (c) Implement the pseudo-code **NOP** # No effect to any register or memory location just delay for a cycle, as a single or a couple of MIPS instruction(s). [3]

3. Translate the instruction ***f = g - A[B[4]];*** in C to equivalent MIPS. Assume that the variables f, and g are assigned to registers $s0 and $s1, respectively and the base address of the arrays (of integers) A and B are in registers $s6 and $s7, respectively. [8]

P. T. O

4. Consider a 16 bit floating point format (H2017) with 5-bit exponent field. Assume it uses the same principle of normalized numbers of IEEE 754 as discussed in class.

(a) State the Range of numbers that can be represented in the normalization form. [3]
(b) State the lowest fraction (precision) that can be represented. [2]
(c) Represent $(46.5)_{10}$ and $(0.625)_{10}$ in H2017 format binary representation. [4]

5. (a) Show the data path and control signal connections for a single cycle processor design of MIPS (components shown below Fig. 1) for the following instructions specifying the range of bits at the appropriate place. (you need to show only those datapath connection(s) and control signals required for that instruction (executing all the stages correspondingly), no credit will be given if anything extra line or a single connection line is missing).

(i) BEQ (Branch if equal) instruction of the MIPS instruction set architecture. [4]

(ii) JR (Jump Register), executing this instruction control needs to transfer to the new location specified by the Register. [4]

(b) Fill the control signal input accordingly as below [8]

Instruction	Rdst	RW	ASrc	MW	MR	M2R	Brn	Jmp
BEQ								
JR								

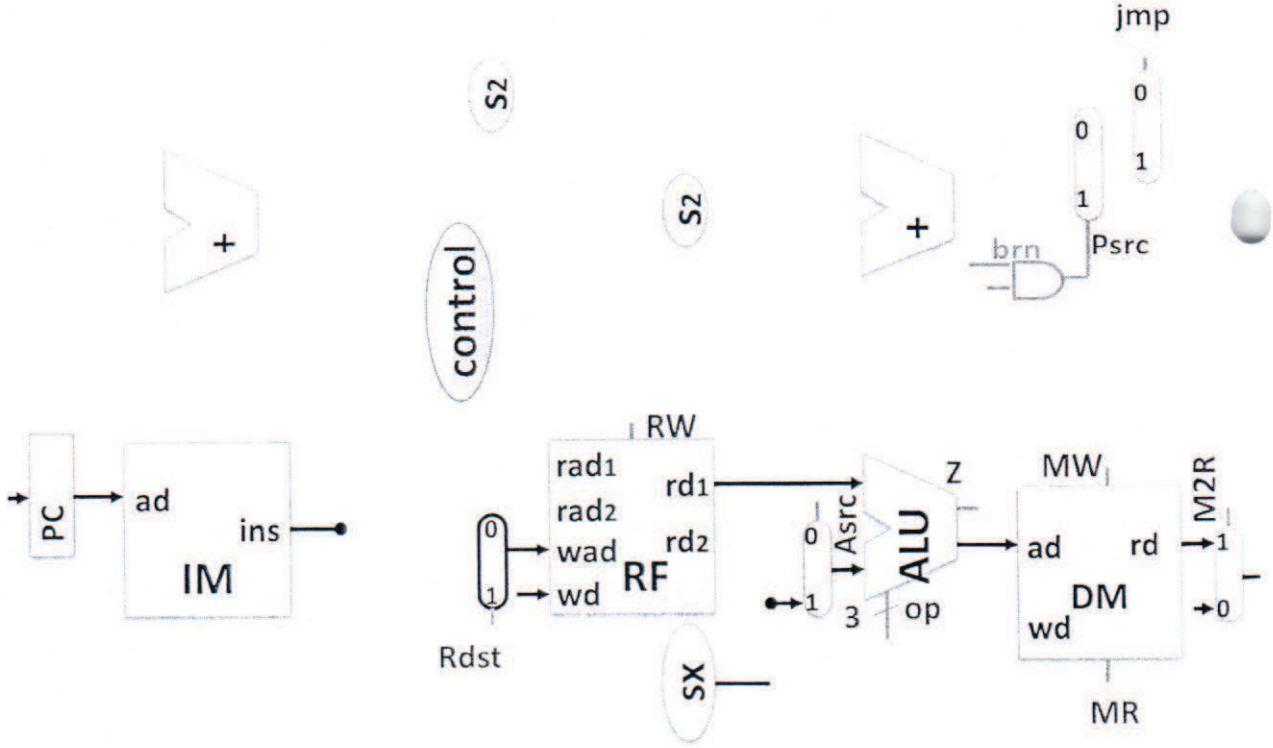

Fig. 1

Good Luck