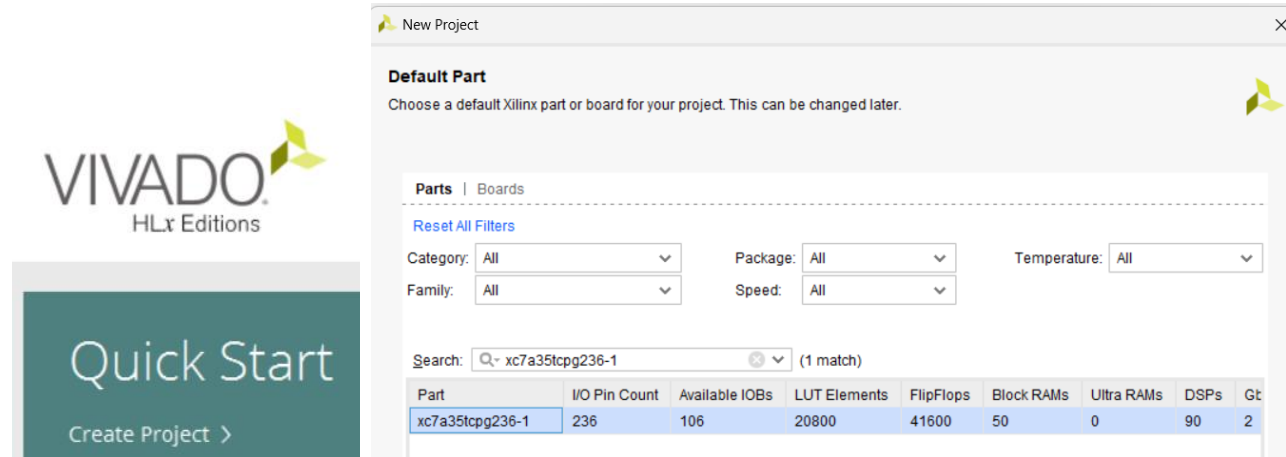


This guide will create a custom IP core for microblaze to handle all the basic IO interfaces on Basys3 board. Moreover, it will handle the switching signals for seven segment display.

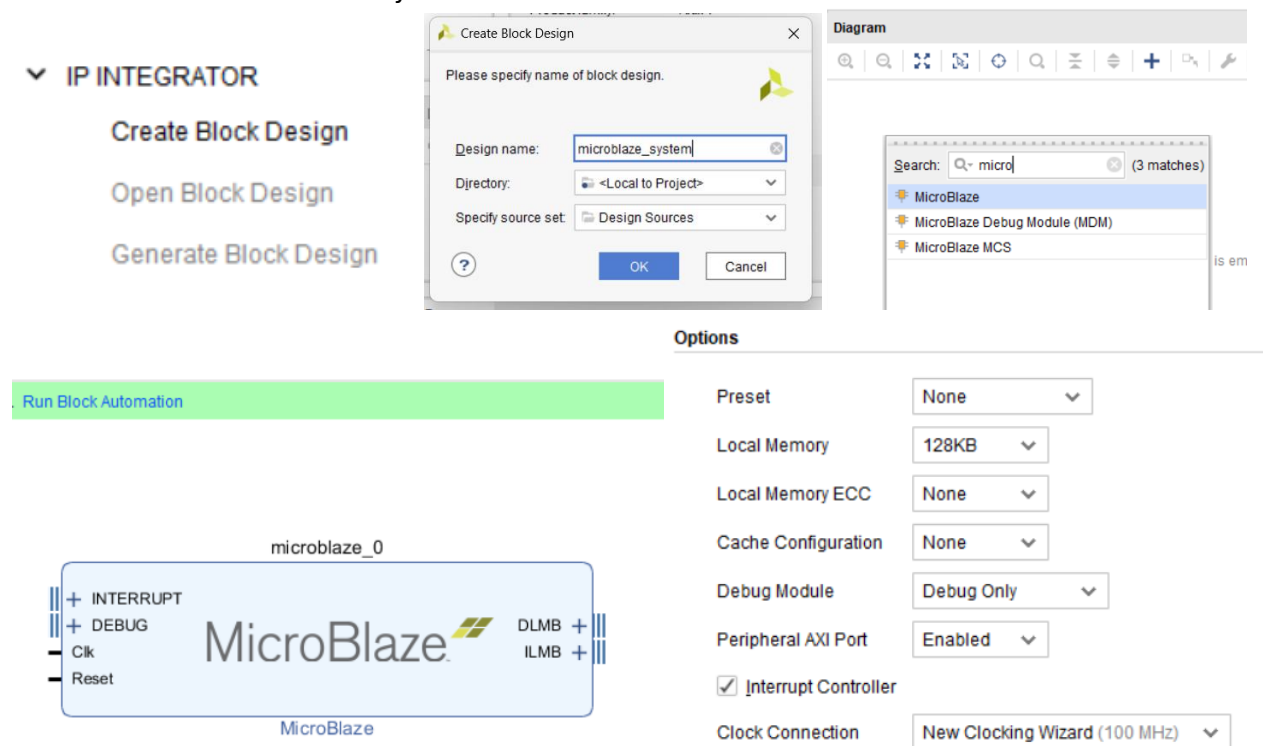
This guide has been inspired from “Building Custom AXI IP” guide from Xilinx

<https://www.xilinx.com/content/dam/xilinx/training/embedded/emdb/Building-Custom-AXI-IP.pdf>

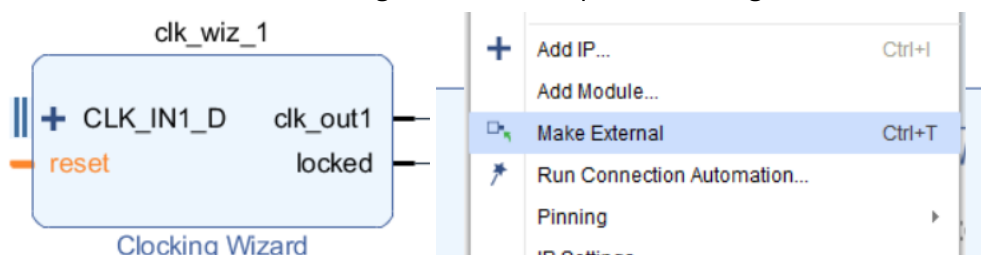
- 1- Create a new Vivado project. Instead of using board file, select the part number i.e. “xc7a35tcpg236-1”.



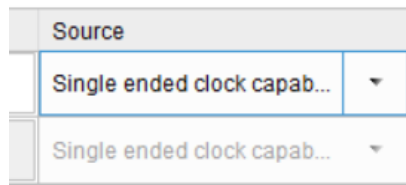
- 2- Create a minimal microblaze system.



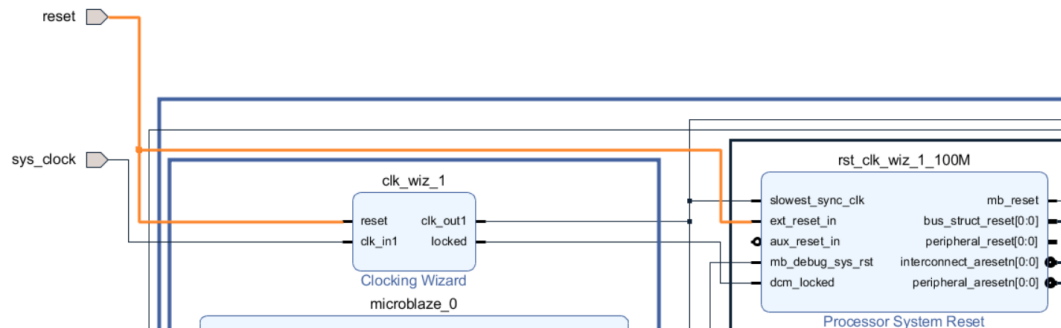
Run Connection automation. Right click “reset” pin of clocking wizard. Make it external.



Similarly, make clk_in1_d external as well after setting it 'single ended'.

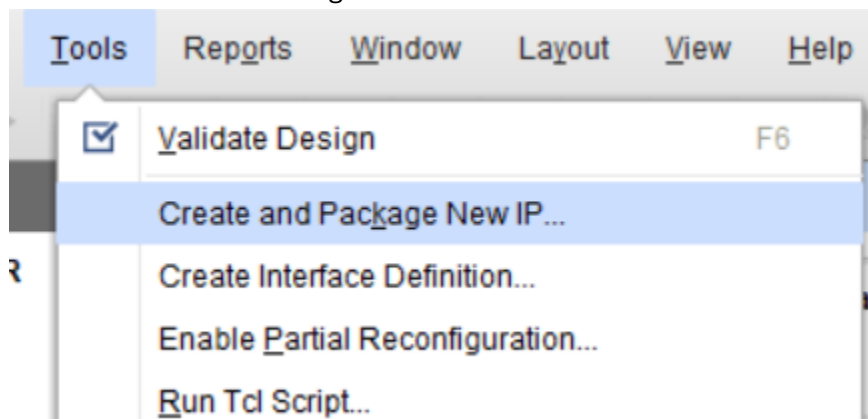


Make the following reset connection manually.

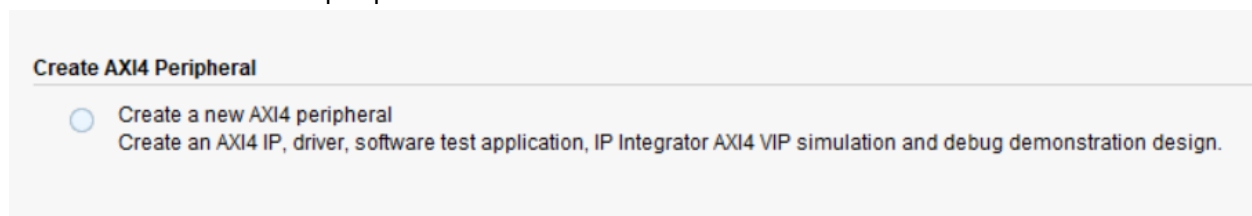


3- Add UARTlite IP. Run connection automation.

4- Select "Create and Package New IP" from tools.



Select create a new AXI4 peripheral.



Give it a name e.g. "multi_io"

Peripheral Details

Specify name, version and description for the new peripheral



Name:

Version:

Display name:

Description:

IP location:

☐ Overwrite existing

- 5- Leave the default connections intact. In the next screen, select “edit IP”

Create and Package New IP

Add Interfaces

Add AXI4 interfaces supported by your peripheral

☐ Enable Interrupt Support

Interfaces

S00_AXI

Name S00_AXI

Interface Type Life

Interface Mode Slave

Data Width (Bits) 32

Memory Size (Bytes) 64

Number of Registers 4 [4, 512]

Create Peripheral

Peripheral Generation Summary

1. IP (xilinx.com:user:multi_io:1.0) with 1 interface(s)
2. Driver(v1_00_a) and testapp [more info](#)
3. AXI4 VIP Simulation demonstration design [more info](#)
4. AXI4 Debug Hardware Simulation demonstration design [more info](#)

Peripheral created will be available in the catalog :

D:/RnD/Frameworks/FPGA/basys3/getting_started/ublaze_custom_ip/.ip_repo

Next Steps:

- ☐ Add IP to the repository
- ☒ Edit IP
- ☐ Verify Peripheral IP using AXI4 VIP
- ☐ Verify peripheral IP using JTAG interface

This will open a new Vivado project for IP customization.

- 6- Open the Verilog file for the newly generated IP.

Sources

Design Sources (2)

- multi_io_v1_0 (multi_io_v1_0.v) (1)
- multi_io_v1_0_S00_AXI_inst: multi_io_v1_0_S00_A

```
`timescale 1 ns / 1 ps

module multi_io_v1_0 #
(
    // Users to add parameters here

    // User parameters ends
    // Do not modify the parameters beyond this line

    // Parameters of Axi Slave Bus Interface S00_AXI
    parameter integer C_S00_AXI_DATA_WIDTH  = 32,
    parameter integer C_S00_AXI_ADDR_WIDTH  = 4
)
(
```

There would be two files.

- 7- Add ports for leds, dip switches, push buttons and seven segment display. Write Verilog code for the desired functionality. Set other IP-related parameters if needed in the components.xml. See the “Building Custom AXI IP” guide from Xilinx for details. Close the IP project.

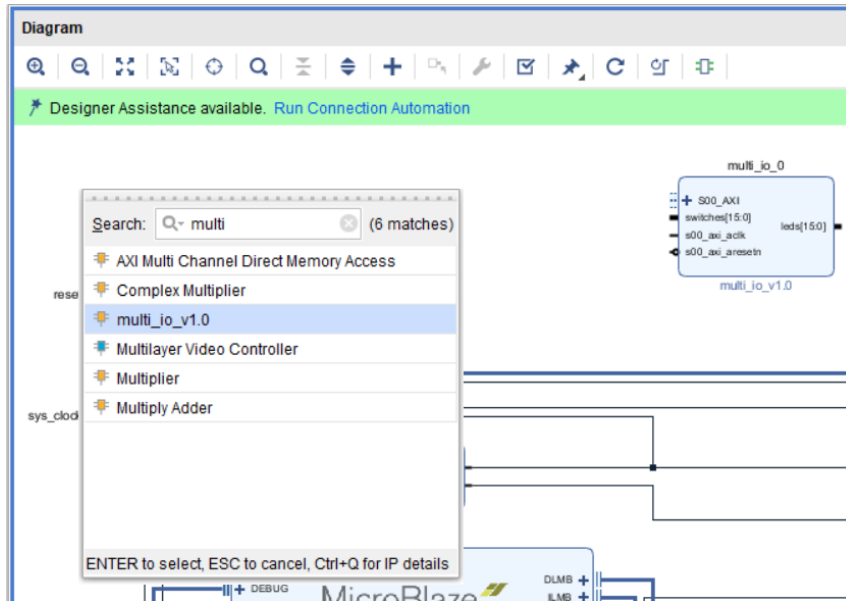
Sources

Design Sources (2)

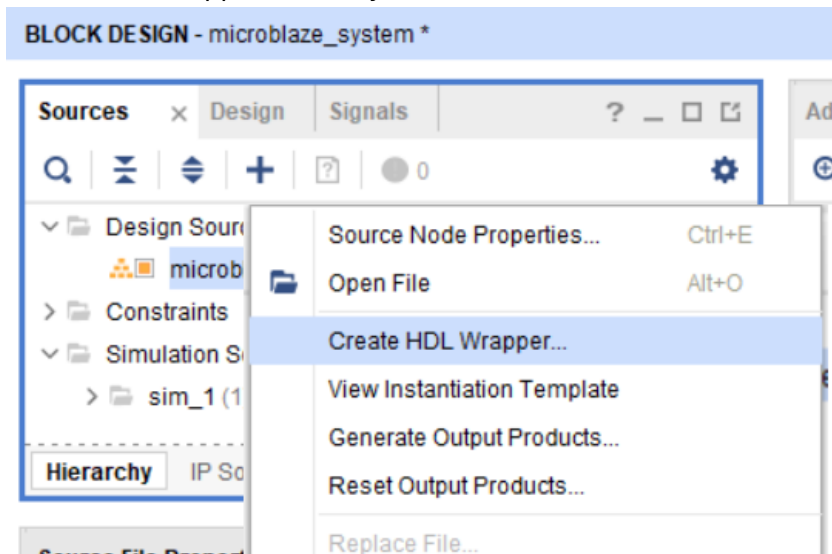
- multi_io_v1_0 (multi_io_v1_0.v) (1)
- IP-XACT (1)
 - component.xml

Constraints

8- Add the custom IP in microblaze board file. Make interfaces external.



9- Create HDL wrapper for the system.



10- Add the constraint file for Basys3 and manually add all the signals. Generate Bitstream and write code in SDK.