The FPGA configuration data is stored in files called bitstreams that have the .bit file extension. Bitstreams are stored in SRAM-based memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port. Basys3 FPGA can be programmed in 3 ways i.e. USB JTAG, USB Flash Drive and SPI Flash. Select the appropriate jumper location for each configuration.

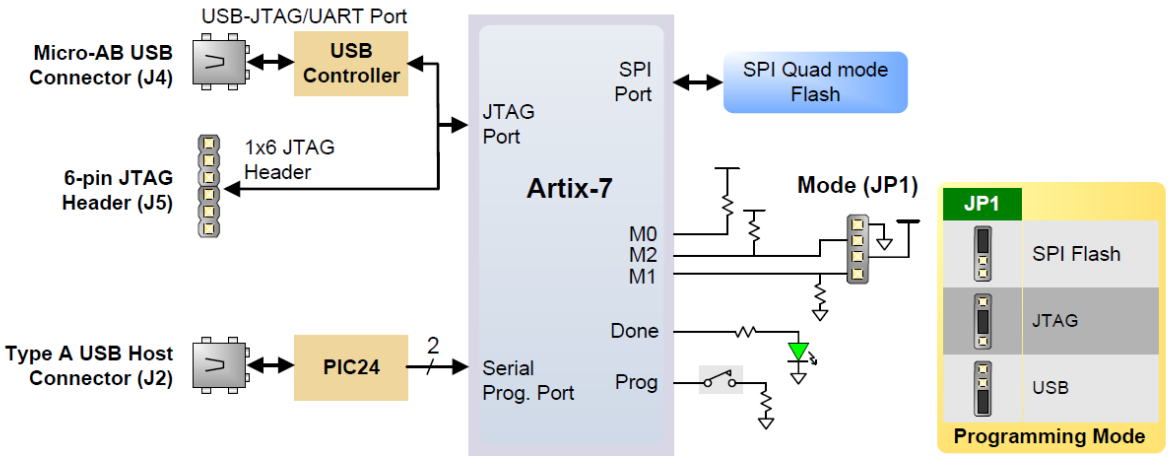
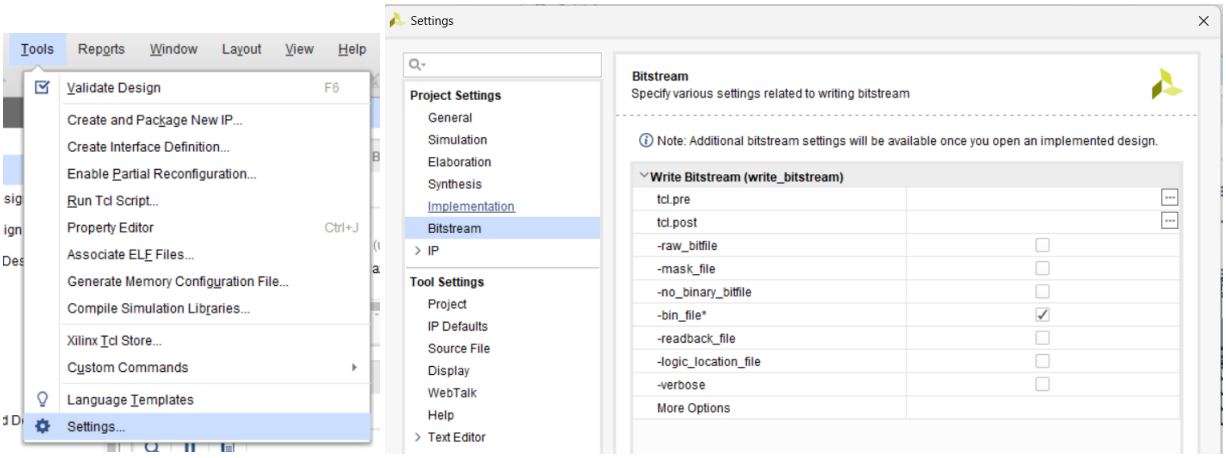


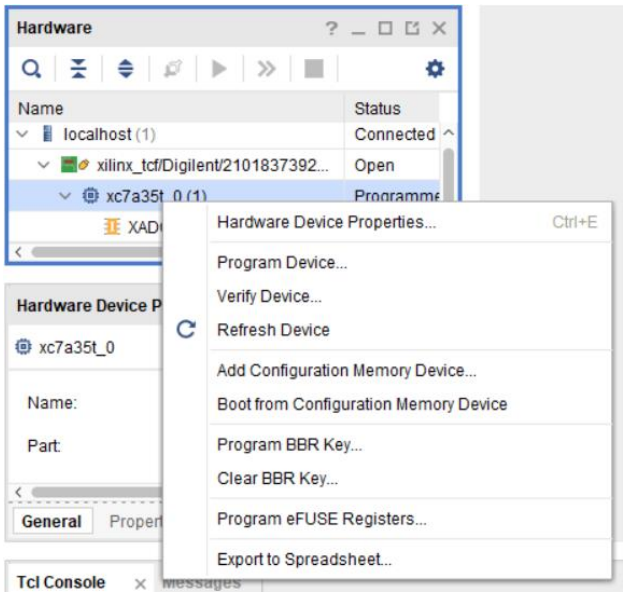

*Figure 3. Basys 3 configuration options.*

For QSPI Flash programming, go to project settings and select generation of “bin” file.

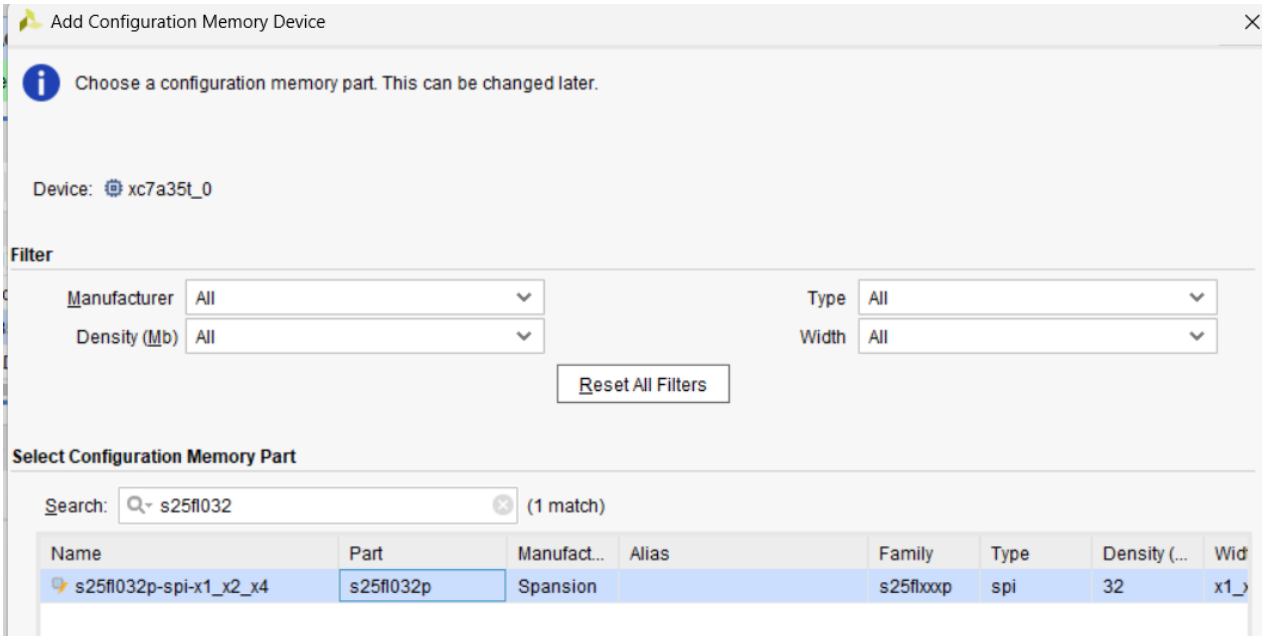


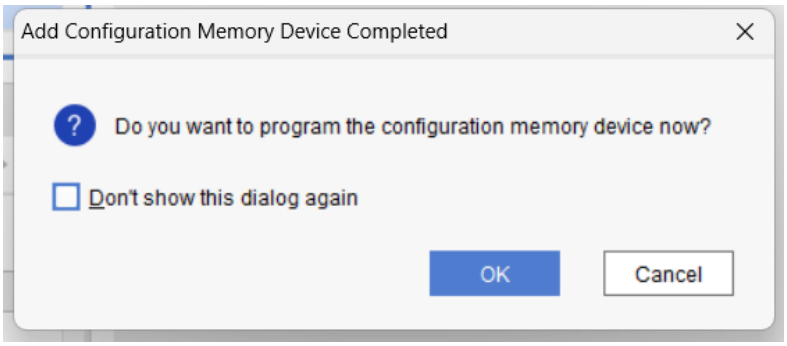

Resynthesize the project and create bitstream files.

In the hardware manager, select “Add configuration memory device”




Select “s25fl032” flash device and program.



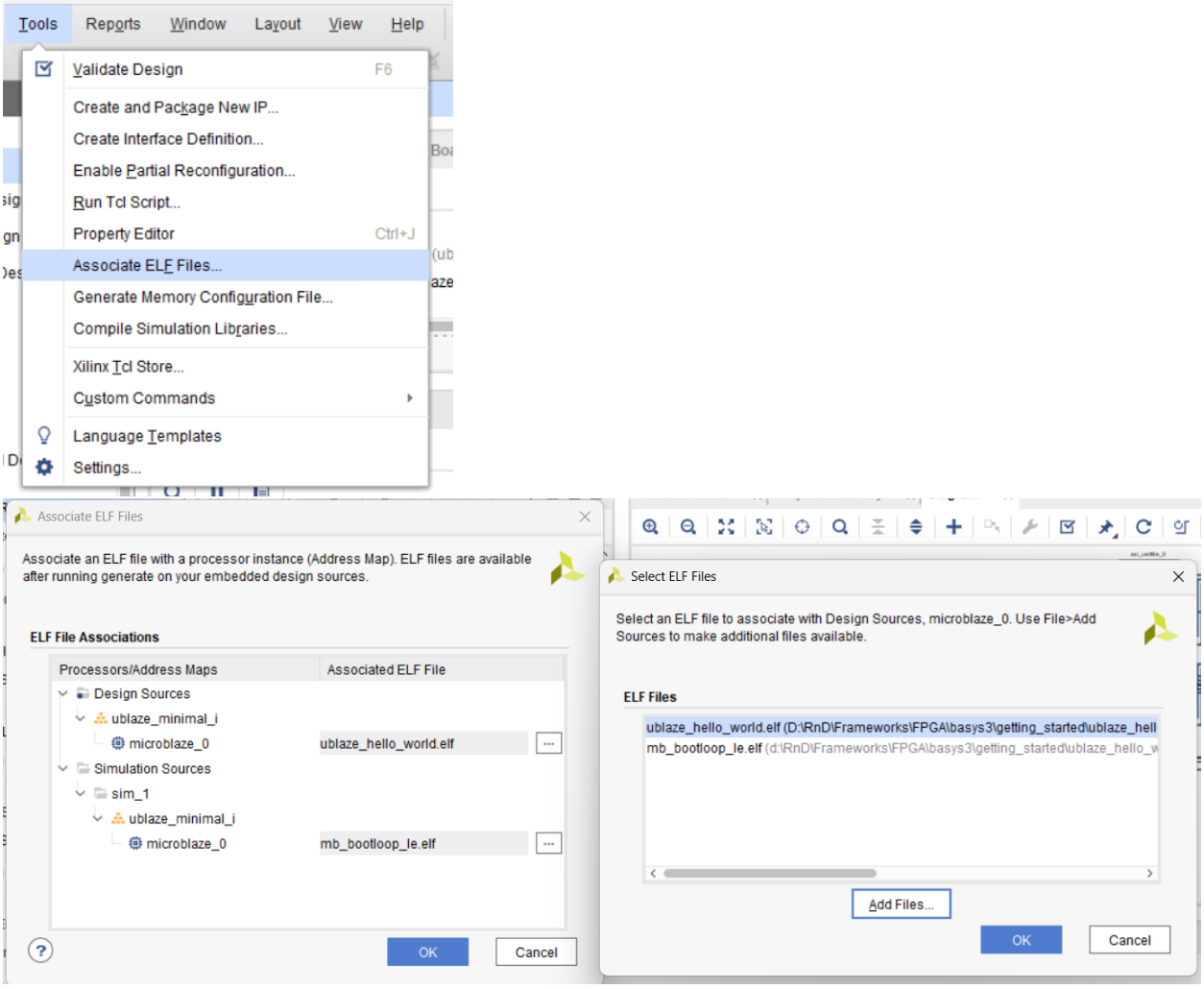



After programming finishes, press the reset button and wait a few seconds for the program to load.

**How to add the software "elf" file to the bitstream?**

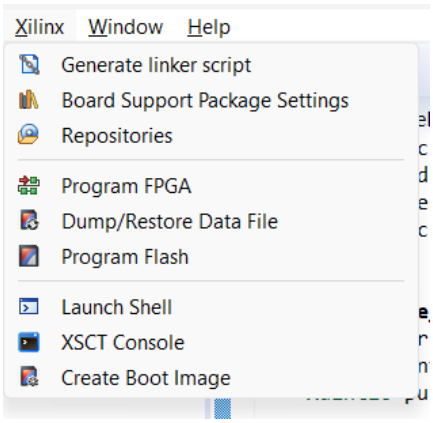
There are two ways to program the microblaze CPU in the design.

1) Generate the "elf" file in Xilinx SDK. Associate this file with bitstream in Vivado.




The generated bin file will now be updated with this elf file and be used to run the microblaze CPU.

2) In SDK, select "Program Flash"




Give the path to the updated bit file usually named “download.bit” in the software project directory. Select the same flash device and program.