**Processor Design**

**CS 3220**

**Final Report**

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**Design Choices**

Most of the design choices made during the creation of this project were taken to make sure the design comply with the *skeleton* and *interface* stated in the project description. Some changes made to the Lifetime FIFO so that the last value dequeued from the FIFO does not immediately gone until new value enqueued to the FIFO. This is so that the module able to handle the case when enqueue and dequeue signal are asserted together, in particular when the FIFO is also empty. Nevertheless, the overall behavior does not changed much except that it will now no longer guaranteed to output value 0 whenever the FIFO is empty. In the MACC, module sign shifting also implemented using bit concatenation instead as the original solution using ‘>>>’ operator does not always work correctly during the testing phase.

**­­Limitations**

The Lifetime FIFO is again the only limitations that I really noticed. The design I used for the Lifetime FIFO this time is similar with the one I submitted for the midterm and both has limitation that it will not compile due to not fit to the device if the memory depth is too deep. However, I managed to get it at least working for this project by manually setting the address width of the FIFO to 8. Another limitations of the design is that it only support the integer version and the FIFO requires to be initialized with 0’s.