Georgia Institute of Technology

School of Computer Science

CS3220: Fall, 2015

Project 2: Single Cycle Processor

Version 1.1

Due: Friday, October 16th, 2015 at 10:00pm

Project description:

In this project, you will design a single-cycle processor and synthesize it on your FPGA board. The processor should be able to support a specific ISA. The ISA will be developed and released on the course of next week, but you can start working on the rest of the project.

Note that there is no performance requirement (the logic optimization is not needed) and the only criterion for this project is the functionality.

Do not procrastinate. To get you started, we have provided you with a Project2.zip file with settings, timing requirements, and some of the Verilog codes for the design. It is highly recommended to begin working on the assembler and on the processor design immediately. You can manually create an object file to test your design until your assembler works. Once your assembler works, if your design still has problems, you could use the assembler to create test programs that can help you expose the problems in the design.

Within Project2.zip you'll find two assembly files Test2.a32 and Sorter2.a32, and a sample object file Sample.mif. The object file is an example of an object file generated from assembly code. You should implement your own assembler that reads the assembly code and generates the object files.

What to hand in via T-Square:

There are two things you have to submit.

(1) A brief 1-page report (PDF). Each person should submit his or her own report. The report should describe the approach taken when implementing the project, which problems were encountered, how the problems were fixed, and what the student's own contribution (i.e. which member of the group did what) to the project was. Note that it is fine if the two members of the group worked together (as in, sat together and got something working), and it is OK to say so in the report. If your report is missing, you will lose 50% of the points that you would otherwise earn. You should follow the following specific naming format:

SCProc[Student's Full Name].pdf (e.g. SCProcJongsePark.pdf).

(2) Zip file including the Quartus Project files and **ALL** the files that comprise the project (Verilog files, assembler, assembled .mif files, Quartus project file, etc.) (ZIP file)

If you miss to upload any file that your project requires, you will not be allowed to fix your project by pulling files from somewhere else. Your design should include a separate module for the controller of the single-cycle processor. You should name this file SCProcController.v. The project directory name and the zip file name should comply with the following naming formats:

Directory: SCProc[Student's Full Name] (e.g. SCProcJongsePark)
Zip file: SCProc[Student's Full Name].zip (e.g. SCProcJongsePark.zip)

Finally, you should submit your files through t-square.

Rules:

This project is a team project so you must work together with your teammate. The zip file you submit should be the same as the one submitted by your teammate but each person should write their own report.