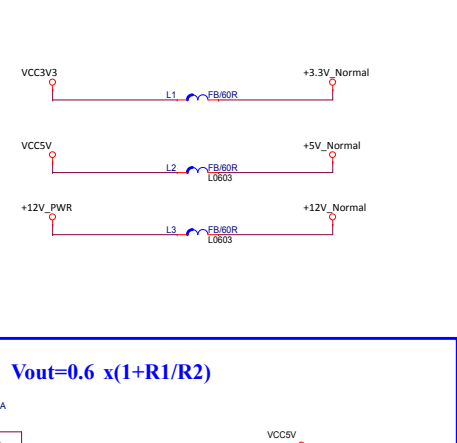


+12V DC-POWER Input

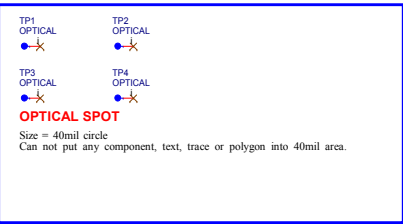
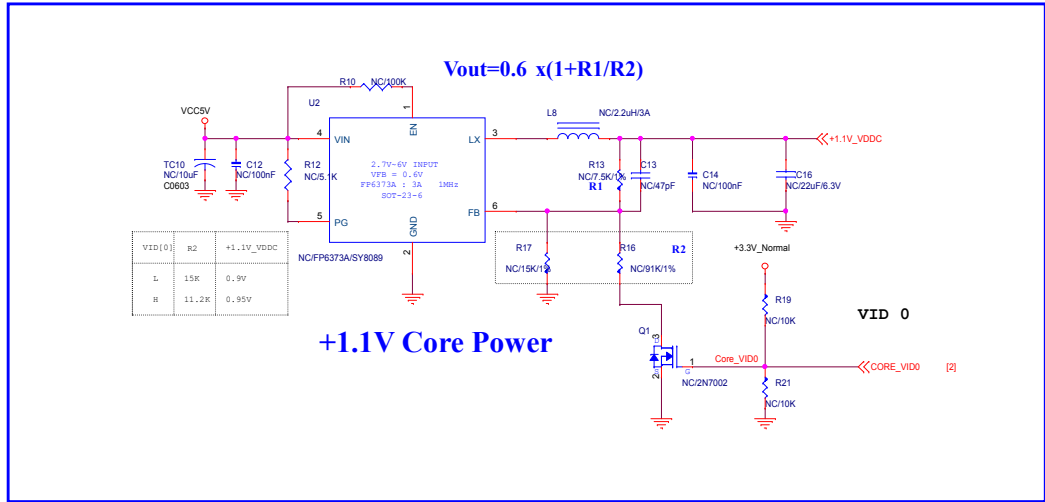
The diagram illustrates the +12V DC-POWER input circuit. It starts with a DC-JACK (J1) where the input signal enters through pin 1, labeled 'DC-IN-JACK'. The signal line is red and passes through a fuse (F1, FUSE 24V/5A) and a diode (D10, 1N4001) in series. The diode is oriented with its cathode towards the input. After the diode, the signal line splits: one branch goes to a capacitor (EC1, 470uF/25V) and the other to a capacitor (C1, 100nF). Both capacitors are connected to ground. The output is labeled '+12V_PWR'.



+5V Power

5V DC-DC $V_{out} = 0.6 \times (1 + R1/R2)$

LOW ESR capacitor is strongly recommended for C2



+3.3V_Power

$V_{out} = 0.6 \times (1 + R1/R2)$

2.7V~6V INPUT
VFB = 0.6V
FP6373A : 1A 1MHz
SO23-6

Select 1A or 2A DC/DC depend on Opration Current

Select 1A or 2A DC/DC depend on Oprarion Current

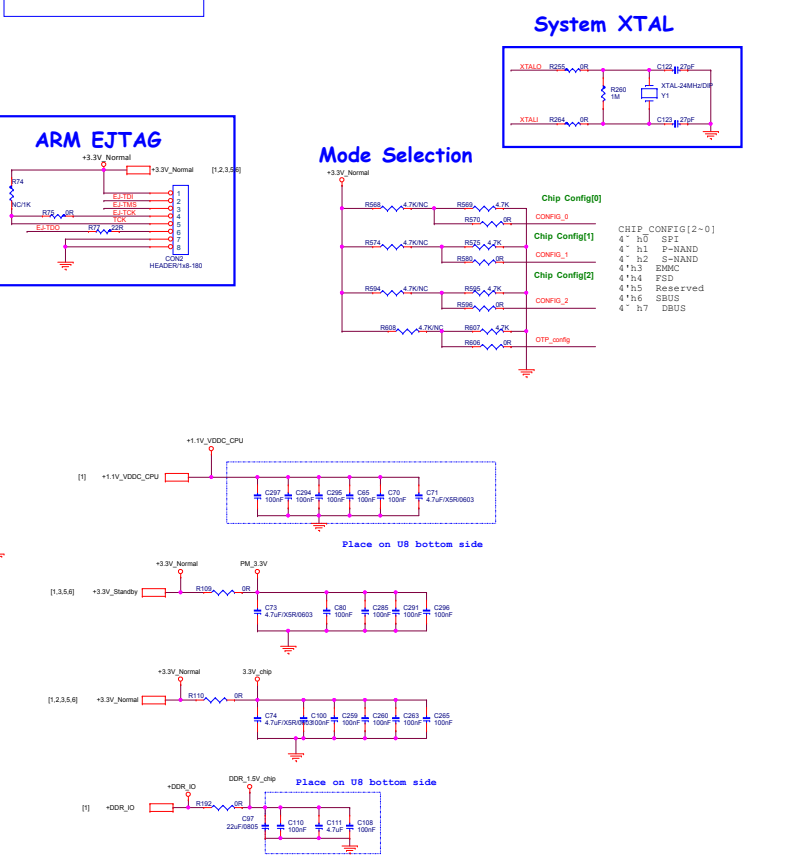
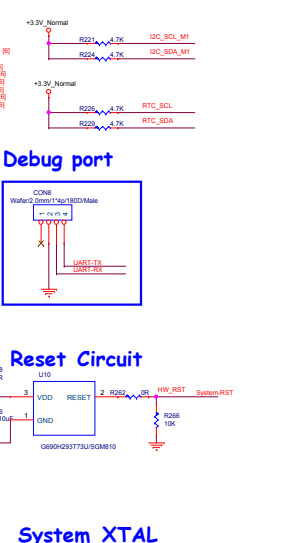
+1.1V CPU Power and Core Power $V_{out} = 0.6 \times (1 + R1/R2)$

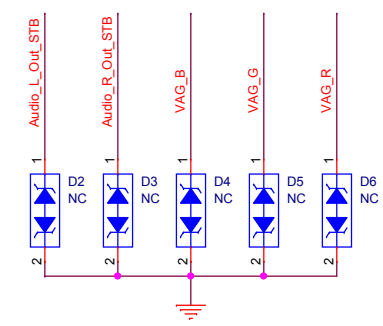
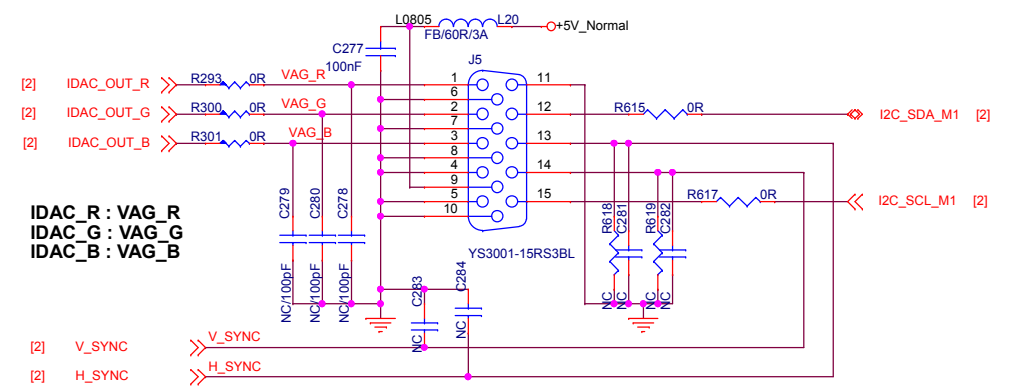
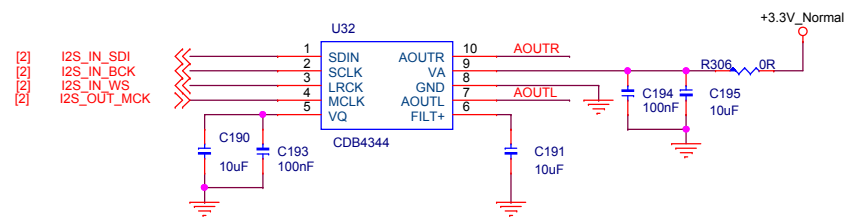
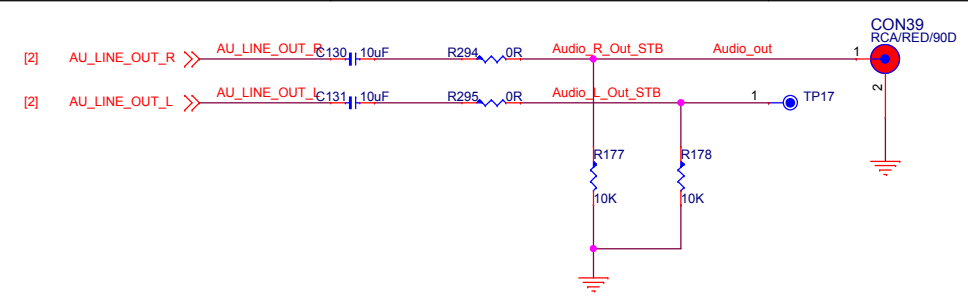
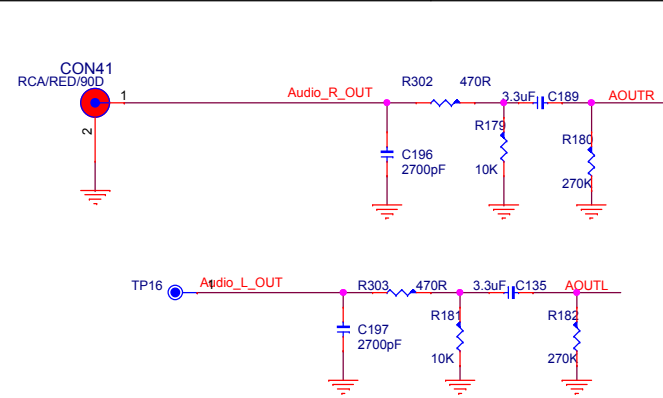
VID[1]	R2	+1.1V_VDDC_CPU
L	113K	1V
H	100K	1.05V

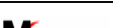
VID[1]	R2	+1.1V_VDDC_CP
L	113K	1V
H	100K	1.05V

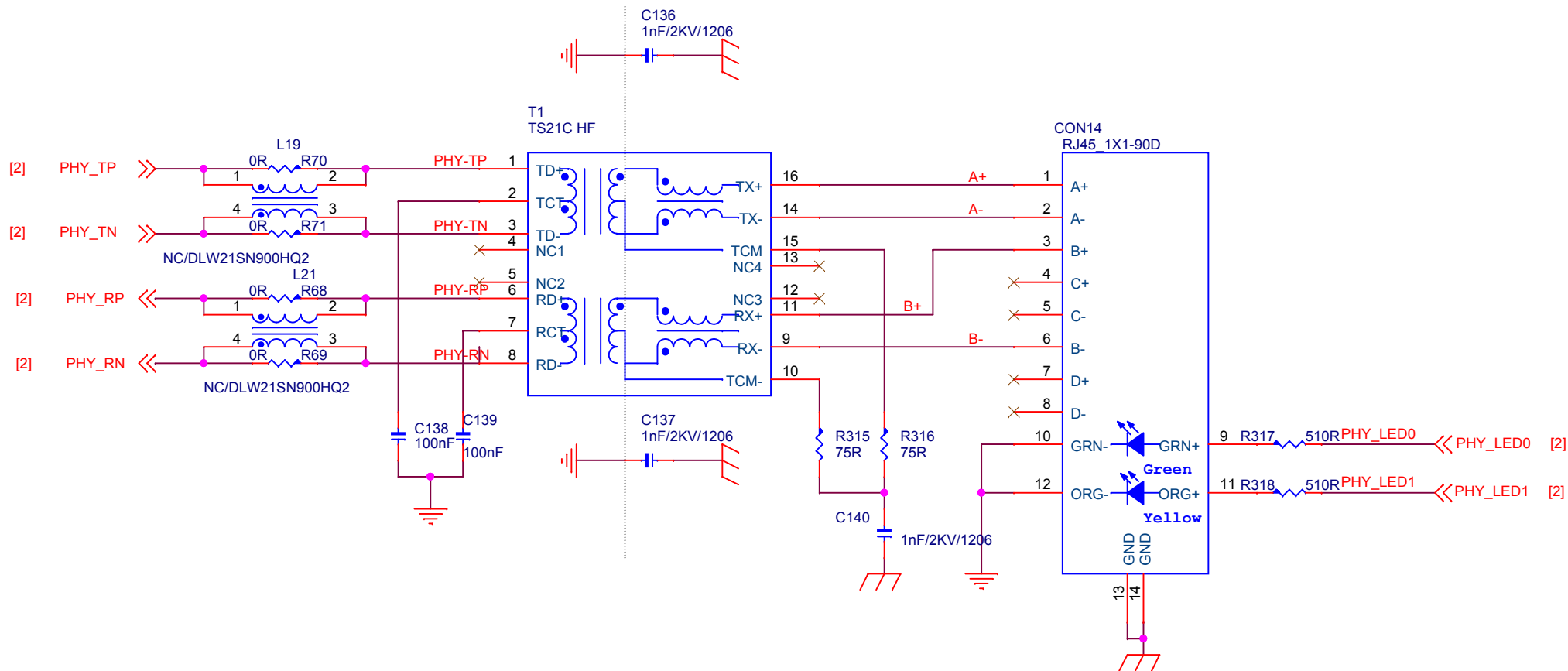
+1.5V DDR3 Power **$V_{out} = 0.6 \times (1 + R_1/R_2)$**

The circuit diagram shows the FP6373A (U3) configured as a voltage regulator. The input (VIN, pin 4) is connected to VCC5V through a 100K resistor (R14). The output (LX, pin 3) is connected to the +DDR_IO line through an inductor (L9, 2.2uH/3A). The feedback (FB, pin 6) is connected to ground through a resistor network consisting of R4 (R0402, 100K/1%) and R3 (TR3, 150K/1%). The enable (EN, pin 1) is connected to VCC5V. The ground (GND, pin 2) is connected to ground. The input is also filtered by capacitors TC13 (10uF, C0603) and TC14 (100uF, C0402). The output is filtered by capacitors TC11 (22uF/6.3V, C0805) and TC12 (100uF, C0402). The output voltage is labeled +DDR_IO.






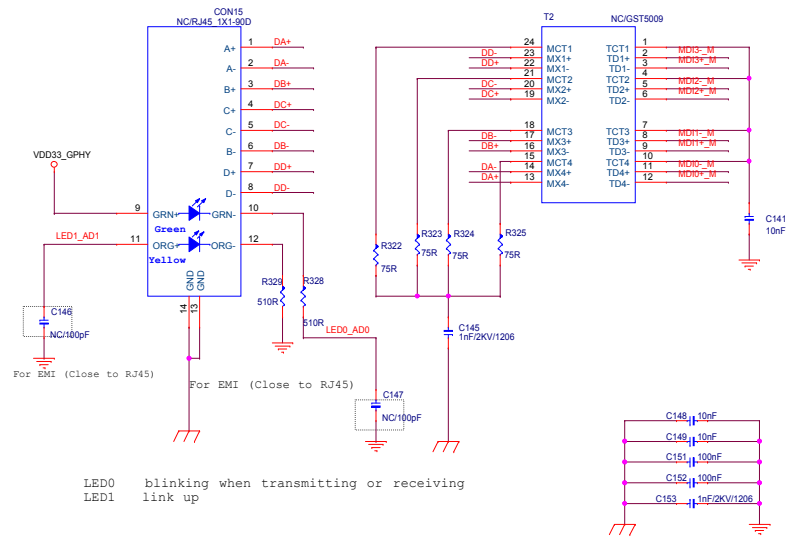
	ORG MStar Semiconductor(SZ),Inc.		
	Title MStar NVR Demo		
	Size B	Document Number	Rev 1.1
	03_Video/Audio Output-Input		
	Date: Tuesday, May 23, 2017 Sheet 3 of 11		



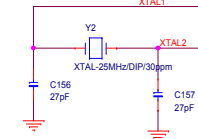
PAD_LED_PM[1] Active when linked in 100Base-TX and blinking when transmitting or receiving
 PAD_LED_PM[0] Active when linked.

	ORG MStar Semiconductor(SZ),Inc.		
	Title MStar NVR Demo		
	Size Custom	Document Number 04_EPHY	Rev 1.1
	Date: Tuesday, May 23, 2017	Sheet 4 of 11	

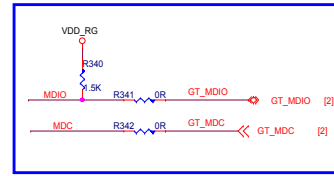
RJ45 & Transformer & CMC



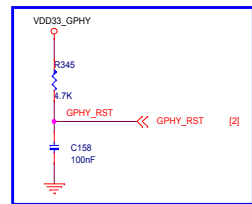
XTAL



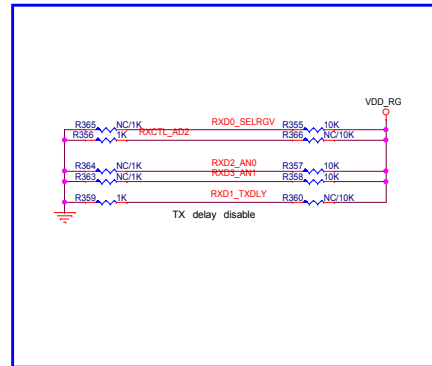
If use external clock then the XTAL2 need connect to GND for RTL8211E.



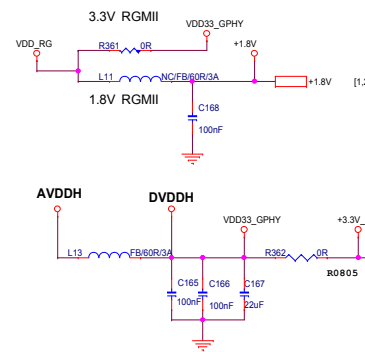
PHY Reset



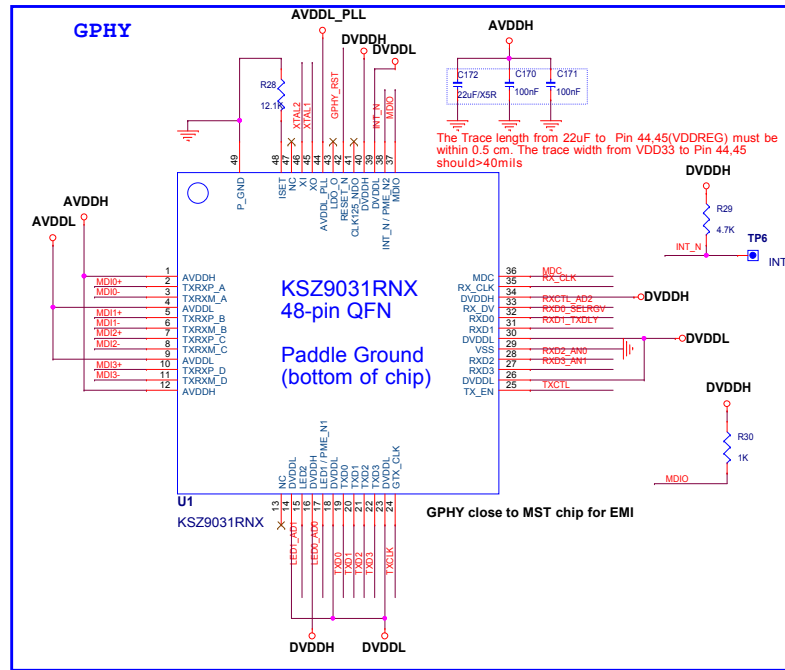
Configuration Setting



RGMII Power



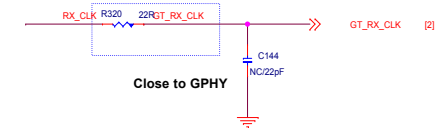
PHY



MDC/MDIO RGMII Rx (PHY to MAC)

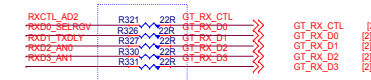
Equal length within 100mil for RX group

Close to GPY

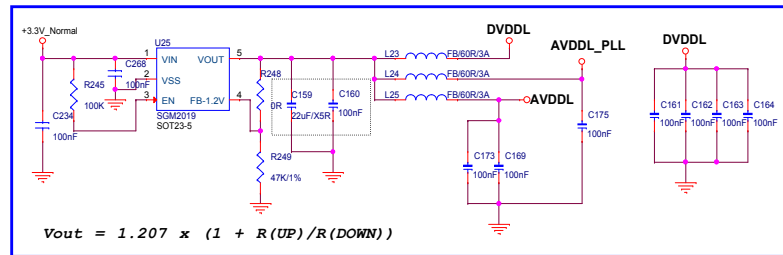


Close to SOC

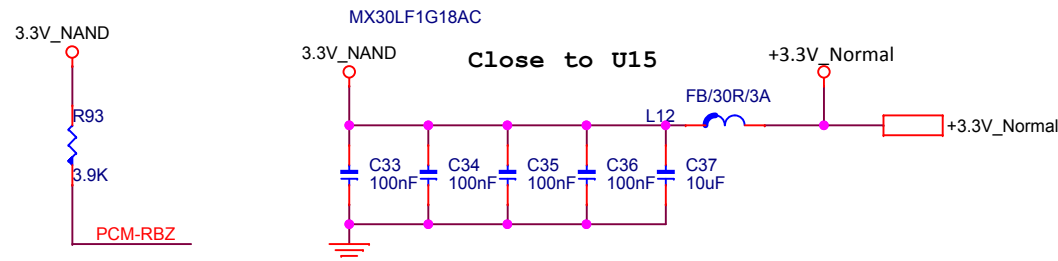
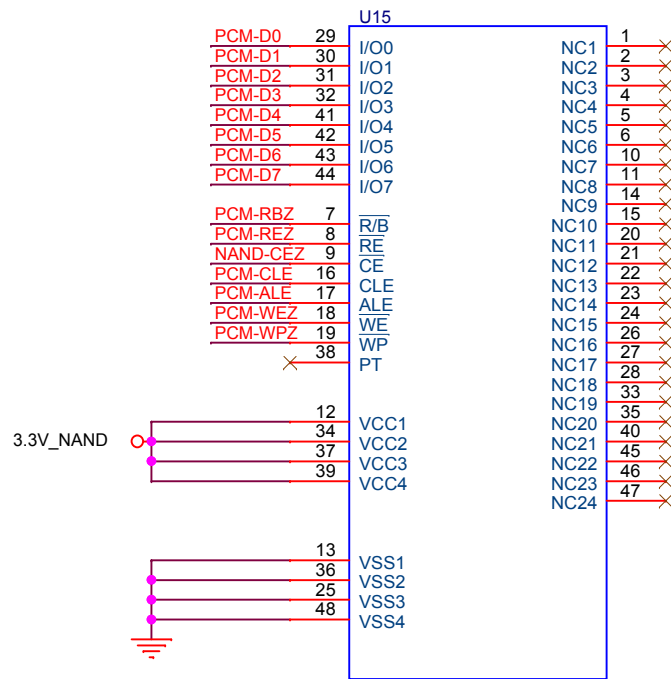
Equal length within 100mil for TX group



RGMII Tx (MAC to PHY)



Nand Flash



Main Chip To NAND Flash

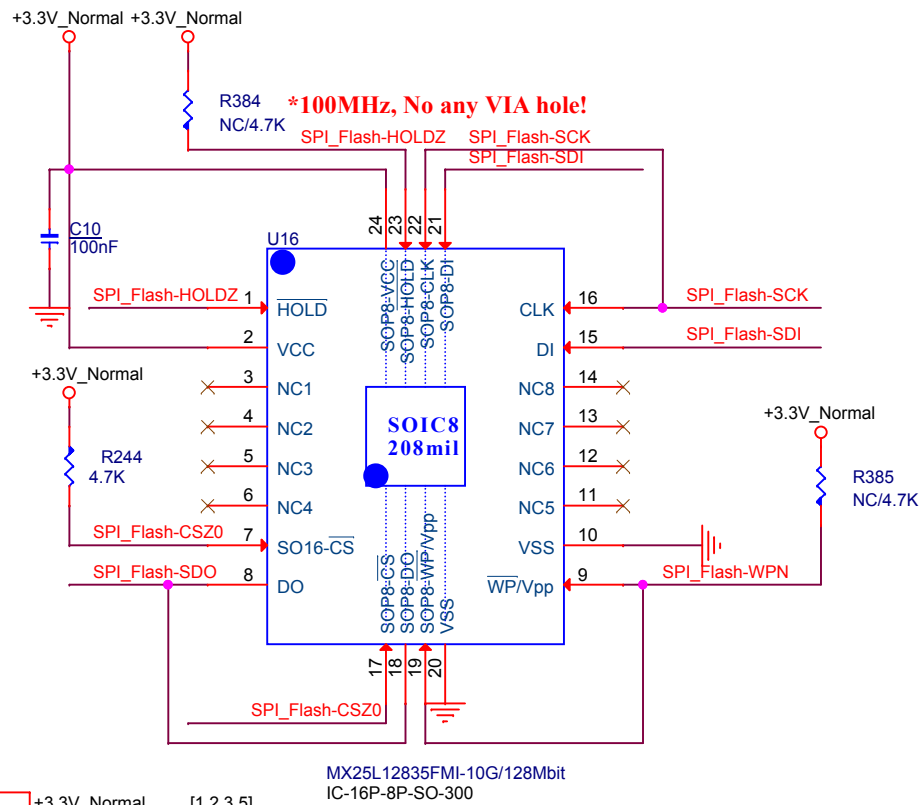
PCM-D7	R408	0R	PCM_D7
PCM-D6	R412	0R	PCM_D6
PCM-D5	R415	0R	PCM_D5
PCM-D4	R406	0R	PCM_D4
PCM-D3	R417	0R	PCM_D3
PCM-D2	R416	0R	PCM_D2
PCM-D1	R411	0R	PCM_D1
PCM-D0	R404	0R	PCM_D0

PCM-WEZ	R409	0R	PCM_WEZ
PCM-CLE	R414	0R	PCM_CLE
NAND-CEZ	R410	0R	NAND_CEZ
PCM-RBZ	R405	0R	PCM_RBZ
PCM-WPZ	R407	0R	PCM_WPZ
PCM-ALE	R403	0R	PCM_ALE
PCM-REZ	R413	0R	PCM_REZ

PCM_D0	<<	PCM_D0	[2]
PCM_D1	<<	PCM_D1	[2]
PCM_D2	<<	PCM_D2	[2]
PCM_D3	<<	PCM_D3	[2]
PCM_D4	<<	PCM_D4	[2]
PCM_D5	<<	PCM_D5	[2]
PCM_D6	<<	PCM_D6	[2]
PCM_D7	<<	PCM_D7	[2]

PCM_ALE	<<	PCM_ALE	[2]
PCM_REZ	<<	PCM_REZ	[2]
NAND_CEZ	<<	NAND_CEZ	[2]
PCM_RBZ	<<	PCM_RBZ	[2]
PCM_WPZ	<<	PCM_WPZ	[2]
PCM_CLE	<<	PCM_CLE	[2]
PCM_WEZ	<<	PCM_WEZ	[2]

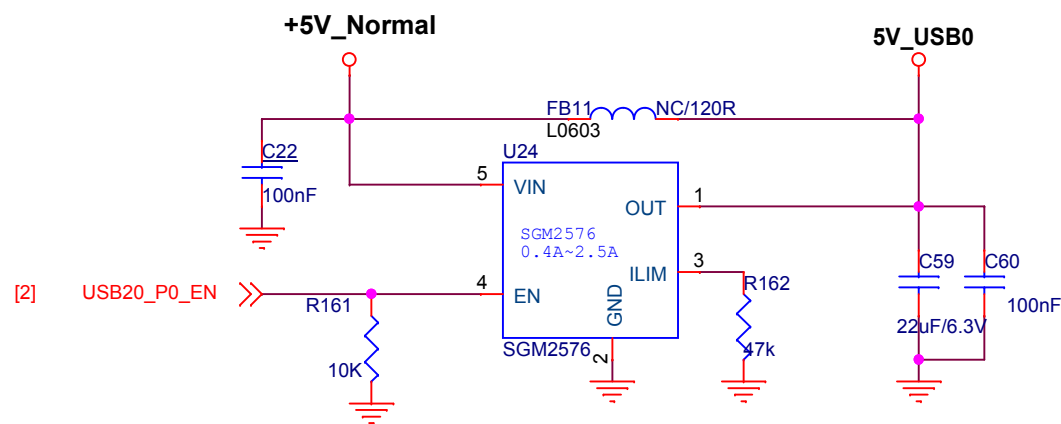
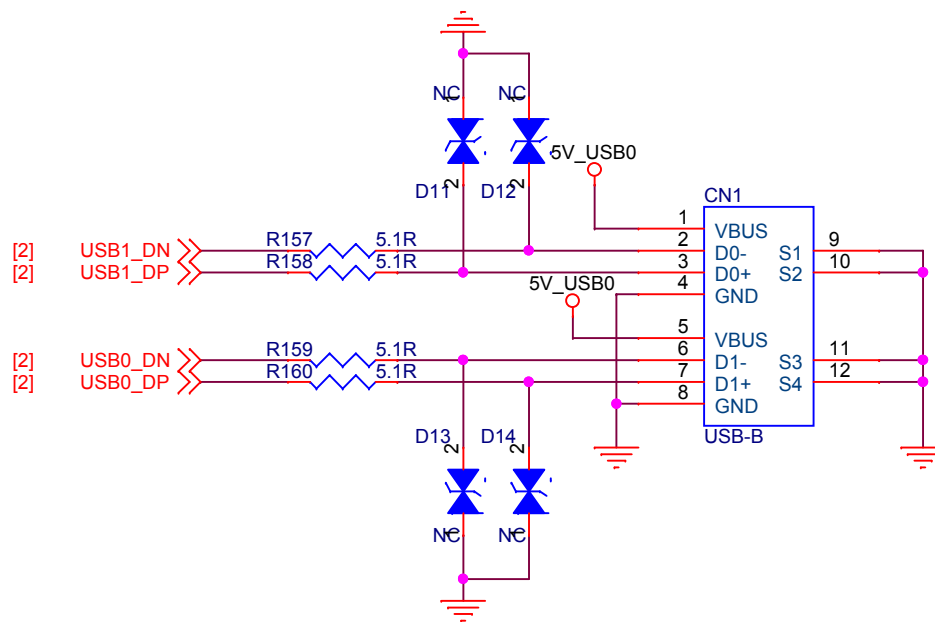
Serial Flash

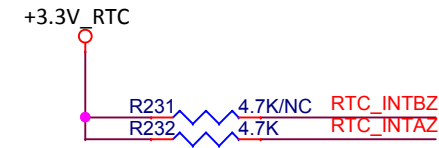
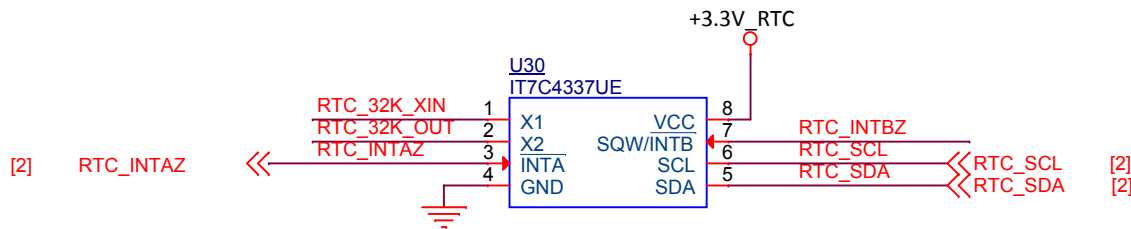
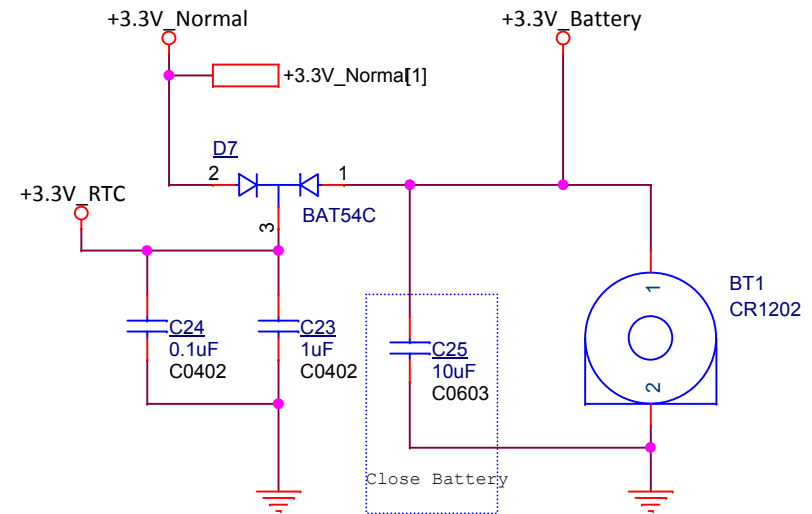
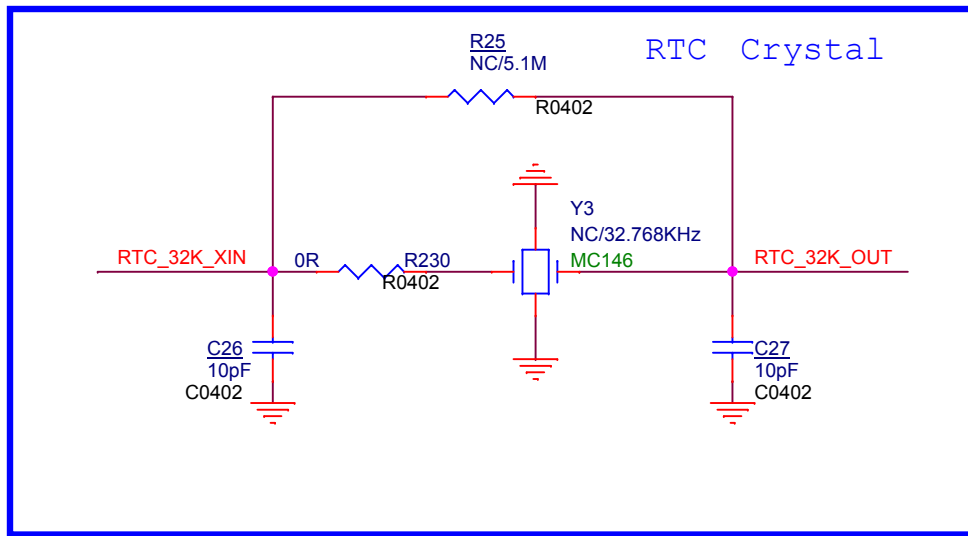


SPI_Flash-SCK	<<	SPI_Flash-SCK	[2]
SPI_Flash-CSZ0	<<	SPI_Flash-CSZ0	[2]
SPI_Flash-SDI	<<	SPI_Flash-SDI	[2]
SPI_Flash-SDO	<<	SPI_Flash-SDO	[2]
SPI_Flash-WPN	<<	SPI_Flash-WPN	[2]
SPI_Flash-HOLDZ	<<	SPI_Flash-HOLDZ	[2]

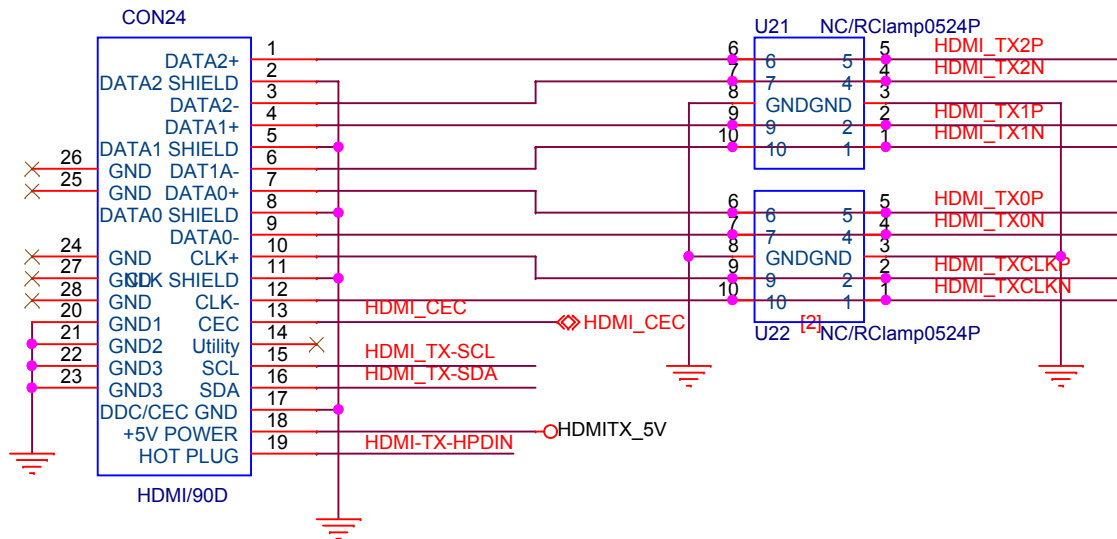
Co-layout

	ORG MStar Semiconductor(SZ),Inc.	
	Title MStar NVR Demo	
	Size Custom	Document Number 06_NorFlash_NandFlash
	Date: Tuesday, May 23, 2017	Rev 1.1

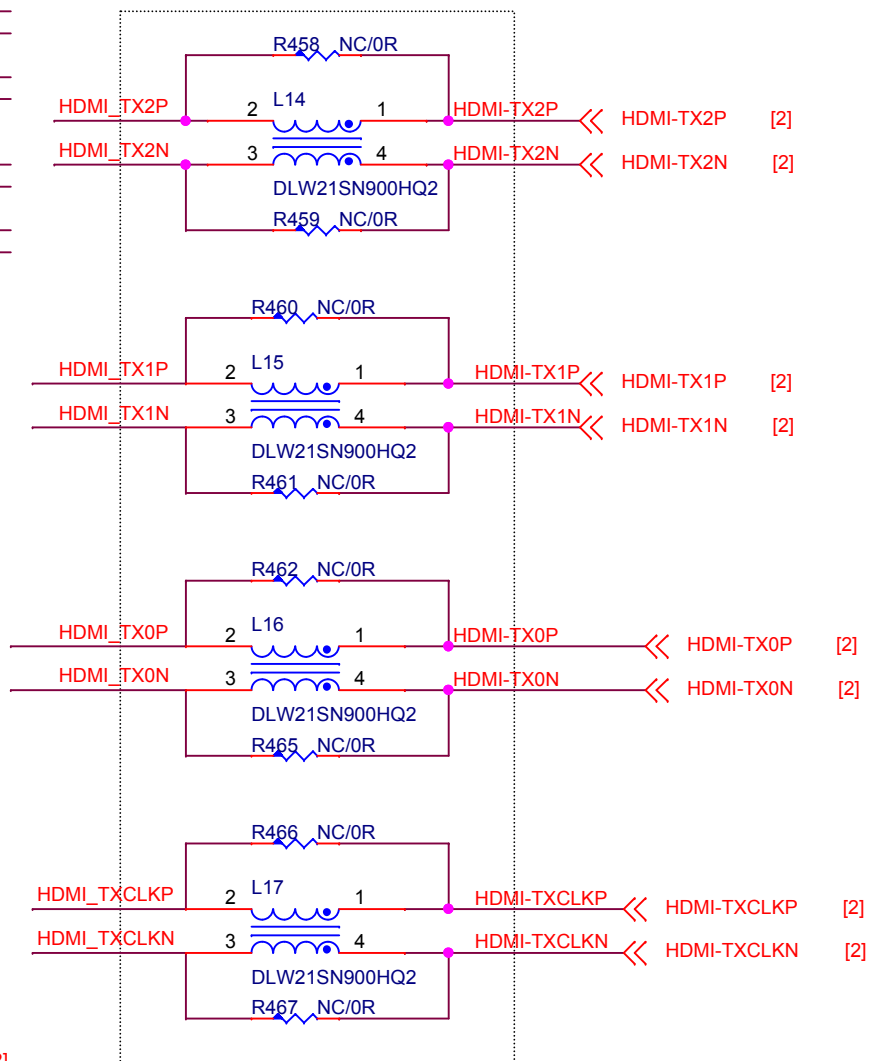




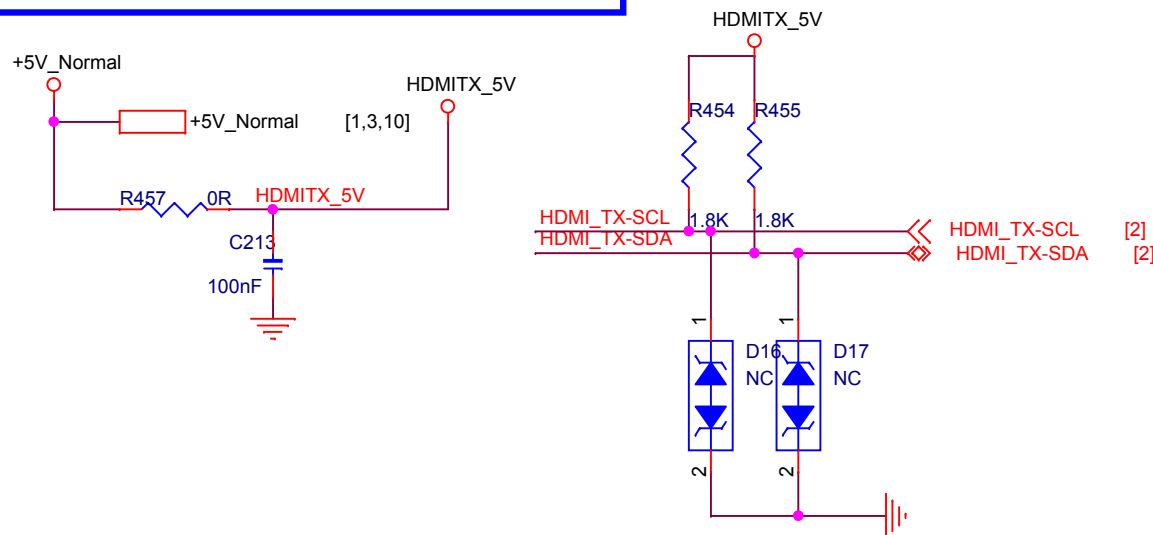
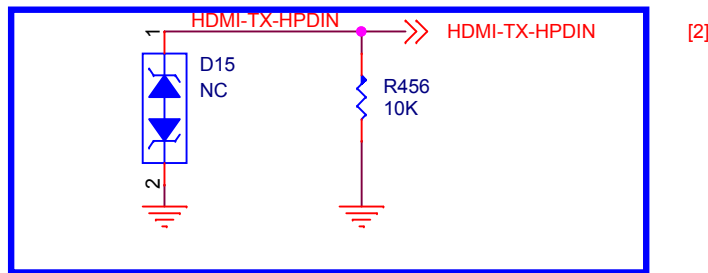
close to connector



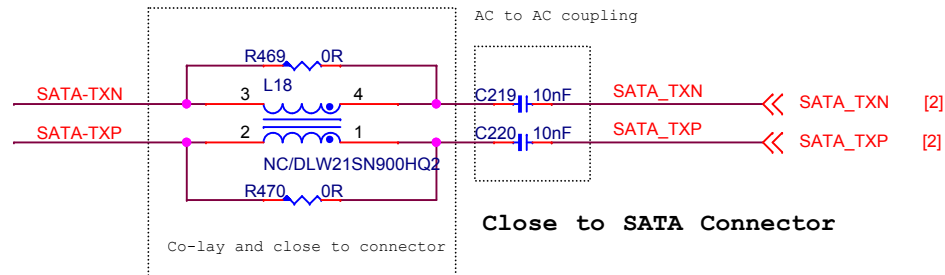
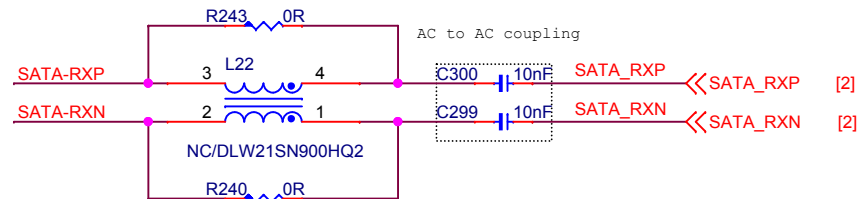
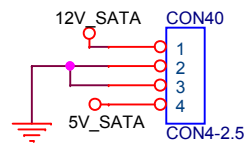
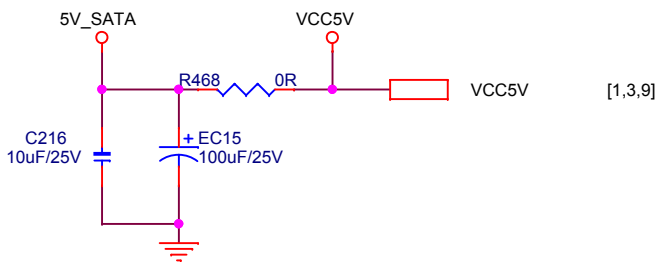
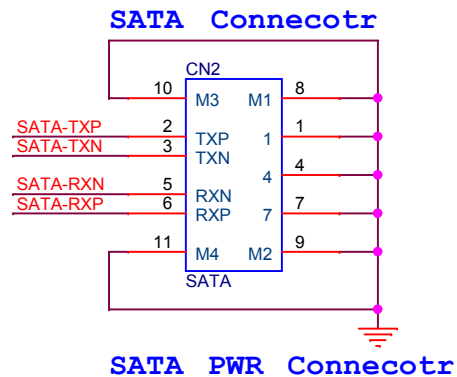
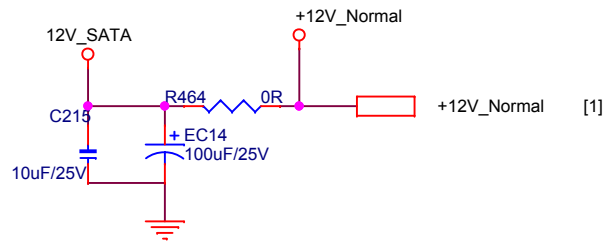
Co-lay and close to connector (For EMI)



HDMI TX Hot-Plug Control




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	Title MStar NVR Demo		
	Size A	Document Number 09_HDMI	Rev 1.1
	Date: Tuesday, May 23, 2017	Sheet 9 of 11	



SATA Differential trace. Impedance is 100ohm.

History

Version	Date	Description
V1.0	2016.06.14	First release
V1.1	2017.01.17	1.USB Power VCC5V -----> +5V_Normal 2.Add DDR MCP Power CAP C61 and C66 ---> 470nF Modify Pin Out and modify GPIO 119~148 net name 3.Add +1.1V_VDDC_CPU and +1.1V_VDDC by R620 connect

	ORG MStar Semiconductor(SZ),Inc.		
	Title MStar NVR Demo		
	Size Custom	Document Number 11_History	Rev 1.1
	Date: Tuesday, May 23, 2017 Sheet 11 of 11		