ECE 581 MICROPROCESSOR SYSTEM DESIGN

TEST PLAN - TEAM 11

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GROUP 11 – MSD PROJECT TEST CASES PLAN

Note: ACTIVATE and PRECHARGE commands would be required for all of the 16 test cases scenarios discussed below, since we are implementing Closed Page Policy with No Bank Parallelism.

Test Case Scenarios	Description	Bank group	Bank	Row	Column	Instruction	Time
1	Accesses to same row in the same bank group and bank different column sequential reads	1 1 1	0 0 0	122 122 122	122 221 210	Read Read Read	2 3 4
2	Accesses same row , bank group and but different banks	1 1 1	0 1 2	122 122 122	122 221 210	Read Read Write	2 3 4
3	Accesses to different row in the same bank and bank group	1 1 1	0 0 0	121 122 123	122 221 210	Read Read Write	2 3 4
4	Accesses to different bank group	0 1 2	0 0 0	122 122 122	122 221 210	Read Write Read	2 3 4
5	Accesses to the same column	1 1 1	0 0 0	122 122 122	111 111 111	Read Read Write	2 3 4
6	Accesses to the different row, bank and bank group	0 1 2	2 1 0	123 122 212	111 213 101	Read Read Read	2 3 4
7	Accesses to same row in the same bank group and bank with sequential writes	1 1 1	0 0 0	122 122 122	122 221 210	Write Write Write	2 3 4
8	Accesses to same row in the same bank group and bank with sequential reads	1 1 1	0 0 0	122 122 122	122 221 210	Read Read Read	2 3 4

Other Test Case Scenarios:

1)Check for the trace file giving an incorrect address and check the output whether it's showing error messages or not.

2)Check for the output file whether it’s showing the correct output or not. If not, then proper error messages are shown.

3) Validating the timing constraints for read instructions and ensuring that the timing constraints such as tRP, tRCD, tRAS, tCAS, etc. are as fulfilled as per the requirements. We will check all the timing given in the timing constraints and compare it with the required output.

4) Validating the timing constraints for write instructions and ensuring that the timing constraints such as tRP, tRCD, tRAS, tCAS, etc. are as expected as per the requirements. We will check all the timing given in the timing constraints and compare it with the required output.

5) Checking the CPU clock with a huge time difference: testing that whether there is a new CPU instruction after a very long gap. Suppose the first instruction is given at time #10 and the other is given at time #1000. We need to validate that the correct instruction is displaying or not after a very long-time gap for such an instruction.

6) Checking the CPU clock with multiple consecutive instructions: testing the functionality of the memory controller when there are instructions given on consecutive CPU cycles.

7) Out of Range Scenario: If value of cores or operations exceed beyond the predefined range. The controller should ideally drop any such requests which violate predefined boundary conditions and display an error message.

8) Queue Full: If the queue is filled to its maximum of 16 requests, it should stall the CPU i.e. other requests should not be pushed until popping of the previous instructions in the queue doesn’t take place. Here, we assume that the controller handles all the requests by simultaneously enqueueing and dequeueing requests.

9) Queue Empty: Controller should wait / idle from when the first set of instructions is done processing and until the next set of requests arrives from the CPU.