

Timing diagram showing the clock signal (CLK) and the outputs Q_1 , Q_2 , and Q_3 of a 3-bit shift register. The clock signal is a periodic square wave. The outputs Q_1 , Q_2 , and Q_3 are square waves that shift right by one clock cycle relative to each other. Q_1 has the highest frequency, Q_2 has the same frequency as Q_1 but is phase-shifted, and Q_3 has the same frequency as Q_2 but is phase-shifted again.