Beijing-Dublin International College

SEMESTER II FINAL EXAMINATION - 2016/2017

School of Computer Science

COMP2007J: Principles of Computer Organisation

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Time Allowed: 120 minutes

Instructions for Candidates

Candidates must answer any two questions worth 50 marks each. The candidate must clearly identify which two 50 mark questions are to be graded, otherwise the first two will be graded only. The distribution of marks (in brackets) shown as a percentage gives an approximate indication of the relative importance of each part of the question.

Answers are to be supplied in this exam paper in the boxes provided below each question. Candidates may use rough paper.

BJUT Student ID: _____ UCD Student ID: _____

I have read and clearly understand the Examination Rules of both Beijing University of Technology and University College Dublin. I am aware of the Punishment for Violating the Rules of Beijing University of Technology and/or University College Dublin. I hereby promise to abide by the relevant rules and regulations by not giving or receiving any help during the exam. If caught violating the rules, I accept the punishment thereof.

Honesty Pledge: _____ (Signature)

Instructions for Invigilators

Non-programmable calculators are permitted. This is a closed-book exam.
Rough paper is to be provided for candidates.

Score Obtained

Question 1:

Computer Function, Instruction Cycle and Interrupts

(a) List and briefly describe the four main functions of a computer. **(5 marks)**

(b) The processor instruction cycle is typically made up of the *fetch cycle* and the *execute cycle*. Briefly explain each of these. Include a diagram. **(10 marks)**

(c) What is an *interrupt*? List the four most common types of interrupts. **(5 marks)**

(d) The initial state of a von Neumann computer is shown in Table 1 (all data is shown as hexadecimal values). Available opcodes are shown in Table 2.

Address	Data
000	100F
001	200D
002	100E
003	200F
004	100D
005	200E
006	43D8
007	EA29
008	0F69
009	6CDD
00A	2BE5
00B	AF15
00C	2004
00D	0007
00E	71DC
00F	D0E0
...	

Table 1: The initial state of a von Neumann computer.

Opcode	Instruction
1	Load Accumulator (AC) from memory
2	Store AC to memory
3	Add to AC from memory
4	Jump to address (store address in Program Counter)

Table 2: Available opcodes

(i) Using the table below, show the state of the registers for 6 iterations of the instruction cycle.

(12 marks)

1	0	0	0		Program Counter (PC)
					Accumulator (AC)
					Instruction Register (IR)
2					Program Counter (PC)
					Accumulator (AC)
					Instruction Register (IR)
3					Program Counter (PC)
					Accumulator (AC)
					Instruction Register (IR)
4					Program Counter (PC)
					Accumulator (AC)
					Instruction Register (IR)
5					Program Counter (PC)
					Accumulator (AC)
					Instruction Register (IR)
6					Program Counter (PC)
					Accumulator (AC)
					Instruction Register (IR)

(ii) Show the state of memory at the end of the 6th iteration in the table below.

(3 marks)

Address	Data
000	
001	
002	
003	
004	
005	
006	
007	
008	
009	
00A	
00B	
00C	
00D	
00E	
00F	
...	

(iii) What is the purpose of this program? **(5 marks)**

(e) Consider a system that supports multiple interrupts based on priority. The priority of devices is as follows (higher numbers mean higher priority):

- Printer: 2
- Communications: 3
- Disk: 4
- Scanner: 5

A user program begins at time t=0. The following interrupts occur (we assume that each interrupt handler runs for 10 units of time. e.g. if a handler begins at t=10, it will finish at t=20).

- t=5 Communications
- t=10 Printer
- t=12 Scanner
- t=20 Disk

Draw a time sequence diagram to show how these interrupts are handled. The diagram must show the time that each interrupt begins and ends. **(10 marks)**

(Total 50 marks)

Score Obtained

Question 2:

Internal Memory

(a) Traditionally, main memory can be made from either Static RAM (SRAM) or Dynamic RAM (DRAM). Describe what is meant by "dynamic" RAM. Include a diagram. **(6 marks)**

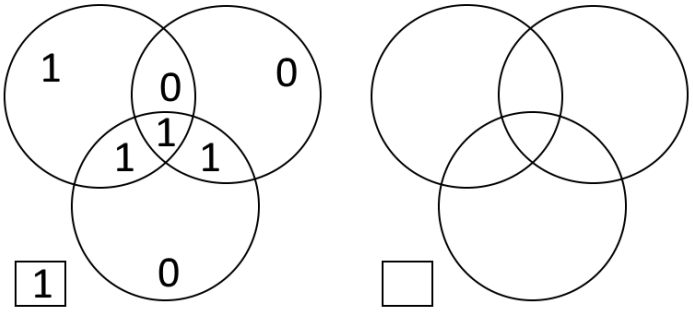
(b) Describe what is meant by "static" RAM. Include a diagram. **(6 marks)**

(c) Using the table below, compare Static RAM (SRAM) and Dynamic RAM (DRAM) in terms of speed, size, cost and what they are most commonly used for. **(8 marks)**

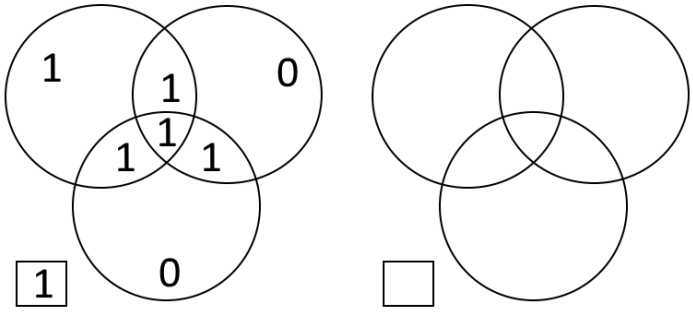
	DRAM	SRAM
Speed		
Size		
Cost		
Use		

(d) Briefly explain, using a diagram, why a *memory hierarchy* is often used in a computer. **(14 marks)**

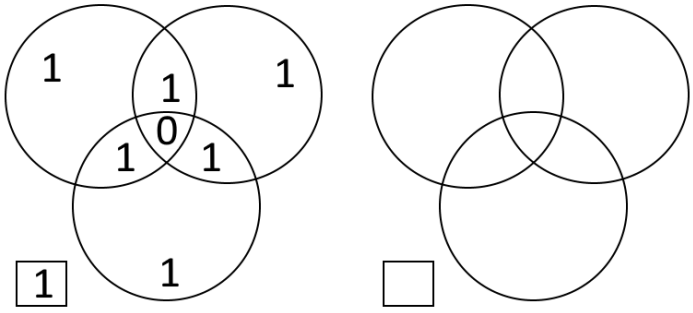
(e) Each of the following diagrams illustrates a Hamming SEC-DEC code. For each diagram, state how many errors are detected, and correct any errors if possible. Your answer should clearly state the number of errors and show the correction, if possible. If it is not possible to correct the error(s) you should write "correction not possible" underneath the diagram. **(16 marks)**



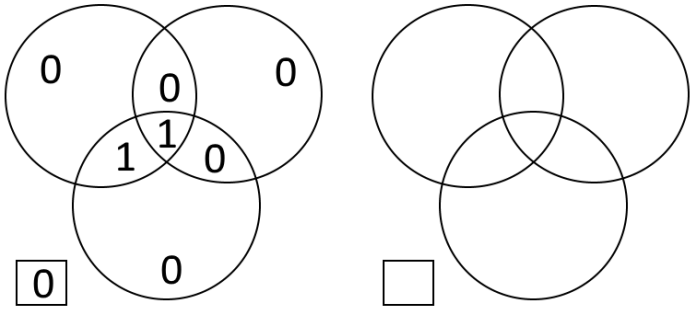
(a) Number of errors detected =



(b) Number of errors detected =



(c) Number of errors detected =



(d) Number of errors detected =

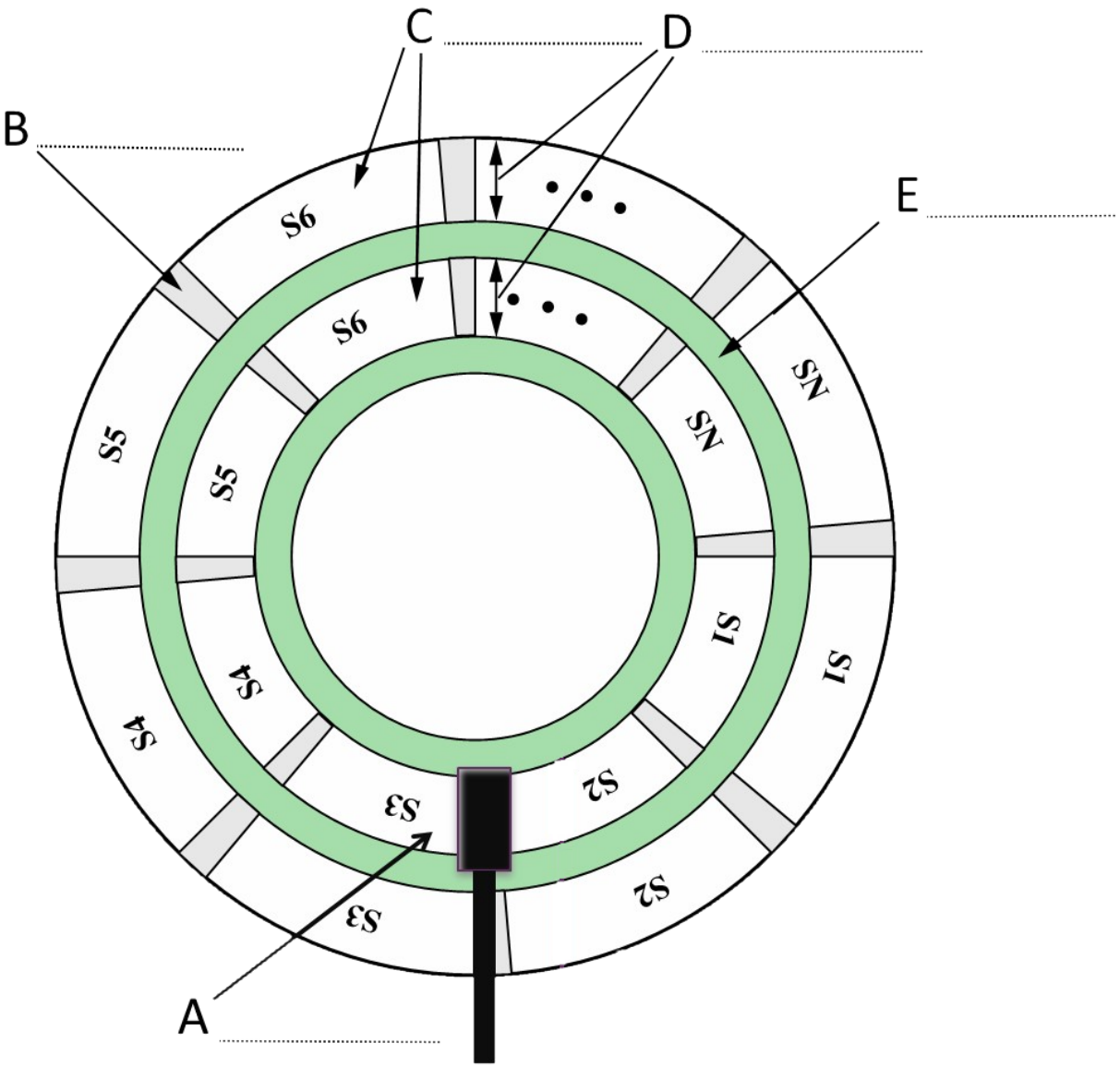
(Total 50 marks)

Score Obtained

Question 3:

External Memory

(a) Using the diagram below, show how a magnetic disk is typically divided so that data can be stored on it by identifying the parts labelled A – E. **(5 marks)**



(b) Using the table below briefly describe the seven RAID levels. State how many disks are required and list one advantage and one disadvantage of each of the RAID levels.
(25 marks)

Level	Description	Disks Required	Advantage	Disadvantage
0				
1				
2				

Level	Description	Disks Required	Advantage	Disadvantage
3				
4				
5				
6				

Input/Output

(c) List each of the 5 major functions of I/O modules. **(5 marks)**

(d) Describe *programmed*, *interrupt-driven* and *direct memory access* Input/Output (I/O). **(15 marks)**

Programmed I/O:

Interrupt-driven I/O:

Direct memory access (DMA):

(Total 50 marks)

oOo