Semester One of Academic Year (2014---2015) of BJUT

《 Principles of Computer Organisation (COMP2007J)》

Exam Paper A

Exam Instructions： Answer any TWO questions

Honesty Pledge：

I have read and clearly understand the Examination Rules of Beijing University of Technology and am aware of the Punishment for Violating the Rules of Beijing University of Technology. I hereby promise to abide by the relevant rules and regulations by not giving or receiving any help during the exam. If caught violating the rules, I would accept the punishment thereof.

Pledger： ___________ **Class No：** ___________

BJUT Student ID： ___________ **UCD Student ID**___________

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Notes：

The exam paper has 3 parts on 6 pages, with a full score of 100 points. You are required to use the given Examination Book only.

Total Score of the Exam Paper（For teachers' use only）

Item	Q1	Q2	Q3		**Total Score**
Full Score	50	50	50		
Obtained Score					

Obtained score

Question 1:

(a) A computer is made up of four basic types of component. Name and describe each one.

(8 marks)

(b) The processor instruction cycle is typically made up the *fetch cycle* and the *execute cycle*. Briefly explain each of these.

(4 marks)

(c) Consider a system that supports multiple interrupts based on priority. The priority of devices is as follows (higher numbers mean higher priority):

- Printer: 2
- Communications: 3
- Disk: 4
- Scanner: 5

A user program begins at time t=0. The following interrupts occur (we assume that each interrupt hander runs for 10 units of time. e.g. if a handler begins at t=10, it will finish at t=20).

- t=5 Communications
- t=10 Printer
- t=12 Scanner
- t=20 Disk

Draw a time sequence diagram to show how these interrupts are handled. Indicate the start and end time for each interrupt handler.

(12 marks)

(d) The initial state of a van Neumann computer is shown on the next page (all data is shown as hexadecimal values).

Available opcodes are:
0: Jump to address (store address in Program Counter)
1: Load Accumulator (AC) from memory
2: Add to AC from memory
3: Store AC to memory

Show the state of the registers for 8 iterations of the instruction cycle. Also, show the state of memory at the end of the 8th iteration.

(12 marks)

What is the purpose of this program?

(4 marks)

Address	**Data**
000	000A
001	AEF2
002	2001
003	1000
004	0012
005	3102
006	E041
007	2005
008	000F
009	A6E3
00A	1002
00B	2003
00C	2004
00D	0007
00E	71DC
00F	3001
…	

0	0	0	Program Counter (PC)
			Accumulator (AC)
			Instruction Register (IR)

(e) Explain in detail how the timing of bus operations is coordinated when using *synchronous* timing.

(10 marks)

(Total 50 marks)

Obtained score

Question 2:

(a) Consider a computer system with the following details about its memory cache.

- Memory address: 5 bits
- Block size = 4
- Cache lines = 2

The initial contents of memory are shown below.

The following memory addresses are requested by the CPU:

- 11111
- 10001
- 11000
- 11001
- 00000
- 11010
- 00000
- 01110

Assuming the system is using a *direct mapping cache* strategy, state whether each request is a cache hit or a cache miss, and show the state of the cache after *each* request.

Data	Address	Data	Address
2C	00000	17	10000
18	00001	56	10001
22	00010	18	10010
7A	00011	3E	10011
10	00100	05	10100
3F	00101	4A	10101
24	00110	40	10110
3C	00111	78	10111
44	01000	6D	11000
2E	01001	52	11001
52	01010	76	11010
10	01011	4E	11011
14	01100	56	11100
14	01101	05	11101
4D	01110	69	11110
3A	01111	39	11111

(16 marks)

(b) Traditionally, main memory can be made from either *Static RAM (SRAM)* or *Dynamic RAM (DRAM)*. Describe what is meant by "static" and "dynamic", and compare the two types of RAM in terms of size, cost and what they are most commonly used for.

(10 marks)

(c) Consider a computer system that uses a Single Error Correcting (SEC) Hamming code for error correction.

i. With the aid of a diagram, explain in detail how error correcting codes can be used to correct data read from internal memory.

(10 marks)

ii. When reading from internal memory, the following values are read:

Data: `10100110`

Error Correcting code: `1110`

Show what the original data and error correcting code were, before they were stored in memory.

(8 marks)

(d) Describe the difference between Physical cache and Logical cache. Give reference to the placement of the cache and the Memory Management Unit (MMU).

(6 marks)

(Total 50 marks)

Obtained score

Question 3:

(a) With the aid of a diagram, explain how a magnetic disk is typically divided so that data can be stored on it.

(8 marks)

(b) In RAID what is meant by the term Mean Time To Repair (MTTR). What effect will this have on the RAID level used.

(6 marks)

(c) What is the difference between RAID 4 and RAID 5. Which RAID level has a higher write performance. Why?

(10 marks)

(d) List and describe each of the 5 major functions of I/O modules.

(10 marks)

(e) Describe the flow of operations that occurs when accessing an I/O module using Interrupt driven I/O. Why does this provide an advantage over programmed I/O? Discuss a method for hardware polling for interrupt driven I/O.

(16 marks)

(Total 50 marks)