

**Semester Two of Academic Year (2015---2016) of BDIC**

**《 Computer Organization 》**

**Module Code: Comp2007J**

**Exam Paper A**

**Exam Instructions: Answer any TWO Questions**

**Honesty Pledge:**

I have read and clearly understand the Examination Rules of Beijing University of Technology and University College Dublin and am aware of the Punishment for Violating the Rules of Beijing University of Technology and University College Dublin. I hereby promise to abide by the relevant rules and regulations by not giving or receiving any help during the exam. If caught violating the rules, I would accept the punishment thereof.

**Pledger:** \_\_\_\_\_

**Class No:** \_\_\_\_\_

**BJUT Student ID:** \_\_\_\_\_

**UCD Student ID** \_\_\_\_\_

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**Notes:**

The exam paper has 3 parts on 8 pages, with a full score of 100 points. Complete any two parts. You are required to use the given Examination Book only.

**Total score of exam paper (for teacher use only)**

Item	Part 1	Part 2	Part 3	Total Score
Full Score	50	50	50	
Obtained Score				

Obtained score
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**Question 1:**

- a. The initial state of a Von Neumann computer is shown below:

Memory (Instruction)	
Address	Data
000	1100
001	3101
002	3102
003	2103
004	4103
005	5104
006	0000
Memory (Operands)	
Address	Data
100	3213
101	1232
102	3241
103	
104	

CPU Registers

0	0	0		Program Counter (PC)
				Accumulator (AC)
				Instruction Register (IR)

The available opcodes are given below:

Opcode	Description
1	Load AC from specified memory address
2	Store PC in specified memory address
3	Add to AC from specified memory address
4	Divide AC by specified memory address
5	Store AC in specified memory address

Note that for opcode 2, the PC is stored in the specified memory address. The PC is prefixed by a 0. For instance, instruction 2100 stores the current PC (a three digit number) in address 100. If the PC was 435, and instruction 2100 was executed, 0435 would be stored in memory address 100.

- i. Show the state of the registers for the first six iterations of this program. Your answer book should have six of the following tables, each correctly completed and numbered 1-6:

CPU Registers				
				Program Counter (PC)
				Accumulator (AC)
				Instruction Register (IR)

**(18 marks)**

- ii. Show the final state (after six iterations) of the operand memory addresses by copying and filling out the following table once:

Memory (Operands)	
Address	Data
100	
101	
102	
103	
104	

**(6 marks)**

- iii. What does this program do?

**(2 marks)**

- iv. If the input (memory address 100) was 3212 instead of 3213 at the beginning of the program, a problem would occur before the program stops. What is this problem?

**(4 marks)**

- b. The processor instruction cycle is normally broken down into two phases called the fetch cycle and the execute cycle. Describe each of these.

**(8 marks)**

- c. Consider a system that supports multiple nested interrupts based on priority. The priority of the devices is as follows (higher numbers mean higher priority):

- Printer: 1
- Disk: 2
- Communications: 3

A user program begins at  $t = 0$ . The following interrupts occur (we can assume that each interrupt handler runs for 10 units of time - e.g. if a handler begins at  $t=10$  it will finish at  $t=20$ , provided it itself is not interrupted):

- $t = 10$  Printer
- $t = 15$  Communications
- $t = 20$  Disk

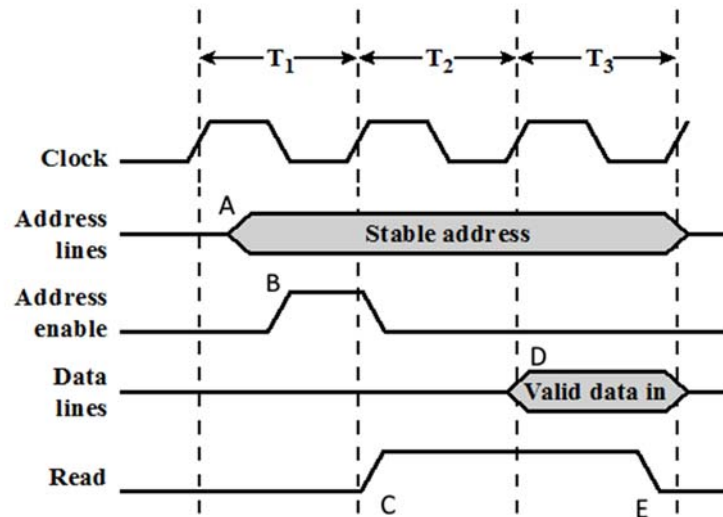
Draw a single time sequence diagram to show how these interrupts are handled.

**(12 marks)**

Obtained score

**Question 2:**

- a. The diagram below shows a read operation being performed on a synchronous bus. Describe events A, B, C, D and E.

**(15 marks)**

- b. Explain the key differences between multiplexed and dedicated bus types.

**(9 marks)**

- c. What bus factor determines the maximum memory capacity of a computer system?

**(5 marks)**

- d. What is a key bus factor in determining overall system performance?

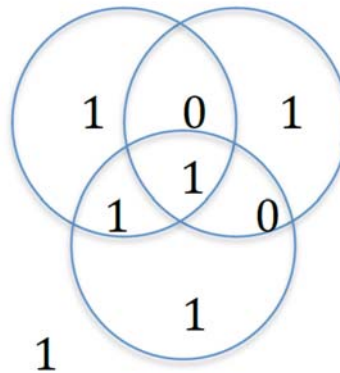
**(5 marks)**

- e. Each of the following diagrams illustrates a Hamming SEC-DEC code. For each diagram, state how many errors are detected, and correct any errors if possible. If it is not possible, state so.

Your answer should clearly state the number of errors and the correction, if possible. If the correction is not possible. Say 'correction not possible'

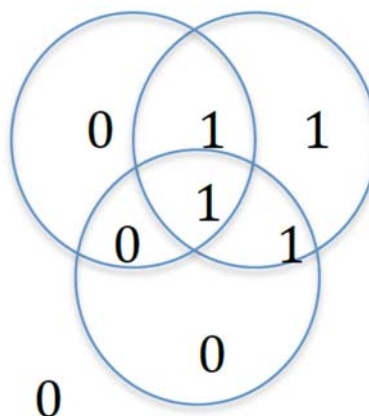
- It is recommended that you write "Number of detected errors = \_\_\_\_" for each answer.
- It is recommended that to show a correction, you copy the diagram, correct it, and label it "corrected diagram".
- If it is not possible to correct the error(s) it is recommended you write "correction not possible".

i.



(8 marks)

ii.



(8 marks)

Obtained score

**Question 3:**

- a. Below shows a snapshot of internal memory in a system with 4-bit memory addresses, a block size of 2, and 2 cache lines. The system uses Associative Mapping with a Least Recently Used (LRU) replacement algorithm.

Block Number		Memory Addresses
000	{	DE 0000
		16 0001
001	{	02 0010
		A5 0011
010	{	DA 0100
		1F 0101
011	{	7E 0110
		35 0111
100	{	F4 1000
		DE 1001
101	{	88 1010
		73 1011
110	{	A8 1100
		75 1101
111	{	B9 1110
		27 1111

Show the state of the cache after each of the following operations, using the following format each time. (Your answer book should have six of the following tables, one for each operation.)

Cache			
Line	Tag	Word 0	Word 1
0			
1			

- i. Read address 0111

**(3 marks)**

- ii. Read address 0011

**(3 marks)**

- iii. Read address 0110

**(3 marks)**

iv. Read address 0000

(3 marks)

v. Read address 1111

(3 marks)

vi. Read address 1110

(3 marks)

b. Traditionally, main memory can be static RAM (SRAM) or dynamic RAM (DRAM).

Describe what is meant by *static* and *dynamic*, and compare the two types of RAM in terms of size, cost, and what they are most commonly used for.

(10 marks)

c. Copy the table below into your answer book and complete it. Each row should have **one** 'x', indicating which attribute applies more accurately to which technology. The first one has been completed for you, indicating that SSDs are more durable than magnetic disks (HDDs).

Attribute	SSD	HDD
More durable	<b>X</b>	
Greater lifespan		
Lower operating power		
Lower cost (per GB)		
Higher Throughput (MB/s)		
Lower access time		
Lower latency		
Lower random access time		
Higher Input/Output operations per second		
Quieter		
Cooler		
Fewer moving parts		

(12 marks)

d. There are two issues unique to SSDs that are not faced by HDDs. Explain them in detail.

(6 marks)

e. Describe two techniques for prolonging the life of SSDs.

(4 marks)