# 2019 HW3

1. A

| | ROB | Issue | WB | Commit | OP | Dest | Src1 | Src2 |
|---|---|---|---|---|---|---|---|---|
| $I_1$ | -1 | 0 | 3 | 4 | FMUL.D | r0 | f0 | f1 |
| $I_2$ | 0 | 4 | 9 | 10 | FADD.D | r1 | f2 | r0 |

B

| | ROB | Issue | WB | Commit | OP | Dest | Src1 | Src2 |
|---|---|---|---|---|---|---|---|---|
| $I_1$ | -1 | 0 | 3 | 4 | FMUL.D | r0 | f0 | f1 |
| $I_2$ | 0 | 4 | 9 | 10 | FADD.D | r1 | f2 | r0 |
| $I_3$ | 5 | 10 | 15 | 16 | FADD.D | r0 | r1 | f0 |

C

| | ROB | Issue | WB | Commit | OP | Dest | Src1 | Src2 |
|---|---|---|---|---|---|---|---|---|
| $I_1$ | -1 | 0 | 2 | 3 | FLD | r0 | x1 | |
| $I_2$ | 0 | 1 | 3 | 4 | FLD | r1 | x1 | |
| $I_3$ | 1 | 4 | 7 | 8 | FMUL.D | r2 | r0 | r1 |
| $I_4$ | 2 | 8 | 13 | 14 | FADD.D | r3 | f2 | r2 |
| $I_5$ | 4 | 5 | 8 | 15 | FLD | r0 | x1 | |
| $I_6$ | 5 | 14 | 19 | 20 | FADD.D | r1 | r3 | r0 |

2. A   32 GB = $2^{35}$ bit    2048-byte= $2^{14}$ bit    64 bits = $2^6$ bit    A single page may include $2^{14}/2^6 = 2^8$ table entry

First level: $2^{35}/2^{14} = 2^{24}$ pages    Second level: $2^{24}/2^8 = 2^{16}$ pages    fitting in a single page in third level

So we need 3 levels of pages

B   Aliasing: Several virtual addresses are mapped to the same physical address.

Thus, several different entries pointing to same physical data may exist simultaneously in cache

As va[k-1:0]= pa[k-1:0] is ensured, we should have $L+b \leq k$

Otherwise, va[L+b-1:k]= pa[L+b-1:k] should be additionally ensured by hardware.

C   $256 \times 64 \div 2048 = 4$    So at least 4-way SA is needed.

3. A

| Inst | Counter | Pred | Actual |
|---|---|---|---|
| blt | 01 | not taken | taken |
| bge | 01 | not taken | not taken |
| bnez | 01 | not taken | taken |
| blt | 10 | taken | not taken |
| bge | 00 | not taken | taken |
| bnez | 10 | taken | taken |
| blt | 01 | not taken | taken |
| bge | 01 | not taken | not taken |
| bnez | 11 | taken | taken |
| blt | 10 | taken | not taken |
| bge | 00 | not taken | taken |
| bnez | 11 | taken | not taken |

| Branch | Accuracy |
|---|---|
| blt | 0 |
| bge | 1/2 |
| bnez | 1/2 |
| overall | 1/3 |

**B**

| Inst | Global | Counter0 | Counter1 | Prediction | Actual |
|------|--------|----------|----------|------------|--------|
| blt | 0 | 01 | 01 | not taken | taken |
| bge | 1 | 01 | 01 | not taken | not taken |
| bnez | 0 | 01 | 01 | not taken | taken |
| blt | 1 | 10 | 01 | not taken | not taken |
| bge | 0 | 01 | 00 | not taken | taken |
| bnez | 1 | 10 | 01 | not taken | taken |
| blt | 1 | 10 | 00 | not taken | taken |
| bge | 1 | 10 | 00 | not taken | not taken |
| bnez | 0 | 10 | 10 | taken | taken |
| blt | 1 | 10 | 01 | not taken | not taken |
| bge | 0 | 10 | 00 | taken | taken |
| bnez | 0 | 11 | 10 | taken | not taken |

| Branch | Accuracy |
|--------|----------|
| blt | 1/2 |
| bge | 3/4 |
| bnez | 1/4 |
| overall | 1/2 |

**C**  b<4 is strongly associated with last branch b>=5 , so bge benefits most.

**D**  The number of entries in BTB is limited. BHT may help predict if pc misses in BTB.