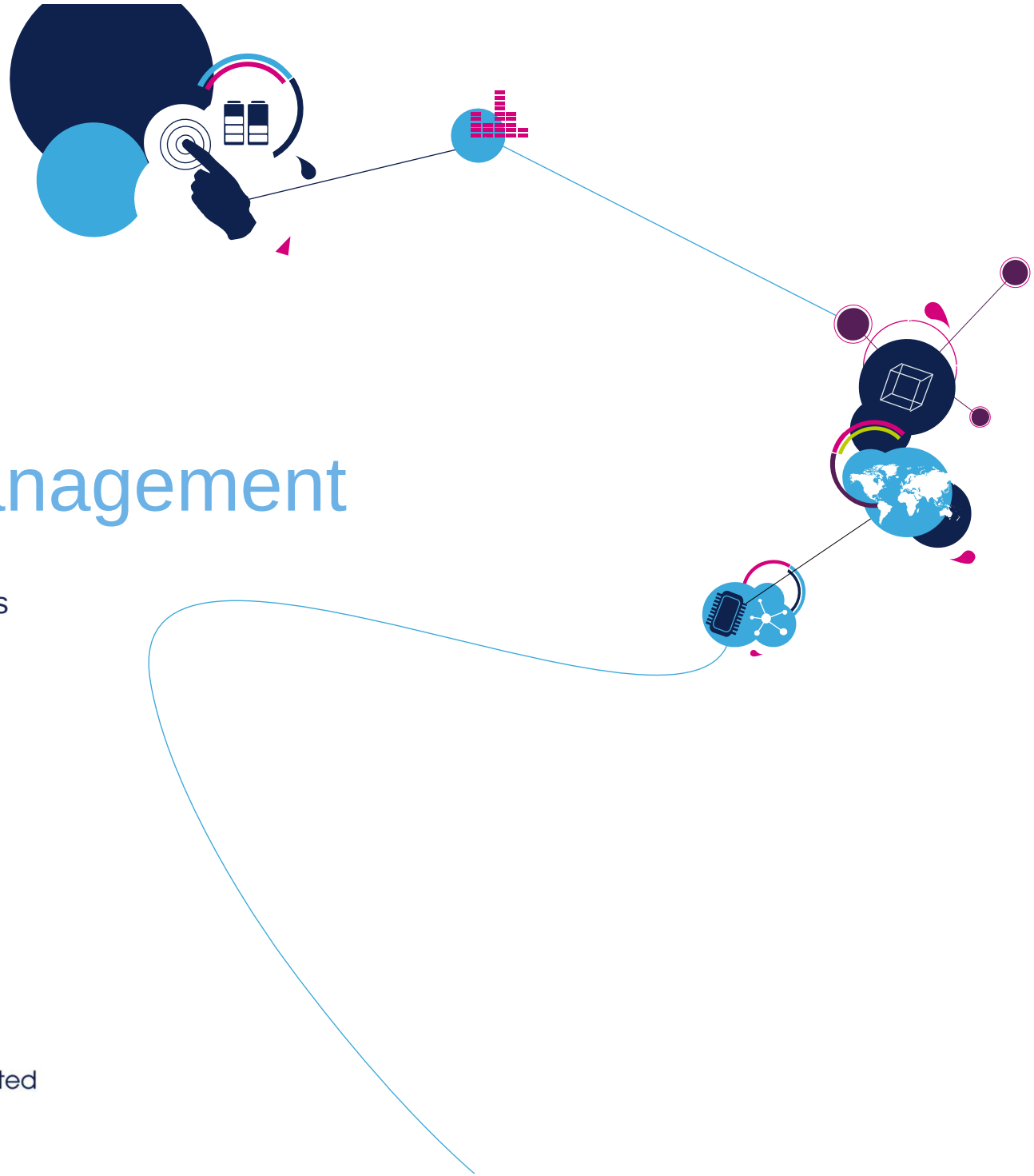

Power management

MCU Division Applications

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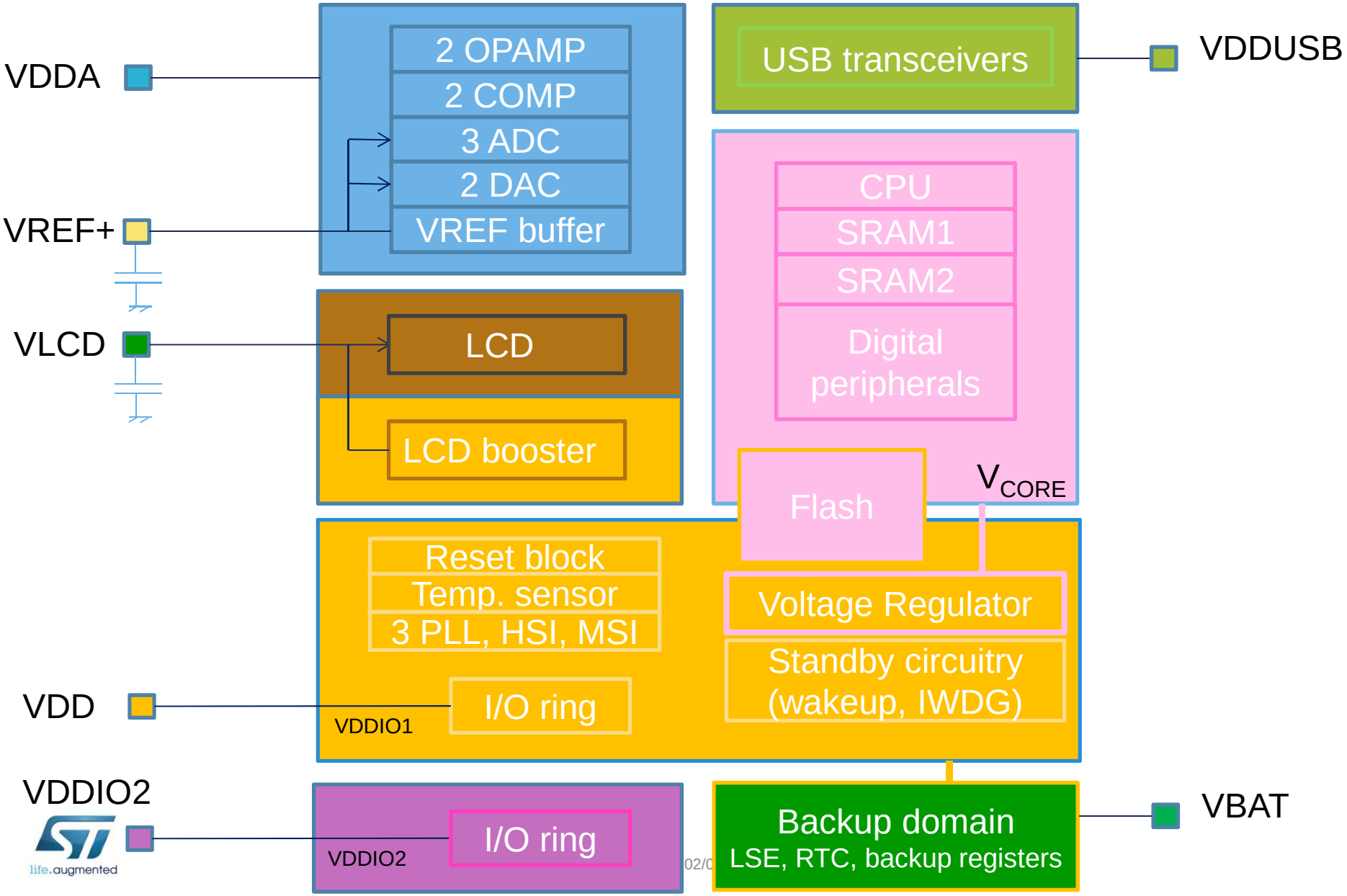
Power schemes (1/3)



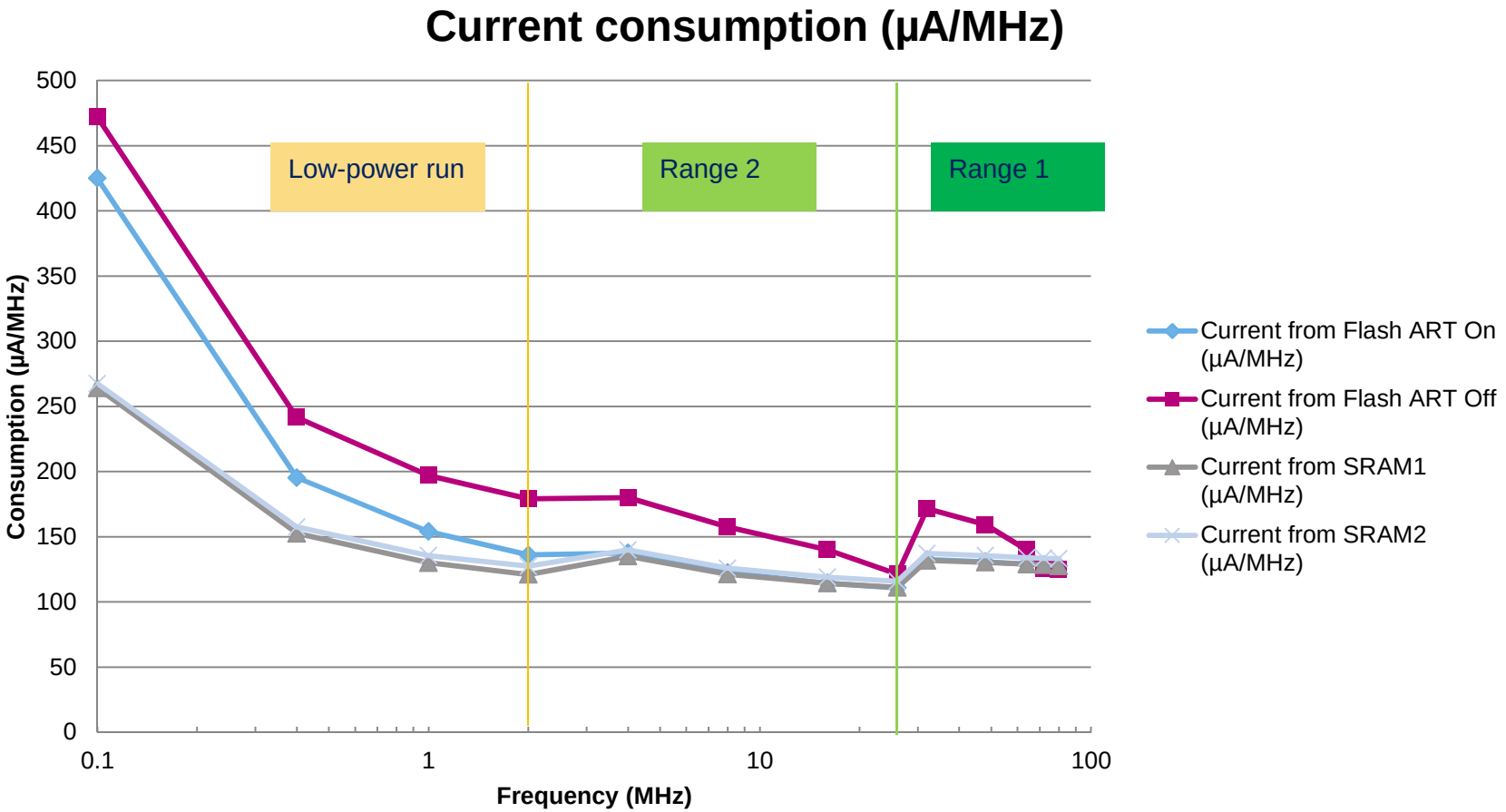
Voltage Regulator

- Two embedded linear voltage regulator supply all the digital circuitries except for the Standby circuitry and the Backup domain. The regulator output voltage (V_{CORE}) can be programmed by software to two different ranges within 1.0 - 1.2 V (typical). This method is called Dynamic Voltage Scaling.
  - Regulator Voltage Range 1: V_{CORE} = 1.2V
  - Regulator Voltage Range 2: V_{CORE} = 1.0V

- Depending on the application mode, the V_{CORE} is provided either by main regulator (MR) or by the low-power regulator (LPR)
  - Main voltage regulator mode (MVR) for Run and Sleep modes.
  - Low-power regulator for LP run, LP sleep, Stop 1 and Stop 2 modes.
  - Regulators OFF in Standby and Shutdown mode.
    - When SRAM2 content is preserved in Shutdown mode, the LPR remains ON and provides SRAM2 supply/

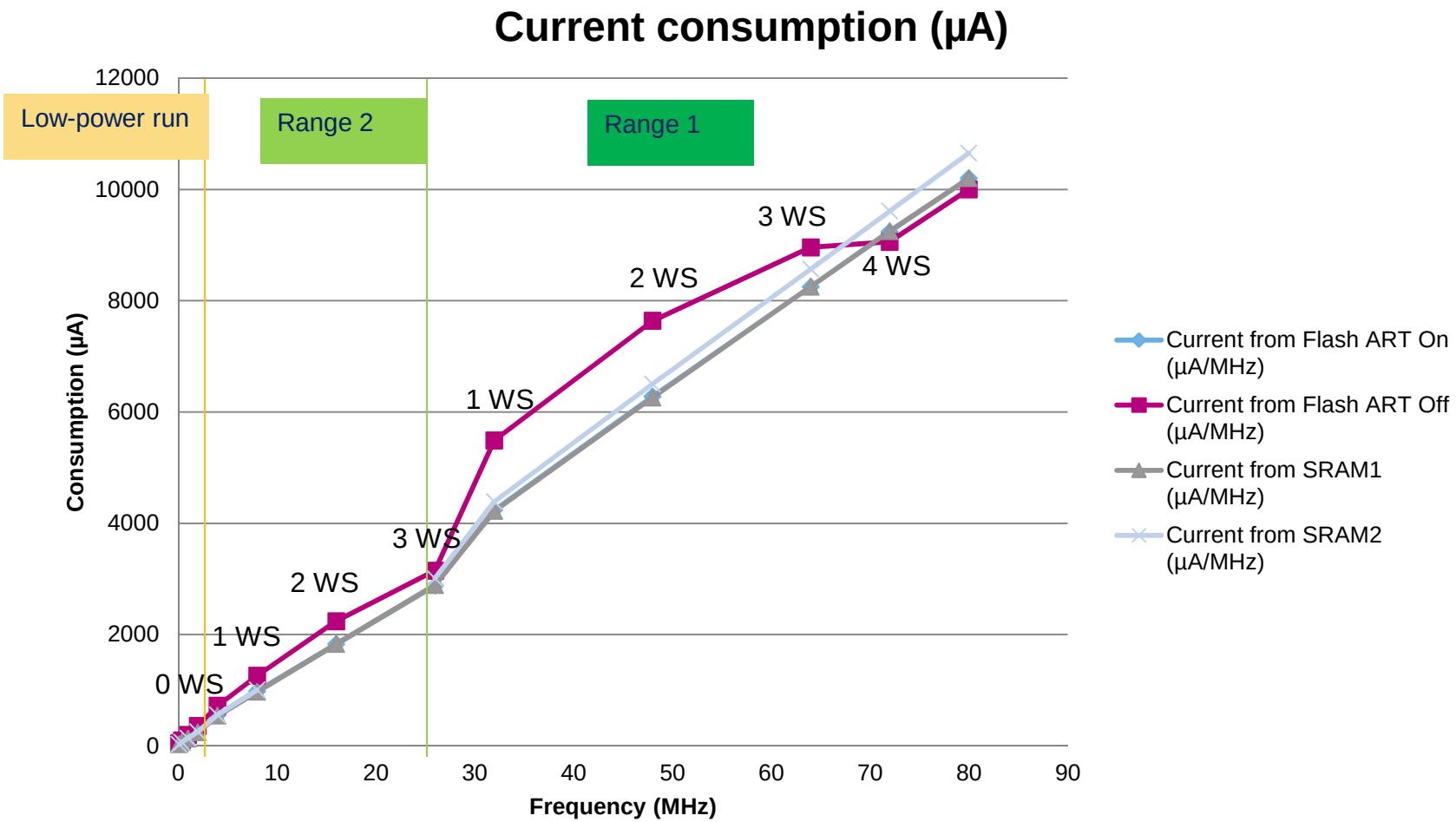
Power optimization versus frequency

- Thanks to voltage scaling and low power regulator RUN consumption can be optimized down to low frequencies



Power optimization versus frequency

- Flash has small dynamic consumption => benefits when the FW has a limited cache usage.



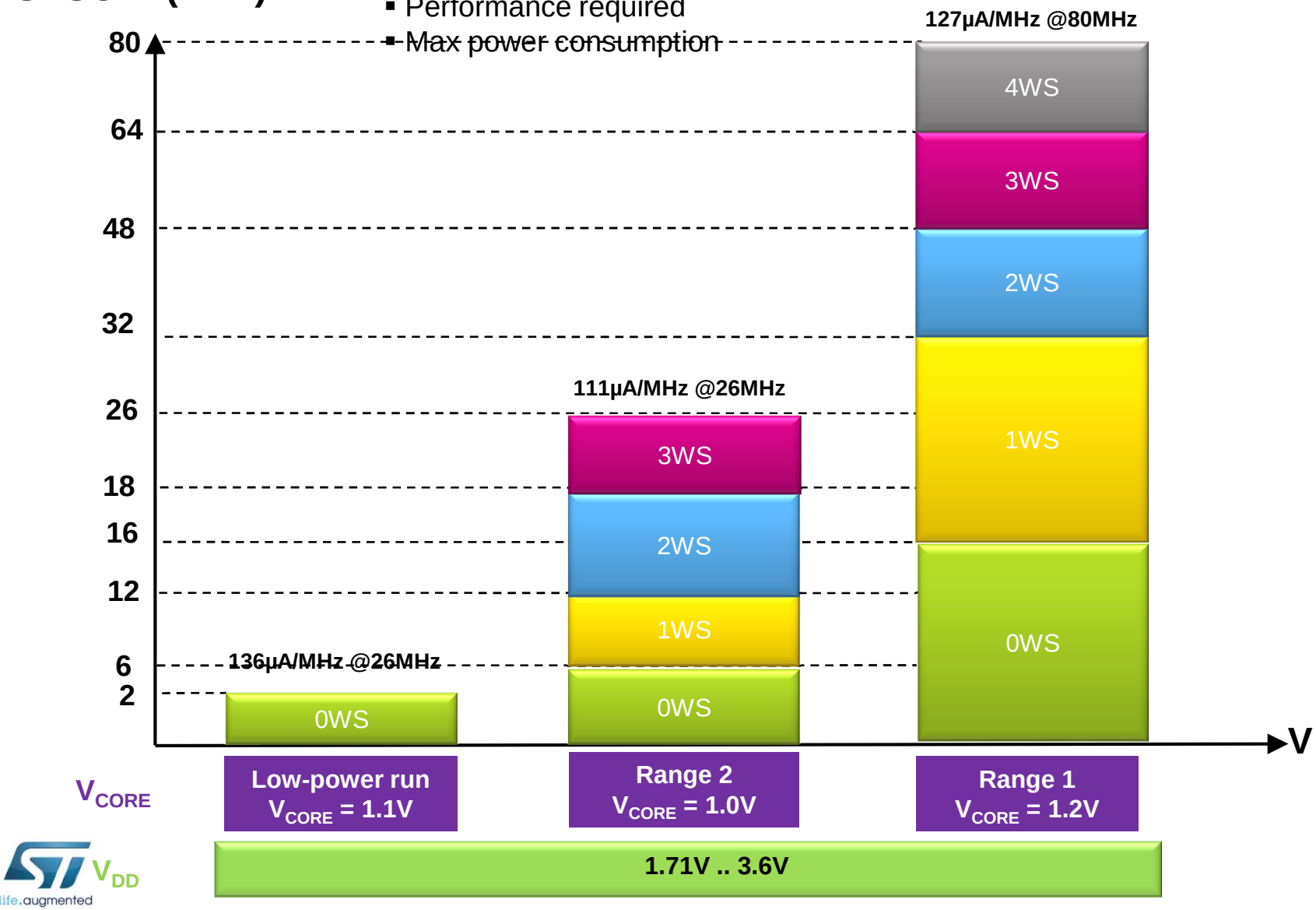
Run and Low-power run modes

- Several options depending on required performance and consumption:
  - Range 1 for SYSCLK up to 80 MHz
  - Range 2 for SYSCLK up to 26 MHz
- Voltage scaling range selected with VOS[1:0] bits in PWR_CR1
- Clock source max frequency depending on voltage scaling range:

Voltage range	MSI	HSI	HSE	PLL
Range 1	48 MHz range	16 MHz	48 MHz	80 MHz VCO max = 344 MHz
Range 2	24 MHz range	16 MHz	26 MHz	26 MHz VCO max = 128 MHz

Dynamic voltage scaling in Run mode

- Voltage scaling optimizes the product efficiency (Consumption vs Performance)
- User selects a Range (voltage scaling) according to :
  - Performance required
  - Max power consumption



Run and Low-power run modes

- Each peripheral clock can be configured to be ON or OFF in Run and Low-power run modes thanks to RCC_AHB1ENR, RCC_AHB2ENR, RCC_AHB3ENR, RCC_APB1ENR1, RCC_APB1ENR2, RCC_APB2ENR
  - For the peripherals with independent clock : the bit controls both AHB/APB and kernel clock
  - By default all peripheral clocks are OFF, except Flash interface clock
  - SRAM1 and SRAM2 clocks are always ON in Run mode

- When running from SRAM1 or SRAM2 (in Run or Low-power run):
  - Flash can put in power-down mode by setting **RUN_PD** bit in FLASH_ACR
  - Flash clock can be switched off by clearing **FLASHEN** bit in RCC_AHB1ENR
  - Flash MUST NOT be accessed when it is switched off (no hardware protection) => interrupt must be mapped in SRAM (using Vector Table Offset Register CortexM4 register)

STM32L4 Power Mode

Run mode

Run Mode Range 1
Ex: execution from Flash

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
  - Range 1 (up to 80MHZ)
  - Range 2 (up to 26MHZ)
- Low Power regulator (LPR) up to 2MHz

Range 1
127uA/MHz at 80 MHz
(10.2mA)

Range 2
111uA/MHz at 26 MHz
(2.9 mA)

- Active cell
- Frozen cell
- Cell in power-down
- Available Periph and clock

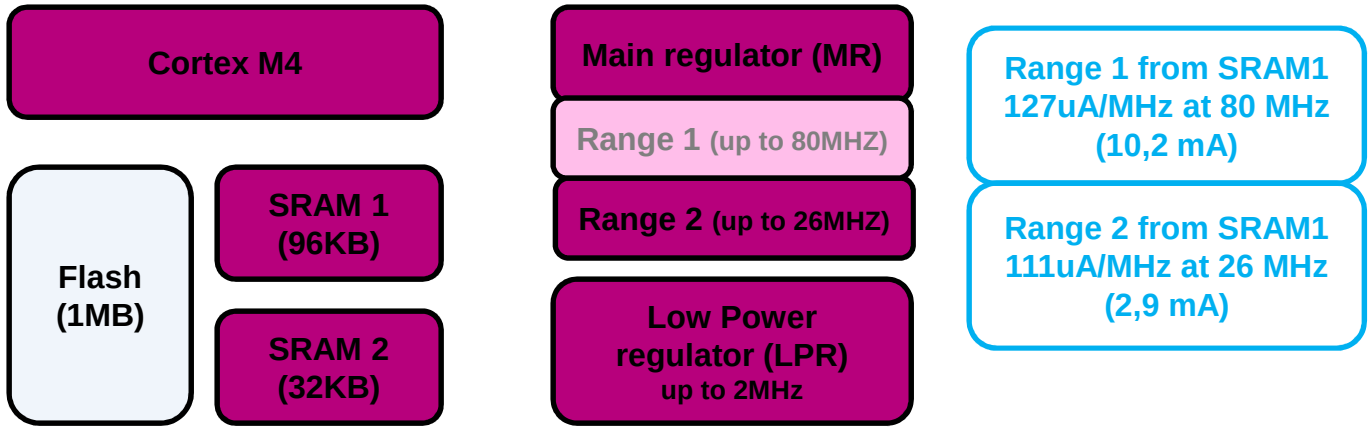
STM32L4 Power Mode

Run mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Run Mode Range 2
Ex: execution from SRAM



Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

Run and Low-power run modes

- Current consumption in Run mode depends on several parameters:
  - Executed binary code (program itself + compiler impact)
  - Program location in memory
  - Device software configuration
  - I/O pin loading and switching rate
  - Temperature
  - Execution from Flash or SRAM
    - When execution from Flash: ART accelerator configuration (Cache, Prefetch)
    - When execution from SRAM: SRAM1 or SRAM2

Run and Low-power run modes

- When executing from Flash, the best configuration is:
  - I-CACHE ON, D-CACHE ON, PREFETCH **OFF**

		ART ON (Cache ON, Prefetch Off)	ART OFF
Range 1@80MHz (4 WS)	Consumption(mA/MHz)	0,136	0.117
	Performance (Coremark/MHz)	3.32	1,55
	Energy Efficiency (Coremark/mA)	**24.4**	13.2
Range 2@26MHz (3 WS)	Consumption(mA/MHz)	0,118	0,111
	Performance (Coremark/MHz)	3.35	1,85
	Energy Efficiency (Coremark/mA)	**28,4**	16,6

Run and Low-power run modes

- When executing from SRAM, the best configuration is:
  - Execution from SRAM2

		Code & Data in SRAM1	Code in SRAM2, Data in SRAM1
Range 1@80MHz	Consumption(mA/MHz)	0,130	0.137
	Performance (Coremark/MHz)	2,37	3,42
	Energy Efficiency (Coremark/mA)	18,2	**25,0**

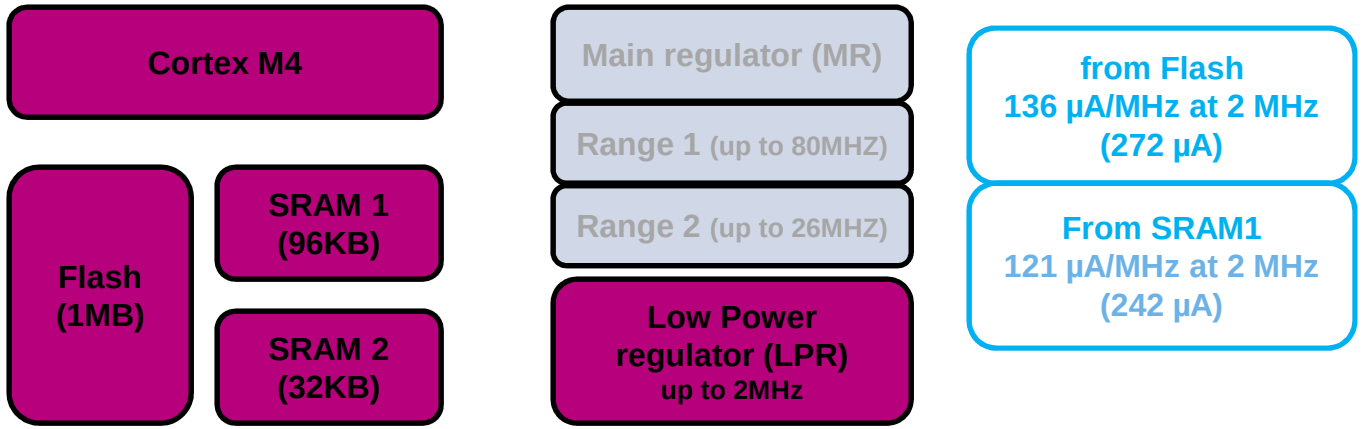
STM32L4 Power Mode

Low-power run mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Low-power run mode
Ex: execution from Flash



Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

Sleep and Low-power sleep modes

- **Sleep and Low-power sleep mode**: Core stopped, peripherals kept running
  - Entered from by executing special instructions
    - **WFI** (Wait For Interrupt)
      - Exit: any peripheral interrupt acknowledged by the Nested Vectored Interrupt Controller (NVIC)
    - **WFE** (Wait For Event)
      - An *event* can be an interrupt enabled in the peripheral control register but NOT in the NVIC or an EXTI line configured in event mode
      - Exit: as soon as the event occurs ➔ No time wasted in interrupt entry/exit
  - Two mechanisms to enter this mode
    - **Sleep Now**: MCU enters SLEEP mode as soon as WFI/WFE instruction are executed
    - **Sleep on Exit**: MCU enters SLEEP mode as soon as it exits the lowest priority ISR
      - The stack is not popped before entering the sleep, it will not be pushed when the next interrupt occurs, saving running time
    - **Controlled by CortexM4 reg System Control Register[SLEEPONEXIT]**

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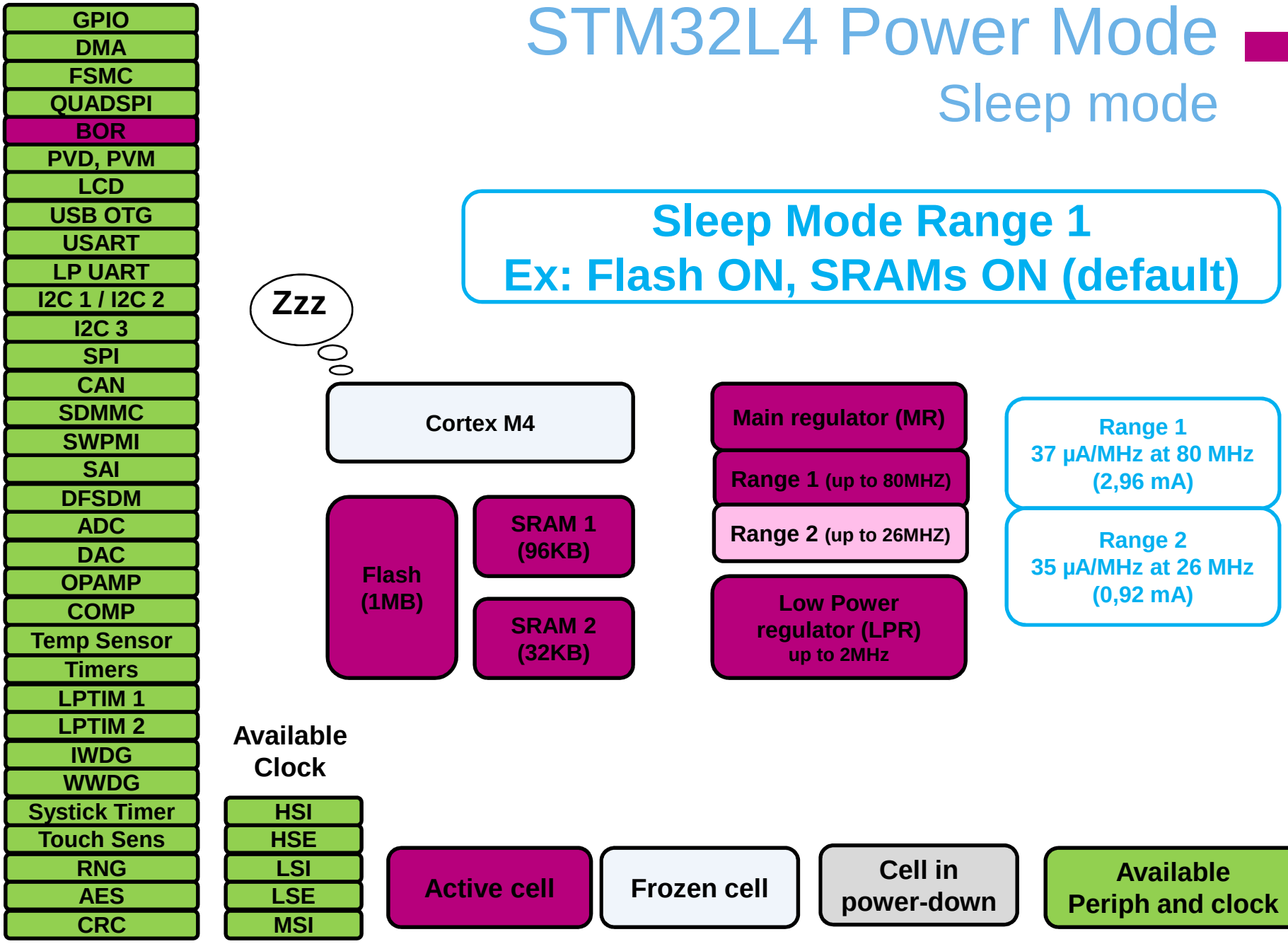
Sleep and Low-power sleep modes

- Entered by executing WFI or WFE either when
  - Main regulator is ON => Sleep mode
  - Main regulator is OFF => Low-power sleep mode
- Each peripheral clock can be configured to be ON or OFF in Sleep or Low-power sleep modes thanks to RCC_AHB1SMENR, RCC_AHB2SMENR, RCC_AHB3SMENR, RCC_APB1SMENR1, RCC_APB1SMENR2, RCC_APB2SMENR
  - For the peripherals with independent clock : the bit controls both AHB/APB and kernel clock
  - This bit controls also the kernel clock in Stop mode
- **By default, FLASH, SRAM1 and SRAM2 clocks are ON in Sleep or Low-power sleep modes**
  - They can be disabled during Sleep/Low-power sleep by clearing **FLASHSMEN**, **SRAM1SMEN**, **SRAM2SMEN**
  - Flash can be put in power-down during Sleep/Low-power sleep by setting **SLEEP_PD** in FLASH_ACR

STM32L4 Power Mode

Sleep mode

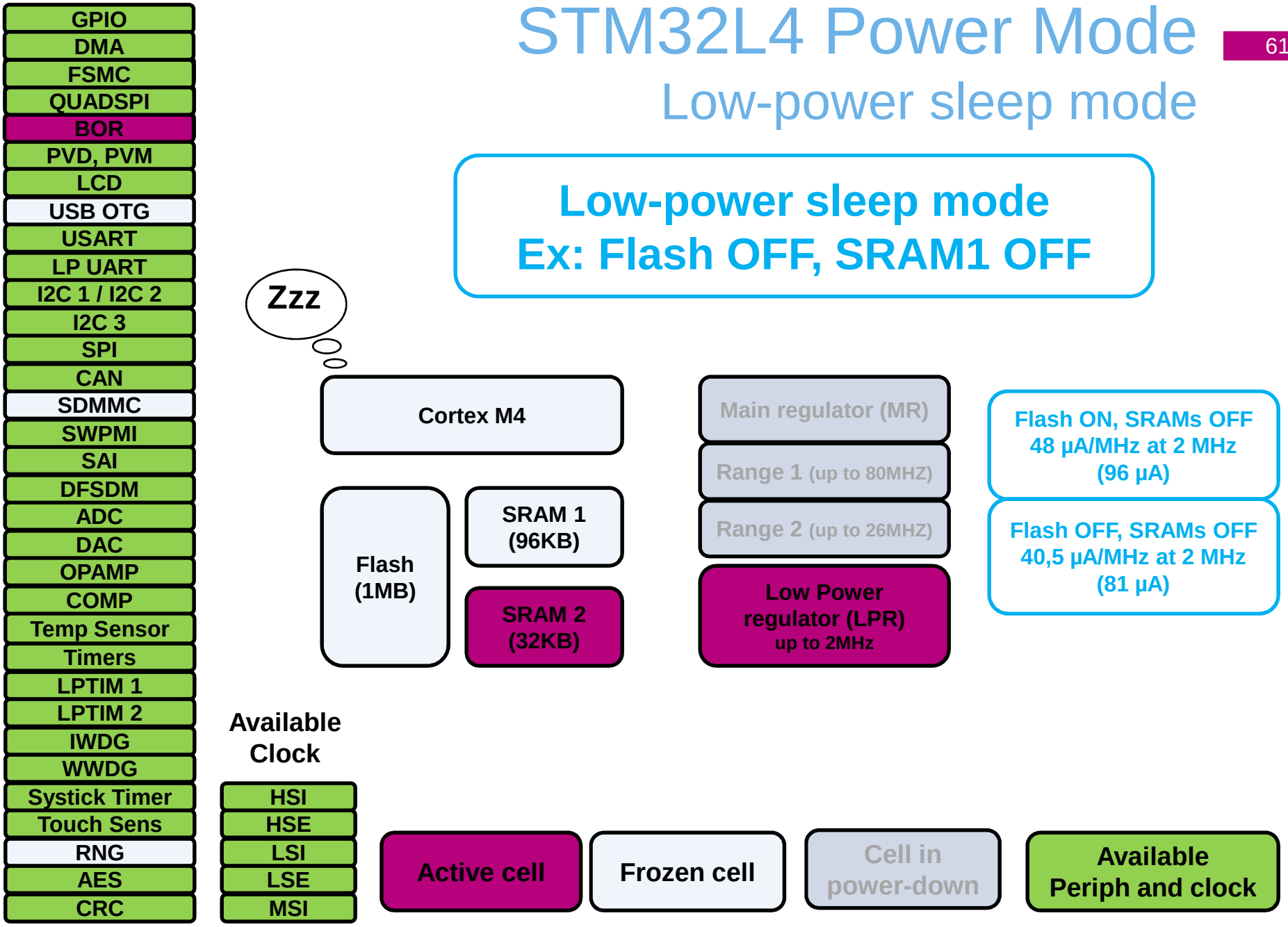
Sleep Mode Range 1
Ex: Flash ON, SRAMs ON (default)



STM32L4 Power Mode

Low-power sleep mode

Low-power sleep mode
Ex: Flash OFF, SRAM1 OFF



Batch Acquisition mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low power.

1. Only the needed communication peripheral + 1 DMA + 1 SRAM (SRAM1 or SRAM2) are configured with clock enable in Sleep mode

2. Flash is put in power-down mode and Flash clock is gated off during Sleep

3. Enter either Sleep or Low-power sleep mode
   - Note that I2C clock can be at 16 MHz even in low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI.

Low-power modes

- Next low-power modes are selected with **LPMS** in PWR_CR1
  - LPMS = 000 : Stop 1 mode selection with regulator in main mode
  - LPMS = 001 : Stop 1 mode selection with regulator in low-power mode
  - LPMS = 010 : Stop 2 mode selection
  - LPMS = 011 : Standby mode selection
  - LPMS = 1xx : Shutdown mode selection
- Before entering Stop 2 mode :
  - All the peripherals which cannot be enabled in Stop 2 mode must be either disabled by clearing the Enable bit in the peripheral itself, or put under reset state through control bit in the RCC

STM32L4 Power Mode

Stop 1 Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os kept, and configurable

Stop 1 w/ RTC on LSE quartz → **7,9 µA @3.0V**
7.6 µA @1.8V

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

6us wake-up from Flash
4us wake-up from RAM

STM32L4 Power Mode

Stop 1 Mode

Stop 1 w/o RTC ⇒ **7,5 µA @ 3.0V**
7.3 µA @ 1.8V

Available Peripheral

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

6us wake-up from Flash
4us wake-up from RAM

STM32L4 Power Mode

Stop 2 Mode

Stop 2 w/ RTC on LSE quartz → **1.66 µA @3.0V**
1.43 µA @1.8V

Available Peripheral

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

7us wake-up from Flash
5us wake-up from RAM

STM32L4 Power Mode

Stop 2 Mode

Stop 2 w/o RTC ⇒ **1.25 µA @3.0V**
1.19 µA @1.8V

Available Peripheral

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

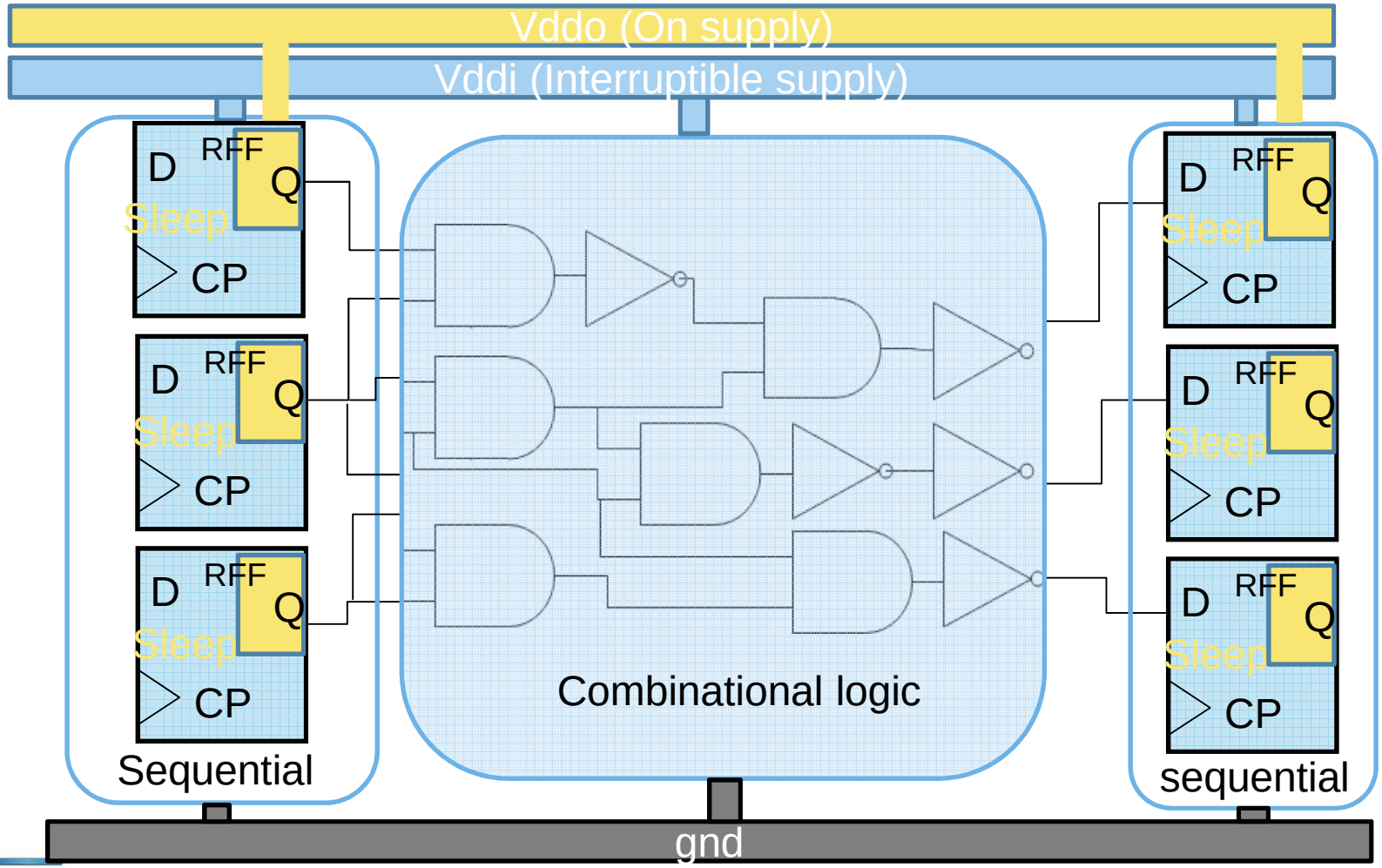
Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

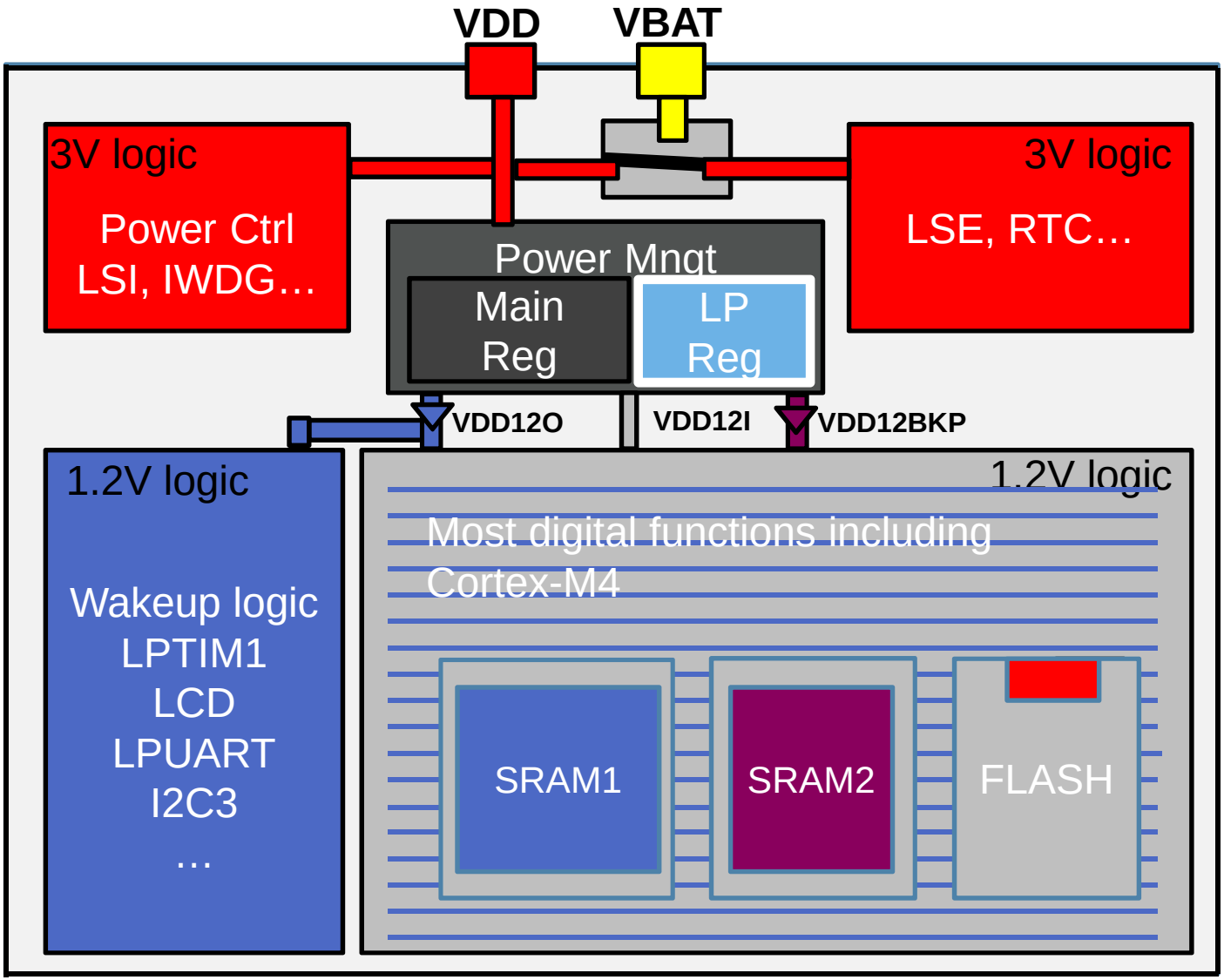
7us wake-up from Flash
5us wake-up from RAM

Design : Stop 2 Retention Registers

- With retention registers. One ultra low leakage latch saves information in each flip flop. Everything else can be shutoff (including 2/3rd of each flip flop)



Design : Stop 2 power domains



STM32L4 Power Mode

Standby Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Standby w/ SRAM2 w/o RTC

405 nA @ 3.0V
363 nA @1.8V

Zzz

Cortex M4

Main regulator (MR)

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Low Power regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Available Clock

- HSI
- HSE
- **LSI**
- **LSE**
- MSI

Wake-up event

- **NRST**
- **BOR**
- **RTC + Tamper**
- **IWDG**
- **5 WKUP pins**

14 us wake-up

STM32L4 Power Mode

Standby Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Standby w/ RTC on LSE quartz

674 nA @ 3.0V
433 nA@ 1.8V

- Cortex M4
- Main regulator (MR)
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Low Power regulator (LPR)
- **Backup domain**
- **Backup Register (32x32-bits)**
- **RTC**

Available Clock

- HSI
- HSE
- **LSI**
- **LSE**
- MSI

Wake-up event

- **NRST**
- **BOR**
- **RTC + Tamper**
- **IWDG**
- **5 WKUP pins**

14 us wake-up

STM32L4 Power Mode

Standby Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down

Standby ⇒ **169 nA @ 3.0V**
128 nA @ 1.8V

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Low Power regulator (LPR)
- **Backup domain**
  - **Backup Register (32x32-bits)**
  - **RTC**

Available Clock

- HSI
- HSE
- **LSI**
- **LSE**
- MSI

Wake-up event

- **NRST**
- **BOR**
- **RTC + Tamper**
- **IWDG**
- **5 WKUP pins**

14 us wake-up

Standby mode

- Ultra Low Power **BOR** always ON (V_{BOR0})
  - Higher thresholds brings additional consumption
- Configurable **pull-up or pull-down on all I/Os**
  - PWR_PUCRx registers (x = A,B,…H)
  - PWR_PDCRx registers (x = A,B,…H)
  - Configuration applied when **APC** is set in PWR_CR3 register.
- Possibility to **backup 32kbytes SRAM2**
  - Set **RRS** bit in PWR_CR3 register
- 128 bytes backup registers
- The polarity of each of the **5** wakeup pins is configurable
- Wakeup clock is **MSI configurable from 1 to 8MHz**.

Shutdown mode : NEW!

- Similar to standby mode but
  - **NO power monitoring:** no BOR, no switch to VBAT
  - **NO LSI** , no IWDG
  - **BOR reset** is generated when exiting Shutdown mode

    => all registers except those in Backup domain are reset.

    => reset generated on the pad
- 128 bytes backup registers
- Wakeup sources : **5** wakeup pins, RTC
- Wakeup clock is MSI 4 MHz.

STM32L4 Power Mode

Shutdown Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

Shutdown w/ RTC on LSE quartz ⇒ **476 nA @ 3.0V**
265 nA @ 1.8V

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Low Power regulator (LPR)

Backup domain
- Backup Register (32x32-bits)
- RTC

Available Clock

- HSI
- HSE
- LSI
- **LSE**
- MSI

Wake-up event

- NRST
- RTC + Tamper
- 5 WKUP pins

250 us wake-up

STM32L4 Power Mode

Shutdown Mode

Available Peripheral

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

Shutdown → **77 nA @ 3.0V**
43 nA @ 1.8V

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Low Power regulator (LPR)

Available Clock

- HSI
- HSE
- LSI
- **LSE**
- MSI

- **Backup domain**
  - **Backup Register (32x32-bits)**
  - **RTC**

Wake-up event

- **NRST**
- **RTC + Tamper**
- **5 WKUP pins**

256 us wake-up

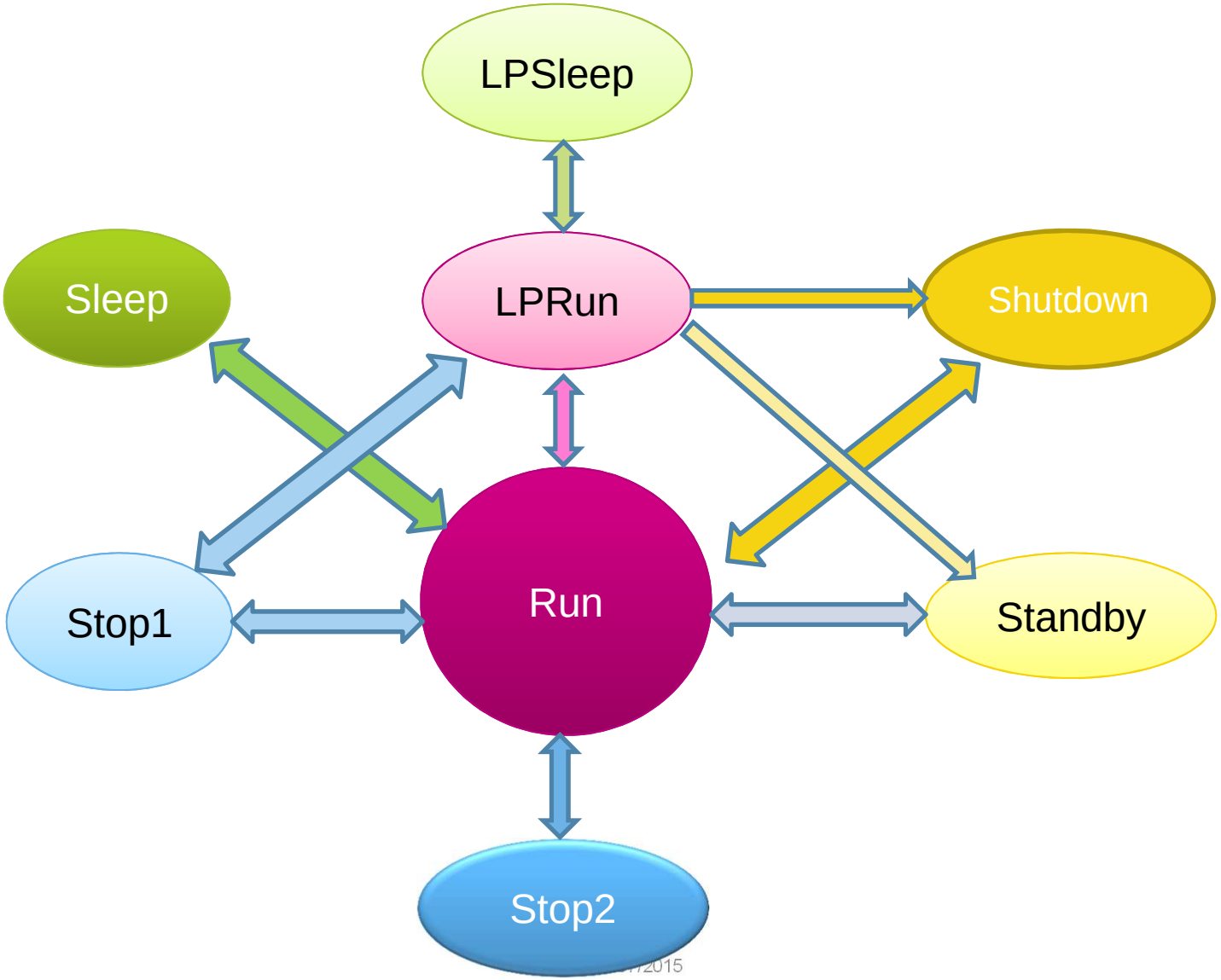
Low-power modes summary

Mode	Regulator	CPU	Flash	SRAM	Clocks	Peripherals In Bold : wakeup source	Consumption @ 1.8V	Wakeup time
Run	R1	Yes	ON(1)	ON	Any	All	127 µA/MHz	N/A
	R2					All except OTG, SDMMC, RNG	111 µA/MHz	
LPRun	LPR	Yes	ON(1)	ON	Any *except PLL*	All except OTG, SDMMC, RNG	136 µA/MHz	TBD
Sleep	R1	No	ON(1)	ON(2)	Any	All **Any IT or event**	37 µA/MHz	6 cycles
	R2						35 µA/MHz	
LPSleep	LPR	No	ON(1)	ON(2)	Any *except PLL*	All except OTG, SDMMC, RNG **Any IT or event**	40 µA/MHz	6 cycles
Stop 1	LPR	No	OFF	ON	LSE/LSI	**Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, COMPx**,DACx,OPAMPx,**USARTx, LPUART,I2Cx,LPTIMx,OTG_FS, SWPMI**	7.3µA w/o RTC 7.6 µA w/RTC	4 µA RAM 6 µA Flash
Stop 2	LPR	No	OFF	ON	LSE/LSI	**Reset pin, all I/Os BOR,PVD,PVM,RTC,LCD,IWDG, COMPx,LPUART,I2C3,LPTIM1**	1.2 µA w/o RTC 1.4 µA w/RTC	5 µs RAM 7 µs Flash
Standby	LPR	DOWN	OFF	SRAM2 ON	LSE/LSI	**Reset pin, 5 WKUPx pins BOR, RTC, IWDG**	+ 235 nA	14 µs
	OFF			DOWN			128 nA w/o RTC 433 nA w/RTC	
Shutdown	OFF	DOWN	OFF	DOWN	LSE	**Reset pin, 5 WKUPx pins RTC**	43 nA w/o RTC 265 nA w/RTC	256 µs

1. Can be put in power-down and clock can be gated off
2. SRAM1 and SRAM2 can be gated off independently

life.augmented

Low-power modes transitions

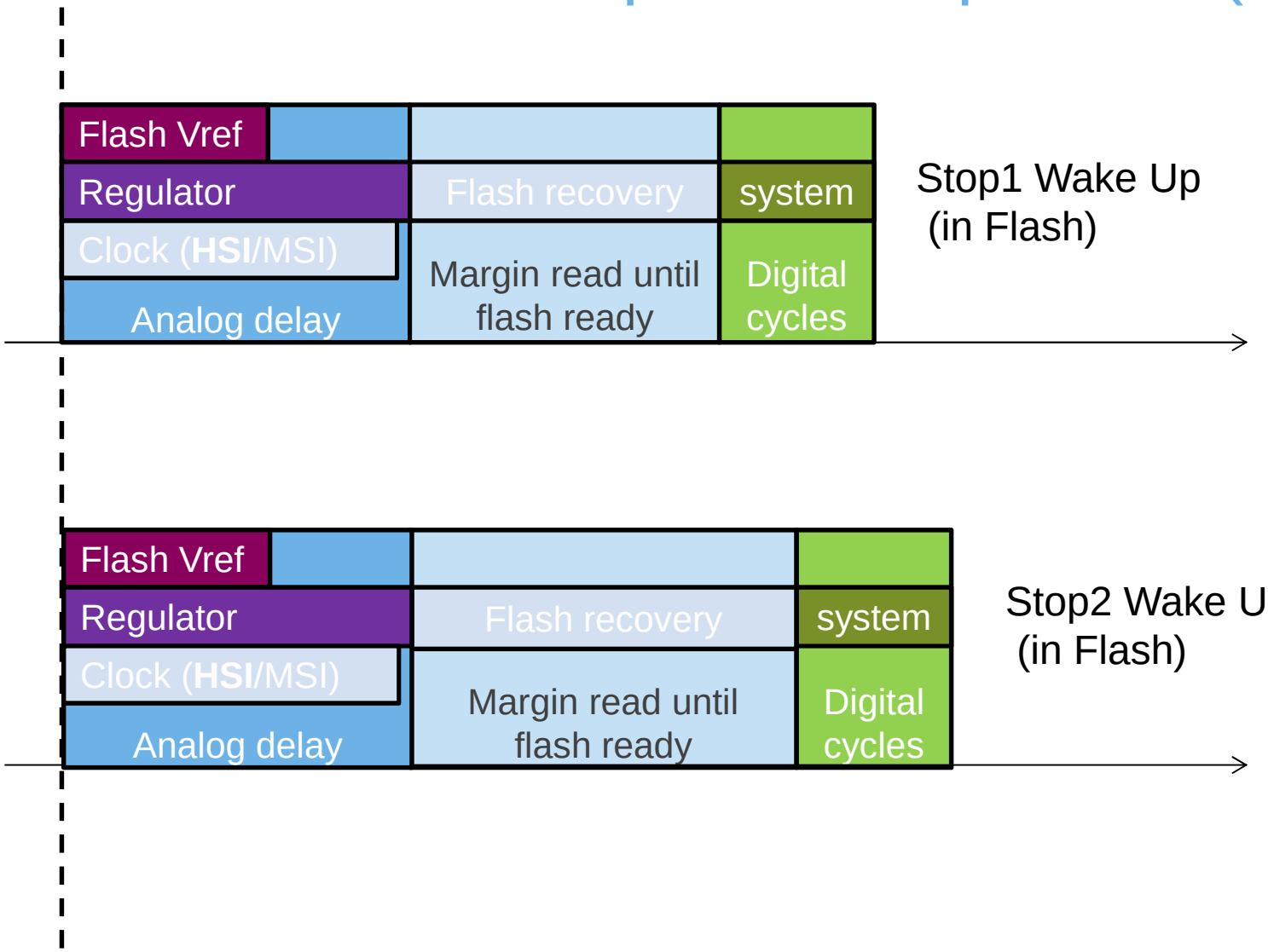


Wakeup from Stop

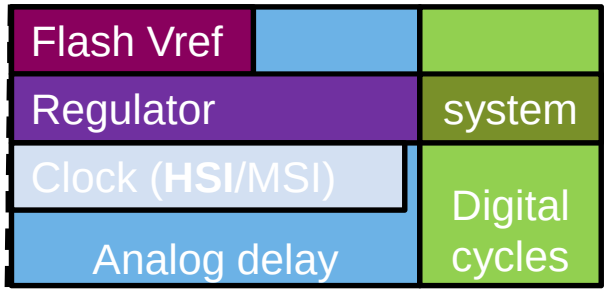
Wakeup time	Wakeup clock	Flash/SRAM	Typ	Unit
From Stop 1	MSI = 48 MHz	Flash	6.2	µs
		SRAM	4.5	
	HSI = 16 MHz	Flash	6.3	
		SRAM	5.5	

Wakeup time	Wakeup clock	Flash/SRAM	Typ	Unit
From Stop 2	MSI = 48 MHz	Flash	8	µs
		SRAM	5.1	
	HSI = 16 MHz	Flash	7.3	
		SRAM	5.7	

Wakeup from Stop mode (Flash)



Wakeup from Stop mode (RAM)



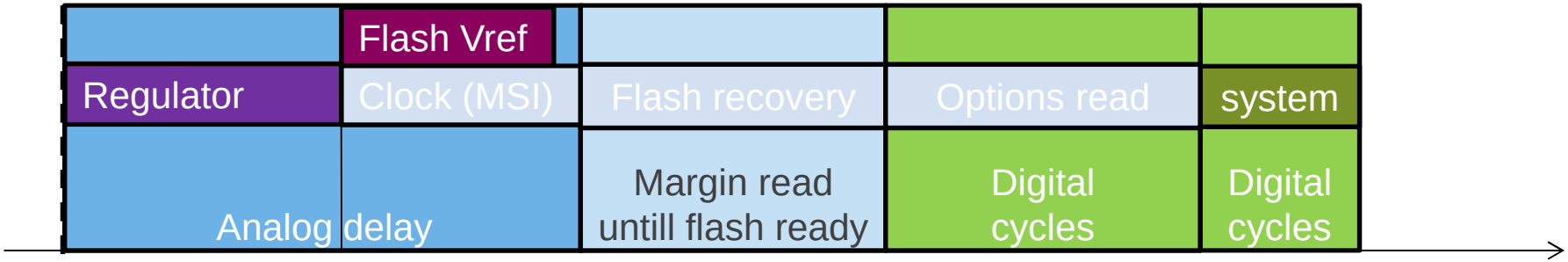
Stop1 or 2 Wake Up (in RAM or CACHE RAM)

- When the wakeup is done in Flash : the wakeup time can be shorter if the wakeup code is located in the instruction Cache, the prefetch buffer or the Cortex pipeline.

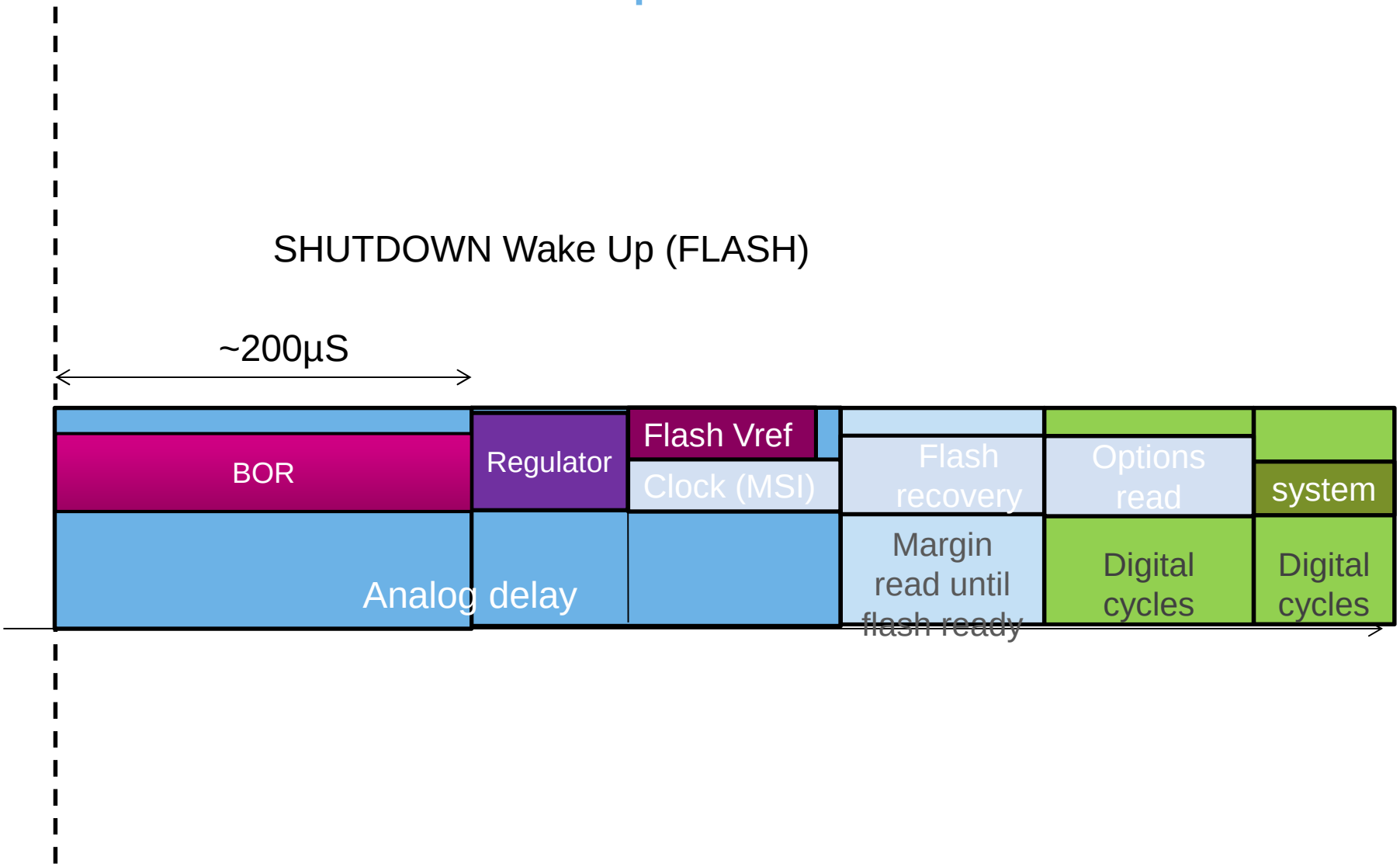
- The temporization to wait for the flash recovery occurs only when the flash access is done.

Wakeup from Standby mode

STANDBY Wake Up (FLASH)



Wakeup from Shutdown mode



Debug capability in LP modes

- Depends on DBGMCU_CR configuration
- DBG_STANDBY, DBG_STOP, DBG_SLEEP =0: No clock, no debug
- **DBG_STANDBY=1**: (FCLK=On, HCLK=On) In this case, the digital part is not unpowered and FCLK and HCLK are provided by the internal RC oscillator which remains active. This bit also allows debug in Shutdown mode.
- **DBG_STOP**= 1: (FCLK=On, HCLK=On) In this case, when entering STOP mode, FCLK and HCLK are provided by the internal RC oscillator which remains active in Stop 1 or Stop 2 mode.
- **DBG_SLEEP**: 1: (FCLK=On, HCLK=On) In this case, when entering Sleep or Low-power sleep mode, HCLK is fed by the same clock that is provided to FCLK (system clock as previously configured by the software