

Binary operations (x = x operation y)

| | |
|--------------------|----------------|
| Add/Subtract | MOV |
| 64 bits in edx:eax | + ADD reg, reg |
| ADD [lo], eax | - SUB reg, imm |
| ADC [hi], edx | XOR reg, imm |
| SUB [lo], eax | OR reg, [mem] |
| SBB [hi], edx | AND reg, [mem] |

x = x - y - cf SBB [mem], reg
x = x + y + cf ADC [mem], reg

set zf if (x and y) = 0 TEST [mem], imm
flags <- x - y CMP [mem], imm

Unary operations

(x = operation x)
NOT reg
x = -x NEG reg
x = x + 1 INC [mem]
x = x - 1 DEC [mem]

No operation and undefined instruction

NOP (db 90h)
UD2 (db 0Fh, 0Bh)

Zero or sign extension

MOVZX reg32, reg8 | byte [mem]
MOVSX reg32, reg16 | word [mem]
reg16, reg8 | byte [mem] eq. to movsx eax, ax CWDE

Conditions

if eax = ebx then G1
CMP eax, ebx
JNZ @F
G1
@@:
if eax = ebx then G1
else G2
CMP eax, ebx
JNZ @F
G1
JMP end
@@: G2
end:

For loops

for ecx=5 to 1 do G1
MOV ecx, 5
@@: G1
DEC ecx
JNZ @B
eax = 0
for ecx=0 to 9 do
eax = eax + a[ecx]
XOR eax, eax
MOV ecx, -(4 * 10)
@@: ADD eax, \[a + 40 + ecx]
ADD ecx, 4
JNZ @B

Spin-Wait Loop
acq: XOR eax, eax
INC eax
XCHG eax, [cs]
OR eax, eax
JNZ spin_loop
shared data access
spin_loop: PAUSE
CMP [cs], 0
JNE spin_loop
JMP acq

if eax=x then x=y, zf=1 else zf=0 LOCK CMPXCHG [mem] | reg, reg
if edx:eax=x then x=ecx:ebx, zf=1 else zf=0 LOCK CMPXCHG8B qword[mem]
You should check support for CMPXCHG8B with CPUID. Requires Pentium or higher.

Win32 Assembly Cheat Sheet

Memory [mem]
[reg + reg * (1|2|4|8) + abs_address]
Some parts may be omitted, e.g.,
[abs_address + reg] or [reg + reg * 4]

LEA instruction

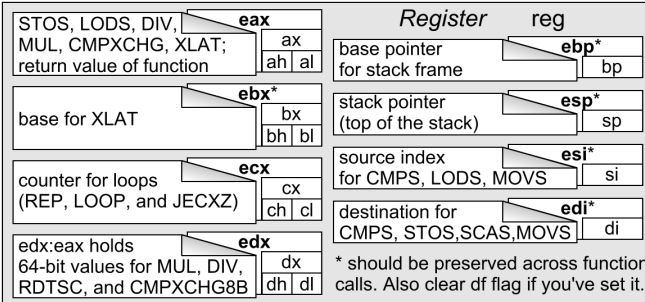
eax = eax * 5 LEA eax, [eax + eax * 4]
ebx = eax + ecx LEA ebx, [eax + ecx]
ebx = eax - 10 LEA ebx, [eax - 10]

Multiplication and division

ax = al * x MUL reg
dx:ax = ax * x IMUL [mem]
edx:eax = eax * x
al = ax / x DIV reg
ax = dx:ax / x IDIV [mem]
eax = edx:eax / x
remainder: ah, dx, edx
x = x * y IMUL reg, reg
x = y * z IMUL reg, reg, imm
reg, [mem], imm

Shifts

cf <- x <- 0 SHL(SAL) reg, imm
0 <- x <- cf SHR reg, imm
x <- x <- cf SAR reg, cl
cf <- x <- ROL [mem], imm
x <- x <- cf ROR [mem], imm
cf <- x <- RCL [mem], cl
x <- x <- cf RCR
cf <- x <- y SHRL reg, cl
y <- x <- cf SHRD [mem], reg, imm
Big-endian <-> little-endian BSWAP reg32
Requires 486



dx = sign(ax) CWD
edx = sign(eax) CDQ
eq. to movsx ax, al CBW
eq. to movsx eax, ax CWDE

Do-while loops

do G1
while eax ≠ ebx
@@: G1
CMP eax, ebx
JNZ @B
while eax ≠ ebx
do G1
CMP eax, ebx
JZ skiploop
@@: G1
CMP eax, ebx
JNZ @B
skiploop:

Switch...case

if eax=0 then G0
else if eax=1
then G1 else GD
CMP eax, 2
JAE def
JMP [t + eax * 4]
case0: G0
JMP @F
case1: G1
JMP @F
def: GD
@@:
t dd case0, case1

Flags

carry/borrow for addition/subtraction
set if the result of the previous operation is 0
set if the result is < 0
set if there's a signed overflow
if set, string operations go in reversed direction

Conditional jumps

JE(JZ) x = y
JNE(JNZ) x ≠ y
JG(JNLE) x > y
JL(JNGE) x < y
JGE(JNL) x ≥ y
JLE(JNG) x ≤ y
JC
JNC
JZ
JNZ
JS
JNS
JO
JNO
push flags PUSHF
pop flags POPF

Branchless code

if cc then x=1 else x=0 SETcc reg8 | byte [mem]
if cc then x=y CMOVcc reg16, reg16 | word [mem]
Check support for CMOVcc with CPUID. Requires Pentium pro or Athlon.
set cf if x < y (unsigned) CMP x, y
make bitmask from cf SBB eax, eax
if cf then increment eax ADC eax, 0

String operations

fill ecx elements from [edi] with aq REP STOSq
move ecx elements from [esi] to [edi] REP MOVsq
find aq in ecx elements at [edi] REPE SCASq
find non-aq in ecx elements at [edi] REPNE SCASq
After execution of the instruction, [edi] will point at the found value.
compare [esi] with [edi] (ecx elem's) REPE CMPSq
zf will be set if equal. Use JA/JB to find which string is greater.
find the first equal elements in [esi] and [edi] (ecx elem's) REPNE CMPSq
[esi] and [edi] will point at the equal elements afterwards.
q is B(byte), W(word), or D(word). Correspondingly, aq is al, ax, or eax.

Synchronization

exchange: x=y, y=x XCHG [mem] | reg, reg
x=x+y, y=x LOCK XADD [mem] | reg, reg

Time measurement

edx:eax = clocks RDTSC
Requires Pentium or Athlon. Flush the pipeline with CPUID.

CPUID instruction

eax=0 => eax=maxeax, ebx='Auth', edx='enti', ecx='AMD'
'Genu', 'inel', 'ntel'
eax=1 => eax:8:11=family, eax:4:7=model, edx:0:sse3,
ecx:4:rdtsc, 15=cmov, 23=mmx, 25=sse, 26=sse2
eax=8000_0000h => eax=max eax for extended functions
eax=8000_0001h => edx:31=3Dnow, edx:30=3Dnow-ext
eax=8000_0002h, .3h, .4h => eax:ebx:ecx:edx=namestring
Requires Pentium (may work on some 486's).