

CPE 690: Introduction to VLSI Design

Lecture 1

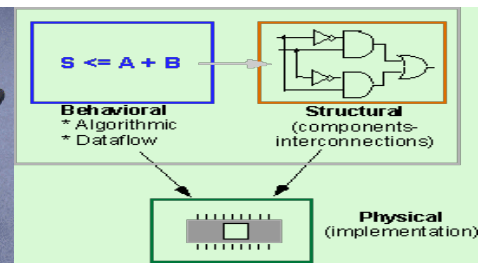
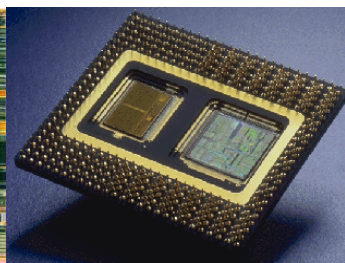
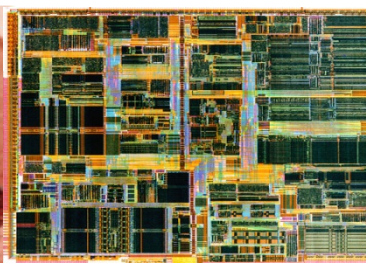
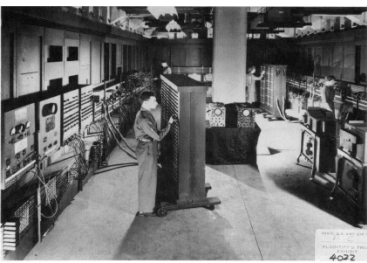
Introduction to Digital VLSI Design

Bryan Ackland

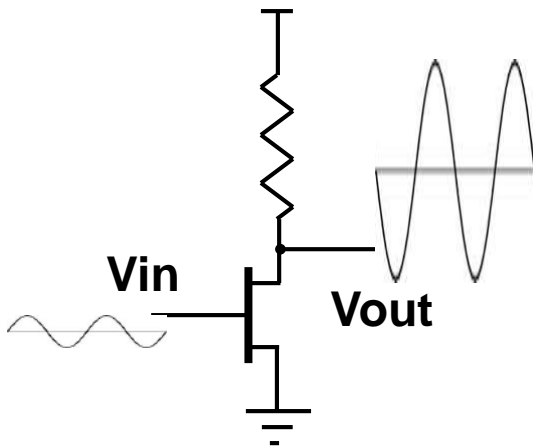
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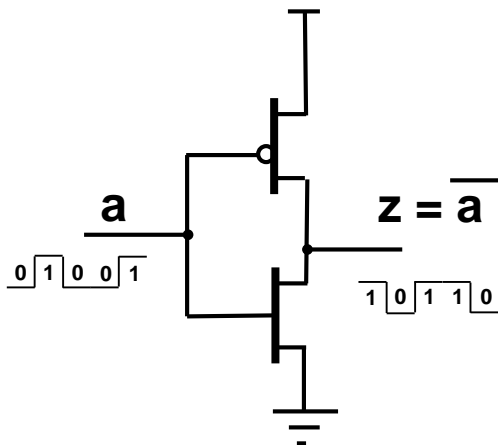
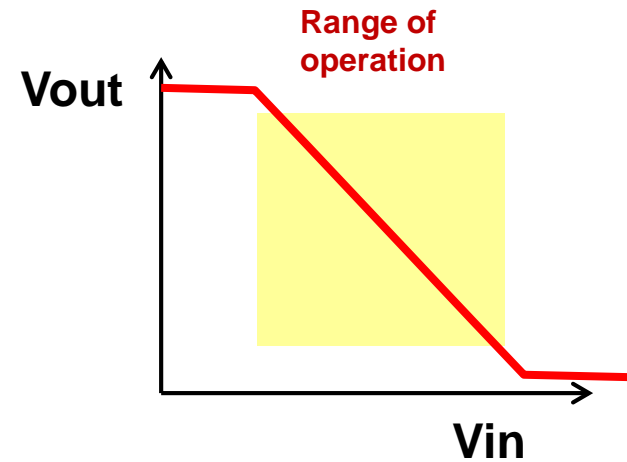


Analog & Digital Amplification



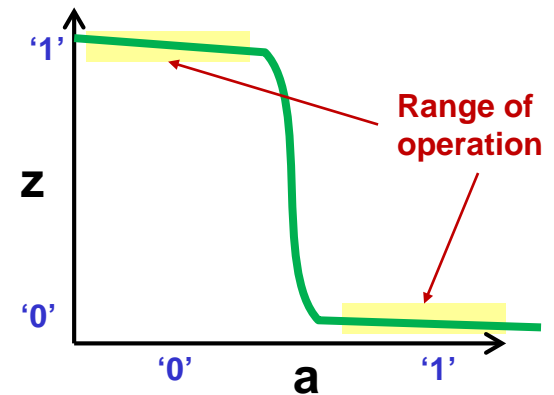
ANALOG

Circuit voltage represents continuous signal



DIGITAL

Circuit voltage represents one of two states: '0' and '1'



MIXED SIGNAL: Analog and digital in same circuit (chip)

Why Analog ?

- Analog circuits:
 - Complex functions with few transistors
 - Needed to interface to outside world
 - Low power (per function)
 - Circuit complexity limited by noise & component variation (process, temperature, voltage etc.)
 - Analog design requires significant skill and experience
 - Limited design automation and little re-use of circuits
 - Advanced (nanometer) processes provide reduced signal to noise ratio (because of reduced voltages)
 - Difficult to test

Why Digital ?

- Digital circuits:
 - Thousands of transistors to do simplest real-world function
 - Higher power dissipation (per function)
 - Highly immune to noise & component (process) variation
 - Same result every time
 - Highly reliable circuits with hundreds of millions of transistors
 - Significant re-use (libraries) and design automation (synthesis, formal verification)
 - Digital designers don't need deep circuit knowledge
 - Nanometer processes provide higher speed, greater density and lower power
 - Much simpler to test

What is VLSI ?

VERY LARGE SCALE



A circuit that has $10^4 \sim 10^9$ transistors on a single chip

Maximum number of transistors is still growing: quadruples every 24 months (Moore's law!)

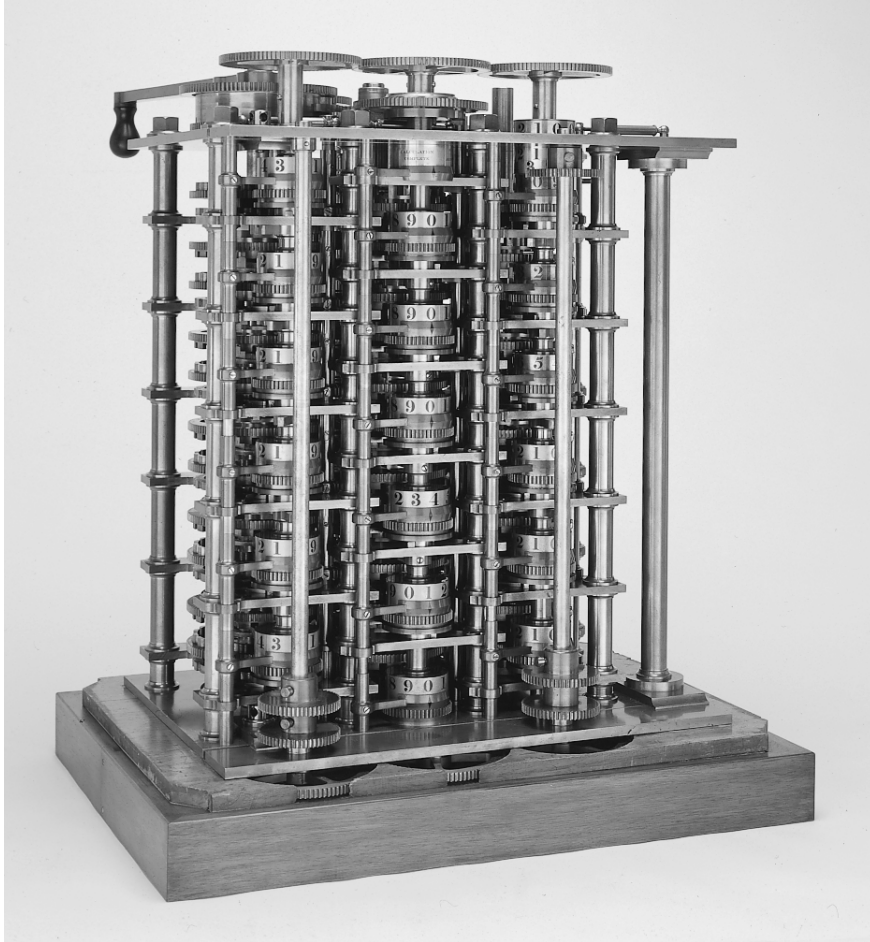
INTEGRATED CIRCUIT



Technique where many circuit components and the wiring that connects them are manufactured simultaneously on a monolithic compact (silicon) chip (or die)

First Digital Computer: Babbage Difference Engine

(1832)



- Executed basic operations (add, sub, mult, div) in arbitrary sequences
- Operated in two-cycle sequence, “Store”, and “Mill” (execute)
- Included features like pipelining to make it faster.
- Complexity: 25,000 parts.
- Cost: £17,470 (in 1834!)

ENIAC - The first electronic computer (1946)



- 100 kHz clock
- 20 words memory
(~ 100 bytes)
- 5000 operations/sec

10 feet tall, 30 tons

1,000 square feet of floor- space

More than 70,000 resistors

10,000 capacitors

6,000 switches

18,000 vacuum tubes

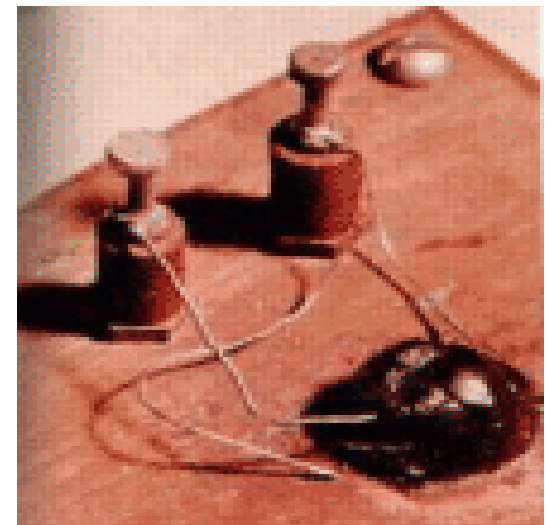
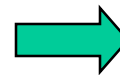
Requires 150 kilowatts of power;

Transistor Age...

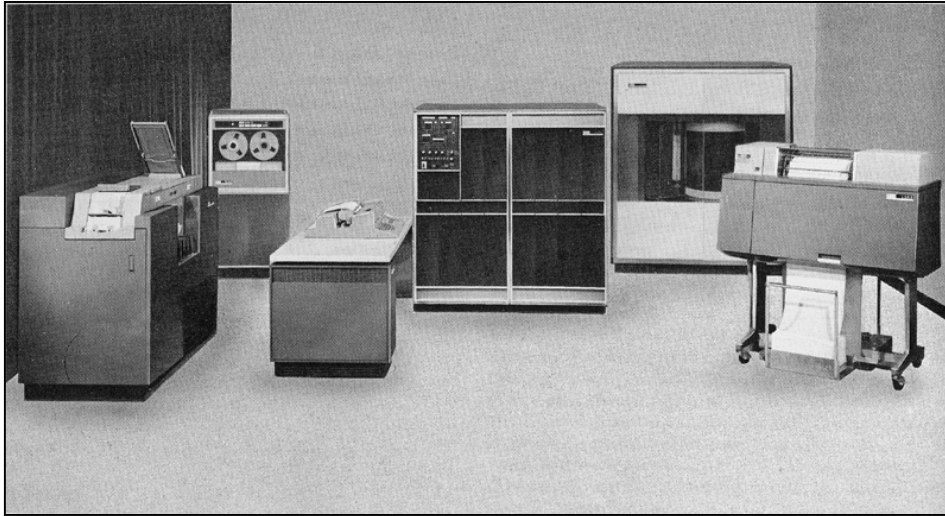


← 1947: Bardeen and Brattain create point-contact transistor (gain=18)

1951: Shockley develops junction transistor which can be manufactured in quantity.



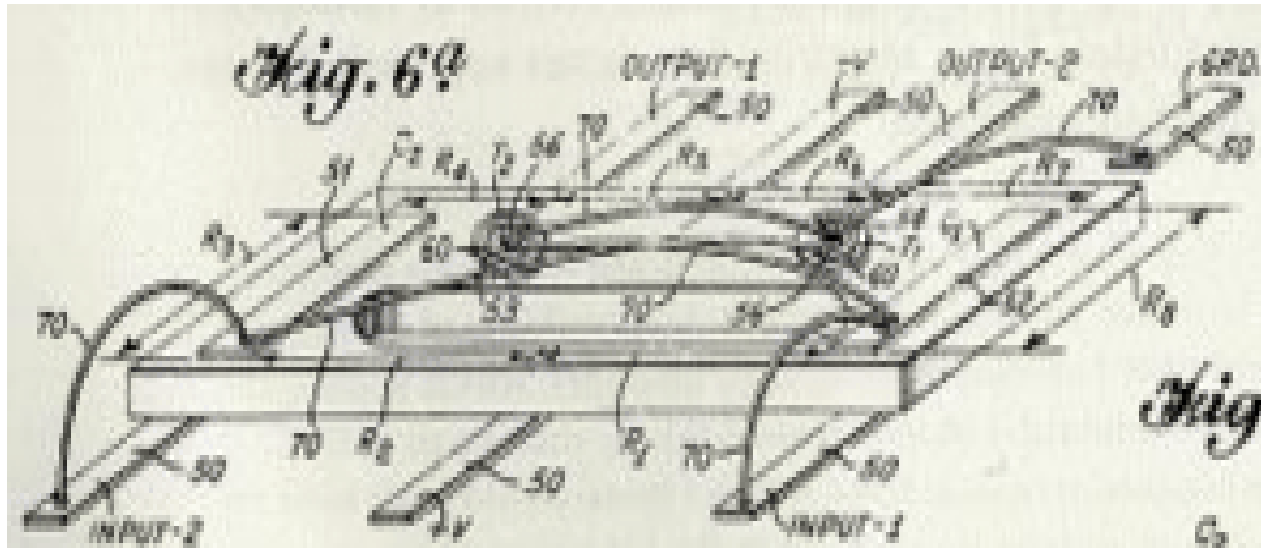
IBM 1401 - Transistor electronic computer (1959)



- Diode-transistor logic
 - 9,000 germanium transistors, 14,000 diodes
- Up to 16k x 6-bit words of magnetic core memory
- Binary-coded-decimal computation
 - 8-digit decimal add in 300 μ s
- Fortran and Cobol compilers
 - Used in payroll & accounting applications
- \$83,000 or \$2,500/month
- Up to 12 kW power



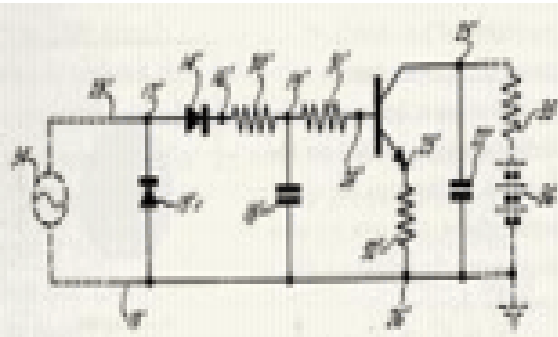
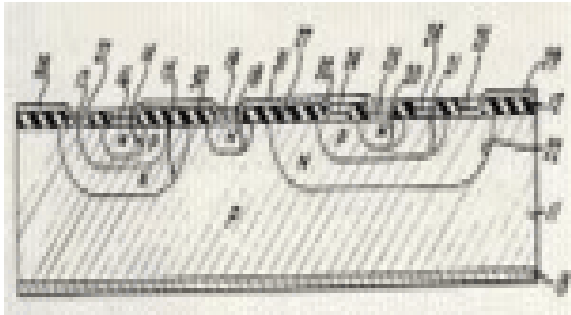
The Integrated Circuit



Jack Kilby, working at Texas Instruments, invented a monolithic “integrated circuit” in July 1959.

He constructed the flip-flop shown in the patent drawing above.

Planar transistors

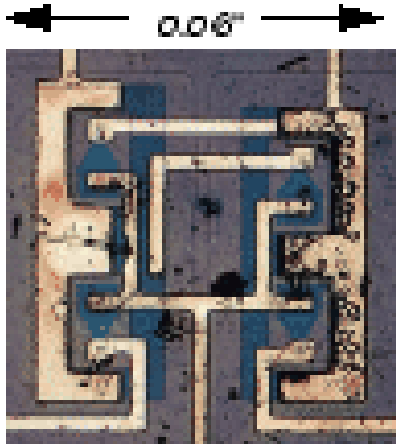


In mid 1959, Noyce develops the first true IC using planar transistors:

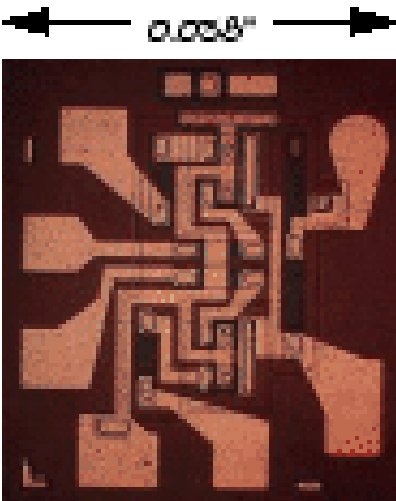
- Reverse biased pn junctions for isolation
- Diode-isolated silicon resistors and
- SiO₂ insulation
- Evaporated metal wiring on top

This enabled designers to place and connect multiple transistors on silicon die using sophisticated “printing process”

First Digital ICs – early 60's

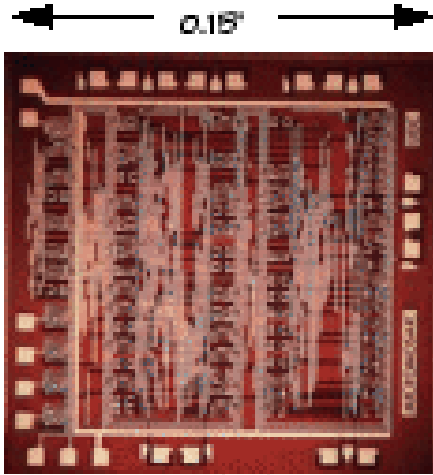


1961: TI and Fairchild introduced first logic IC's: dual flip-flop with 4 transistors (cost ~\$50)



1963: Densities and yields improve. This circuit has four flip-flops.

Continuing Development – late 60's



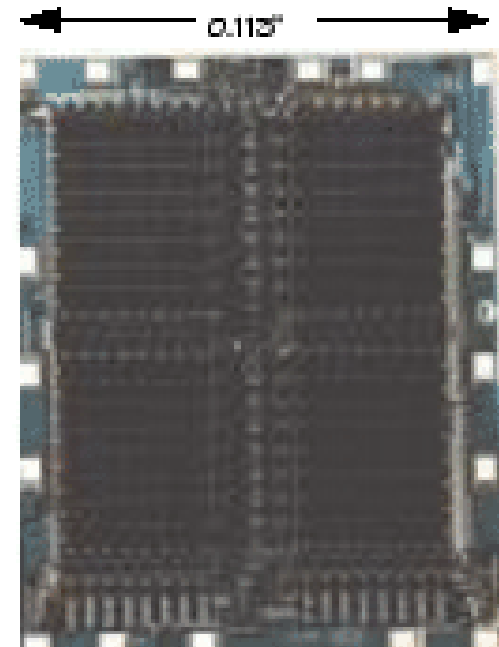
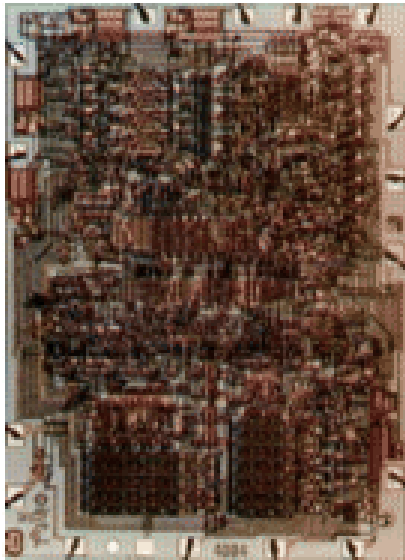
1967: Fairchild markets the first semi-custom chip. Transistors (organized in columns) can be easily rewired to create different circuits. Circuit had ~150 logic gates.

1968: Noyce and Moore leave Fairchild to form Intel. By 1971 Intel had 500 employees;

(By 2004, 80,000 employees in 55 countries and \$34.2B in sales)

Continuing Development early 70's

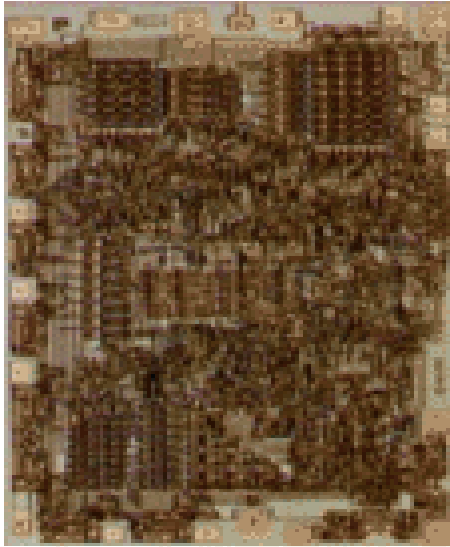
1970: Intel starts selling a 1k bit RAM.



1971: Ted Hoff at Intel designed the first microprocessor.

The 4004 had 4-bit busses and a clock rate of 108 KHz. It had 2300 transistors and was built in a 10 um process.

Continuing Development – Microprocessor



1972: 8008 introduced.

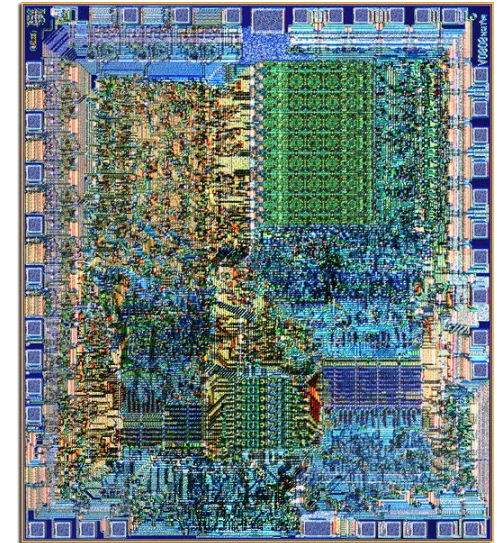
3,500 transistors supporting
a byte-wide data path.

1974: Introduction of the 8080 – first “truly
usable microprocessor”

8-bit data, 16-bit address bus (up to 64kB memory)

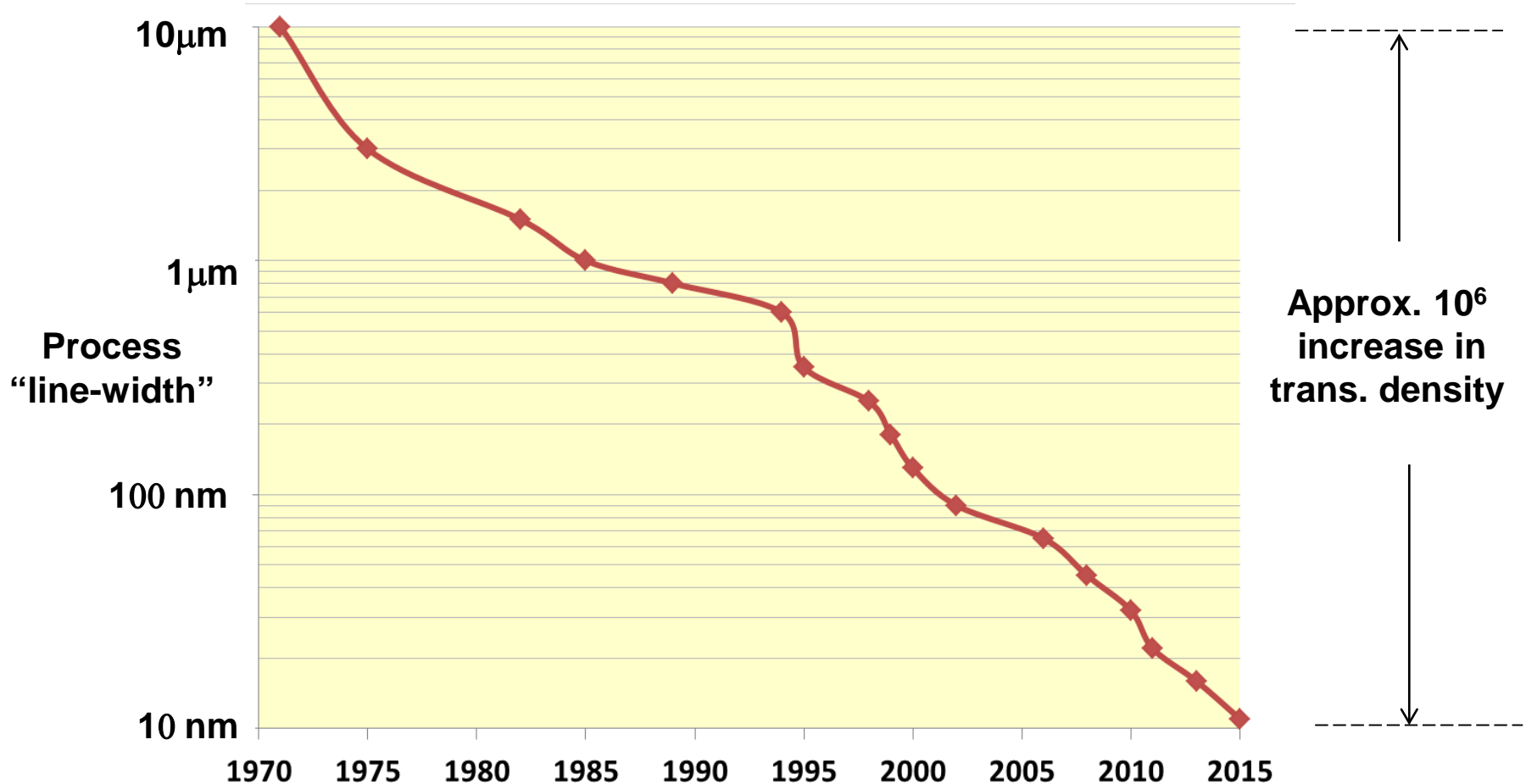
6,000 transistors in a 6 μ m process.

Clock rate was 2 MHz.



Exponential Growth

Planar “printing process” enabled continuing reductions in process “line width” which has led to increased density in transistors/mm²



What has brought about this extraordinary growth?

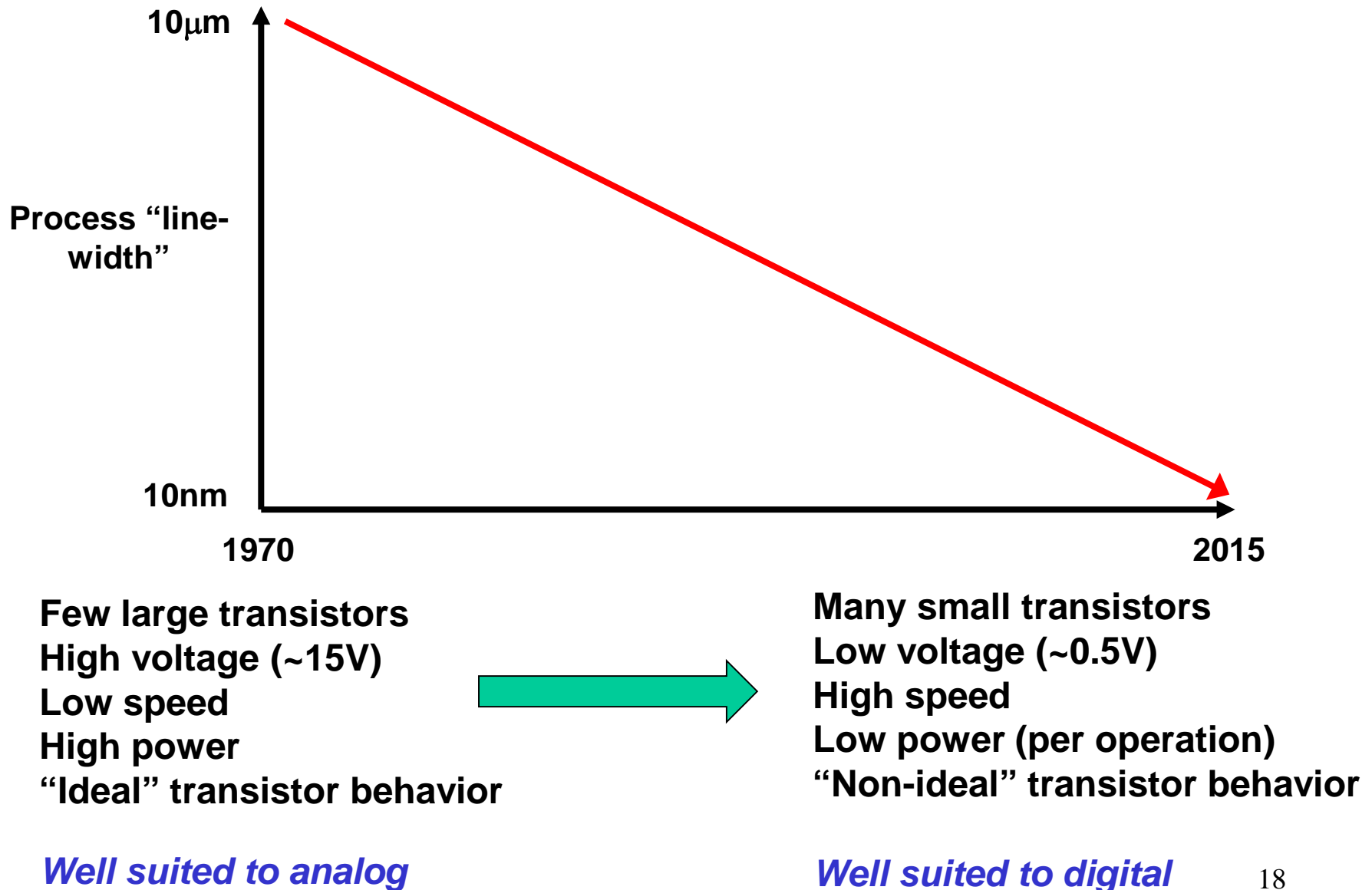
Huge investments in and major advances in:

- Solid State Physics
- Materials Science
- Lithography and fab
- Device modeling
- Circuit design and layout
- Architecture design
- Algorithms
- CAD tools

Cost of building 65nm fab is around \$3B !

Cost of building 22nm fab is around \$7B !

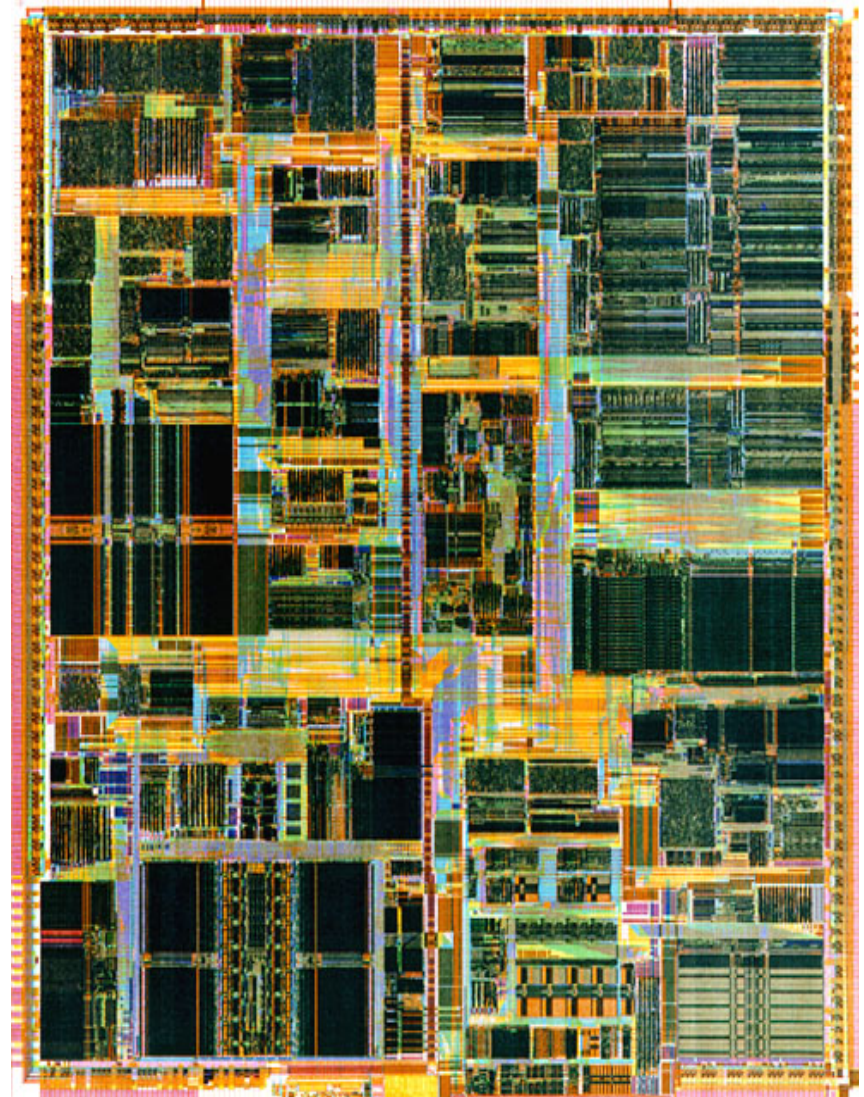
Analog vs. Digital Revisited



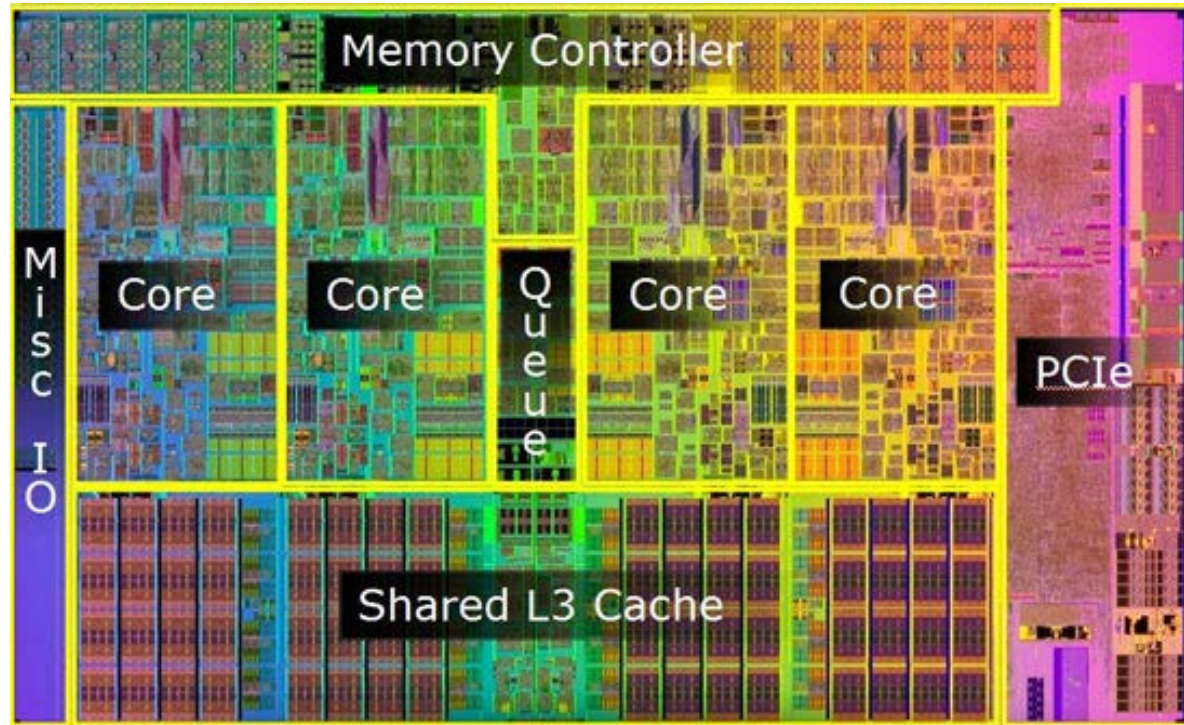
High Performance Digital: Pentium 4 – 0.18 um

0.18-micron process technology

- Introduced in 2000 (1.5, 1.4 GHz)
- Level Two cache: 256 KB
Advanced Transfer Cache
- System Bus Speed: 400 MHz
- SSE2 SIMD Extensions
- Transistors: **42 Million**
- Typical Use: Desktops and entry-level workstations



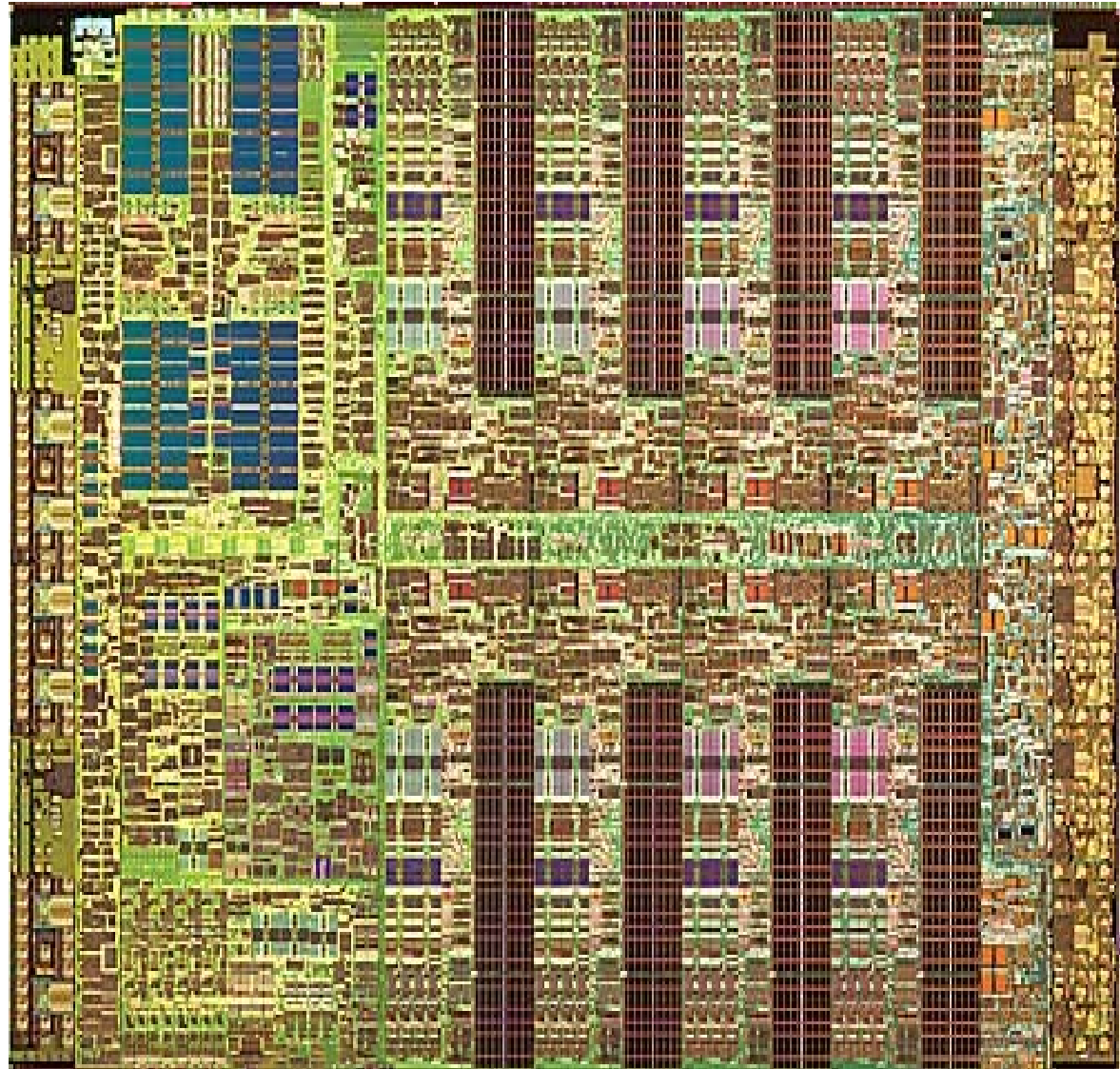
High Performance Digital: Intel i5– 45 nm



- Introduced 2009 (2.6 GHz)
- Level 3 cache: 8MB
- 4 cores / 4 threads
- Transistors: 774 Million
- 95 W

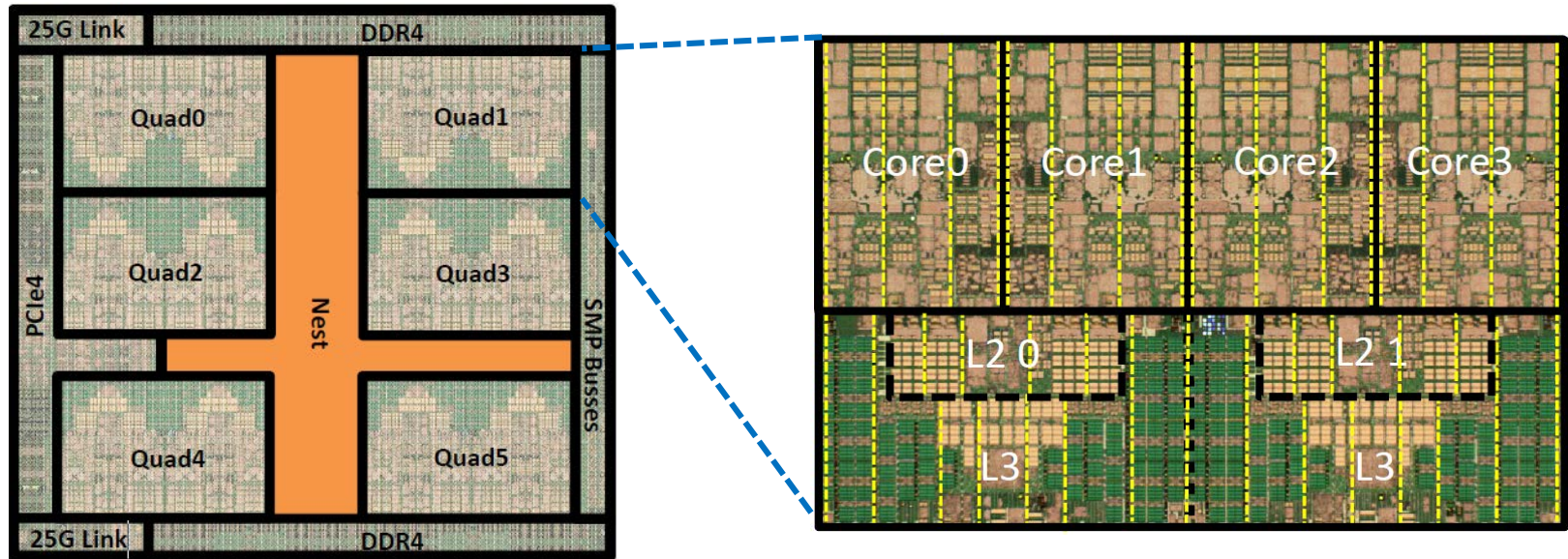
Supercomputer for Sony's PlayStation 3 – 45nm

- IBM/Toshiba chip has 9 processor cores
- 192 billion floating-point operations per second
- 240 M transistors
- Optimized for graphics & multimedia



IBM Power 9 Processor

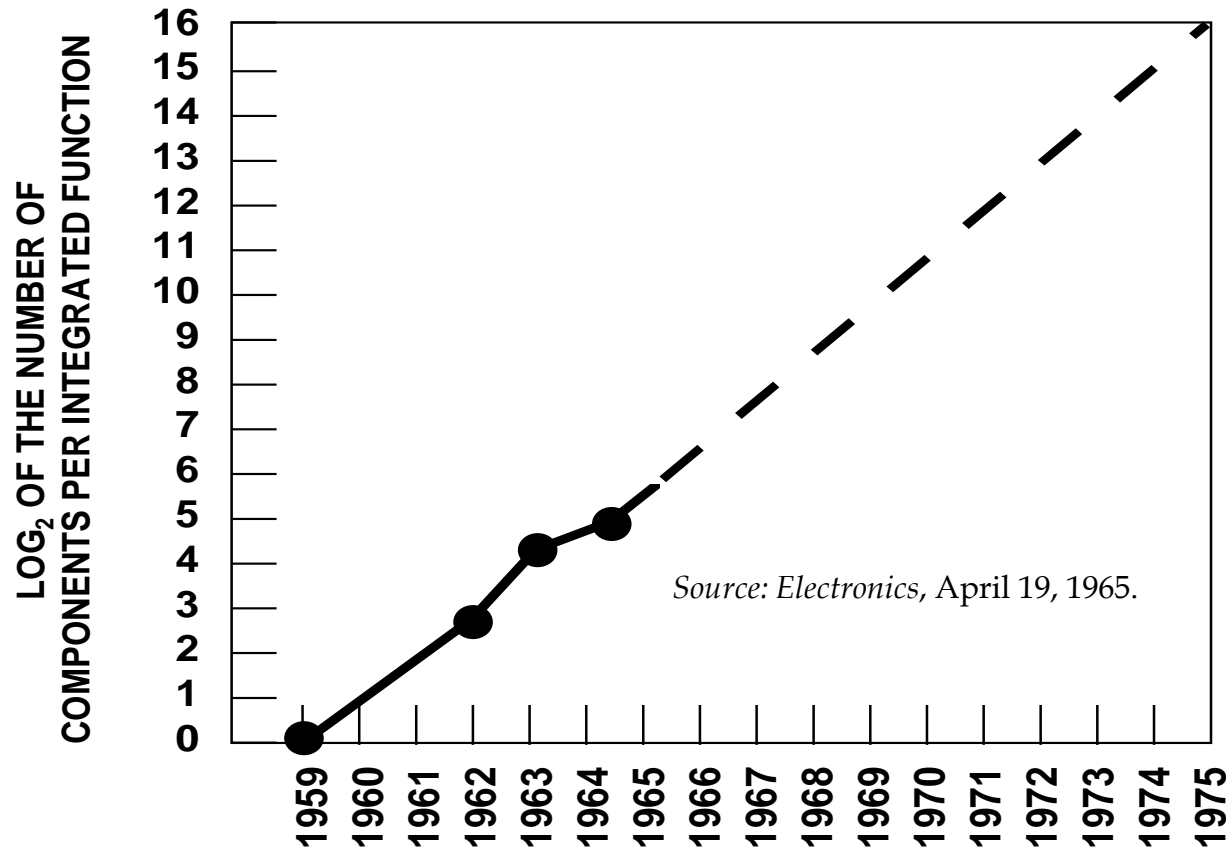
IEEE ISSCC 2017



- 14 nm SOI FinFET process with 17 levels interconnect
- 24 x 64-bit 4.0 GHz cores optimized for cognitive computing
- 8.0B transistors
- 6 MB L2 / 120 MB L3
- 12.9 Tb/s I/O BW
- 695 mm² die (approx. 1.1 inches square)

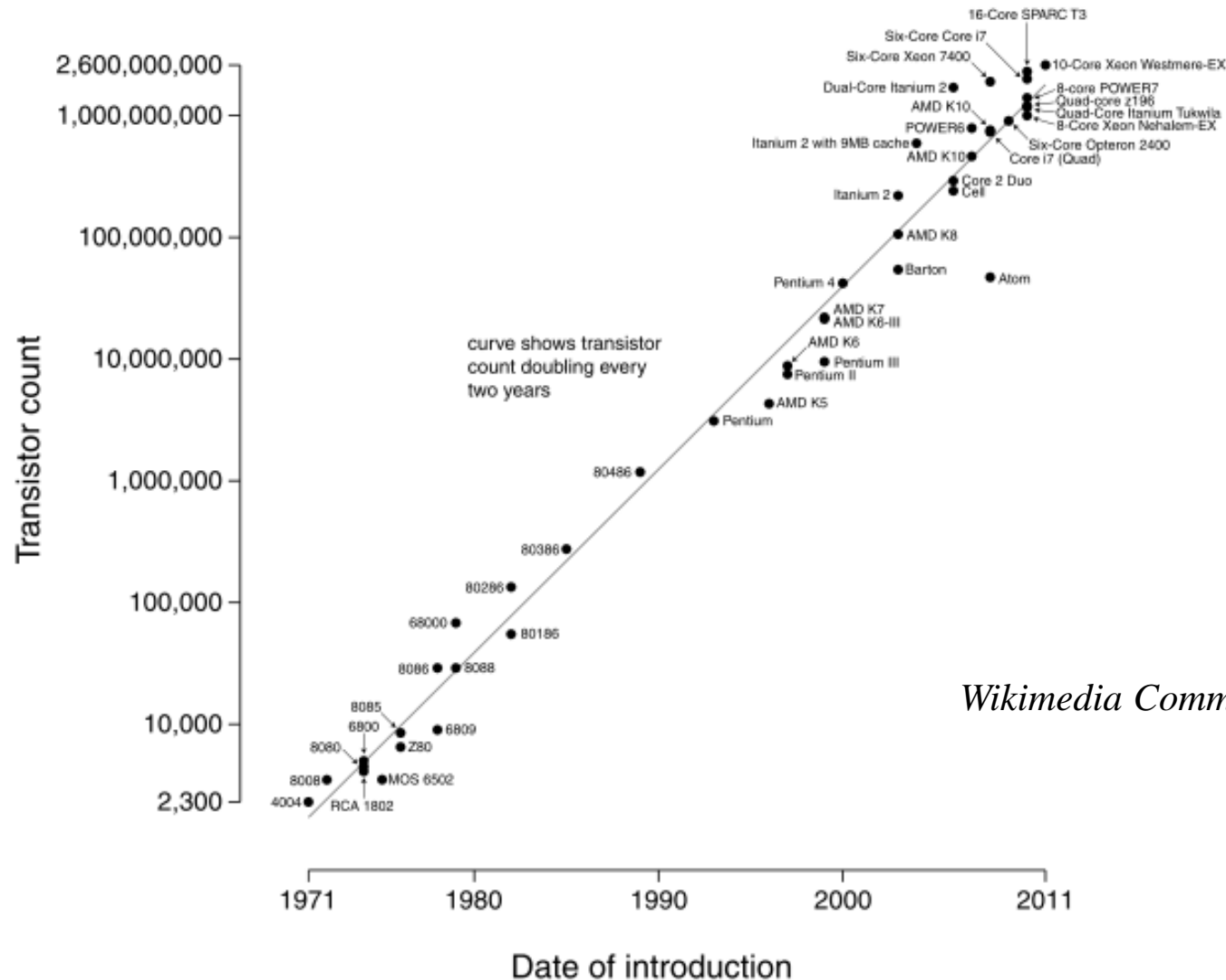
Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip approximately doubled every 12 months.



- He made a prediction that IC **cost effective component count** would continue to double every 12 months

Moore's Law – how it checked out



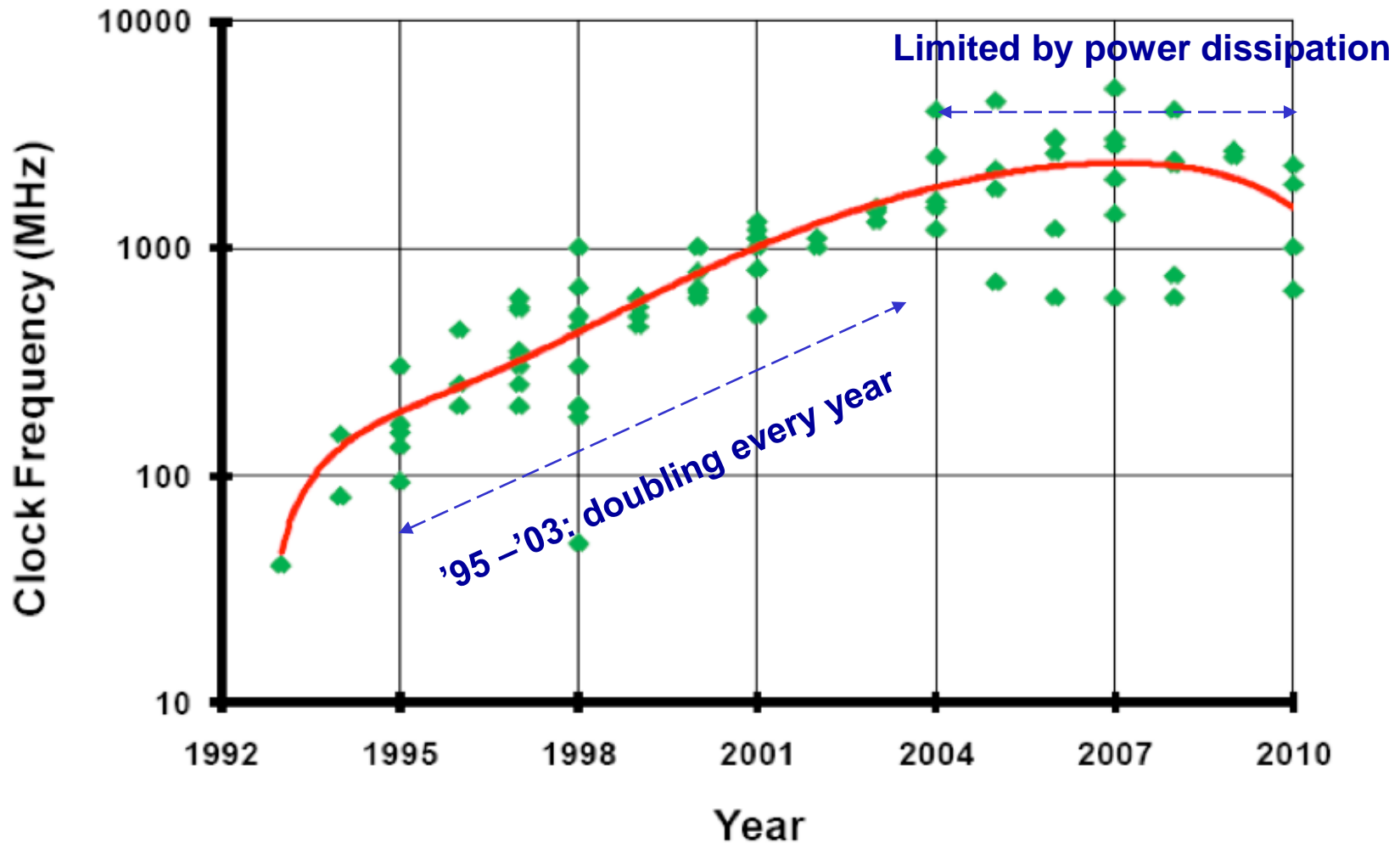
- Actual growth has been a doubling every 18-24 months

Technology Directions: SIA Roadmap

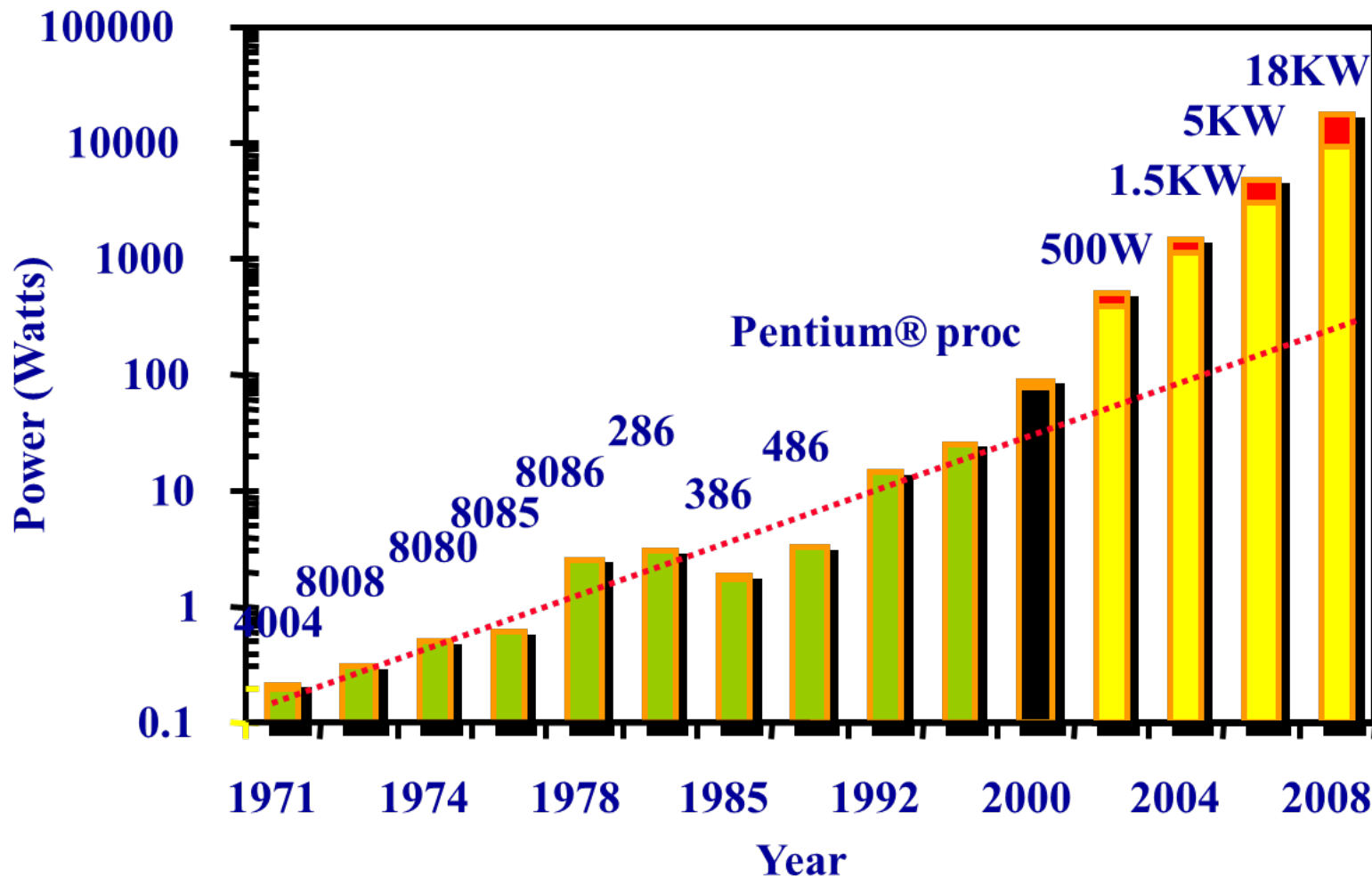
| Year | 1999 | 2002 | 2005 | 2008 | 2011 | 2014 |
|------------------------------|-------|------|------|------|-------|-------|
| Feature size (nm) | 180 | 130 | 100 | 70 | 50 | 35 |
| Logic trans/cm ² | 6.2M | 18M | 39M | 84M | 180M | 390M |
| Cost/trans (mc) | 1.735 | .580 | .255 | .110 | .049 | .022 |
| #pads/chip | 1867 | 2553 | 3492 | 4776 | 6532 | 8935 |
| Clock (MHz) | 1250 | 2100 | 3500 | 6000 | 10000 | 16900 |
| Chip size (mm ²) | 340 | 430 | 520 | 620 | 750 | 900 |
| Wiring levels | 6-7 | 7 | 7-8 | 8-9 | 9 | 10 |
| Power supply (V) | 1.8 | 1.5 | 1.2 | 0.9 | 0.6 | 0.5 |
| High-perf pow (W) | 90 | 130 | 160 | 170 | 175 | 183 |

- Roadmap has become a self-fulfilling prophecy!

Microprocessor Clock Frequency

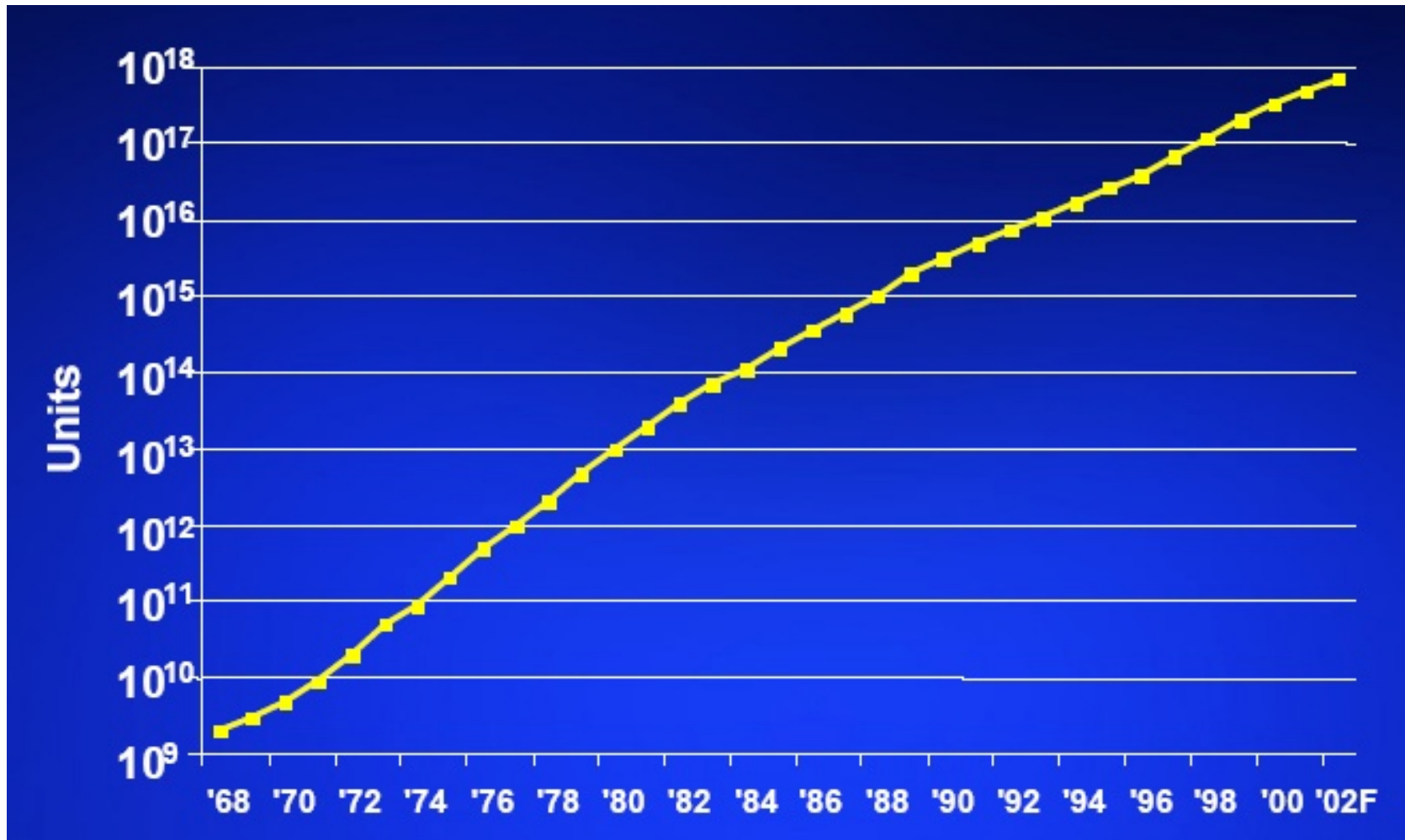


Microprocessor Power Projection 2000



- Increasing processing speed thru clock rate is power prohibitive
- Solution today is use of parallelism (#processors, #threads)

Transistors shipped per year



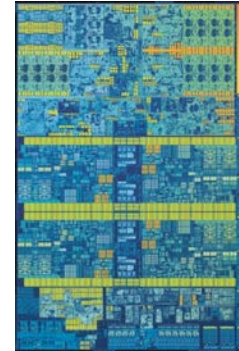
Source: Dataquest/Intel, 8/02

Decades of Progress

Intel 4004 Processor
(1978)

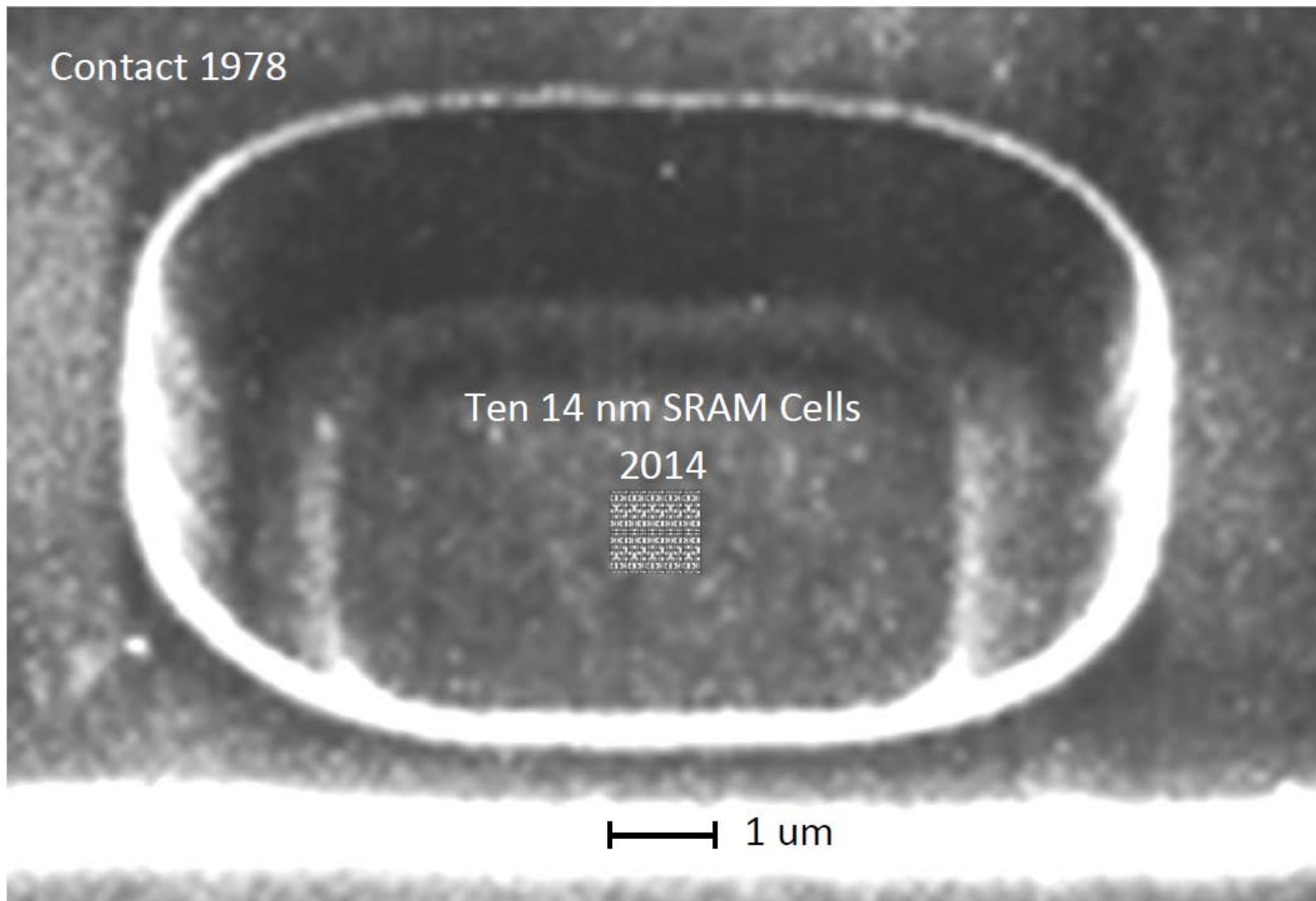


6th Generation Intel Core Processor (2015)



| Processor | | 4004 to 14nm |
|------------------------------|---|--------------|
| Wafer Size | ↑ | 36x area |
| Technology Linewidth | ↓ | 700x |
| Performance | ↑ | 3,500x |
| Price per Transistor | ↓ | 60,000x |
| Transistor Energy Efficiency | ↑ | 90,000x |

What does 700x Scaling Look Like?



Not only Microprocessors...



Smart
Phone



Ethernet router



Video games



Wireless
basestation

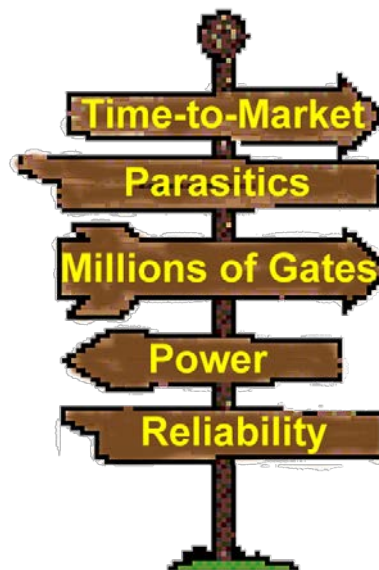


iPod

Digital Design Challenges

“Microscopic Problems”

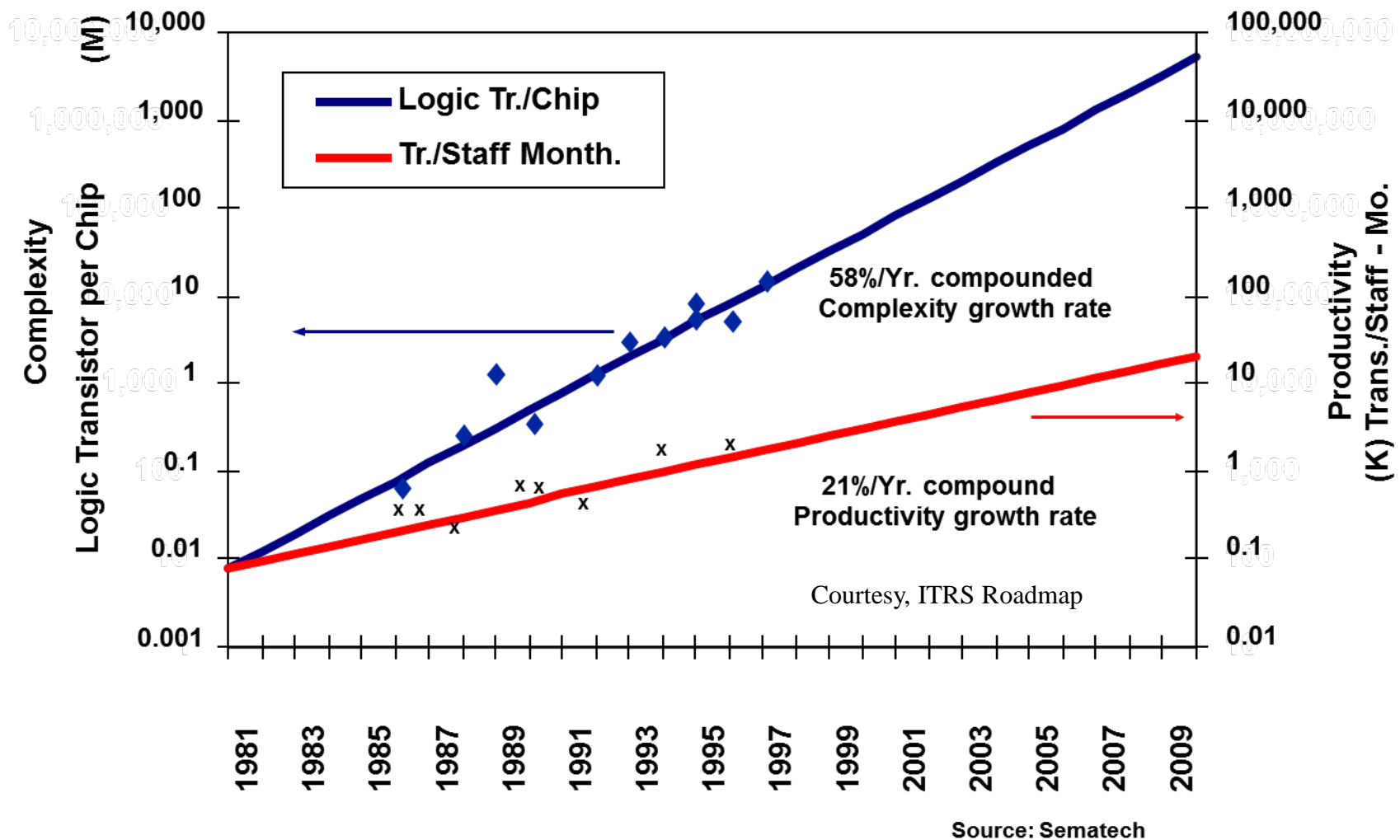
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.



“Macroscopic Issues”

- Time-to-Market
- Chip area
- Yield
- Design Cost
- CAD tools
- Reuse & IP: Portability

Productivity Trends



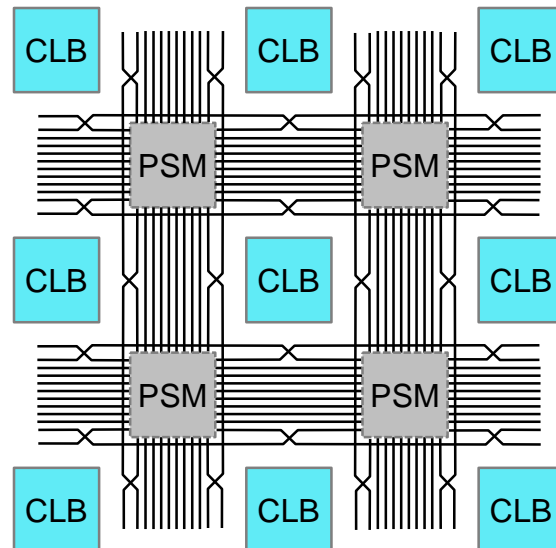
- Today's high-end digital chips can require 50 person-years development

Digital Implementation Options

- **ASIC – Application Specific Integrated Circuit**
 - Chip designed to do a specific dedicated hardware function
 - Synthesis tools place & route gates, memories, alu's, specialized IP (e.g. comm. interfaces, digital filters)
 - Greatest performance, least flexibility
- **Programmable Processors**
 - Microprocessors, DSPs etc.
 - Function determined by software
 - Greatest flexibility, least performance
- **Programmable Logic Device (PLD)**
 - Fixed architecture with programmable hardware functions & interconnect
 - Programmed using fusible links, on-chip RAM, Flash etc.
 - Synthesis tools generate programming sequence
 - Trade-off in performance & flexibility

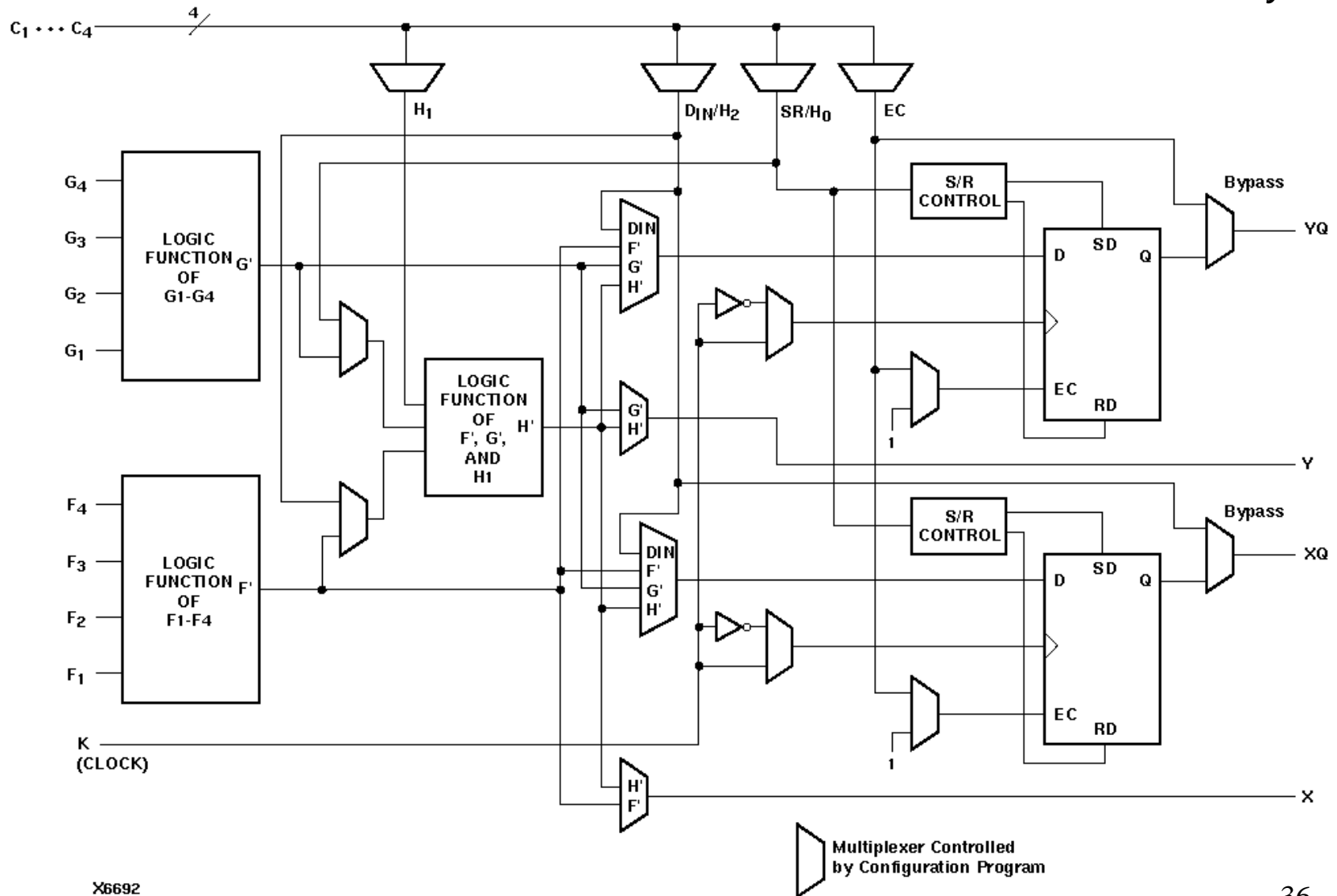
Field Programmable Gate Array (FPGA)

- Most powerful & flexible of today's PLD's
- All function is controlled by on-chip (re)writable RAM
 - Can be configured “in the field”
 - Fast configuration time
 - Easily re-configured (bug fixes, upgrades etc)
- Basic Architecture:
 - Array of Configurable Logic Blocks (CLBs) *surrounded by*
 - Programmable Switch Matrix (PSM)

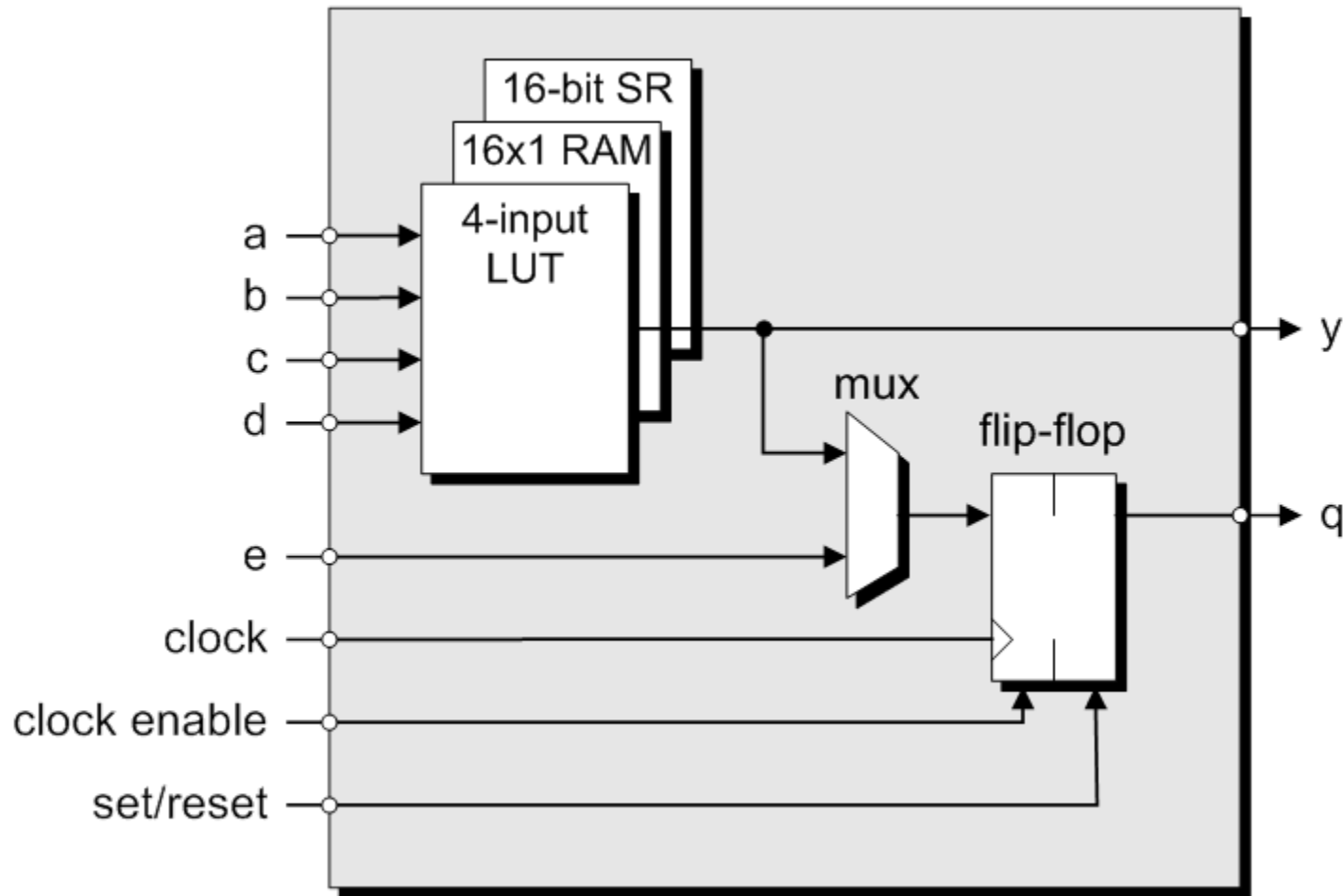


Xilinx XC 4000 Configurable Logic Block

courtesy Xilinx

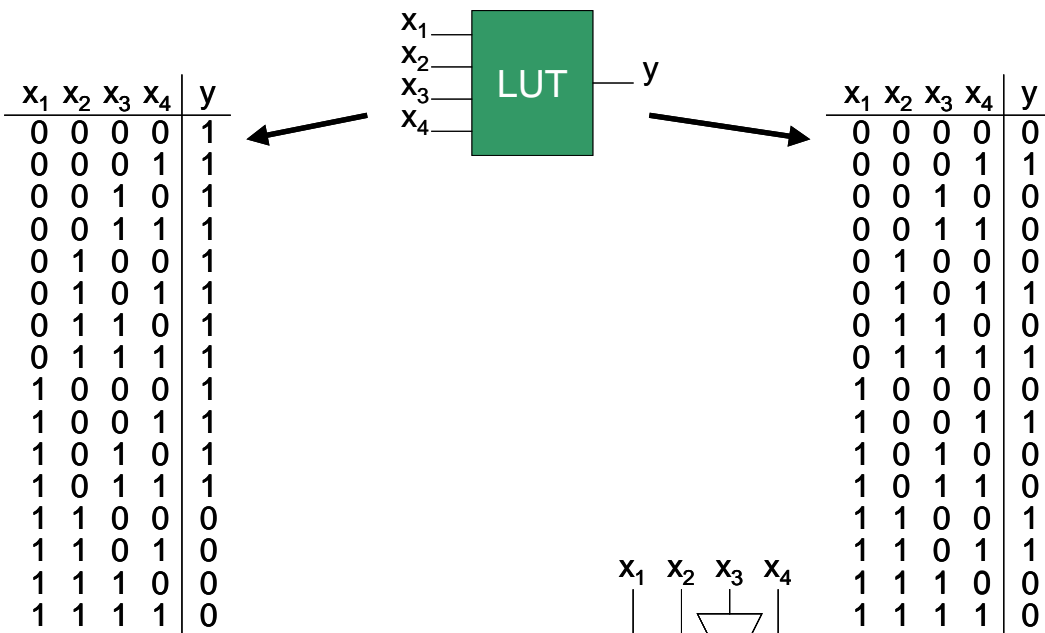


Simplified View of Xilinx Logic Cell

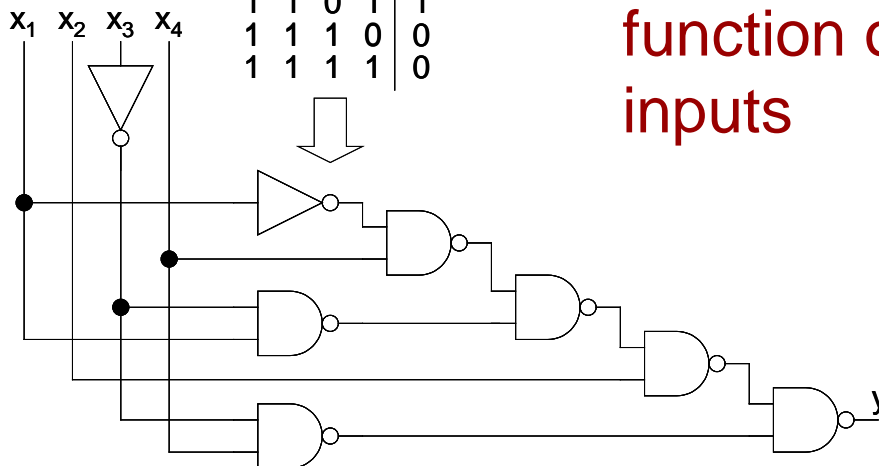
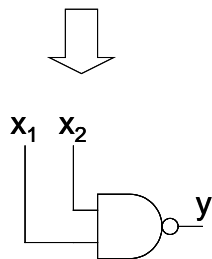


- 8 Logic Cells/Configurable Logic Block

Simplified View of Xilinx Logic Cell



- Look-Up tables are primary elements for logic implementation
- Each LUT can implement any function of 4 inputs



Configuring an FPGA

- Powerful software tools map logic structure on to CLB and PSM resources
- Configuration “code” downloaded to on-chip SRAM
 - CLB look-up tables
 - Extra RAM controls CLB multiplexers
 - Horizontal & vertical routing resources can be cross-connected through switches controlled by SRAM
- Programmable I/O blocks provide
 - CMOS, TTL, LVDS etc.
 - Tri-state, in, out bidirectional
 - Controlled rise/fall times
 - Controlled impedance
 - All configured via on-chip SRAM

FPGA Design Process (1)

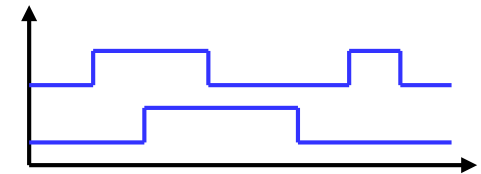
Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds.....

Specification

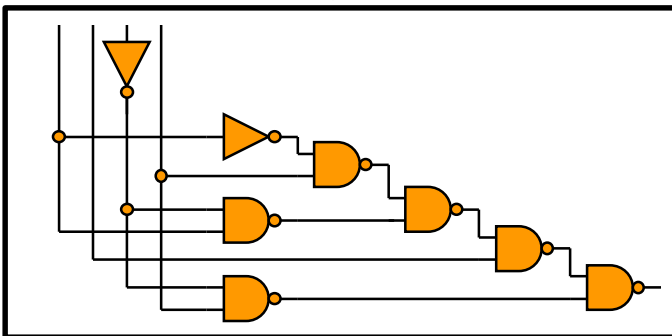
Model in VHDL

```
entity RC5_core is
  port( clock, reset, encr_decr: in std_logic;
        data_input: in std_logic_vector(31 downto 0);
        data_output: out std_logic_vector(31 downto 0);
        out_full: in std_logic;
        key_input: in std_logic_vector(31 downto 0);
        key_read: out std_logic);
end RC5_core;
```

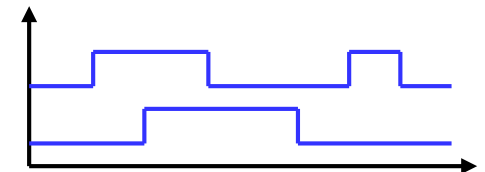
Functional simulation



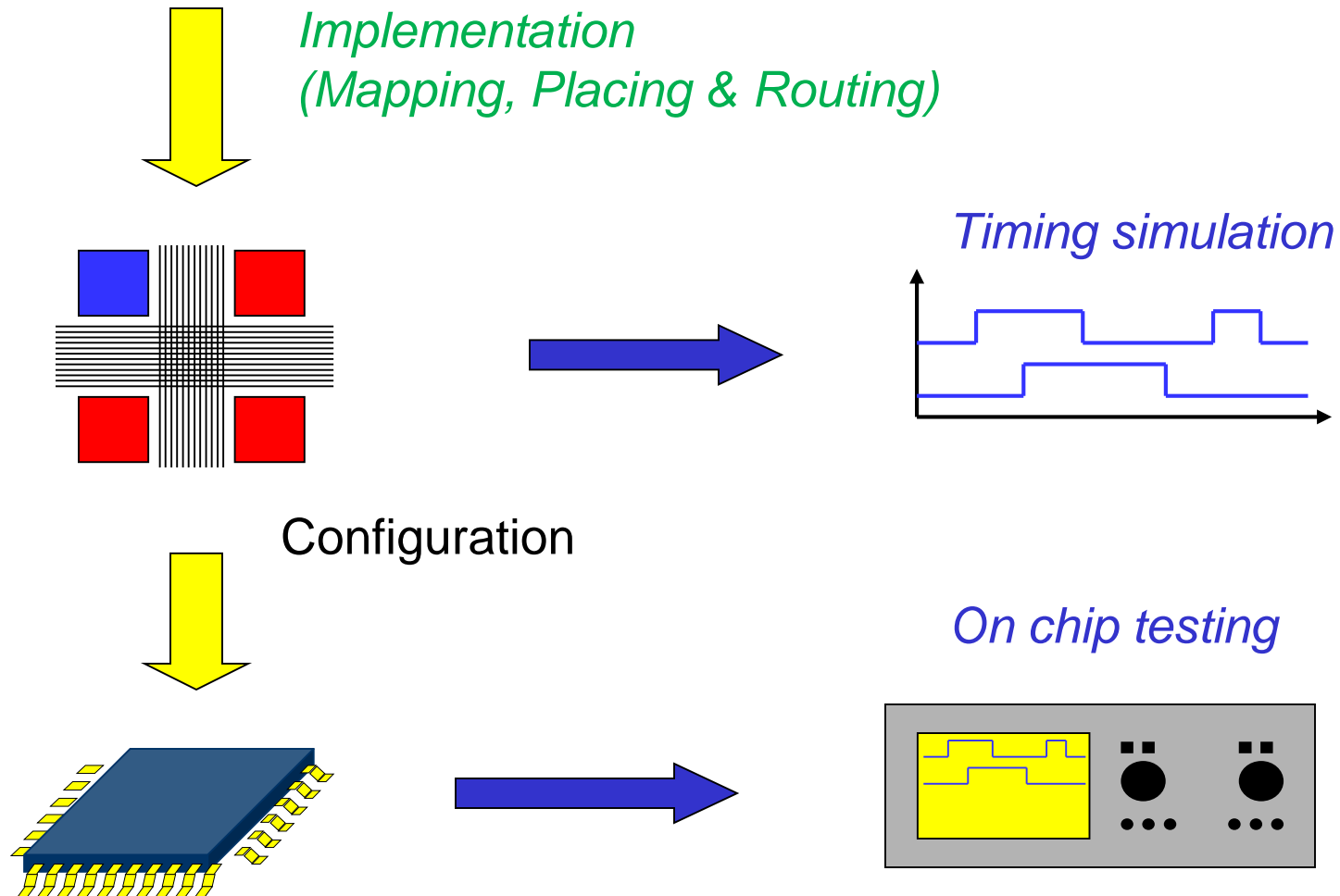
Synthesis



Post-synthesis simulation



FPGA Design Process (2)



Map Report

Design Summary

Number of errors: 0

Number of warnings: 0

Logic Utilization:

Number of Slice Flip Flops: 144 out of 4,704 3%

Number of 4 input LUTs: 173 out of 4,704 3%

Logic Distribution:

Number of occupied Slices: 145 out of 2,352 6%

Number of Slices containing only related logic: 145 out of 145 100%

Number of Slices containing unrelated logic: 0 out of 145 0%

*See NOTES below for an explanation of the effects of unrelated logic

Total Number 4 input LUTs: 210 out of 4,704 4%

Number used as logic: 173

Number used as a route-thru: 5

Number used as 16x1 RAMs: 32

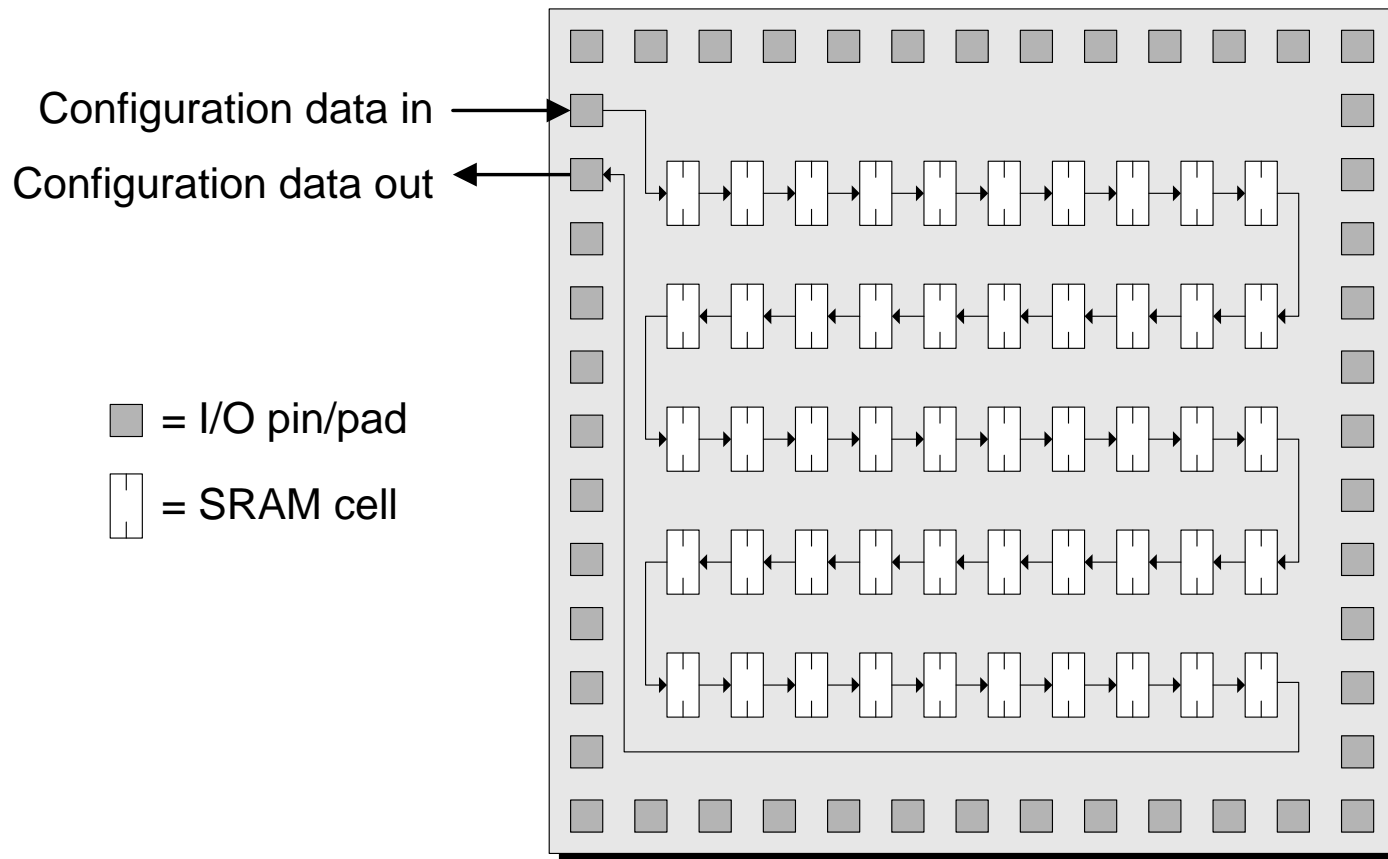
Number of bonded IOBs: 74 out of 176 42%

Number of GCLKs: 1 out of 4 25%

Number of GCLKIOBs: 1 out of 4 25%

FPGA Configuration

- Configuration generates a bit stream file (.bit extension) that is used to serially program the FPGA:



Today's FPGAs

- Also contain higher level functional blocks
 - High density data RAMs
 - Register Files
 - Multipliers
 - Standard bus interfaces
 - Phase locked loop clock generators
 - microprocessor cores
- High density and performance (e.g. Virtex 6):
 - 760,000 logic cells (~ 50,000 CLB's)
 - 38Mb block RAM
 - 2016 DSP slices (2.4 GMAC's)
 - 11 Gb/s serial I/O
 - 1200 I/O pins

FPGA vs. ASIC

ASIC

Higher Density
Higher Performance
More Power Efficient
Lower Unit Cost

FPGA

Flexibility
Field reconfiguration
Faster to market
Lower up-front cost