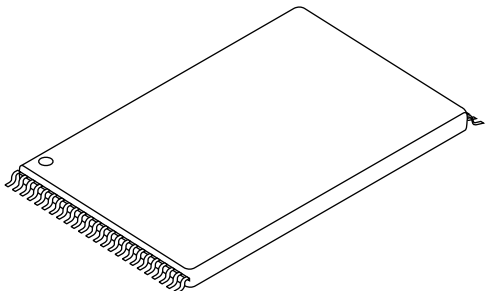
NAND Flash Memory

MT29F8G08AAAWP, MT29F16G08DAAWP, MT29F32G08FAAWP, MT29F8G08AAAC4, MT29F16G08EAAC4, MT29F32G08GAAC4, MT29F8G08AAAC6, MT29F16G08EAAC6, MT29F32G08GAAC6, MT29F64G08KAAC6

Features

- Open NAND Flash Interface (ONFI) 1.0 compliant
- Single-level cell (SLC) technology
- Organization
  - Page size: x8: 4,314 bytes (4,096 + 218 bytes)
  - Block size: 64 pages (256K + 13K bytes)
  - Plane size: 2,048 blocks
  - Device size: 8Gb: 4,096 blocks; 16Gb: 8,192 blocks; 32Gb: 16,384 blocks; 64Gb: 32,768 blocks
- READ performance
  - Random READ: 25µs
  - Sequential READ: 25ns
- WRITE performance
  - PROGRAM PAGE: 250µs (TYP)
  - BLOCK ERASE: 700µs (TYP)
- Endurance
  - 100,000 PROGRAM/ERASE cycles (4-bit ECC[1])
- Data retention: 10 years
- First block (block address 00h) guaranteed to be valid when shipped from factory[1]
- Industry-standard basic NAND Flash command set
- Advanced command set
  - PROGRAM PAGE CACHE MODE
  - PAGE READ CACHE MODE
  - One-time programmable (OTP) commands
  - Two-plane commands
  - Interleaved die operations
  - READ UNIQUE ID (contact factory)
- Operation status byte provides a software method of detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/busy# (R/B#) signal provides a hardware method of detecting PROGRAM or ERASE cycle completion
- WP# signal: entire device hardware write protect
- RESET required after power-up
- INTERNAL DATA MOVE operations supported within the plane from which data is read

Figure 1: 48-Pin TSOP Type 1



Options

- Density[2]
  - 8Gb, 16Gb, 32Gb, 64Gb
- Device width: x8
- Configuration:

	# of die	# of CE#	# of R/B#	I/O
TSOP/LGA	1	1	1	Common
TSOP	2	2	2	Common
TSOP	4	2	2	Common
LGA	2	2	2	Separate
LGA	4	2	2	Separate
LGA	8	4	4	Separate

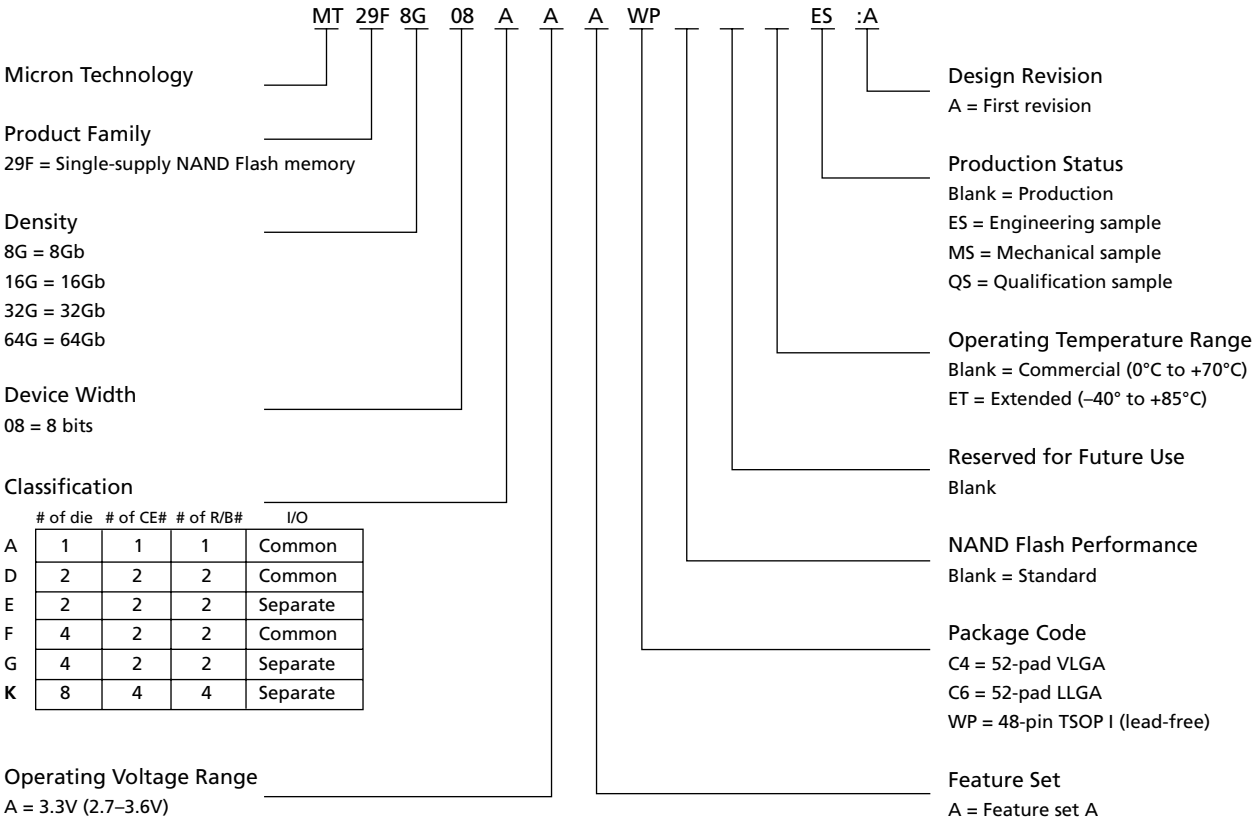
- VCC: 2.7–3.6V
- Package:
  - 48 TSOP type I (lead-free plating)
  - 52-pad LGA
- Operating temperature:
  - Commercial temperature (0°C to 70°C)
  - Extended temperature (–40°C to +85°C)

Notes: 1. For details, see “Error Management” on page 90.
2. For part numbering and markings, see Figure 2 on page 2.

Part Numbering Information

Micron NAND Flash devices are available in several different configurations and densities (see Figure 2).

Figure 2: Part Number Chart



	# of die	# of CE#	# of R/B#	I/O
A	1	1	1	Common
D	2	2	2	Common
E	2	2	2	Separate
F	4	2	2	Common
G	4	2	2	Separate
K	8	4	4	Separate

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part number is offered and valid by using the Micron Parametric Part Search Web site at www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

NAND Flash technology provides a cost-effective solution for applications requiring high-density, solid-state storage. The MT29F8G is an 8Gb NAND Flash memory device. The MT29F16 is a two-die stack that operates as two independent 8Gb devices. The MT29F32G is a four-die stack that operates as two independent 16Gb devices, providing a total storage capacity of 32Gb in a single, space-saving package. MT29F64G is an eight-die stack that operates as four independent 16Gb devices, providing a total storage capacity of 64Gb in a single, space-saving package. Micron® NAND Flash devices include standard NAND Flash features as well as new features designed to enhance system-level performance.

Micron NAND Flash devices use a highly multiplexed 8-bit bus (I/O[7:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND Flash command bus interface protocol. Two additional pins control hardware write protection (WP#) and monitor device status (R/B#).

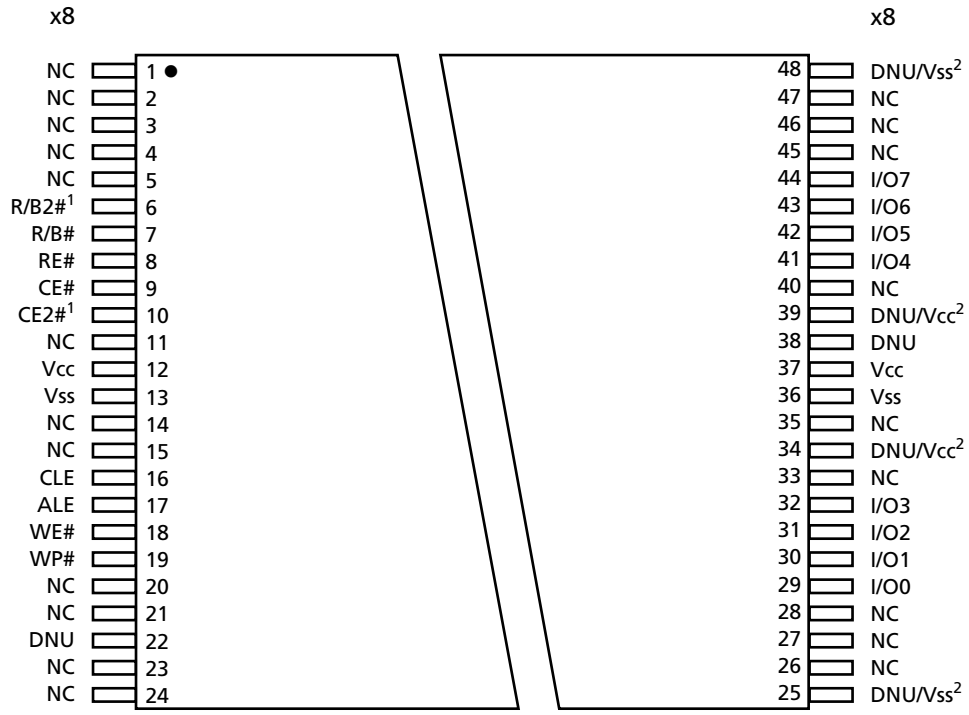
This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, allowing future upgrades to higher densities without board redesign.

The MT29F8G, MT29F16G, MT29F32G, and MT29F64G devices contain two planes per die, for a total of two or four planes. Each plane consists of 2,048 blocks. Each block is subdivided into 64 programmable pages. Each page consists of 4,314 bytes. The pages are further divided into a 4,096-byte data storage region with a separate 218-byte area. The 218-byte area is typically used for error management functions.

The contents of each page can be programmed in ^{t}PROG, and an entire block can be erased in ^{t}BERS. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. PROGRAM/ERASE endurance is specified at 100,000 cycles when using appropriate error correction code (ECC) and error management.

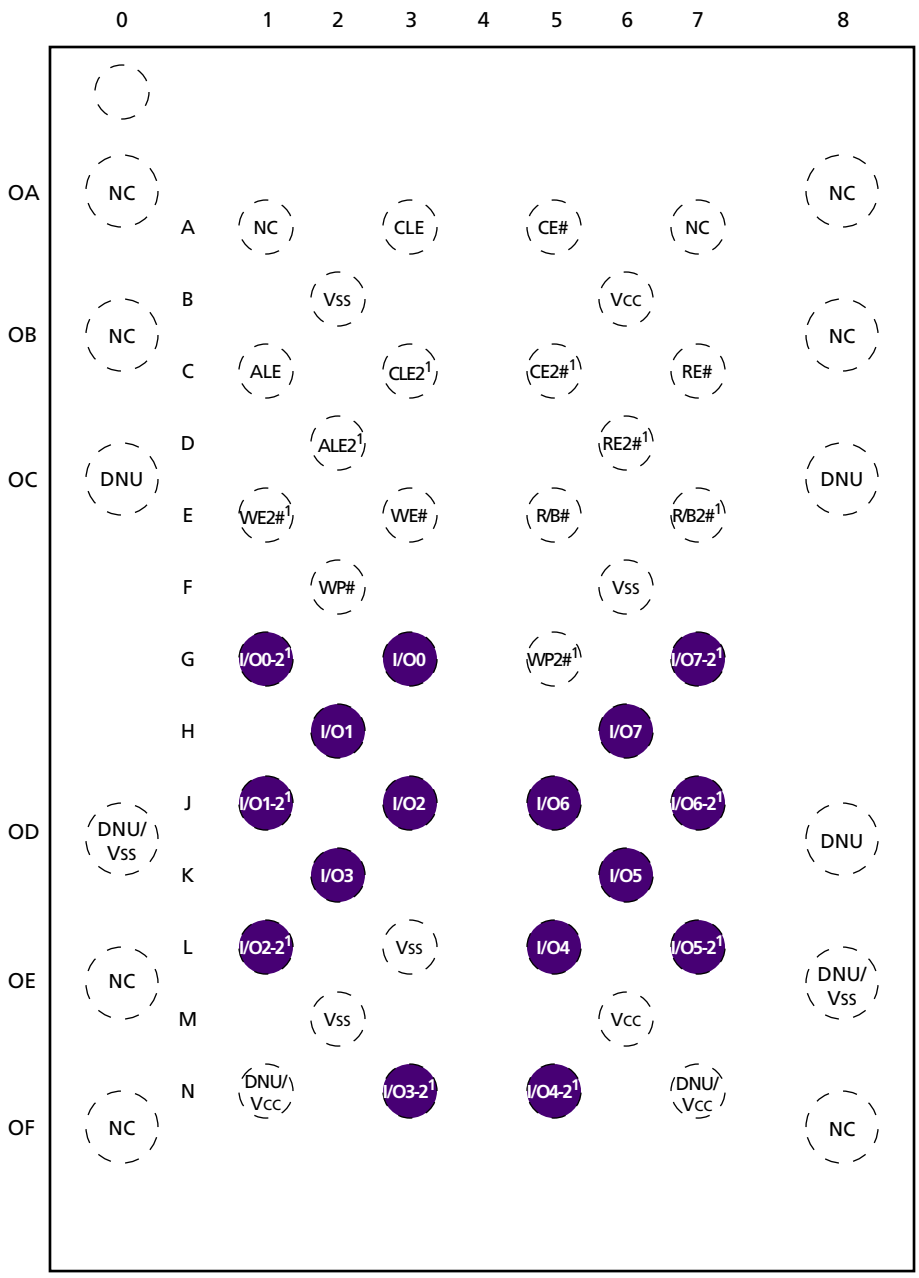
The MT29F8G, MT29F16G, MT29F32G, and MT29F64G are ONFI 1.0-compliant devices. The ONFI 1.0 specification is available at www.onfi.org.

Figure 3: Pin Assignment (Top View) 48-Pin TSOP Type 1



Notes: 1. CE2# and R/B2# on 16Gb and 32Gb devices only. These pins are NC for other configurations.
2. These Vcc and Vss pins are for compatibility with ONFI 1.0. If not supplying Vcc or Vss to these pins, do not use them.

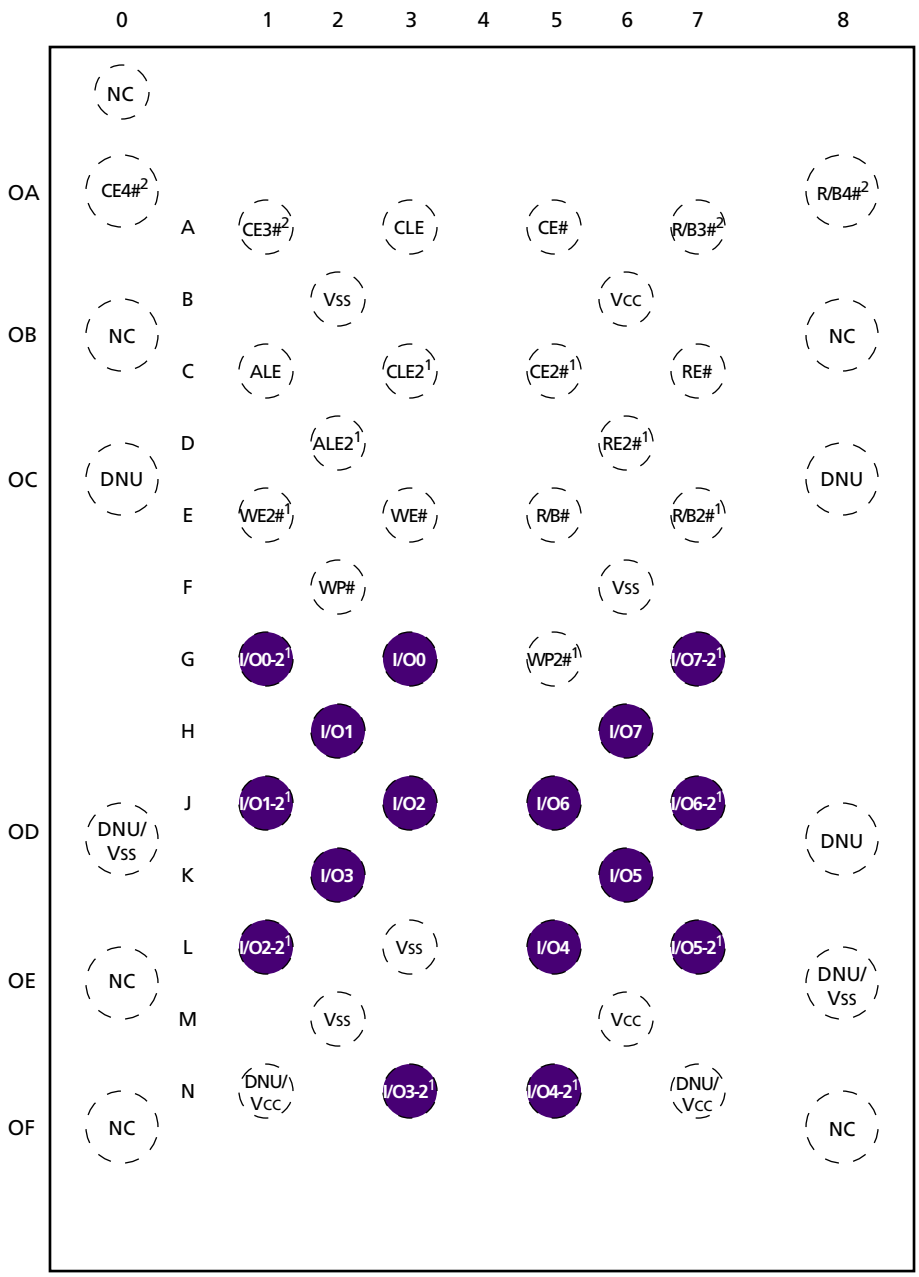
Figure 4: Pad Assignment (Top View) 52-Pad VLGA



Top View, Pads Down

Notes: 1. These signals are available only on the 16Gb and 32Gb devices. These pads are NC for other configurations.

Figure 5: Pad Assignment (Top View) 52-Pad LLGA



Top View, Pads Down

Notes: 1. These signals are available only on the 16Gb, 32Gb, and 64Gb devices. These pads are NC for other configurations.
2. These signals are available only on the 64Gb device. These pads are NC for other configurations.

Table 1: Signal Descriptions

Symbol	Type	Description
ALE, ALE2	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#, CE2#, CE3#, CE4#	Input	Chip enable: This gates transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. For the 16Gb configuration, CE# controls the first 8Gb of memory; CE2# controls the second 8Gb of memory. For the 32Gb configuration, CE# controls the first 16Gb of memory; CE2# controls the second 16Gb of memory. For the 64Gb configuration, CE# controls the first 16Gb of memory; CE2# controls the second 16Gb of memory; CE3# controls the third 16Gb of memory; CE4# controls the fourth 16Gb of memory. See "Bus Operation," starting on page 17, for additional operational details.
CLE, CLE2	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#, RE2#	Input	Read enable: This gates transfers from the NAND Flash device to the host system.
WE#, WE2#	Input	Write enable: This gates transfers from the host system to the NAND Flash device.
WP#, WP2#	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
I/O[7:0], I/O[7-2:0-2] (x8)	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#, R/B2#, R/B3#, R/B4#	Output	Ready/busy: This is an open-drain, active-LOW output, that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, R/B# returns to the high-impedance state. In the 16Gb configuration, R/B# is for the 8Gb of memory enabled by CE#; R/B2# is for the 8Gb of memory enabled by CE2#. In the 32Gb configuration, R/B# is for the 16Gb of memory enabled by CE#; R/B2# is for the 16Gb of memory enabled by CE2#. In the 64Gb configuration, R/B# is for the 16Gb of memory enabled by CE#; R/B2# is for the 16Gb of memory enabled by CE2#; R/B3# is for the 16Gb of memory enabled by CE3#; R'B4# is for the 16Gb of memory enabled by CE4#.
V_{CC}	Supply	V_{CC}: Power supply pin.
V_{SS}	Supply	V_{SS}: Ground connection.
NC	–	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	–	Do not use: DNUs must be left disconnected.

Architecture

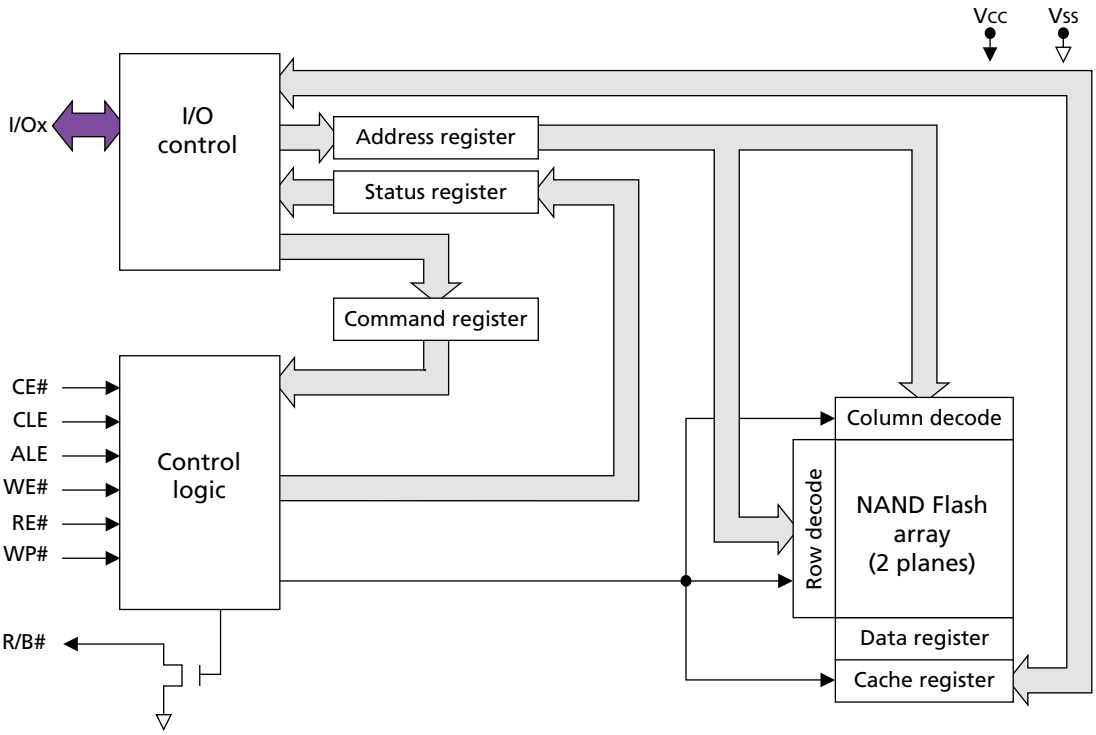
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. This provides a memory device with a low pin count. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder or a column decoder to select a row address or a column address, respectively.

The data are transferred to or from the NAND Flash memory array, byte by byte (x8), through a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data, whereas the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

The NAND Flash memory array is programmed and read in page-based operations and is erased in block-based operations. During normal page operations, the data and cache registers are tied together and act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

These devices also have a status register that reports the status of device operation.

Figure 6: NAND Flash Functional Block Diagram



Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence as shown in Table 3 on page 15. See Figure 7 on page 14 for additional memory mapping and addressing details.

Memory Mapping

Figure 7: Memory Map (x8)

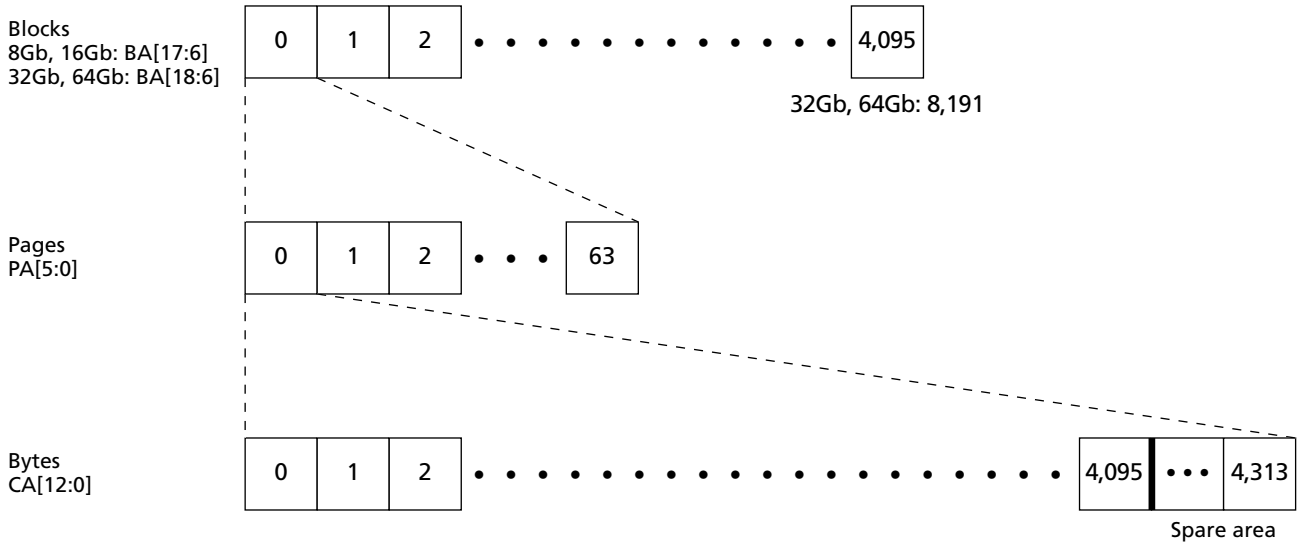


Table 2: Operational Example (x8)

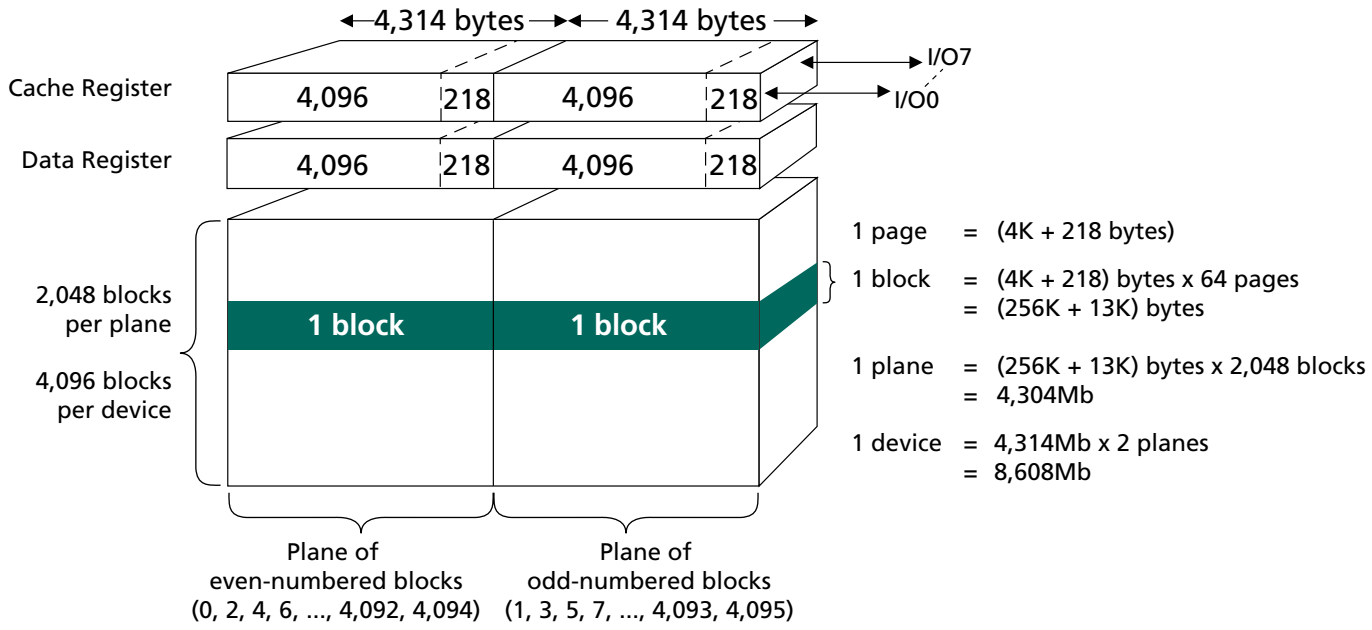
Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x00000110D9	0x00000010DA–0x0000001FFF
0	1	0x0000010000	0x00000110D9	0x00000110DA–0x0000011FFF
0	2	0x0000020000	0x00000210D9	0x00000210DA–0x0000021FFF
…	…	…	…	
4,095	62	0x03FFFE0000	0x03FFFE10D9	0x03FFFE10DA–0x03FFFE1FFF
4,095	63	0x03FFFF0000	0x03FFFF10D9	0x03FFFF10DA–0x03FFFF1FFF

Note: As shown in Table 3 on page 15, the three most significant bits in the high nibble of ADDRESS cycle 2 are not assigned; however, these 3 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.

The 13-bit column address is capable of addressing from 0 to 8,191 bytes, however, only bytes 0 through 4,313 are valid. Bytes 4,314 through 8,191 of each page are "out of bounds," do not exist in the device, and cannot be addressed.

Array Organization

Figure 8: Array Organization for 8Gb and 16Gb x8



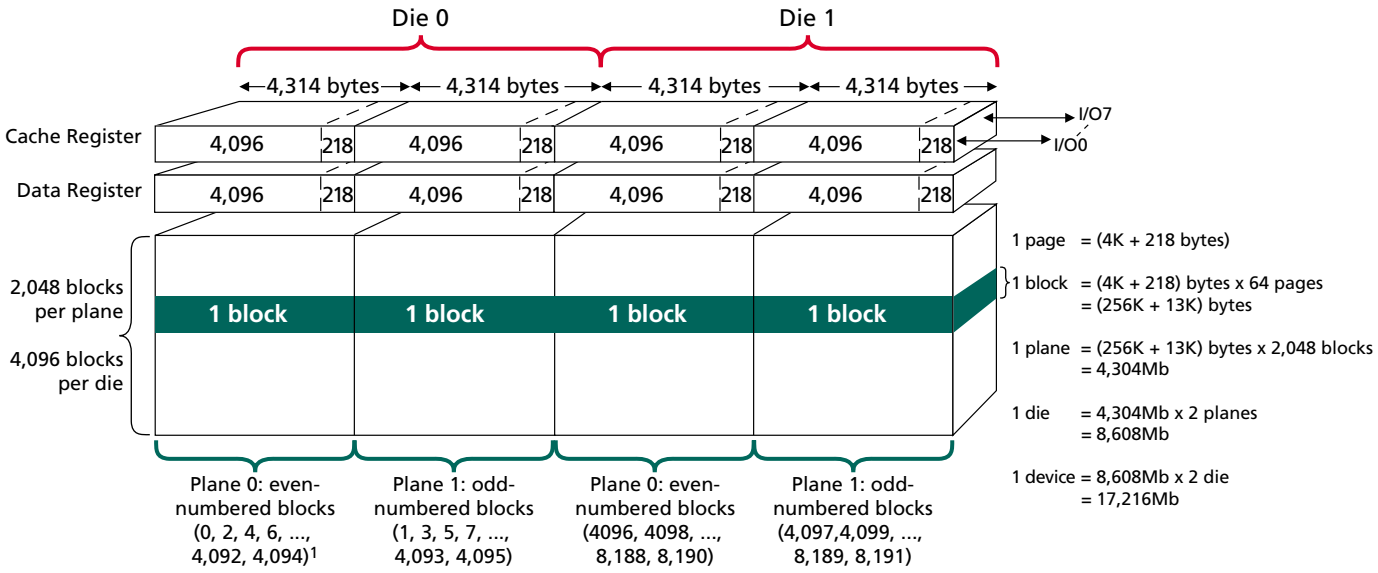
Notes: 1. For the 16Gb MT29F16G08D, the 8Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 3: Array Addressing: 8Gb and 16Gb x8

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7	BA6[3]	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes: 1. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
2. Column address 4,313 (10D9h) is the maximum valid column address.
3. Plane select bit:
0 = plane of even-numbered blocks
1 = plane of odd-numbered blocks

Figure 9: Array Organization for 32Gb and 64Gb x8



Notes: 1. Die 0, Plane 0: BA18 = 0; BA6 = 0
Die 0, Plane 1: BA18 = 0; BA6 = 1
Die 1, Plane 0: BA18 = 1; BA6 = 0
Die 1, Plane 1: BA18 = 1; BA6 = 1
2. For the 32Gb MT29F32G08F and MT29F32G08G devices, the 16Gb array organization shown here applies to each chip enable (CE# and CE2#).
3. For the 64Gb MT29F64G08K device, the 16Gb array organization shown here applies to each chip enable (CE#, CE2#, CE3#, and CE4#).

Table 4: Array Addressing: 32Gb and 64Gb x8

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	CA12	CA11	CA10	CA9	CA8
Third	BA7	BA6[3]	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	BA18[4]	BA17	BA16

Notes: 1. CAx = column address; PAx = page address; BAx = block address.
2. Column address 4,313 (10D9h) is the maximum valid column address.
3. Plane select bit:
0 = plane of even-numbered blocks
1 = plane of odd-numbered blocks
4. Die select bit:
0 = 0–8Gb
1 = 8Gb–16Gb.

Bus Operation

The bus on the MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins, I/O[7:0]. The 16Gb and 32Gb LGA packaged devices each have two independent data I/O and command pads. These are I/O[7:0], CE#, WE#, RE#, CLE, ALE, WP#, and I/O[7-2:0-2], CE2#, WE2#, RE2#, CLE2, ALE2, WP2#. This provides independent data I/O, address, and command control for each half of a 16Gb or 32Gb device.

The 64Gb LGA packaged device has two independent data I/O and command pads. These are I/O[7:0], CE#, CE3#, WE#, RE#, CLE, ALE, WP#, and I/O[7-2:0-2], CE2#, CE4#, WE2#, RE2#, CLE2, ALE2, WP2#. This provides independent data I/O, address, and command control for each 16Gb portion of the 64Gb device.

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control NAND Flash device READ and WRITE operations. On the 16Gb, CE# and CE2# each control independent 8Gb arrays. On the 32Gb, CE# and CE2# each control independent 16Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#. On the 64Gb, CE#, CE2#, CE3#, and CE4# each control independent 16Gb arrays. CE2#, CE3#, and CE4# function the same as CE# for their own arrays; all operations described for CE# also apply to CE2#, CE3#, and CE4#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the Flash memory will accept command, address, and data information.

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 77 on page 102 and Figure 85 on page 109 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a COMMAND cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- the device is not busy.

As exceptions, the device accepts the READ STATUS, TWO-PLANE/MULTIPLE-DIE READ STATUS, and RESET commands when busy. Commands are transferred to the command register on the rising edge of WE# (see Figure 69 on page 97). Commands are input on I/O[7:0].

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH.

Addresses are input on I/O[7:0] only. Bits not part of the address space must be LOW.

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements. See Tables 6–7, starting on page 22.

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

Data is input on I/O[7:0]. See Figure 71 on page 98 for additional data input details.

READ Operations

After a READ command is issued, data is transferred from the memory array to the data register. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. When data is available in the data register, it is clocked out of the part by RE# going LOW. See Figure 76 on page 101 for detailed timing information.

The READ STATUS (70h), or TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command or the R/B# signal can be used to determine when the device is ready.

If a controller is using a timing of 30ns or longer for ^{t}RC, use Figure 72 on page 99 for proper timing. If ^{t}RC is less than 30ns, use Figure 73 on page 99 for extended data output (EDO) timing.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically R/B# would be connected to an interrupt pin on the system controller (see Figure 10 on page 19).

On the 16Gb MT29F16G08DAA, R/B# provides a status indication for the 8Gb section enabled by CE#, and R/B2# does the same for the 8Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 8Gb section.

On the 32Gb MT29F32G08FAA, R/B# provides a status indication for the 16Gb section enabled by CE#, and R/B2# does the same for the 16Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 16Gb section.

On the 64Gb device, R/B# provides a status indication for the 16Gb section enabled by CE#; R/B2# provides a status indication for the 16Gb section enabled by CE2#; R/B3# provides a status indication for the 16Gb section enabled by CE3#; and R/B4# provides a

status indication for the 16Gb enabled by CE4#. R/B#, R/B2#, R/B3#, and R/B4# can be tied together, or they can be used separately to provide independent indications for each 16Gb section.

Rise time for the R/B# pin is determined by the combined capacitive loading of the R/B# circuit and Rp. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10 to 90 percent points on the R/B# waveform, rise time is approximately two time constants (TC).

Time Constants

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figures 11 and 12 on page 20, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp(\text{MIN}) = \frac{V_{CC}(MAX) - V_{OL}(MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

Figure 10: READY/BUSY# Open Drain

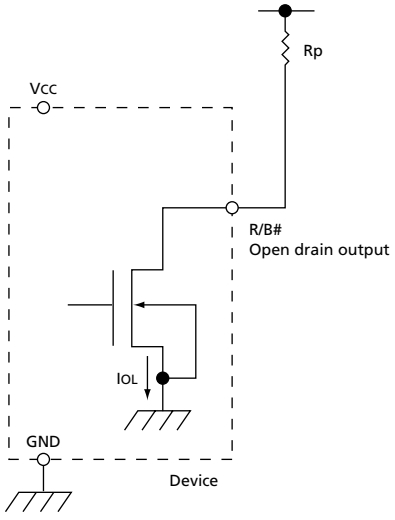
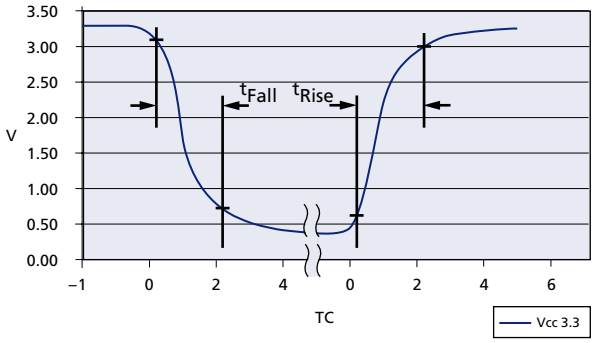


Figure 11: ^{t}Fall and ^{t}Rise



Notes: 1. ^{t}Fall and ^{t}Rise are calculated at 10 percent–90 percent points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 10ns at 3.3V.
4. See TC values in Figure 13 for approximate Rp value and TC.

Figure 12: I_{OL} vs. Rp

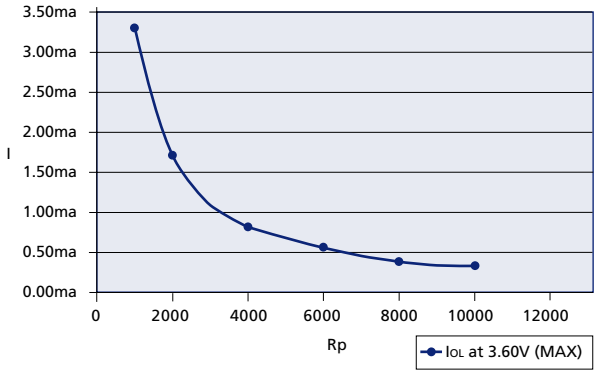


Figure 13: TC vs. Rp

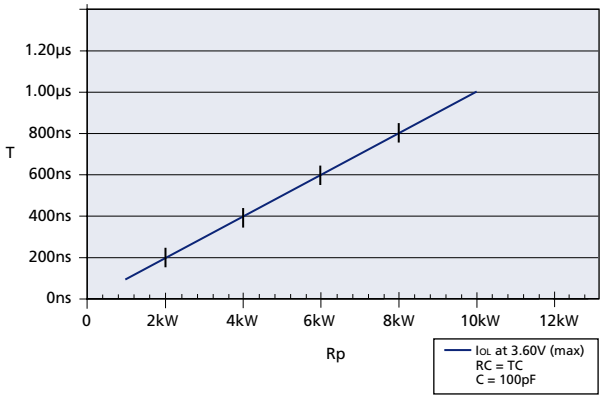


Table 5: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read mode	Command input
L	H	L		H	X		Address input
H	L	L		H	H	Write mode	Command input
L	H	L		H	H		Address input
L	L	L		H	H	Data input	
L	L	L	H		X	Sequential read and data output	
X	X	X	H	H	X	During read (busy)	
X	X	X	X	X	H	During program (busy)	
X	X	X	X	X	H	During erase (busy)	
X	X	X	X	X	L	Write protect	
X	X	H	X	X	0V/Vcc[1]	Standby	

Notes: 1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

Command Definitions

Table 6: Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	2
PAGE READ CACHE MODE SEQUENTIAL	31h	–	No	–	No	3
PAGE READ CACHE MODE RANDOM	00h	5	No	31h	No	4
PAGE READ CACHE MODE LAST	3Fh	–	No	–	No	
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	2, 5
RANDOM DATA READ	05h	2	No	E0h	No	2
READ ID	90h	1	No	–	No	
READ PARAMETER PAGE	ECh	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	2
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	2
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	2, 5
RANDOM DATA INPUT	85h	2	Yes	–	No	2
BLOCK ERASE	60h	3	No	D0h	No	2
RESET	FFh	–	No	–	Yes	2
OTP DATA PROGRAM	A0h	5	Yes	10h	No	
OTP DATA PROTECT	A5h	5	No	10h	No	
OTP DATA READ	AFh	5	No	30h	No	
SET FEATURES	EFh	1	4	–	No	
GET FEATURES	EEh	1	No	–	No	

Notes:
1. Indicates required DATA cycles between COMMAND cycle 1 and COMMAND cycle 2.
2. These commands are valid during busy when an interleaved die operation is being performed. See “Interleaved Die Operations” on page 67 for additional details.
3. The sequential PAGE READ CACHE MODE command should not be issued prior to reading the last page of a block.
4. When using the random PAGE READ CACHE MODE command, the plane select bit must be the same as the page last read.
5. Do not cross plane address boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE. See Figure 8 on page 15 for plane address boundary definitions.

Table 7: Two-Plane Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
TWO-PLANE PAGE READ	00h	5	00h	5	30h	No	
TWO-PLANE READ for INTERNAL DATA MOVE	00h	5	00h	5	35h	No	1
TWO-PLANE RANDOM DATA READ	06h	5	E0h	–	–	No	
TWO-PLANE/MULTIPLE-DIE READ STATUS	78h	3	–	–	–	Yes	2, 3
TWO-PLANE PROGRAM PAGE	80h	5	11h-80h	5	10h	No	3
TWO-PLANE PROGRAM PAGE CACHE MODE	80h	5	11h-80h	5	15h	No	3
TWO-PLANE PROGRAM for INTERNAL DATA MOVE	85h	5	11h-85h	5	10h	No	1, 3
TWO-PLANE BLOCK ERASE	60h	3	D1h-60h	3	D0h	No	3

Notes: 1. Do not cross plane address boundaries when using TWO-PLANE READ for INTERNAL DATA MOVE and TWO-PLANE PROGRAM for INTERNAL DATA MOVE. See Figure 8 on page 15 for plane address boundary definitions.
2. The TWO-PLANE/MULTIPLE-DIE READ STATUS command must be used to check status during and following interleaved die operations. See “Interleaved Die Operations” on page 67 for additional details.
3. The commands are valid during busy when interleaved die operations are being performed. See “Interleaved Die Operations” on page 67 for additional details.

READ Operations

PAGE READ 00h-30h

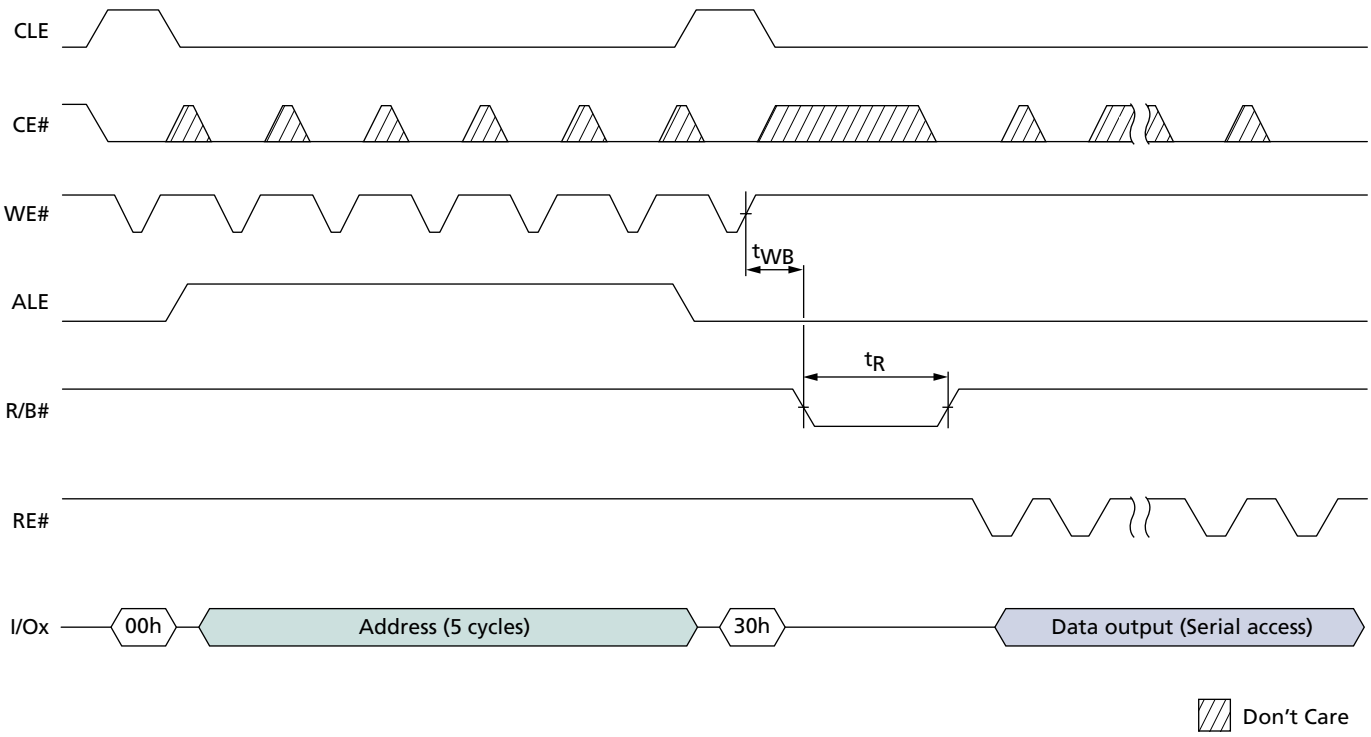
To read a page from the NAND Flash array, write the 00h command to the command register, then write 5 ADDRESS cycles, and conclude with the 30h command.

To determine the progress of the data transfer from the NAND Flash array to the data register (^{t}R), monitor the R/B# signal; or alternately, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must re-issue the READ (00h) command to receive data output from the data register. See Figure 81 on page 105 and Figure 82 on page 106 for examples. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address and going to the end of the page, read the data by repeatedly pulsing RE# at up to the maximum ^{t}RC rate (see Figure 14).

For improved READ operation performance use PAGE READ CACHE MODE operations (see pages 34 through 36).

Figure 14: PAGE READ Operation



RANDOM DATA READ 05h-E0h

The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h) sequence.

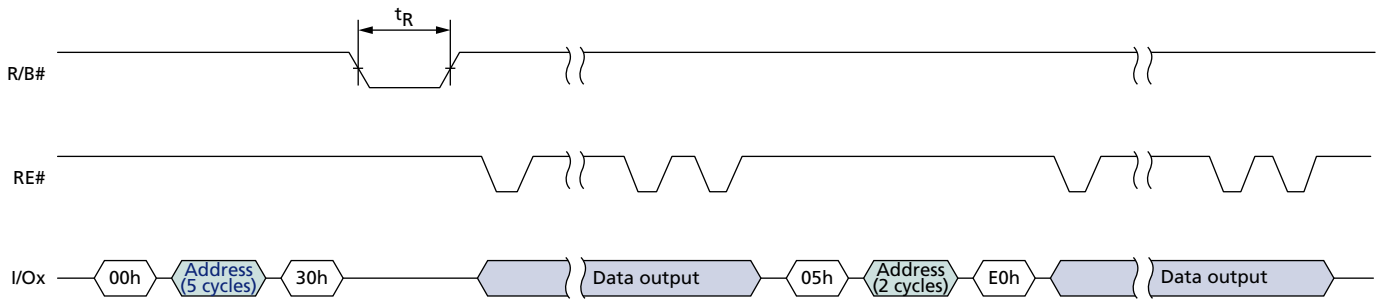
Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (2 cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 15).

The RANDOM DATA READ command changes the column address of the die last addressed.

Figure 15: RANDOM DATA READ Operation

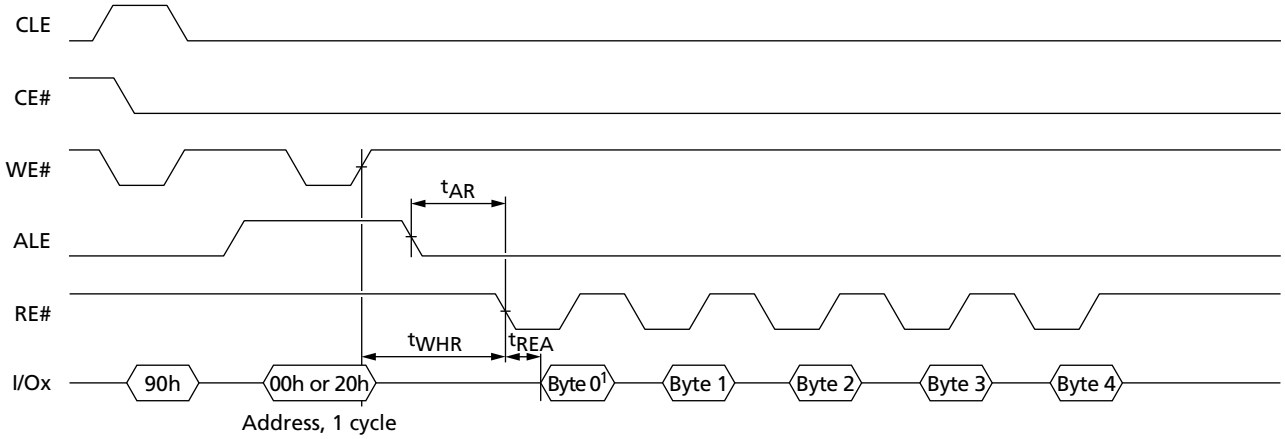


READ ID 90h

The READ ID command is used to read the 5 bytes of identifier codes programmed into the devices. The READ ID command reads a 5-byte table that includes manufacturer's ID, device configuration, and part-specific information. See Table 9 on page 27, which shows complete listings of all configuration details.

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued (see Figure 16).

Figure 16: READ ID Operation



Notes: 1. See Table 9 on page 27 for byte definitions.

Table 8: Device ID and Configuration Codes for Address 00h

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1	Device ID										
MT29F8G08AAA	8Gb, x8, 3V	1	1	0	1	0	0	1	1	D3h	
MT29F16G08[D/E]AA	16Gb, x8, 3V	1	1	0	1	0	0	1	1	D3h	2
MT29F32G08[F/G]AA	32Gb, x8, 3V	1	1	0	1	0	1	0	1	D5h	3
MT29F64G08KAA	64Gb, x8, 3V	1	1	0	1	0	1	0	1	D5h	3
Byte 2											
Number of die per CE	1							0	0	00b	
	2							0	1	01b	
Cell type	SLC					0	0			00b	
Number of simultaneously programmed pages	2			0	1					01b	
Interleaved operations between multiple die	Not supported		0							0b	
	Supported		1							1b	
Cache programming	Supported	1								1b	
Byte value	MT29F8G08	1	0	0	1	0	0	0	0	90h	
	MT29F16G08	1	0	0	1	0	0	0	0	90h	
	MT29F32G08	1	1	0	1	0	0	0	1	D1h	
	MT29F64G08	1	1	0	1	0	0	0	1	D1h	
Byte 3											
Page size	4KB							1	0	10b	
Spare area size (bytes)	218B						1			1b	
Block size (w/o spare)	256KB			1	0					10b	
Organization	x8		0							0b	
Serial access (MIN)	20ns	0				1				0xxx1b	
Byte value	MT29FxxG08	0	0	1	0	1	1	1	0	2Eh	
Byte 4											
Reserved								0	0	00b	
Planes per CE#	2					0	1			01b	
	4					1	0			10b	
Plane size	4Gb		1	1	0					110b	
Reserved		0								0b	
Byte value	MT29F8G08	0	1	1	0	0	1	0	0	64h	
	MT29F16G08	0	1	1	0	0	1	0	0	64h	
	MT29F32G08	0	1	1	0	1	0	0	0	68h	
	MT29F64G08	0	1	1	0	1	0	0	0	68h	

Notes: 1. b = binary; h = hex.
2. The MT29F16G device ID code reflects the configuration of each 8Gb section.
3. The MT29F32G and MT29F64G device ID code reflects the configuration of each 16Gb section.

Table 9: Device ID and Configuration Codes for Address 20h

Address = 20h	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
Byte 0	"O"	0	1	0	0	1	1	1	1	4Fh	1
Byte 1	"N"	0	1	0	0	1	1	1	0	4Eh	
Byte 2	"F"	0	1	0	0	0	1	1	0	46h	
Byte 3	"I"	0	1	0	0	1	0	0	1	49h	
Byte 4	Undefined	X	X	X	X	X	X	X	X	XXh	

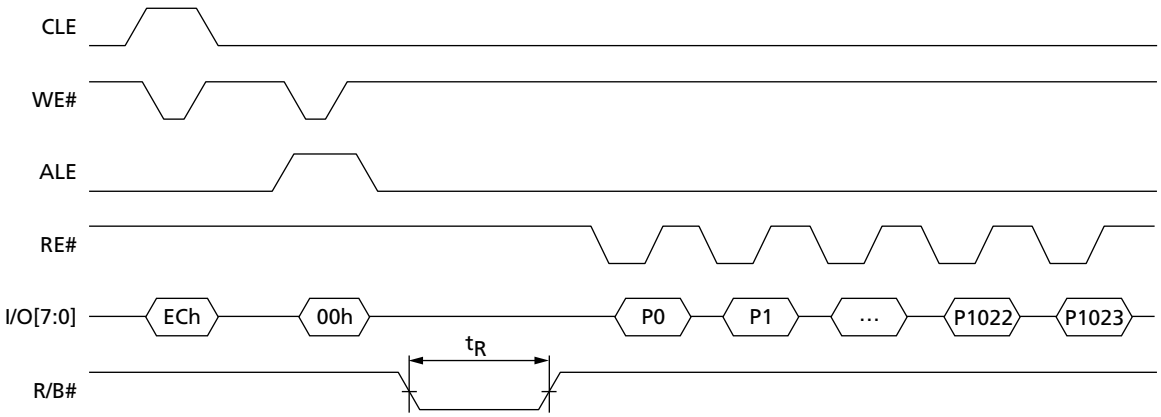
Notes: 1. h = hex.

READ PARAMETER PAGE ECh

The READ PARAMETER PAGE function retrieves the data structure that describes the device's organization, features, timings, and other behavioral parameters. The data structure is repeated at least five times. Figure 17 defines the READ PARAMETER PAGE behavior.

The RANDOM DATA READ (05h-E0h) command is permitted during data output.

Figure 17: READ PARAMETER PAGE (ECh)



Byte values for READ PARAMETER PAGE operations are provided in Table 10 on page 28. When a range of bytes is defined in any row in the table, a number of values are also associated with that row. The lowest byte defined for a row correlates with the first hex value shown in the "Values" column of that row. Unless otherwise stated, the hex values in Table 10 are converted to decimal values to determine the actual timing for any given parameter.

Table 10: Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:2]: Reserved (0) Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	02h, 00h
6–7	Features supported Bit[15:5]: Reserved (0) Bit 4: 1 = supports odd to even page copyback Bit 3: 1 = supports interleaved operations Bit 2: 1 = supports nonsequential page programming Bit 1: 1 = supports multiple logical unit (LUN) operations Bit 0: 1 = supports 16-bit data bus width	MT29F8G08AAA	18h, 00h
		MT29F16G08DAA	18h, 00h
		MT29F16G08EAA	18h, 00h
		MT29F32G08FAA	1Ah, 00h
		MT29F32G08GAA	1Ah, 00h
		MT29F64G08KAA	1Ah, 00h
8–9	Optional commands supported Bit[15:6]: Reserved (0) Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports INTERNAL DATA MOVE Bit 3: 1 = supports TWO-PLANE/MULTIPLE-DIE READ STATUS Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 0 = does not support read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE MODE command	–	1Dh, 00h
10–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters)	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F8G08AAA	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F16G08DAA	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 44h, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F16G08EAA	4Dh, 54h, 32h, 39h, 46h, 31h, 36h, 47h, 30h, 38h, 45h, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F32G08FAA	4Dh, 54h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 46h, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F32G08GAA	4Dh, 54h, 32h, 39h, 46h, 33h, 32h, 47h, 30h, 38h, 47h, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F64G08KAA	4Dh, 54h, 32h, 39h, 46h, 36h, 34h, 47h, 30h, 38h, 4Bh, 41h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 10h, 00h, 00h
84–85	Number of spare bytes per page	–	DAh, 00h
86–89	Number of data bytes per partial page	–	00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page	–	1Bh, 00h
92–95	Number of pages per block	–	40h, 00h, 00h, 00h
96–99	Number of blocks per LUN	–	00h, 10h, 00h, 00h
100	Number of LUNs per CE#	MT29F8G08AAA	01h
		MT29F16G08DAA	01h
		MT29F16G08EAA	01h
		MT29F32G08FAA	02h
		MT29F32G08GAA	02h
		MT29F64G08KAA	02h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	01h
103–104	Bad blocks maximum per LUN	–	50h, 00h
105–106	The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 105 comprises the value. Byte 106 comprises the multiplier.	–	01h, 05h

Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h
110	Number of programs per page	–	04h
111	Partial programming attributes Bit[7:5]: Reserved Bit 4: 1 = partial page layout is partial page data followed by partial page spare Bit[3:1]: Reserved Bit 0: 1 = partial page programming has constraints	–	00h
112	Number of bits ECC correctability	–	04h
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	01h
114	Interleaved operation attributes Bit[7:4]: Reserved (0) Bit 3: Address restrictions for program cache Bit 2: 1 = program cache supported Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	0Eh
115–127	Reserved (0)	–	All 00h
Electrical parameters block			
128	I/O pin capacitance	MT29F8G08AAA	05h
		MT29F16G08DAA	05h
		MT29F16G08EAA	05h
		MT29F32G08FAA	0Ah
		MT29F32G08GAA	0Ah
		MT29F64G08KAA	0Ah
129–130	Timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	1Fh, 00h
131–132	Program cache timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	1Fh, 00h
133–134	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	BCh, 02h
135–136	^{t}BERS Maximum BLOCK ERASE time (µs)	–	B8h, 0Bh
137–138	^{t}R Maximum PAGE READ time (µs)	–	19h, 00h
139–140	^{t}CCS Minimum change column setup time (ns)	–	46h, 00h
141–163	Reserved (0)	–	All 00h
Vendor block			

Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for read cache functions	–	01h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for READ UNIQUE ID	–	01h
169	Programmable I/O drive strength support Bit[7:1]: Reserved (0) Bit 1: 1 = Support for programmable I/O drive strength by ECh command Bit 0: 0 = No support for programmable I/O drive strength by B8h command	–	02h
170	Number of programmable I/O drive strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable I/O drive strength settings	–	04h
171	Programmable I/O drive strength feature address Bit[7:0] = Feature address used with programmable I/O drive strength by ECh command	–	80h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:1]: Reserved (0) Bit 0: 1 = Supports OTP mode	–	01h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	02h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:4]: Reserved (0) Bit[3:0] = Number of OTP pages	–	0Ah
179–252		–	All 00h
253	Parameter Page Revision	–	01h

Table 10: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
254–255	Integrity CRC	MT29F8G08AAA	D9h, 5Ch
		MT29F16G08DAA	04h, 7Ch
		MT29F16G08EAA	8Ah, 8Eh
		MT29F32G08FAA	2Fh, 4Ah
		MT29F32G08GAA	A1h, B8h
		MT29F64G08KAA	ABh, 93h
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
768–1,023	Value of bytes 0–255	–	See bytes 0–255
1,024–1,279	Value of bytes 0–255	–	See bytes 0–255
1,278–1,535	Value of bytes 0–255	–	See bytes 0–255
1,536–1,791	Value of bytes 0–255	–	See bytes 0–255
1,792–2,047	Value of bytes 0–255	–	See bytes 0–255
2,048–2,303	Value of bytes 0–255	–	See bytes 0–255
2,304–2,559	Value of bytes 0–255	–	See bytes 0–255
2,560–2,815	Value of bytes 0–255	–	See bytes 0–255
2,816–3,071	Value of bytes 0–255	–	See bytes 0–255
3,072–3,327	Value of bytes 0–255	–	See bytes 0–255
3,328–3,583	Value of bytes 0–255	–	See bytes 0–255
3,584–4,095	Value of bytes 0–255	–	See bytes 0–255
4,096–4,313	Reserved (FFh)	–	All FFh

READ STATUS 70h

NAND Flash devices have an 8-bit status register that the software can read during device operation. Table 11 describes the status register.

After a READ STATUS (70h) command, all READ cycles are from the status register until a new command is given. Changes in the status register are seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ cycle to see these changes.

In devices that have more than one die sharing a common CE# pin, the READ STATUS (70h) command reports the status of the die that was last addressed. During interleaved die operations, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be used to select the die that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as both die will respond until the next operation is issued.

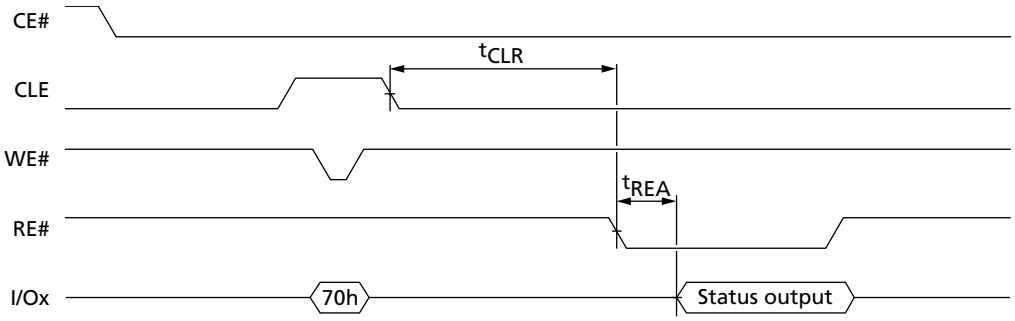
While monitoring the status register to determine when the transfer from the Flash array to the data register (^{t}R) is complete, the user must re-issue the READ (00h) command to make the change from STATUS to DATA. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

Table 11: Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0[1]	Pass/fail	Pass/fail (N)	–	–	Pass/fail	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
1	–	Pass/fail (N -1)	–	–	–	0 = Successful PROGRAM 1 = Error in PROGRAM
2	–	–	–	–	–	0
3	–	–	–	–	–	0
4	–	–	–	–	–	0
5	Ready/busy	Ready/busy[2]	Ready/busy	Ready/busy[2]	Ready/busy	0 = Busy 1 = Ready
6	Ready/busy	Ready/busy cache[3]	Ready/busy	Ready/busy cache[3]	Ready/busy	0 = Busy 1 = Ready
7[4]	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected

Notes:
1. Status register bit 0 reports a "1" if a TWO-PLANE PROGRAM or TWO-PLANE BLOCK ERASE operation fails on one or both planes. Status register bit 1 reports a "1" if a TWO-PLANE PROGRAM PAGE CACHE MODE operation fails on one or both planes. Use TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) to determine the plane on which the operation failed.
2. Status register bit 5 is "0" during the actual programming operation. If cache mode is used, this bit will be "1" when all internal operations are complete.
3. Status register bit 6 is "1" when the cache is ready to accept new data. R/B# follows bit 6 (see Figure 19 on page 36 and Figure 22 on page 39).
4. Status register bit 7 typically mirrors the status of the WP# pin. However, when the OTP PROGRAM DATA command is used, status register bit 7 returns "0" if the OTP area is protected. This bit is not modified until the next PROGRAM or ERASE command is issued.

Figure 18: Status Register Operation for READ STATUS



PAGE READ CACHE MODE Operations

Micron NAND Flash devices have a cache register that can be used to increase READ operation speed. Data can be output from the device's cache register while concurrently moving a page from the NAND Flash array to the data register.

To begin a PAGE READ CACHE MODE sequence, begin by reading a page from the NAND Flash array to the cache register using the PAGE READ (00h-30h) command (see "PAGE READ 00h-30h" on page 24). R/B# goes LOW during ^{t}R (status register bits 6 and 5 = 00). After ^{t}R (R/B# is HIGH and status register bits 6 and 5 = 11), issue either of these commands:

- PAGE READ CACHE MODE SEQUENTIAL (31h) command to begin copying the next sequential page from the NAND Flash array to the data register
- PAGE READ CACHE MODE RANDOM (00h-31h) command to begin copying the page specified in this command from the NAND Flash array to the data register.

After the PAGE READ CACHE MODE SEQUENTIAL or PAGE READ CACHE MODE RANDOM command has been issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR1 while the next page begins copying into the data register. After ^{t}DCBSYR1, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that a page is being copied from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

After outputting the desired number of bytes from the cache register, it is possible to either begin an additional PAGE READ CACHE MODE (31h or 00h-31h) operation or issue the PAGE READ CACHE MODE LAST (3Fh) command.

If an additional PAGE READ CACHE MODE (31h or 00h-31h) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR2 while the data register is copied to the cache register, then the next page begins copying into the data register. After ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10, indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

If the PAGE READ CACHE MODE LAST (3Fh) command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for ^{t}DCBSYR2 while the data register is copied into the cache register. After ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11, indicating

that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

During device busy times, ^{t}DCBSYR1 and ^{t}DCBSYR2, the only valid commands are READ STATUS (70h, 78h) and RESET (FFh). Until status register bit 5 = 1, the only valid commands during PAGE READ CACHE MODE operations are READ STATUS (70h, 78h), READ (00h), PAGE READ CACHE MODE (31h and 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

PAGE READ CACHE MODE SEQUENTIAL 31h

The PAGE READ CACHE MODE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. To issue this command, write 31h to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}DCBSYR1 or ^{t}DCBSYR2. After ^{t}DCBSYR1 or ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register by toggling RE# beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

Do not issue the 31h command after reading the last page of the block into the data register. Instead, issue the 3Fh command. Crossing block boundaries with the PAGE READ CACHE MODE SEQUENTIAL (31h) command is prohibited.

PAGE READ CACHE MODE RANDOM 00h-31h

The PAGE READ CACHE MODE RANDOM (00h-31h) command reads the specified page into the data register while the previous page is output from the cache register. To issue this command, write 00h to the command register, then write 5 address cycles to the address register. Conclude the sequence by writing 31h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for either ^{t}DCBSYR1 or ^{t}DCBSYR2. After ^{t}DCBSYR1 or ^{t}DCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 10 to indicate that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

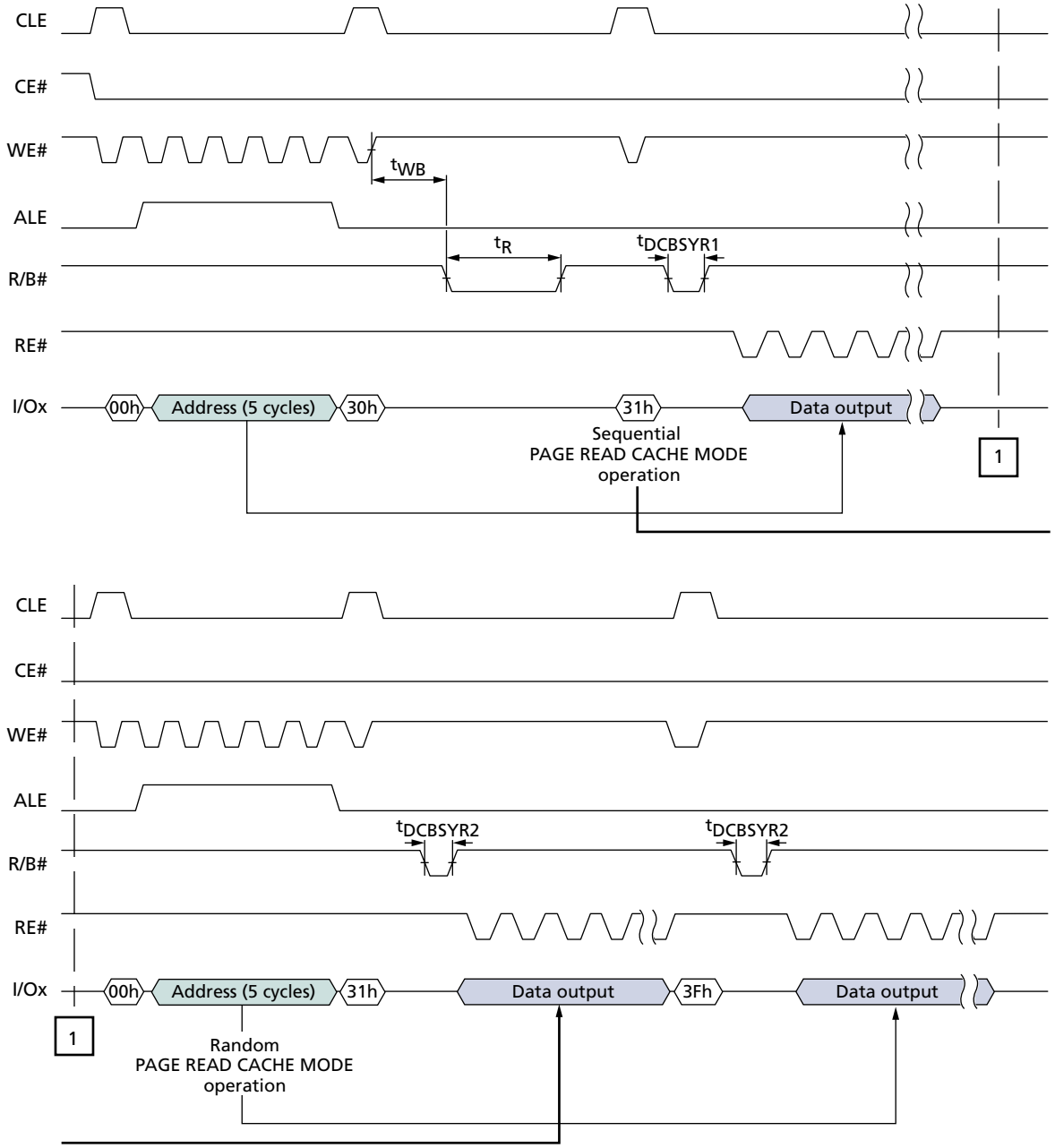
Do not issue the 00h-31h command to a different plane than the previously read page—the plane-select bit must be set to the same value. If crossing plane boundaries is required, complete the PAGE READ CACHE MODE operation using the 3Fh command, then start a PAGE READ (00h-30h) operation to the new plane.

PAGE READ CACHE MODE LAST 3Fh

The PAGE READ CACHE MODE LAST (3Fh) command copies a page from the data register to the cache register without beginning a new PAGE READ CACHE MODE operation. To issue the PAGE READ CACHE MODE LAST command, write 3Fh to the command register.

After this command is issued, R/B# goes LOW (status register bits 6 and 5 = 00) for tDCBSYR2. After tDCBSYR2, R/B# goes HIGH and status register bits 6 and 5 = 11 to indicate that the cache register is available and that the NAND Flash array is ready. At this point data can be output from the cache register, beginning at column address 0, by toggling RE#. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output by the device.

Figure 19: PAGE READ CACHE MODE Operation



PROGRAM Operations

PROGRAM PAGE 80h-10h

Micron NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, the from the least significant page address to the most significant page address (that is, 0, 1, 2, …63). Random page address programming is prohibited.

Micron SLC NAND Flash devices support partial-page programming operations. This means that any single bit can only be programmed one time before an erase is required; however, the page can be partitioned such that a maximum of four programming operations are allowed before an erase is required.

SERIAL DATA INPUT 80h

PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by 5 ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects "1s" that are not successfully written to "0s."

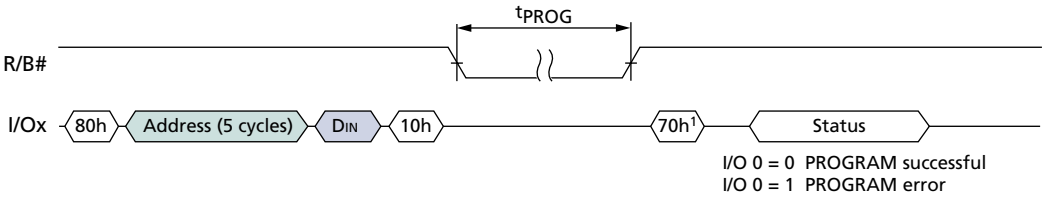
R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the programming operation.)

Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed (see Figure 20). The command register stays in read status register mode until another valid command is written to it.

RANDOM DATA INPUT 85h

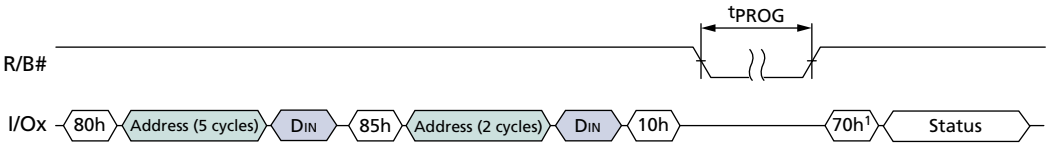
After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figure 21 on page 38 for the proper command sequence.

Figure 20: PROGRAM and READ STATUS Operation



Notes: 1. Command can be 70h or 78h.

Figure 21: RANDOM DATA INPUT



PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by 5 cycles of address, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE PROGRAM (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

The PROGRAM PAGE CACHE MODE command can cross block boundaries. If a PROGRAM PAGE CACHE MODE operation crosses die boundaries, handle as described in "Interleaved PROGRAM PAGE CACHE MODE Operations" on page 71.

RANDOM DATA INPUT commands are allowed during PROGRAM PAGE CACHE MODE operations.

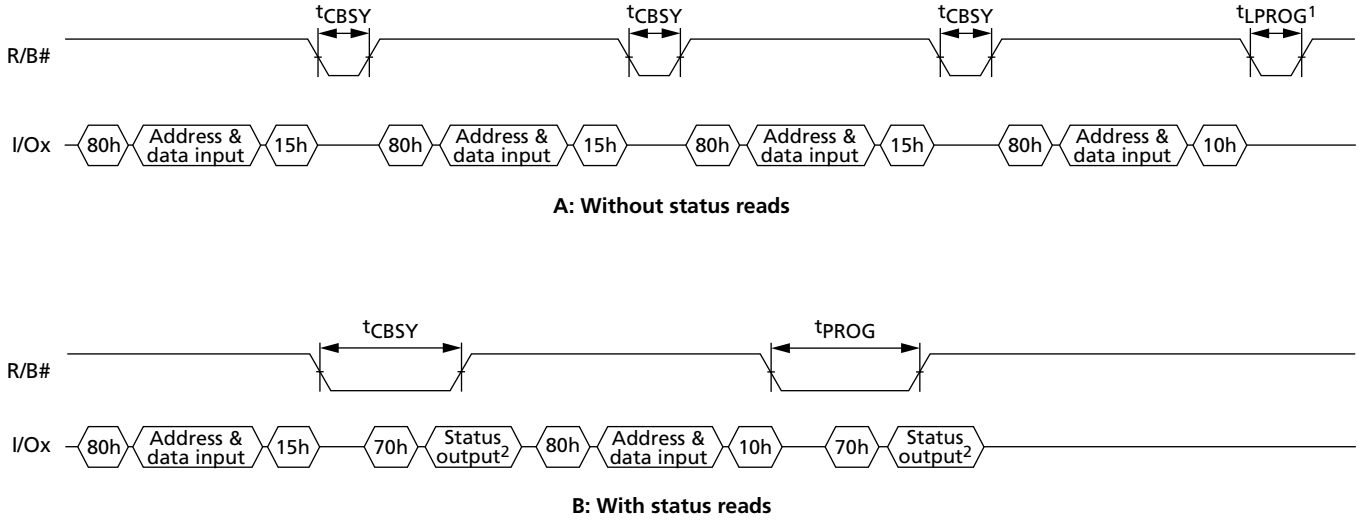
Bit 6 (cache R/B#) of the status register can be read by issuing the READ STATUS (70h or 78h) commands to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 22 on page 39).

Bit 1 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a "1" (ready state) (see Figure 22 on page 39).

Figure 22: PROGRAM PAGE CACHE MODE Example



Notes: 1. Command can be 70h or 78h. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass fail. RE# can stay LOW or pulse multiple times after a 70h or 78h command.

Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. Data moves are only supported within the plane from which data is read.

READ FOR INTERNAL DATA MOVE 00h-35h

The READ for INTERNAL DATA MOVE (00h-35h) command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First, 00h is written to the command register, then the internal source address is written (5 cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

All 5 ADDRESS cycles are required when a READ for INTERNAL DATA MOVE command is issued.

After a READ for INTERNAL DATA MOVE (00h-35h) command is issued and R/B# returns HIGH, signifying operation completion, the data transferred from the source page into the cache register may be read out by toggling RE#. Data is output sequentially from the column address originally specified with the READ FOR INTERNAL DATA MOVE (00h-35h) command. RANDOM DATA READ (05h-E0h) commands can be issued without limit after the READ FOR INTERNAL DATA MOVE command.

The memory device is now ready to accept the PROGRAM for INTERNAL DATA MOVE command. Refer to the description of this command in the following section.

PROGRAM for INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. The sequence: 85h, destination address (5 cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS command and bit 6 of the status register can be used instead of the R/B# line to determine when the write is complete. Bit 0 of the status register indicates if the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data is transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h (see Figures 23 and 24 on page 41).

Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that exceeds the minimum required ECC.

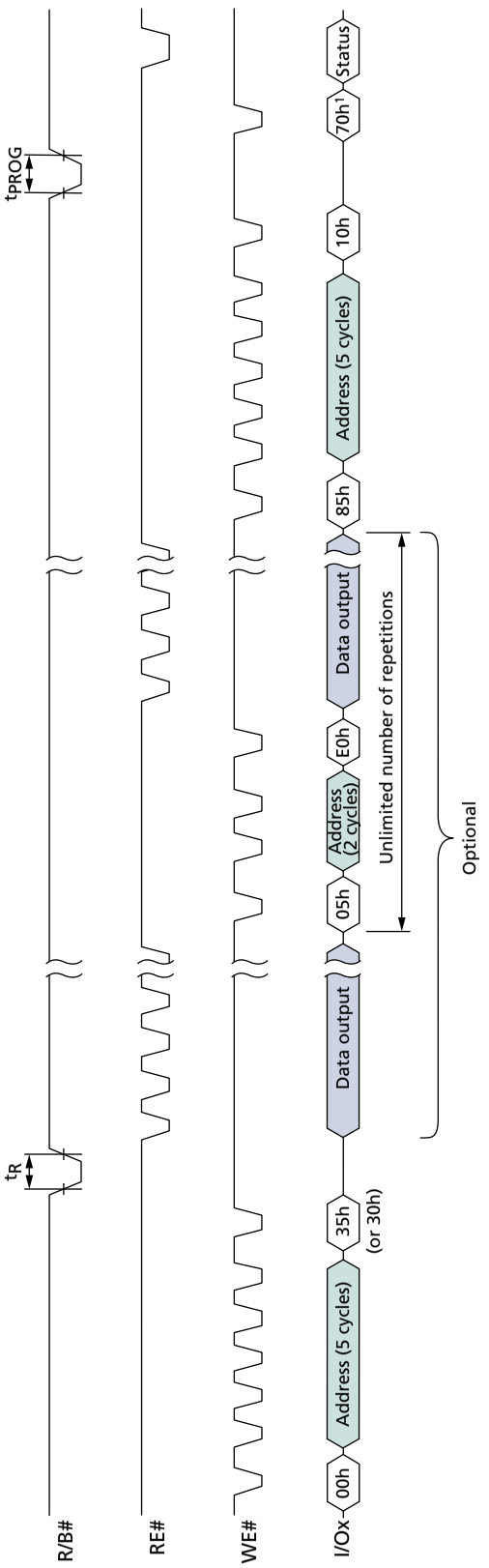


Figure 23: INTERNAL DATA MOVE

Notes: 1. Command can be 70h or 78h.

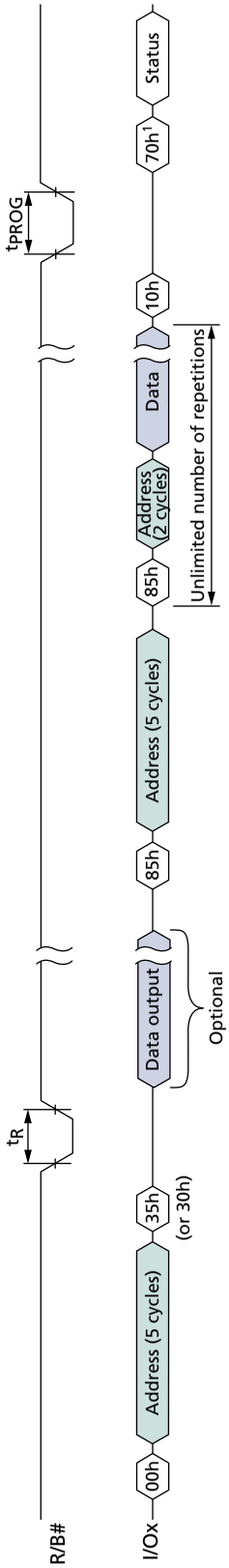


Figure 24: INTERNAL DATA MOVE with Optional Data Output and RANDOM DATA Input

Notes: 1. Command can be 70h or 78h.

BLOCK ERASE Operation

BLOCK ERASE 60h-D0h

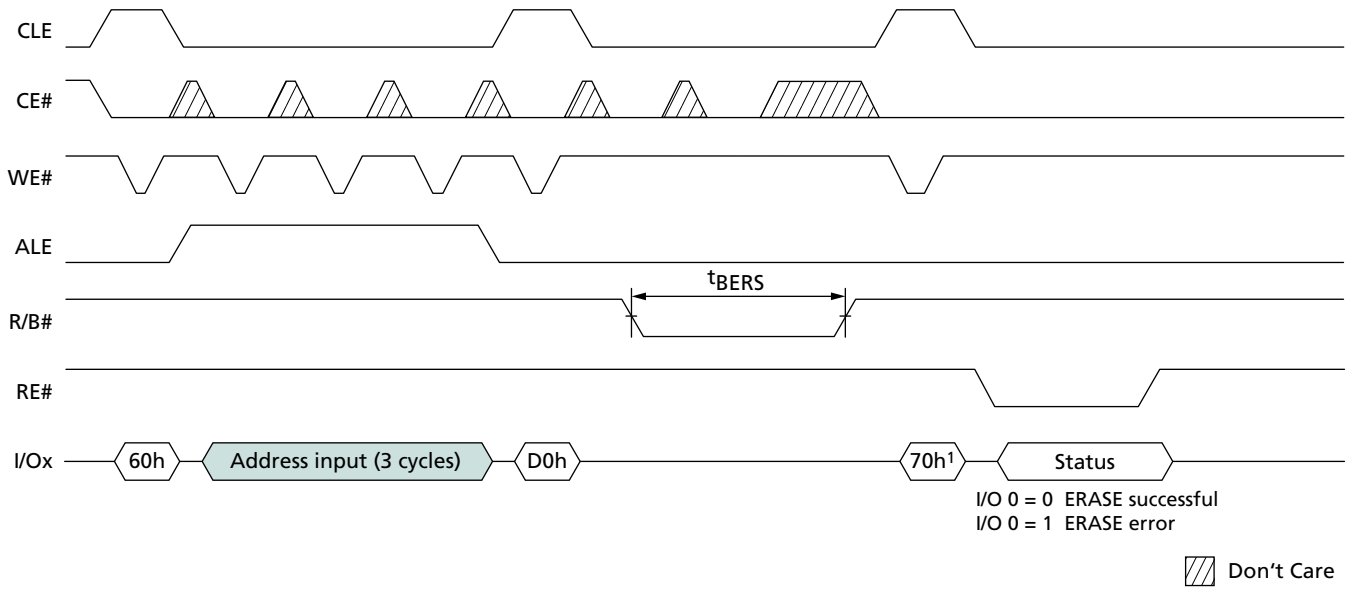
Erasing occurs at the block level. For example, the MT29F8G08AxA device has 4,096 erase blocks, organized into 64 pages per block, 4,314 bytes per page (4,096 + 218 bytes). Each block is 269K bytes (256K + 13K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 25).

The last 3 cycles of addresses of the 5-cycle addressing sequence are required for a BLOCK ERASE operation. The first 2 cycles of addresses must not be used. Although the page address bits are loaded, they are a "Don't Care" and are ignored for BLOCK ERASE operations, since these bits normally specify the page address within a block. See "Addressing" on page 13 for details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then 3 cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h and 78h) commands can be used to check the status of the error. When bit 6 is "1," the ERASE operation is complete. Bit 0 indicates a pass/fail condition where "0" is pass (see Figure 25, and Table 11 on page 33).

Figure 25: BLOCK ERASE Operation



Notes: 1. Command can be 70h or 78h.

One-Time Programmable (OTP) Area

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (4,314 bytes) of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in a non-written state (all bits are "1s"). Programming enables the user to program only "0" bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as "one-time programmable," Micron provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

OTP programming and protection are accomplished in two discrete operations. First, using the OTP DATA PROGRAM (A0h-10h) command, an OTP page is programmed entirely in one operation. Programming can occur on other pages within the OTP area in a similar manner. Second, the OTP area is permanently protected from further programming using the OTP DATA PROTECT (A5h-10h) command. The pages within the OTP area can always be read using the OTP DATA READ (AFh-30h) command, whether or not it is protected.

To determine whether or not the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and following OTP operations.

OTP DATA PROGRAM A0h-10h

The OTP DATA PROGRAM (A0h-10h) command is used to write data to the pages within the OTP area. An entire page is programmed at one time. There is no ERASE operation for the OTP pages.

OTP DATA PROGRAM enables programming into an offset of an OTP page, using the two bytes of column address (CA[12:0]). The command is compatible with the RANDOM DATA INPUT (85h) command. The OTP DATA PROGRAM command will not execute if the OTP area has been protected.

To use the OTP DATA PROGRAM command, issue the A0h command. Issue 5 ADDRESS cycles: the first 2 ADDRESS cycles are the column address, and for the remaining 3 cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Next, write from 1 to 4,314 bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW during the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only command valid during the OTP DATA PROGRAM operation. Bit 5 of the status register will reflect the state of R/B#.

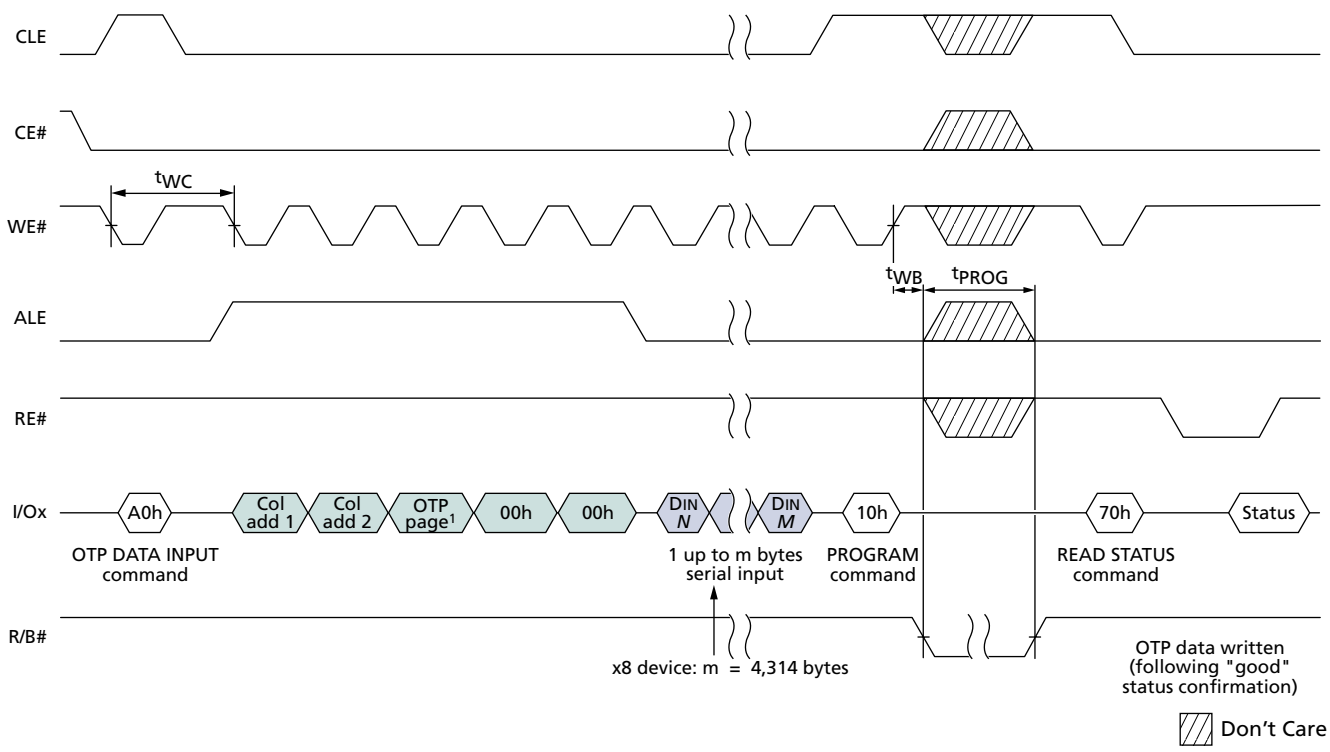
When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 11 on page 33).

It is possible to program each OTP page a maximum of one time.

The OTP DATA PROGRAM command also accepts the RANDOM DATA INPUT (85h) command (see Figure 27 on page 45).

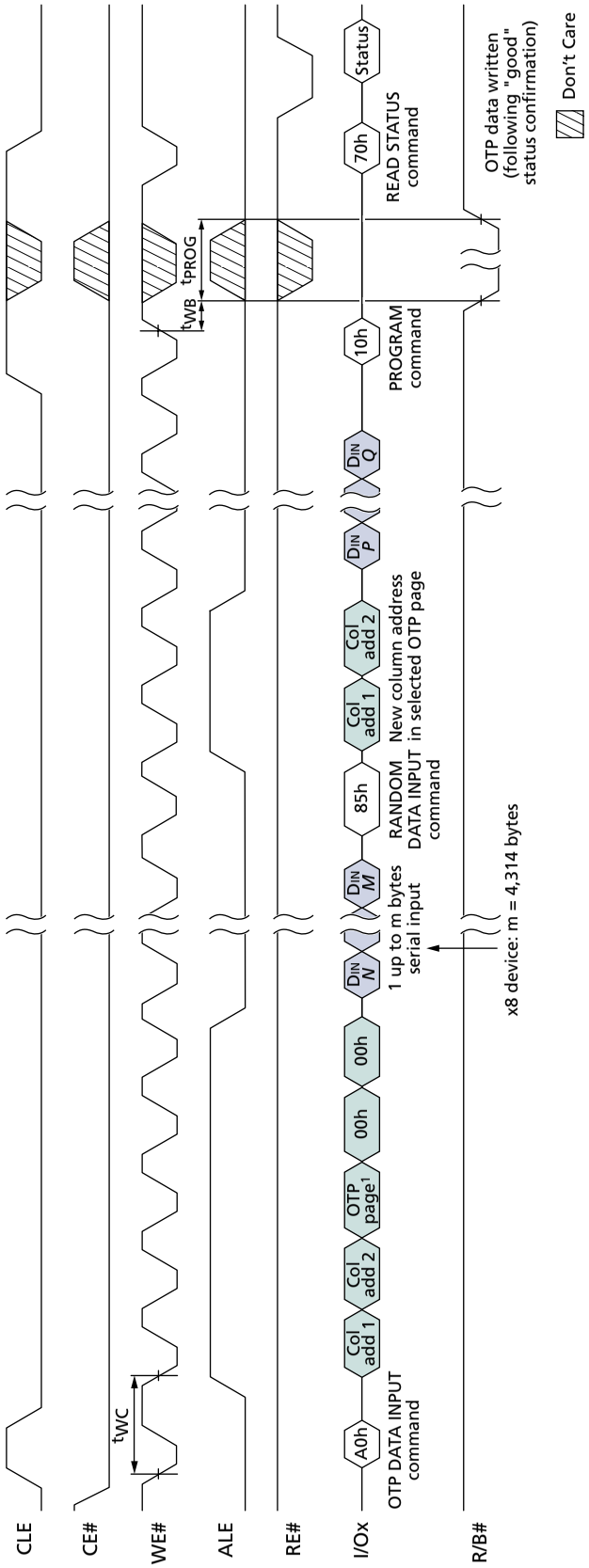
If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for ^{t}OBSY.

Figure 26: OTP DATA PROGRAM



Notes: 1. The OTP page must be within the range 02h–0Bh.

Figure 27: OTP PROGRAM with RANDOM DATA INPUT



Notes: 1. The OTP page must be within the range 02h–0Bh.

OTP DATA PROTECT A5h-10h

The OTP DATA PROTECT (A5h-10h) command is used to protect all the data in the OTP area. After the data is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

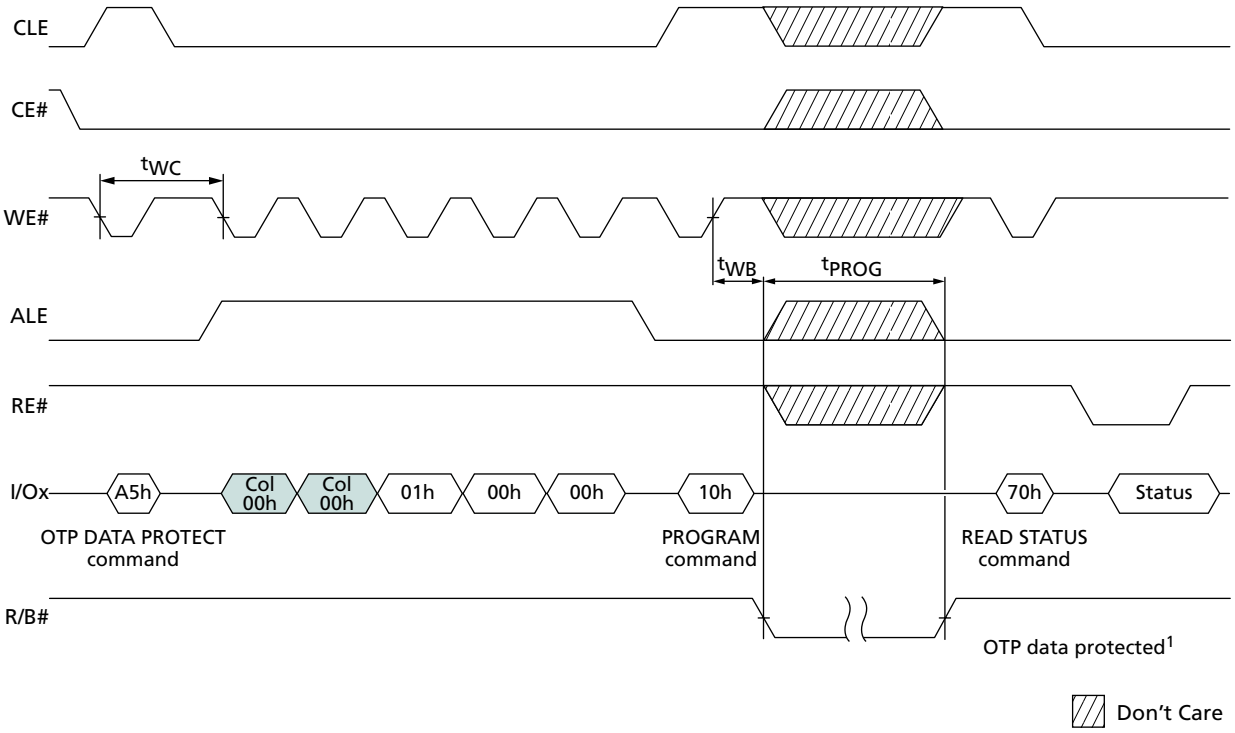
To use the OTP DATA PROTECT command, issue the A5h command. Next, issue the following 5 ADDRESS cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for ^{t}DBSY.

The READ STATUS (70h) command is the only command valid during the OTP DATA PROTECT operation. Bit 5 of the status register will reflect the state of R/B#.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 11 on page 33).

Figure 28: OTP DATA PROTECT



Notes: 1. OTP data is protected following "good" status confirmation.

OTP DATA READ AFh-30h

The OTP DATA READ (AFh-30h) command is used to read data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether or not the area is protected.

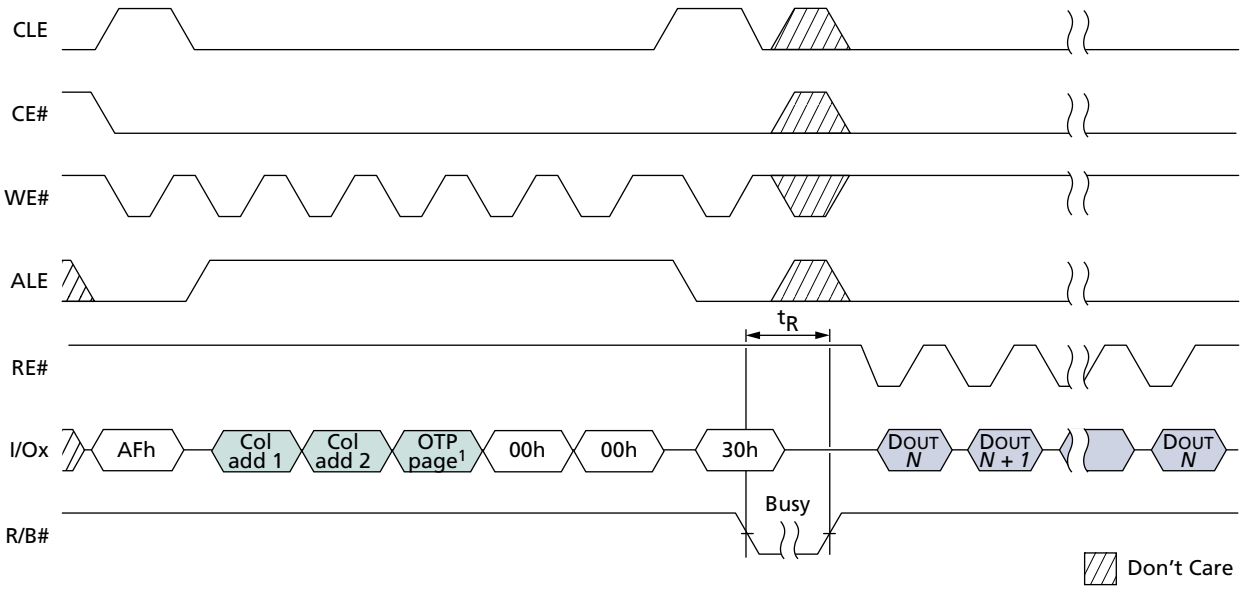
To use the OTP DATA READ command, issue the AFh command. Next, issue 5 ADDRESS cycles: the first 2 ADDRESS cycles are the column address, and for the remaining 3 cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Finally, issue the 30h command.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the OTP DATA READ operation. Bit 5 of the status register will reflect the state of R/B#. For details, refer to Table 11 on page 33.

Normal READ operation timings apply to OTP read accesses (see Figure 29). Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

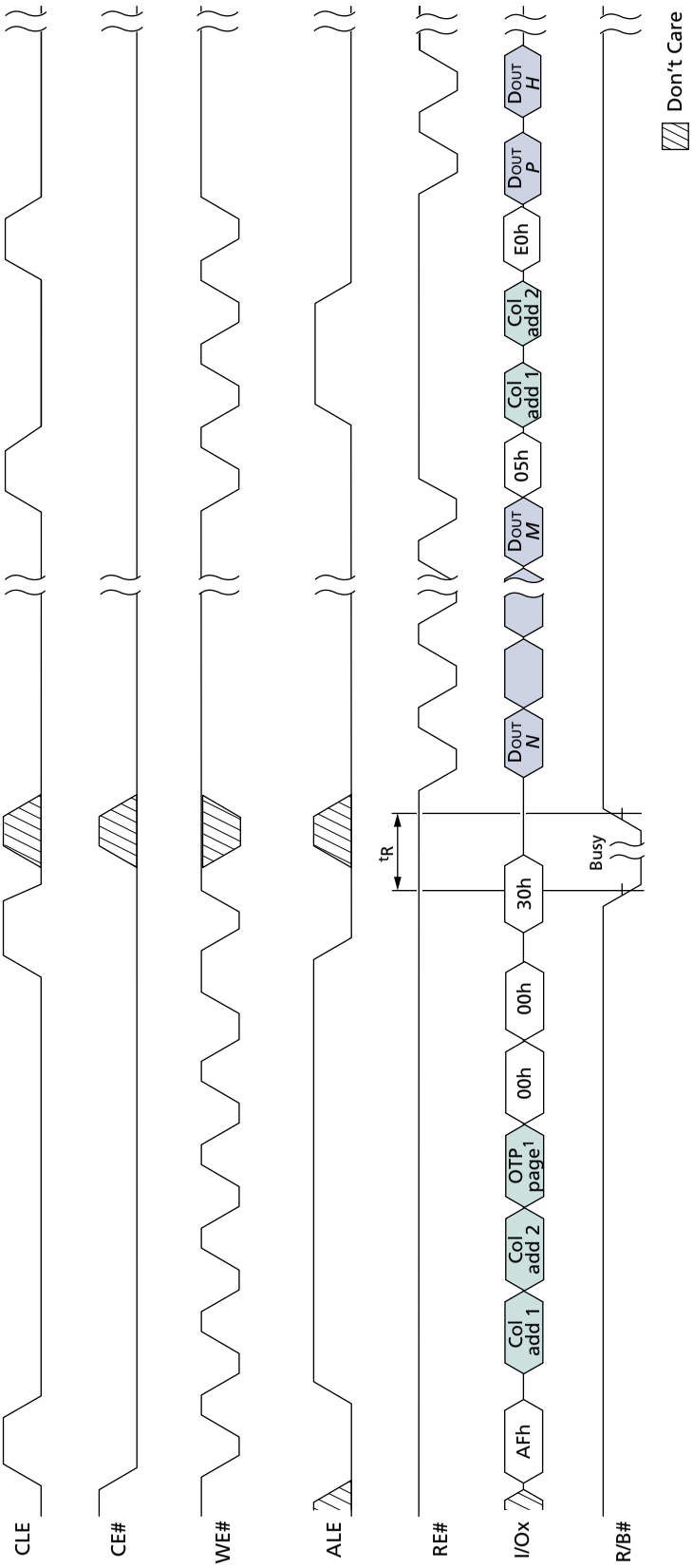
The OTP DATA READ command is compatible with the RANDOM DATA OUTPUT (05h-E0h) command.

Figure 29: OTP DATA READ Operation



Notes: 1. The OTP page must be within the range 02h–0Bh.

Figure 30: OTP DATA READ with RANDOM DATA READ



Notes: 1. The OTP page must be within the range 02h–0Bh.

Features Operations

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to alter NAND Flash device default power-on behaviors. These commands use a one-byte feature address to determine which subfeature parameters are to be read or modified. Each feature address (in the range of 00h to FFh) is defined in Table 12. The GET FEATURES command reads the subfeature parameters (P1–P4) at the specified feature address. The SET FEATURES (EFh) command places subfeature parameters (P1–P4) at the specified feature address.

Table 12: Features Table

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–7Fh	Reserved
80h	Programmable I/O drive strength
81h	Programmable R/B# pull-down strength
82h-FFh	Reserved

GET FEATURES EEh

The GET FEATURES command is used to return the current subfeature parameters (see Table 13 on page 50) at the specified feature address. Figure 31 on page 51 defines GET FEATURES behavior and timing.

R/B# goes LOW (^{t}FEAT) while the subfeature parameters are being loaded from the specified feature address. The READ STATUS (70h) command and the RESET (FFh) command are the only commands available during GET FEATURES operation. Bits 5 and 6 of the status register will reflect the state of R/B#.

Table 13: Feature Address 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1
	Mode 1	Reserved (0)					0	0	1	01h	
	Mode 2	Reserved (0)					0	1	0	02h	
	Mode 3	Reserved (0)					0	1	1	03h	
	Mode 4	Reserved (0)					1	0	0	04h	
	Mode 5	Reserved (0)					1	0	1	05h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes: 1. The timing-mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, addresses, and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power cycled. Supported timing modes are reported in the parameter page.

Table 14: Feature Address 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

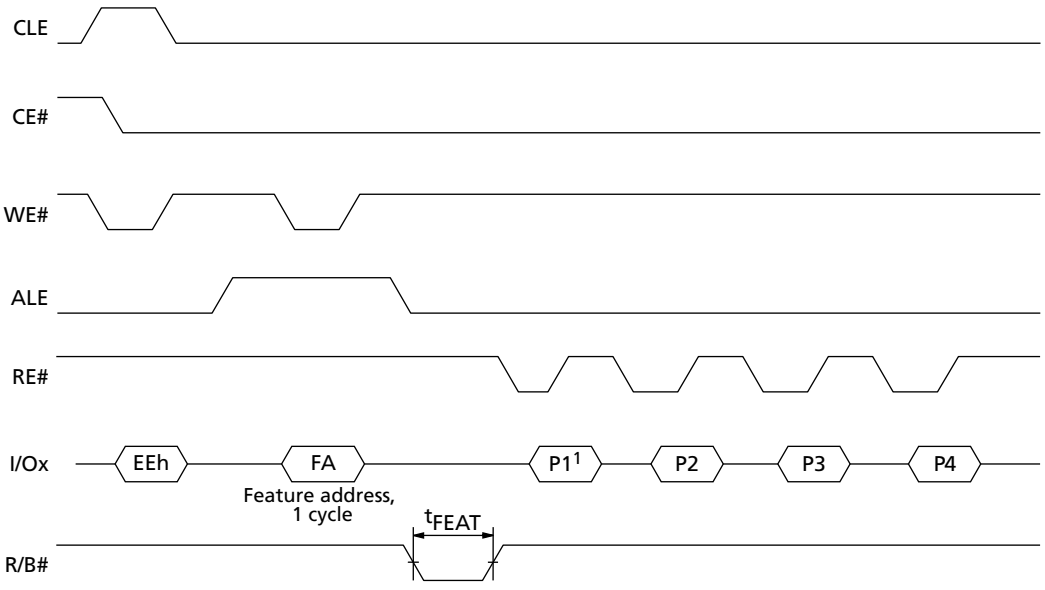
Notes: 1. The PROGRAMMABLE DRIVE STRENGTH feature address is used to change the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The default drive strength is full strength. The device returns to the default drive strength mode when the device is power cycled. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Table 15: Feature Address 81h: Programmable R/B# Pull-down Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Notes: 1. The programmable R/B# pull-down strength feature address is used to change the default R/B# pull-down strength. R/B# pull-down strength should be selected based on expected loading of R/B#. The four supported pull-down strength settings are shown. The default pull-down strength is full strength. The device returns to the default pull-down strength when the device is power cycled.

Figure 31: GET FEATURES Operation



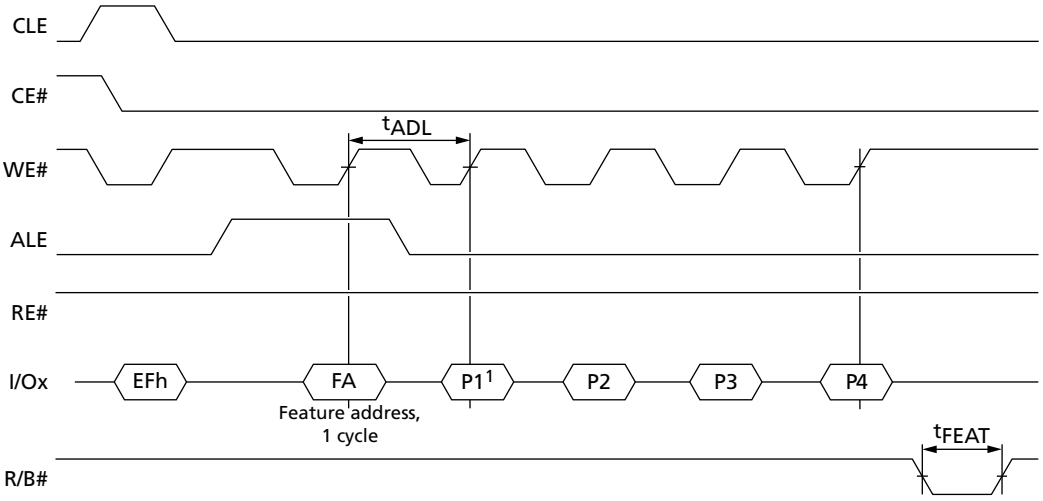
Notes: 1. P1–P4 are the subfeature parameters to be read from the specified feature address (FA).

SET FEATURES EFh

The SET FEATURES command is used to set the subfeature parameters at a specified feature address. These parameters are stored in the device until the device is powered down. The subfeature parameters are applied to all die on the CE# to which this command is issued. Figure 32 depicts SET FEATURES behavior and timing.

After all four subfeature parameters, P1–P4, are issued, R/B# goes LOW for ^{t}FEAT while the subfeature parameters are written to the specified feature address. The READ STATUS (70h) command and the RESET (FFh) command are the only valid commands during SET FEATURES operation. Bits 5 and 6 of the status register will reflect the state of R/B#.

Figure 32: SET FEATURES Operation



Notes: 1. P1–P4 are the subfeature parameters to be written to the specified feature address (FA).

TWO-PLANE Operations

This NAND Flash device is divided into two physical planes. Each plane contains a 4,314-byte data register, a 4,314-byte cache register, and a 2,048-block Flash array. Two-plane commands make better use of the flash arrays on these physical planes by performing PROGRAM, READ, or ERASE operations simultaneously, significantly improving system performance.

Two-Plane Addressing

Two-plane commands require two addresses, one address per plane. These two addresses are subject to the following requirements:

- The least significant block address bit, BA6, must be different for both addresses.
- The most significant block address bit, BA18 for 32Gb and 64Gb devices, must be identical for both addresses.
- The page address bits, PA[5:0], must be identical for both addresses.

TWO-PLANE PAGE READ 00h-00h-30h

The TWO-PLANE PAGE READ (00h-00h-30h) operation is similar to the PAGE READ (00h-30h) operation. It transfers two pages of data from the Flash array to the data registers. Each page must be from a different plane on the same die.

To enter the TWO-PLANE PAGE READ mode, write the 00h command to the command register, then write 5 ADDRESS cycles for plane 0 (BA6 = "0"). Next, write the 00h command to the command register, then write 5 ADDRESS cycles for plane 1 (BA6 = "1"). Finally, issue the 30h command. The first-plane and second-plane addresses must meet the two-plane addressing requirements, and, in addition, they must have identical column addresses.

After the 30h command is written, page data is transferred from both planes to their respective data registers in tR. During these transfers, R/B# goes LOW. When the transfers are complete, R/B# returns HIGH. To read out the data from the plane 0 data register, pulse RE# repeatedly. After the DATA cycle from the plane 0 address completes, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the plane 1 address, then repeatedly pulse RE# to read out the data from the plane 1 data register.

Alternatively, the READ STATUS (70h) command can monitor the data transfers. When the transfers are complete, status register bit 6 is set to "1." To read data from one of the two planes, the user must first issue the TWO-PLANE RANDOM DATA READ (06h-E0h) command followed by 5 ADDRESS cycles (see "TWO-PLANE RANDOM DATA READ 06h-E0h" on page 54). To read out data from the plane and column address specified with the TWO-PLANE RANDOM DATA READ command, pulse RE# repeatedly. When the DATA cycle is complete, issue a TWO-PLANE RANDOM DATA READ (06h-E0h) command to select the other plane. To output the data beginning at the specified column address, pulse RE# repeatedly.

Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is supported during and following a TWO-PLANE PAGE READ operation. The same die to which the TWO-PLANE PAGE READ command was issued must remain selected when data is read out from the NAND Flash device. Otherwise, the data read out will be invalid data for the TWO-PLANE PAGE READ command issued. A die can be selected by issuing a TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command to any valid address location on a die.

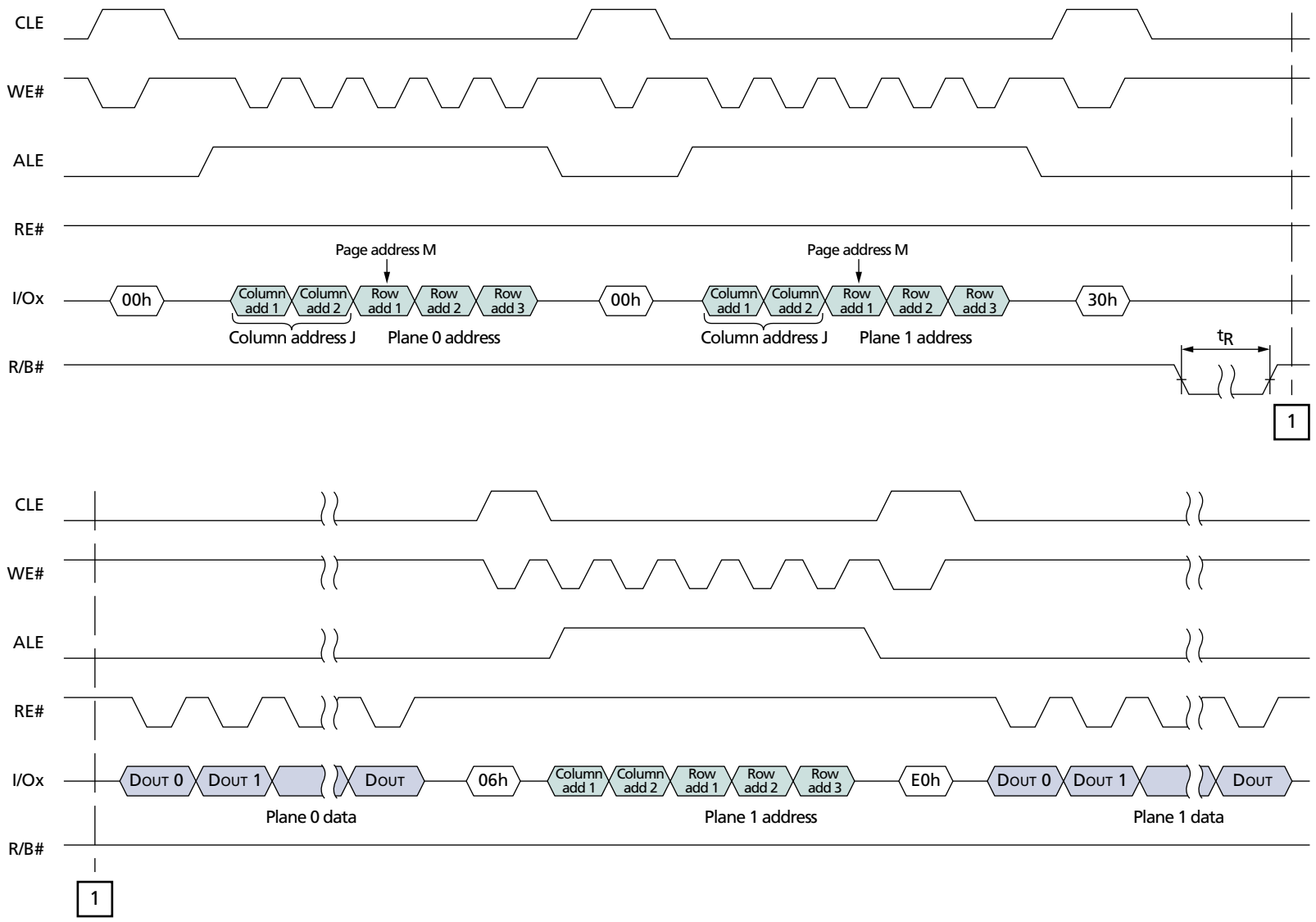
TWO-PLANE RANDOM DATA READ 06h-E0h

The TWO-PLANE RANDOM DATA READ (06h-E0h) command selects a plane and column address from which to read data after a TWO-PLANE PAGE READ (00h-00h-30h) command.

To issue a TWO-PLANE RANDOM DATA READ command, issue the 06h command, then 5 ADDRESS cycles, and follow with the E0h command. Pulse RE# repeatedly to read data from the new plane beginning at the specified column address.

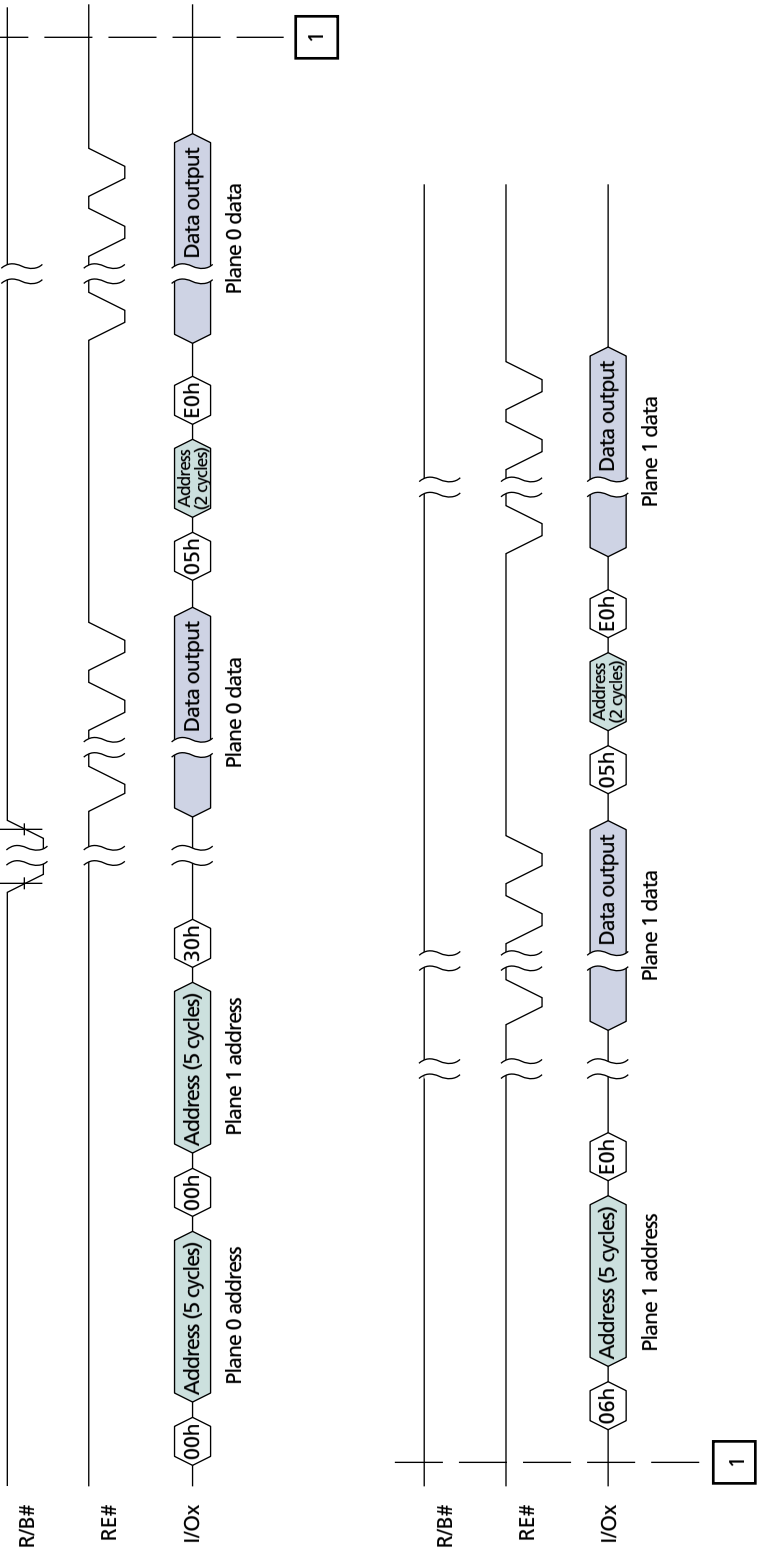
The primary purpose of the TWO-PLANE RANDOM DATA READ command is to select a new plane and column address within that plane. If a new plane does not need to be selected, then it is possible to use the RANDOM DATA READ (05h-E0h) command instead (see "RANDOM DATA READ 05h-E0h" on page 25).

Figure 33: TWO-PLANE PAGE READ



Notes: 1. Column and page addresses must be the same.
2. The least-significant block address bit, BA6, must not be the same for the first- and second-plane addresses.

Figure 34: TWO-PLANE PAGE READ with RANDOM DATA READ



TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h

The TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) operation is similar to the PROGRAM PAGE (80h-10h) operation. It programs two pages of data from the data registers to the Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to most significant page address. Random page programming within a block is prohibited. The first-plane address and the second-plane address must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 53).

To begin the TWO-PLANE PROGRAM PAGE operation, write the 80h command to the command register; write 5 ADDRESS cycles for the first plane; then write the data. Serial data is loaded on consecutive WE# cycles starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH.

The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h and 78h) and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register; write 5 ADDRESS cycles for the second plane; then write the data. The PROGRAM (10h) command is written after the second-plane data input is complete.

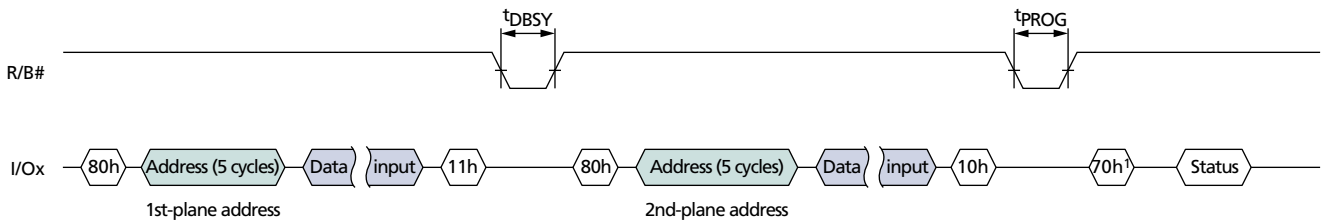
After the 10h command is written, the control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operations to both planes. WRITE verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of the array programming time (tPROG). When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}PROG are READ STATUS (70h, 78h) and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 is "1"), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

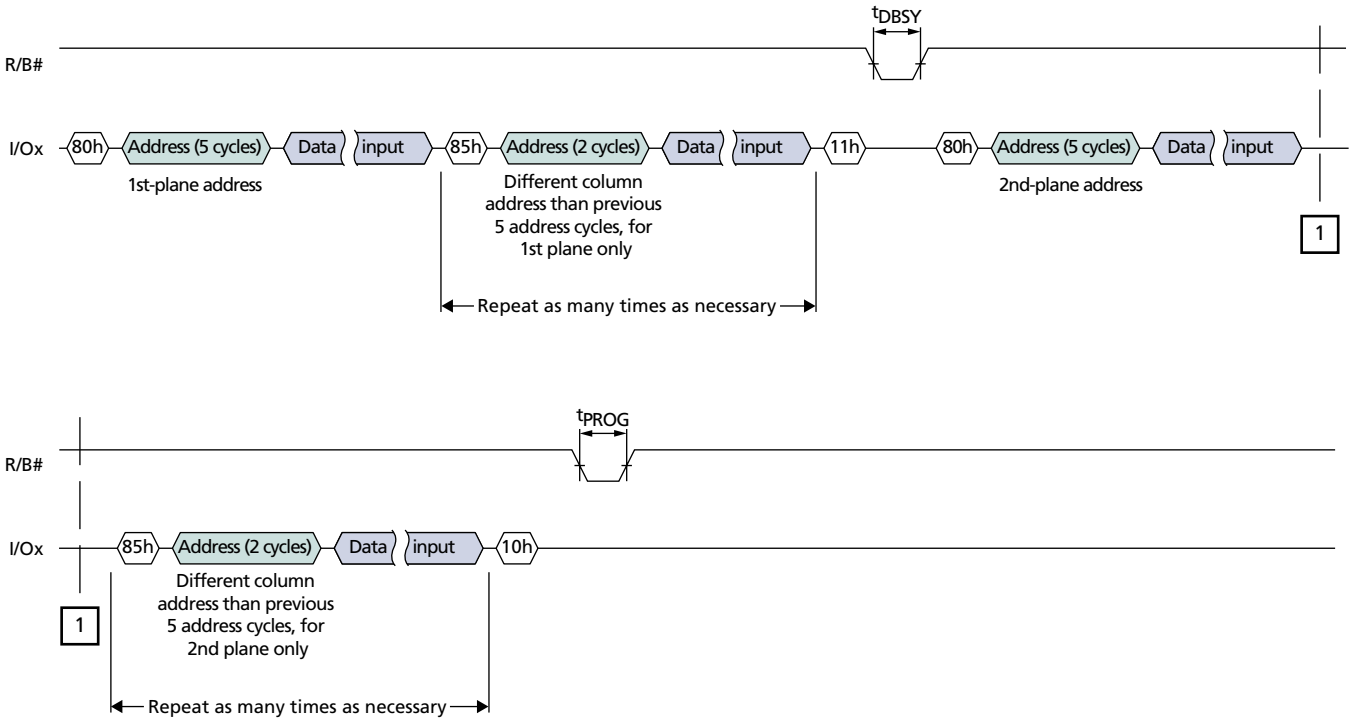
During serial data input for either plane, the RANDOM DATA INPUT (85h) command can be used any number of times to change the column address within that plane. For details on this command, see "RANDOM DATA INPUT 85h" on page 37. Figure 35 on page 57 shows TWO-PLANE PROGRAM PAGE operation.

Figure 35: TWO-PLANE PROGRAM PAGE



Notes: 1. Command can be 70h or 78h.

Figure 36: TWO-PLANE PROGRAM PAGE with RANDOM DATA INPUT



TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h

The TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) operation is similar to the PROGRAM PAGE CACHE MODE (80h-15h) operation. It cache programs two pages of data from the data registers to the NAND Flash arrays. The pages must be programmed to different planes on the same die. Within a block, the pages must be programmed consecutively from the least significant to the most significant page address. Random page programming within a block is prohibited. The first-plane and second-plane address must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 53).

To enter the TWO-PLANE PROGRAM PAGE CACHE MODE, write the 80h command to the command register, write 5 ADDRESS cycles for the first plane, then write the data. Serial data is loaded on consecutive WE# cycles, starting at the given address. Next, write the 11h command. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS command also indicates that the device is ready when status register bit 6 is set to "1."

The PROGRAM PAGE CACHE MODE command can cross block boundaries; it cannot cross die boundaries.

The only valid commands during ^{t}DBSY are READ STATUS (70h and 78h) and RESET (FFh).

After ^{t}DBSY, write the 80h command to the command register, write 5 ADDRESS cycles for the second plane, then write the data. The CACHE WRITE (15h) command is written after the second-plane data input is complete. Data is transferred from the cache registers to the data registers on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data registers and R/B# returns HIGH, memory array programming to both planes begins.

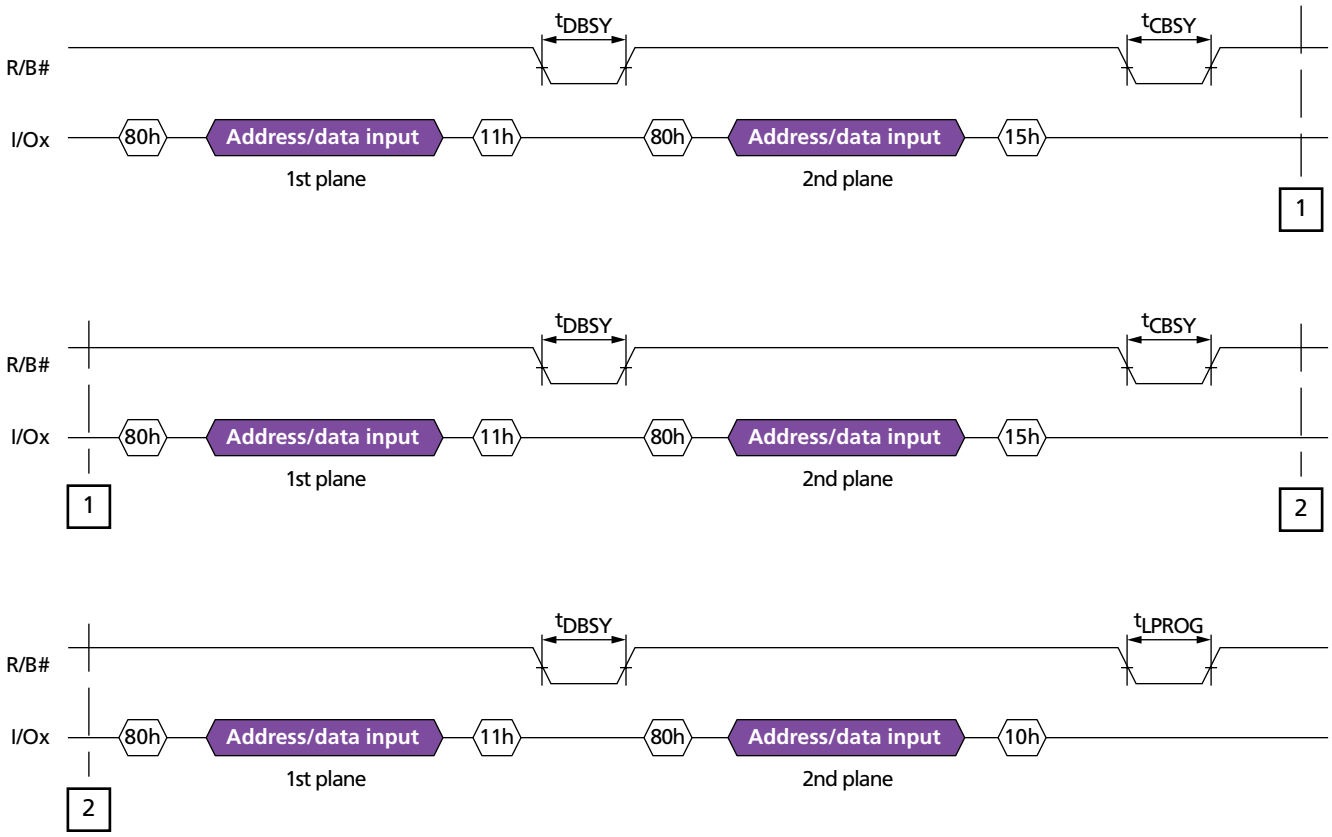
When R/B# returns HIGH, new data can be written to the cache registers by issuing another TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) sequence. The time that R/B# stays LOW (^{t}CBSY) is determined by the actual programming time of the previous operation. For the first cache operation, ^{t}CBSY duration is the time it takes for the data to be copied from the cache registers to the data registers. On the second and subsequent TWO-PLANE PROGRAM PAGE CACHE MODE operations, transfer from the cache registers to the data registers is delayed until the contents of the current data registers have been programmed into the arrays.

If the R/B# pin is used to determine programming completion, the last operation of the program sequence must use the TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) command instead of the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command. If the TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h) command is used for the last operation, then use READ STATUS (70h or 78h) to monitor the operation's progress; status register bit 5 indicates when programming is complete.

To determine when the current TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-10h) operation has completed, issue the READ STATUS (70h) command and check status register bits 5 and 6. When the device is ready, use status register bit 0 to determine if the current operation passed and status register bit 1 to determine if the previous operation passed. If either bit 0 = 1 or bit 1 = 1, indicating a failed operation, then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which current or previous plane operation failed. For more information on status register bit definitions, see Table 11 on page 33.

During the serial data input for either plane, the RANDOM DATA INPUT (85h) command may be used any number of times to change the column address within that plane.

Figure 37: TWO-PLANE PROGRAM PAGE CACHE MODE



TWO-PLANE INTERNAL DATA MOVE 00h-00h-35h/85h-11h-85h-10h

A TWO-PLANE INTERNAL DATA MOVE operation is similar to an INTERNAL DATA MOVE operation, and requires two sequences. Issue a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command first, then the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command. Data moves are only supported within the planes from which data is read. The first-plane and second-plane addresses must meet the two-plane addressing requirements for both the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) and TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) commands (see "Two-Plane Addressing" on page 53).

TWO-PLANE READ for INTERNAL DATA MOVE 00h-00h-35h

The TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is used in conjunction with the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command. First, write 00h to the command register, then write the first-plane internal source address (5 cycles). Again, write 00h to the command register, followed by the second-plane internal source address (5 cycles). Finally, write 35h to the command register. After the 35h command, R/B# goes LOW for ^{t}R while two pages are read into their respective cache registers.

After a TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command is issued, the data transferred from the source pages into the cache registers may be read out by toggling RE#. Data is output sequentially from the column address originally specified by the TWO-PLANE READ FOR INTERNAL DATA MOVE (00h-00h-35h) command, starting with plane 0.

A TWO-PLANE RANDOM DATA READ (06h-E0h) command can be used to select the data transferred from the source pages of each plane. This command will change the starting column address on only the plane being selected. The column address on the plane moved from will remain unchanged from its previous location.

The memory device is now ready to accept the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

Alternatively, two READ for INTERNAL DATA MOVE (00h-35h) commands may be issued, each addressing different planes on the same die, prior to issuing the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command.

TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-85h-10h

After the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command has been issued and R/B# goes HIGH (or the status register bit 6 is "1"), the TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-85h-10h) command is used. Pages must be read from and programmed to the same plane.

First, write 85h to the command register, then write the first-plane destination address (5 cycles), then write 11h to the command register. The 11h command is a "dummy" command that informs the control logic that the first set of data for the first plane is complete. No programming of the NAND Flash array occurs. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1."

The only valid commands during ^{t}DBSY are READ STATUS (70h and 78h) and RESET (FFh).

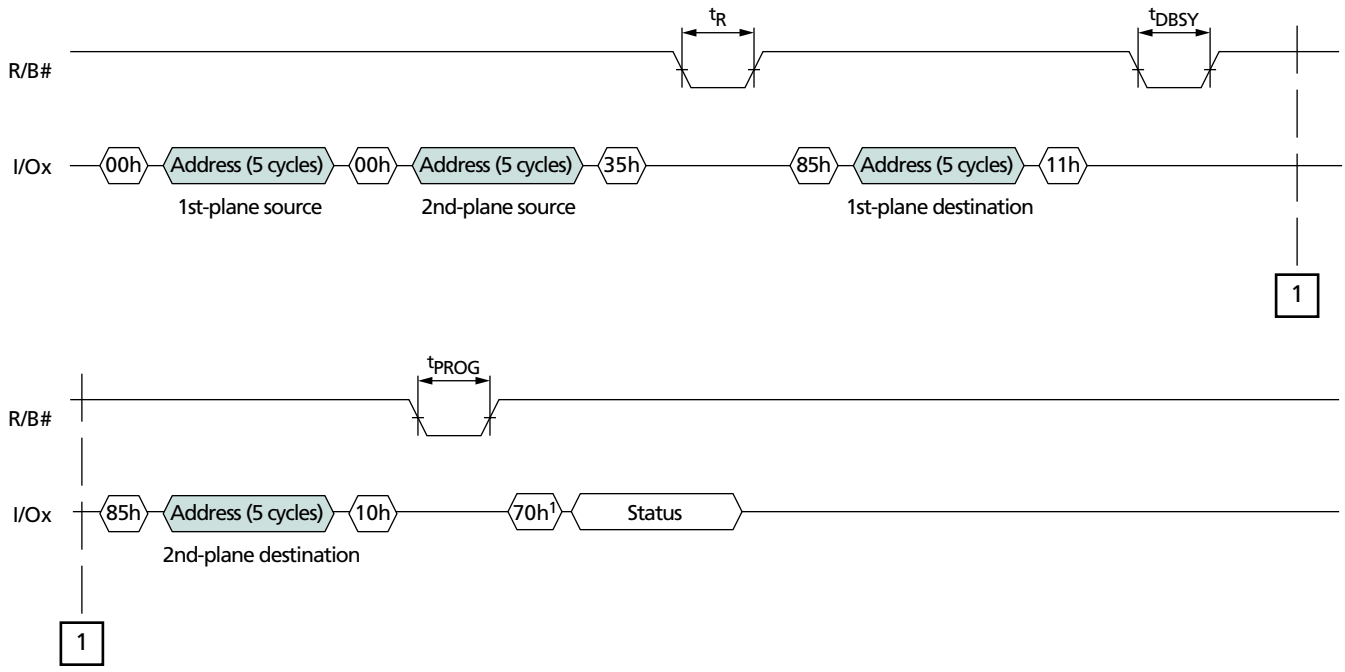
After ^{t}DBSY, write the 85h command to the command register. Then write the second-plane destination address (5 cycles), and then write 10h to the command register. Data is transferred from the cache registers to the data registers on the rising edge of WE#, and programming begins on both planes.

R/B# goes LOW for the duration of array programming time, ^{t}PROG. When programming and verification are complete, R/B# returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when status register bit 6 is set to "1." The only valid commands during ^{t}PROG are READ STATUS (70h and 78h) commands and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 is "1"), use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

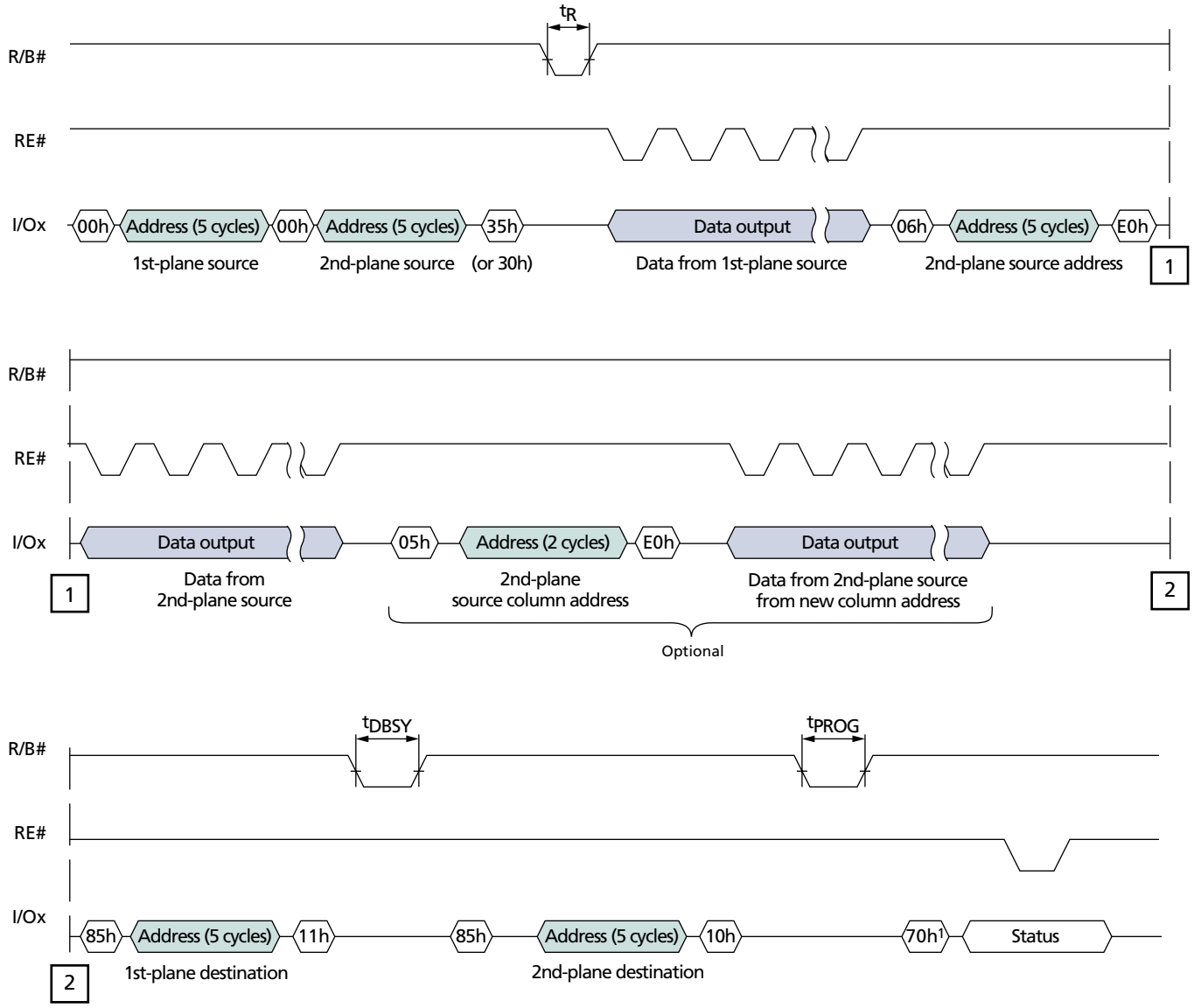
During the serial data input for either plane, the RANDOM DATA INPUT (85h) command may be used any number of times to change the column address within that plane. For details on this command, see "RANDOM DATA INPUT 85h" on page 37. See the example in Figure 40 on page 64.

Figure 38: TWO-PLANE INTERNAL DATA MOVE



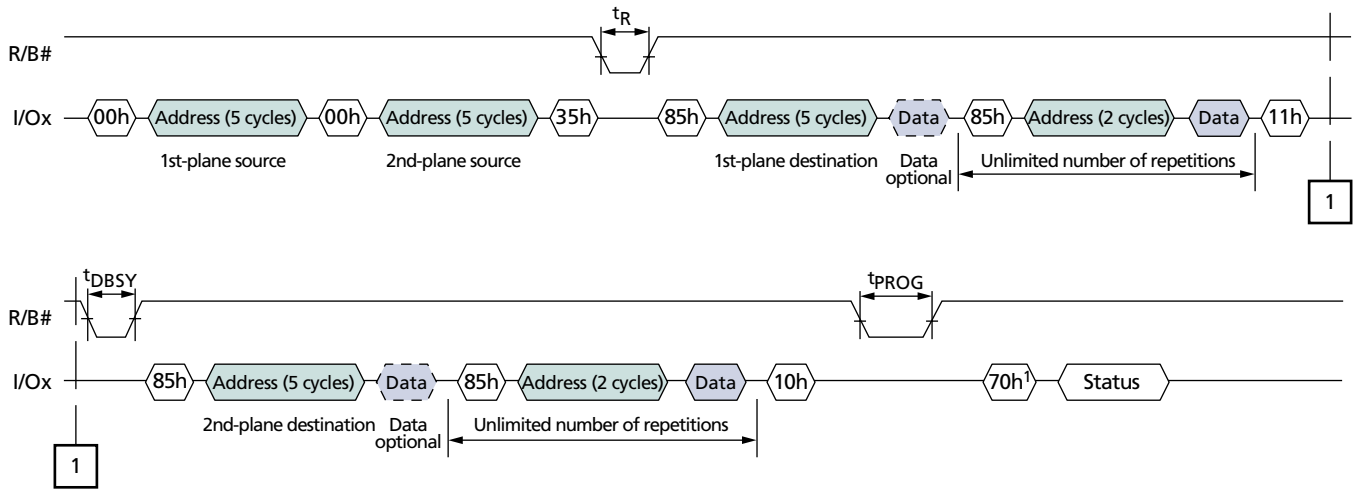
Notes: 1. Command can be 70h or 78h.

Figure 39: TWO-PLANE INTERNAL DATA MOVE with TWO-PLANE RANDOM DATA READ



Notes: 1. Command can be 70h or 78h.

Figure 40: TWO-PLANE INTERNAL DATA MOVE with RANDOM DATA INPUT



Notes: 1. Command can be 70h or 78h.

TWO-PLANE BLOCK ERASE 60h-D1h-60h-D0h

The TWO-PLANE BLOCK ERASE (60h-D1h-60h-D0h) operation is similar to the BLOCK ERASE (60h-D0h) operation. It erases two blocks instead of one. The blocks to be erased must be on different planes on the same die. The first-plane and second-plane addresses must meet the two-plane addressing requirements (see "Two-Plane Addressing" on page 53).

To begin the TWO-PLANE BLOCK ERASE operation, write the 60h command to the command register, followed by 3 ADDRESS cycles of the first-plane block address. Next, write the D1h command. The D1h command is a "dummy" command. R/B# goes LOW for ^{t}DBSY, then returns HIGH. The READ STATUS (70h) command also indicates that the device is ready when the status register bit 6 is set to "1." The only valid commands during ^{t}DBSY are READ STATUS (70h and 78h) and RESET (FFh).

After ^{t}DBSY, write the 60h command to the command register followed by 3 ADDRESS cycles for the second plane. Finally, issue the D0h command.

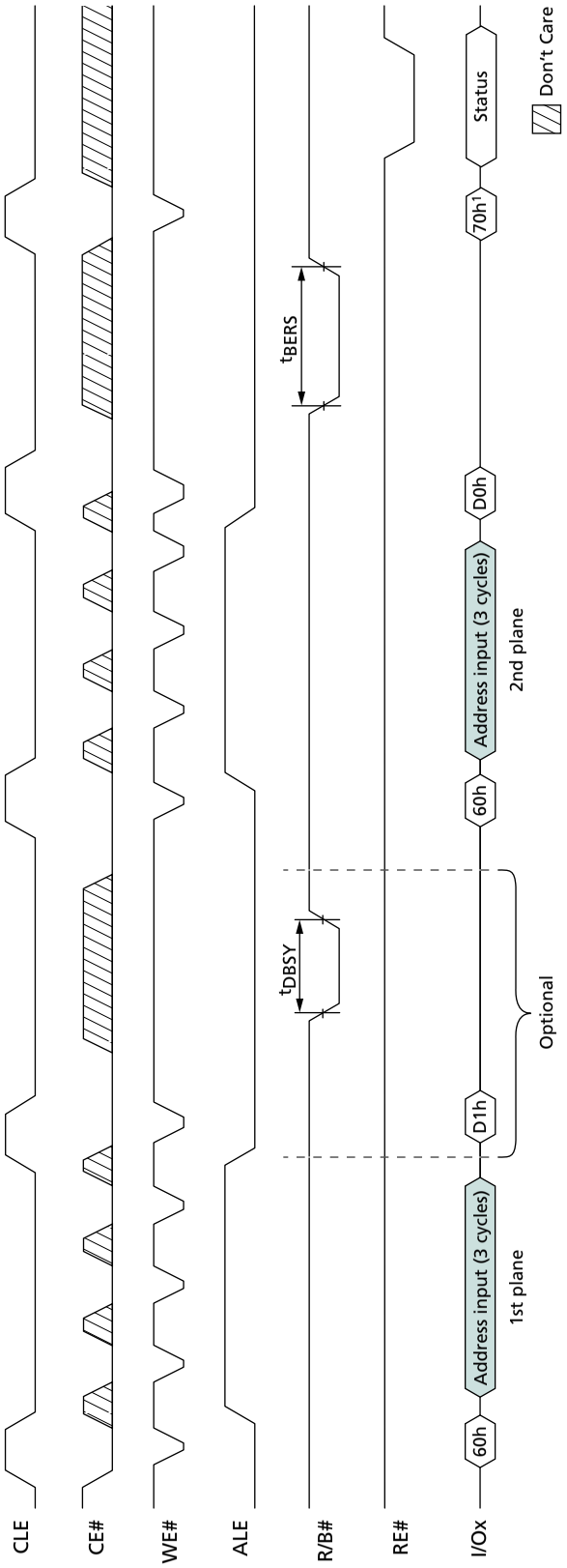
R/B# goes LOW for the duration of block erase time, ^{t}BERS. When block erasure is complete, R/B# returns HIGH. A READ STATUS command also indicates that the device is ready when status register bit 6 is set to "1."

The only valid commands during ^{t}BERS are READ STATUS (70h, 78h) commands and RESET (FFh).

If the READ STATUS (70h) command indicates an error in the operation (status register bit 0 is "1"), then use the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command twice—once for each plane—to determine which plane operation failed.

Alternatively, the D1h command may be omitted. In this case, there is no ^{t}DBSY time.

Figure 41: TWO-PLANE BLOCK ERASE Operation



Notes: 1. Command can be 70h or 78h.

TWO-PLANE/MULTIPLE-DIE READ STATUS 78h

In Micron NAND Flash devices that have two planes and possibly more than one die in a package that share the same CE# pin, it is possible to independently poll the status register of a particular plane and die using the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command. This feature operates regardless of device size, organization, or status. This command can be used to check the status during and after two-plane operations and also to check the status of interleaved die operations.

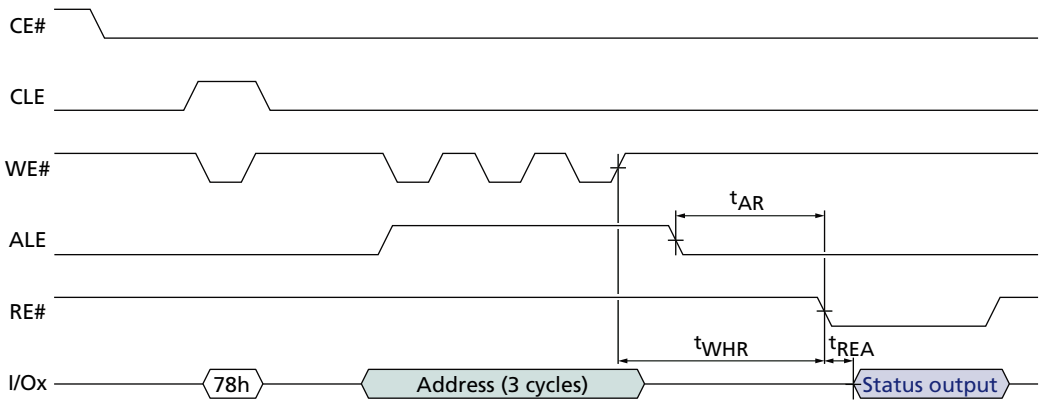
After the 78h command is issued, the device requires 3 ADDRESS cycles containing the block and page addresses, BA[18:6] and PA[5:0]. The most significant block address bit in the third ADDRESS cycle, BA18, selects the proper die, and the least significant block address bit in the first ADDRESS cycle, BA6, selects the proper plane within that die.

After the 78h command and the 3 ADDRESS cycles, the status register is output on I/O[7:0] when RE# is LOW. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to issue a new TWO-PLANE/MULTIPLE-DIE READ STATUS command to see these changes. The status register bit definitions are identical to those reported by the READ STATUS command (see Table 11 on page 33).

In devices that have more than one die sharing a common CE# pin, when one die is not busy (status register bit 5 is "1"), it is possible to initiate a new operation to that die even if the other die is busy. See "Interleaved Die Operations" on page 67.

Use of the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited during and following power-on RESET and OTP commands.

Figure 42: TWO-PLANE/MULTIPLE-DIE READ STATUS Cycle



Interleaved Die Operations

In devices that have more than one die sharing a common CE# pin, it is possible to significantly improve performance by interleaving operations between the die. When both die are idle (R/B# is HIGH or status register bit 5 is "1"), issue a command to the first die. Then, while the first die is busy (R/B# is LOW), issue a command to the other die.

There are two methods to determine operation completion. The R/B# signal indicates when both die have finished their operations. R/B# remains LOW while either die is busy. When R/B# goes HIGH, then both die are idle and the operations are complete. Alternatively, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command can report the status of each die individually. If a die is performing a cache operation, like PROGRAM PAGE CACHE MODE (80h-15h) or TWO-PLANE PROGRAM PAGE CACHE MODE (80h-11h-80h-15h), then the die is able to accept the data for another cache operation when status register bit 6 is "1." All operations, including cache operations, are complete on a die when status register bit 5 is "1."

During and following interleaved die operations, the READ STATUS (70h) command is prohibited. Instead, use the 78h command to monitor status. These commands select which die will report status. Interleaved two-plane commands must also meet the requirements in "Two-Plane Addressing" on page 53.

PAGE READ, TWO-PLANE PAGE READ, PROGRAM PAGE, PROGRAM PAGE CACHE MODE, TWO-PLANE PROGRAM PAGE, TWO-PLANE PROGRAM PAGE CACHE MODE, READ for INTERNAL DATA MOVE, TWO-PLANE READ for INTERNAL DATA MOVE, PROGRAM for INTERNAL DATA MOVE, TWO-PLANE PROGRAM for INTERNAL DATA MOVE, BLOCK ERASE, and TWO-PLANE BLOCK ERASE can be used in any combination as interleaved operations on separate die that share a common CE#.

In interleaved PROGRAM and READ operations, the PROGRAM operation must be issued before the READ operation. The data from the READ operation must be read out before the next PROGRAM operation.

Interleaved PAGE READ Operations

Figure 43 on page 68 shows how to perform interleaved PAGE READ operations. In Figure 43, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE DIE READ STATUS (78h) command.

During interleaved PAGE READ operations, a TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is required before reading data from either die. This ensures that only the die selected by the 78h command responds to a subsequent toggle of the RE# signal after data output is selected with the 00h command.

RANDOM DATA OUTPUT (05h-E0h) commands are permitted during interleaved PAGE READ operations.

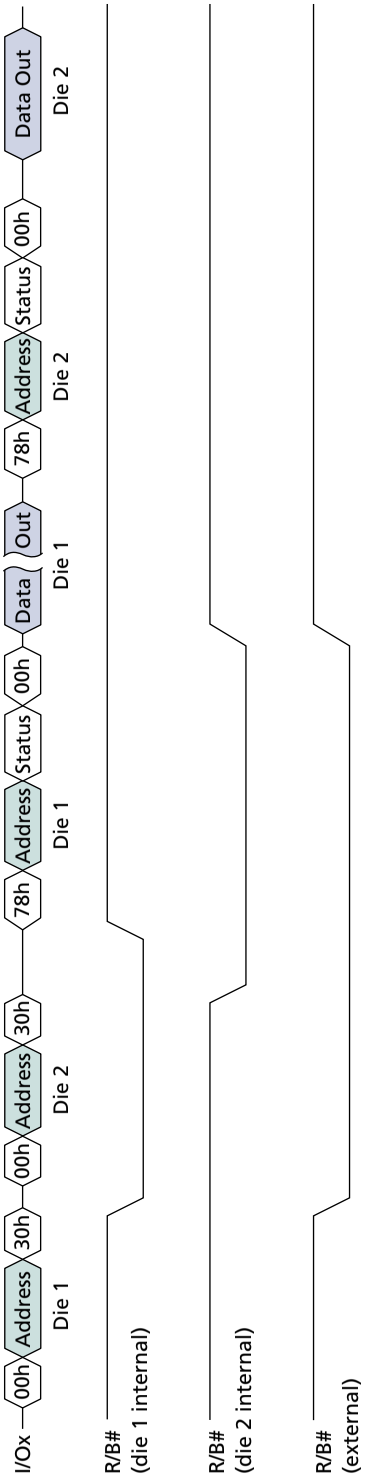


Figure 43: Interleaved PAGE READ with Status Register Monitoring

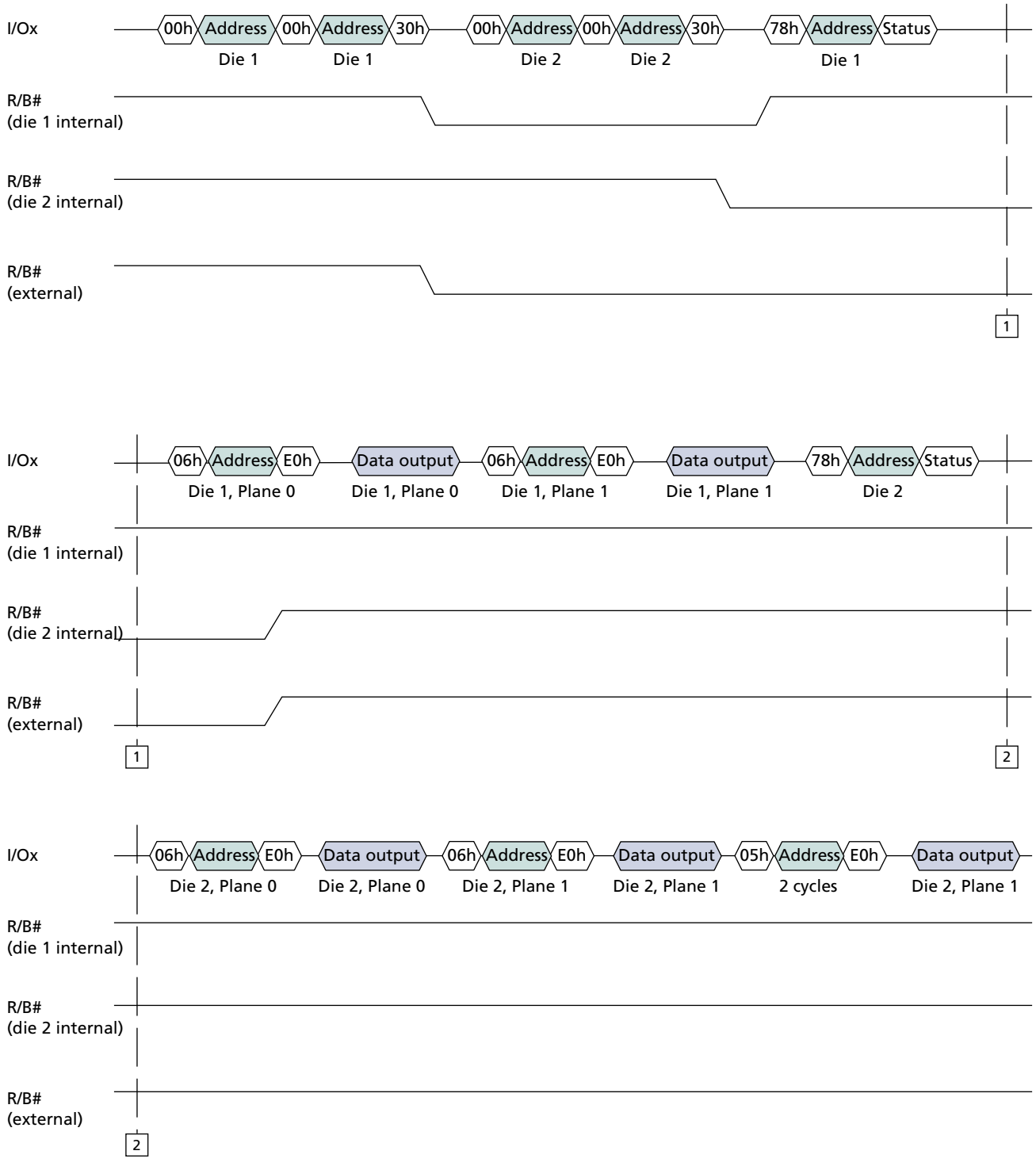
Interleaved TWO-PLANE PAGE READ Operation

Figure 44 on page 70 shows how to perform interleaved TWO-PLANE PAGE READ operations. In Figure 44, the TWO-PLANE/MULITPLE DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PAGE READ operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 53 for details.

RANDOM DATA OUTPUT (05h-E0h) is permitted during interleaved TWO-PLANE PAGE READ operations to change the column address within a plane. TWO-PLANE RANDOM DATA OUTPUT (06h-E0h) is permitted during interleaved TWO-PLANE PAGE READ operations to change planes and column addresses between the planes.

Figure 44: Interleaved TWO-PLANE PAGE READ with Status Register Monitoring



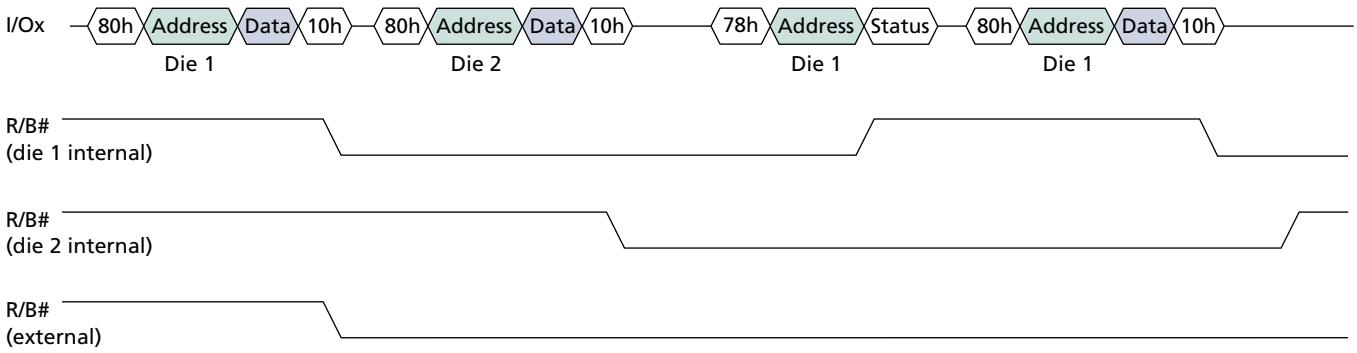
Notes: 1. Two-plane addressing requirements apply.

Interleaved PROGRAM PAGE Operations

Figure 45 shows how to perform interleaved PROGRAM PAGE operations. The status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE operations.

Figure 45: Interleaved PROGRAM PAGE with Status Register Monitoring

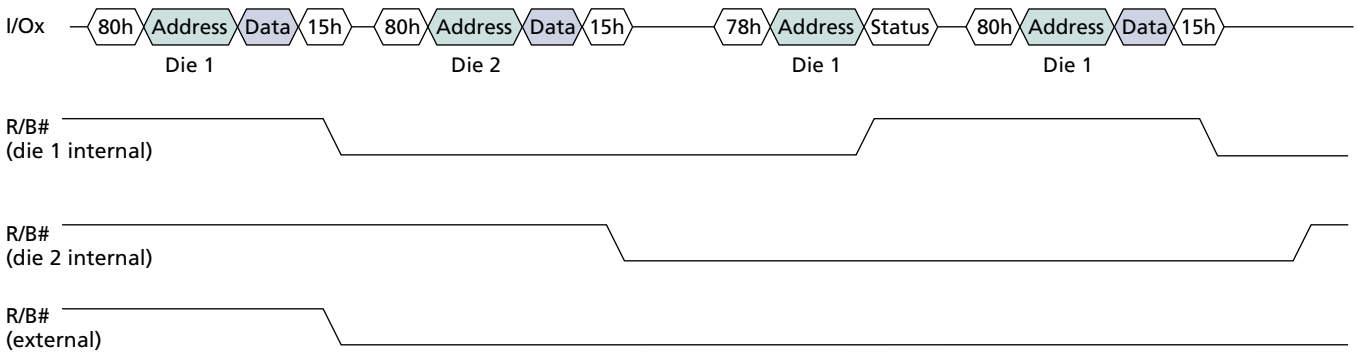


Interleaved PROGRAM PAGE CACHE MODE Operations

Figure 46 shows how to perform interleaved PROGRAM PAGE CACHE MODE operations. The status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

RANDOM DATA INPUT (85h) is permitted during interleaved PROGRAM PAGE CACHE MODE operations.

Figure 46: Interleaved PROGRAM PAGE CACHE MODE with Status Register Monitoring



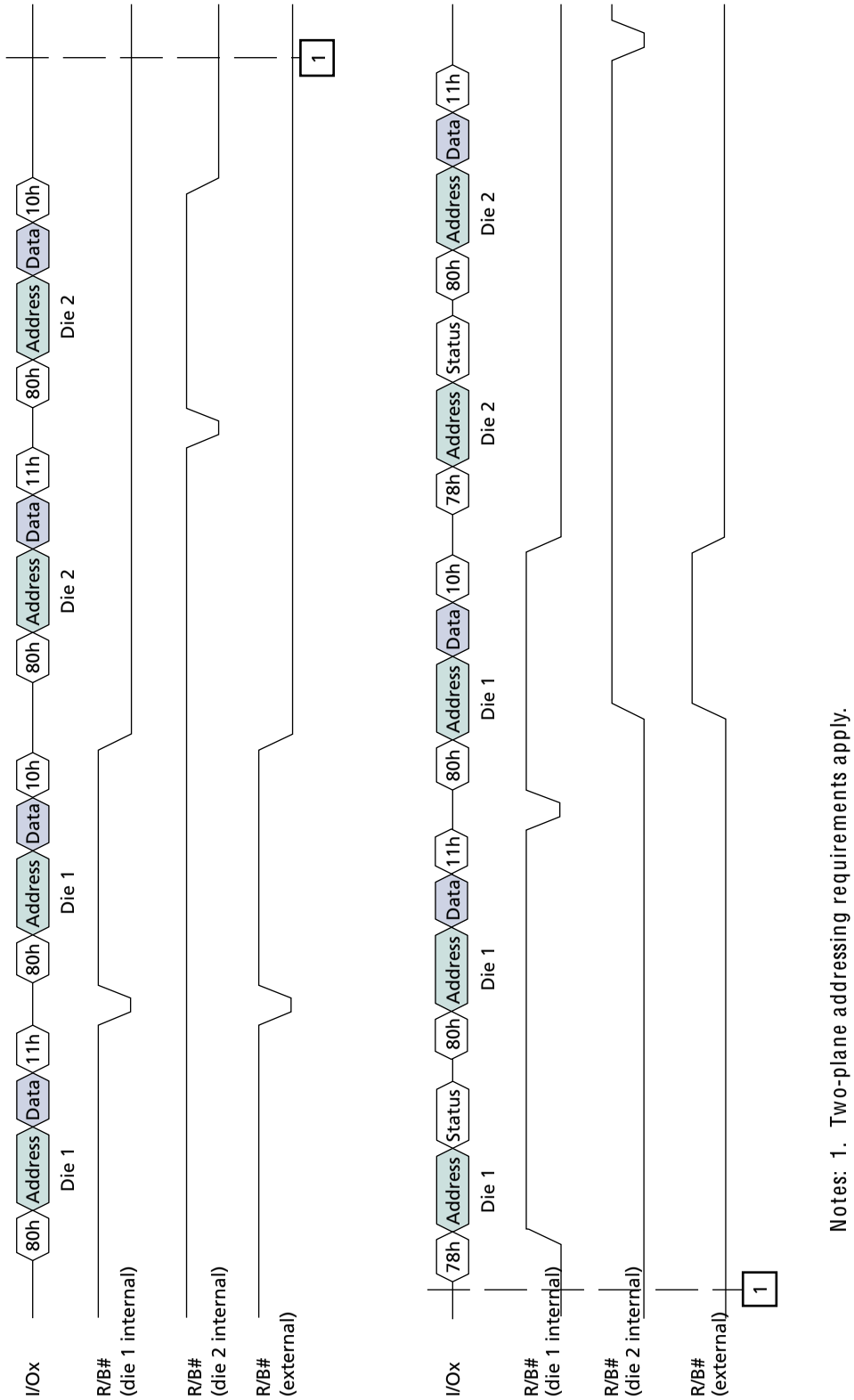
Interleaved TWO-PLANE PROGRAM PAGE Operation

Figure 47 on page 73 shows how to perform interleaved TWO-PLANE PROGRAM PAGE operations. The TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PROGRAM PAGE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 53 for details.

RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE operations.

Figure 47: Interleaved TWO-PLANE PROGRAM PAGE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

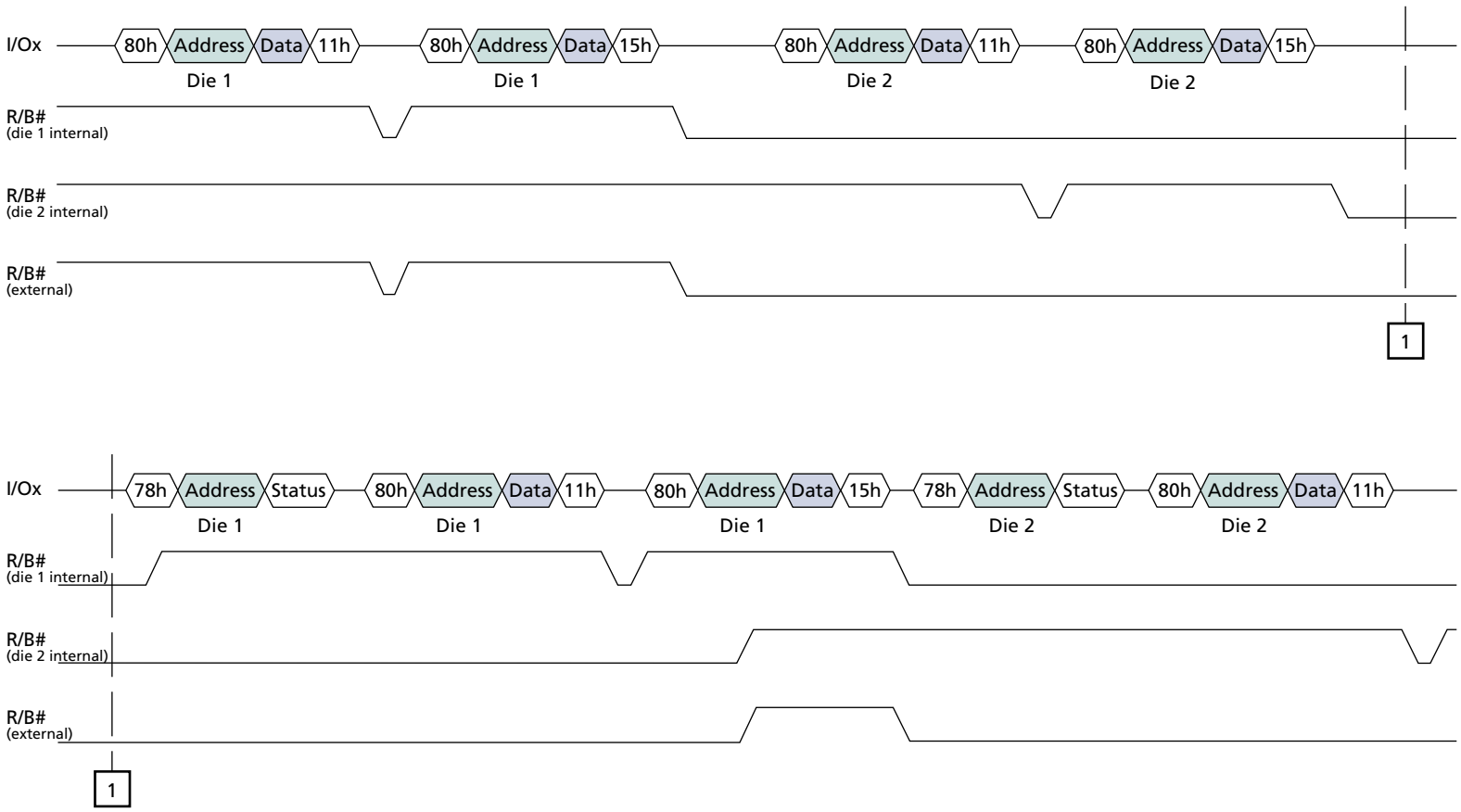
Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE Operations

Figure 48 on page 75 shows how to perform interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations. The status register is monitored with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

The interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 53 for details.

RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM PAGE CACHE MODE operations.

Figure 48: Interleaved TWO-PLANE PROGRAM PAGE CACHE MODE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

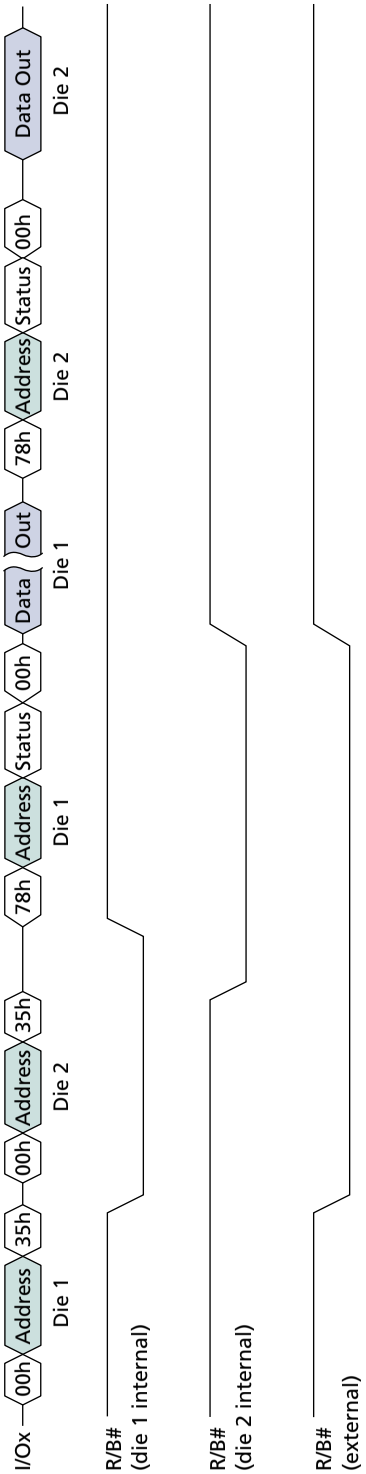
Interleaved READ for INTERNAL DATA MOVE Operations

Figure 49 on page 77 shows how to perform interleaved READ for INTERNAL DATA MOVE operations. In Figure 49, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

The READ for INTERNAL DATA MOVE operations must operate within the same plane.

RANDOM DATA OUTPUT (05h-E0h) commands are permitted during interleaved READ for INTERNAL DATA MOVE operations.

Figure 49: Interleaved READ for INTERNAL DATA MOVE with Status Register Monitoring



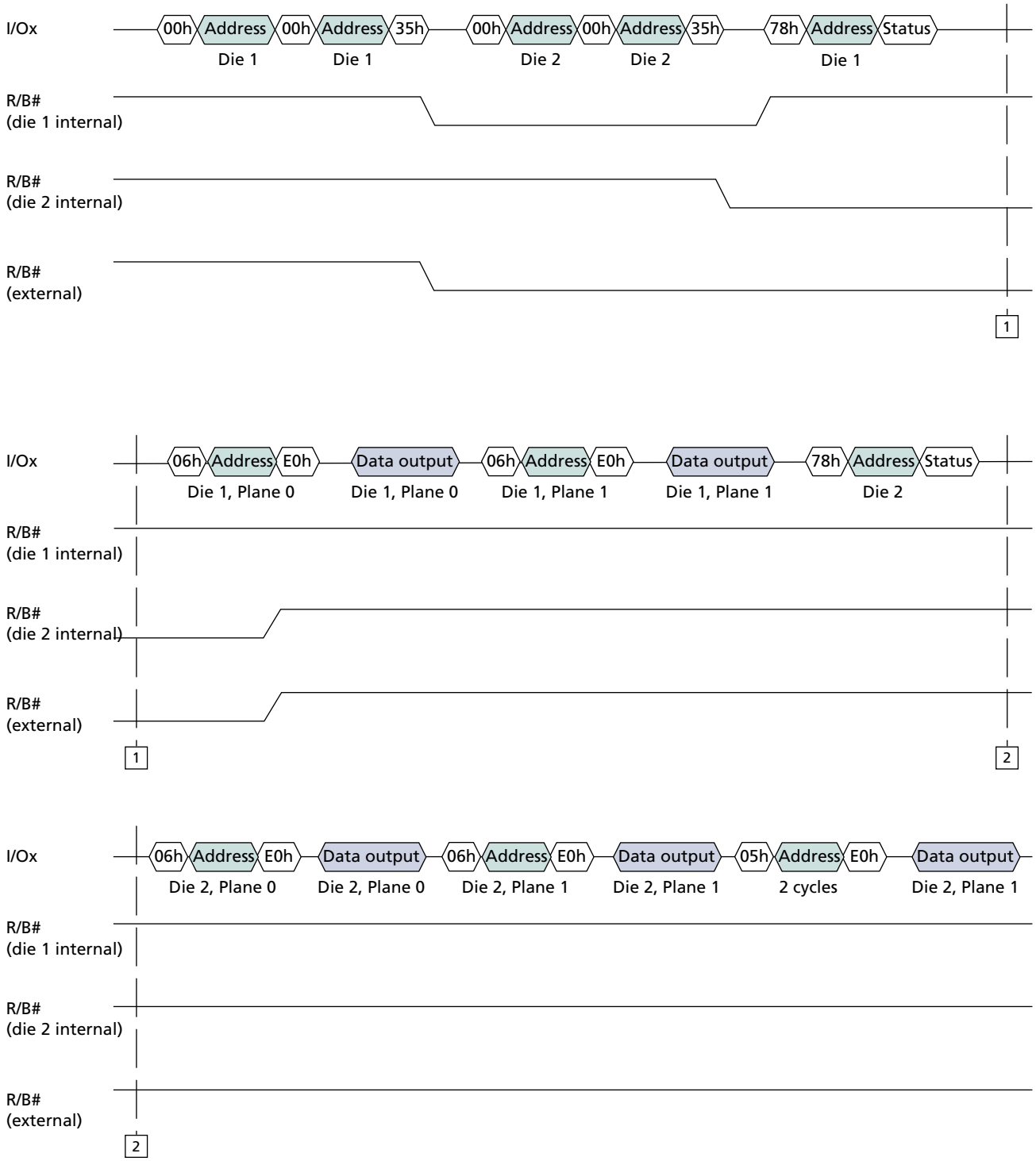
Interleaved TWO-PLANE READ for INTERNAL DATA MOVE Operations

Figure 50 on page 79 shows how to perform interleaved TWO-PLANE READ for INTERNAL DATA MOVE operations. In Figure 50, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE READ for INTERNAL DATA MOVE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 53 for details. The TWO-PLANE READ for INTERNAL DATA MOVE operations must operate within the same plane.

RANDOM DATA OUTPUT (05h-E0h) is permitted during interleaved TWO-PLANE READ for INTERNAL DATA MOVE operations to change the column address within a plane. TWO-PLANE RANDOM DATA OUTPUT (06h-E0h) is permitted during interleaved TWO-PLANE READ for INTERNAL DATA MOVE operations to change planes and column addresses between the planes.

Figure 50: Interleaved TWO-PLANE READ for INTERNAL DATA MOVE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

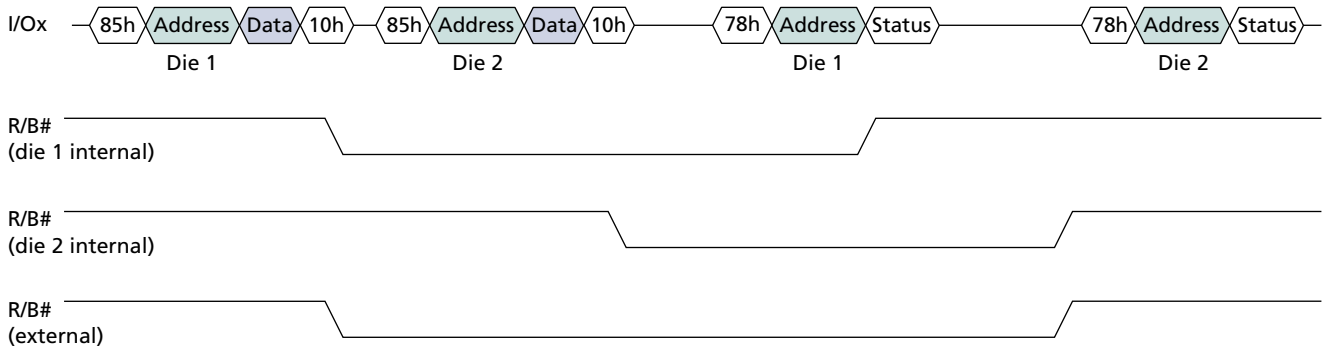
Interleaved PROGRAM for INTERNAL DATA MOVE Operations

Figure 51 shows how to perform interleaved PROGRAM for INTERNAL DATA MOVE operations. In Figure 51, the status register is monitored for operation completion with the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command.

An interleaved READ for INTERNAL DATA MOVE operation is required before a PROGRAM for INTERNAL DATA MOVE operation can be started. See "Interleaved READ for INTERNAL DATA MOVE Operations" on page 76 for a description. The PROGRAM for INTERNAL DATA MOVE operations must operate within the same plane.

RANDOM DATA INPUT (85h) commands are permitted during interleaved PROGRAM for INTERNAL DATA MOVE operations.

Figure 51: Interleaved PROGRAM for INTERNAL DATA MOVE with Status Register Monitoring



Notes: 1. A previous interleaved READ for INTERNAL DATA MOVE operation is required.

Interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE Operations

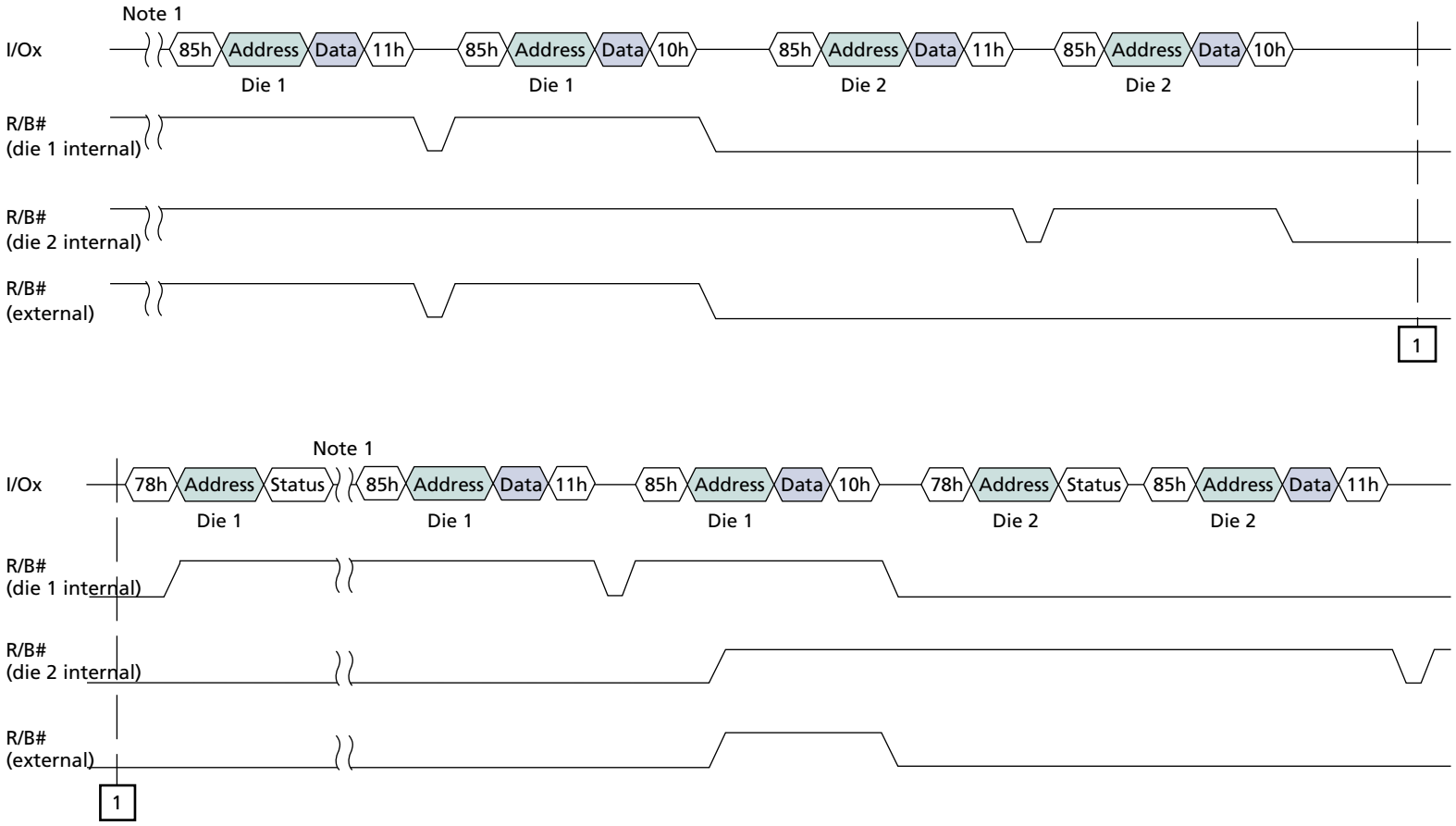
Figure 52 on page 81 shows how to perform interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE operations. In Figure 52, the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 53 for details. The TWO-PLANE PROGRAM for INTERNAL DATA MOVE operations must operate within the same plane.

An interleaved TWO-PLANE READ for INTERNAL DATA MOVE operation is required before a TWO-PLANE PROGRAM for INTERNAL DATA MOVE operation can be started. See "Interleaved TWO-PLANE READ for INTERNAL DATA MOVE Operations" on page 78 for a description.

RANDOM DATA INPUT (85h) is permitted during interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE operations.

Figure 52: Interleaved TWO-PLANE PROGRAM for INTERNAL DATA MOVE with Status Register Monitoring

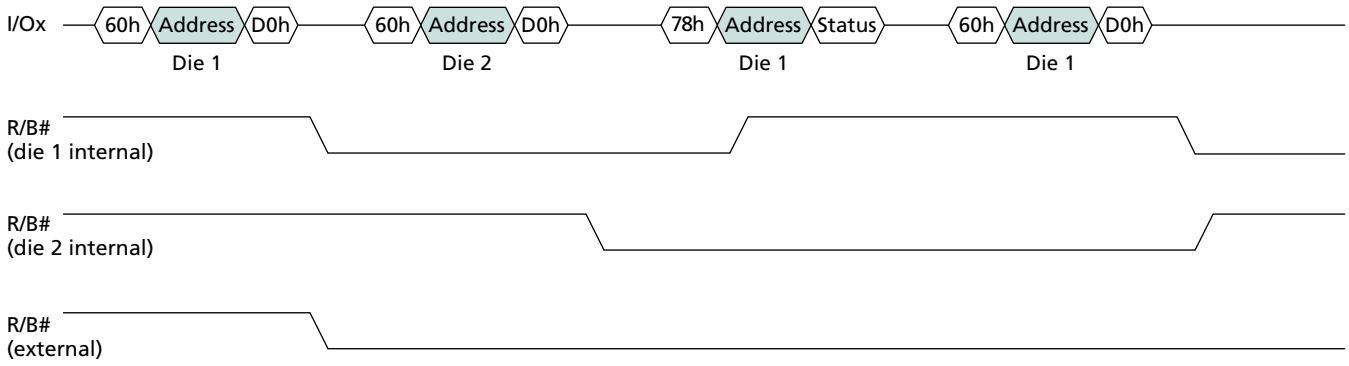


Notes: 1. A previous interleaved TWO-PLANE READ for INTERNAL DATA MOVE operation is required.

Interleaved BLOCK ERASE Operations

Figure 53 shows how to perform interleaved BLOCK ERASE operations. The TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

Figure 53: Interleaved BLOCK ERASE with Status Register Monitoring

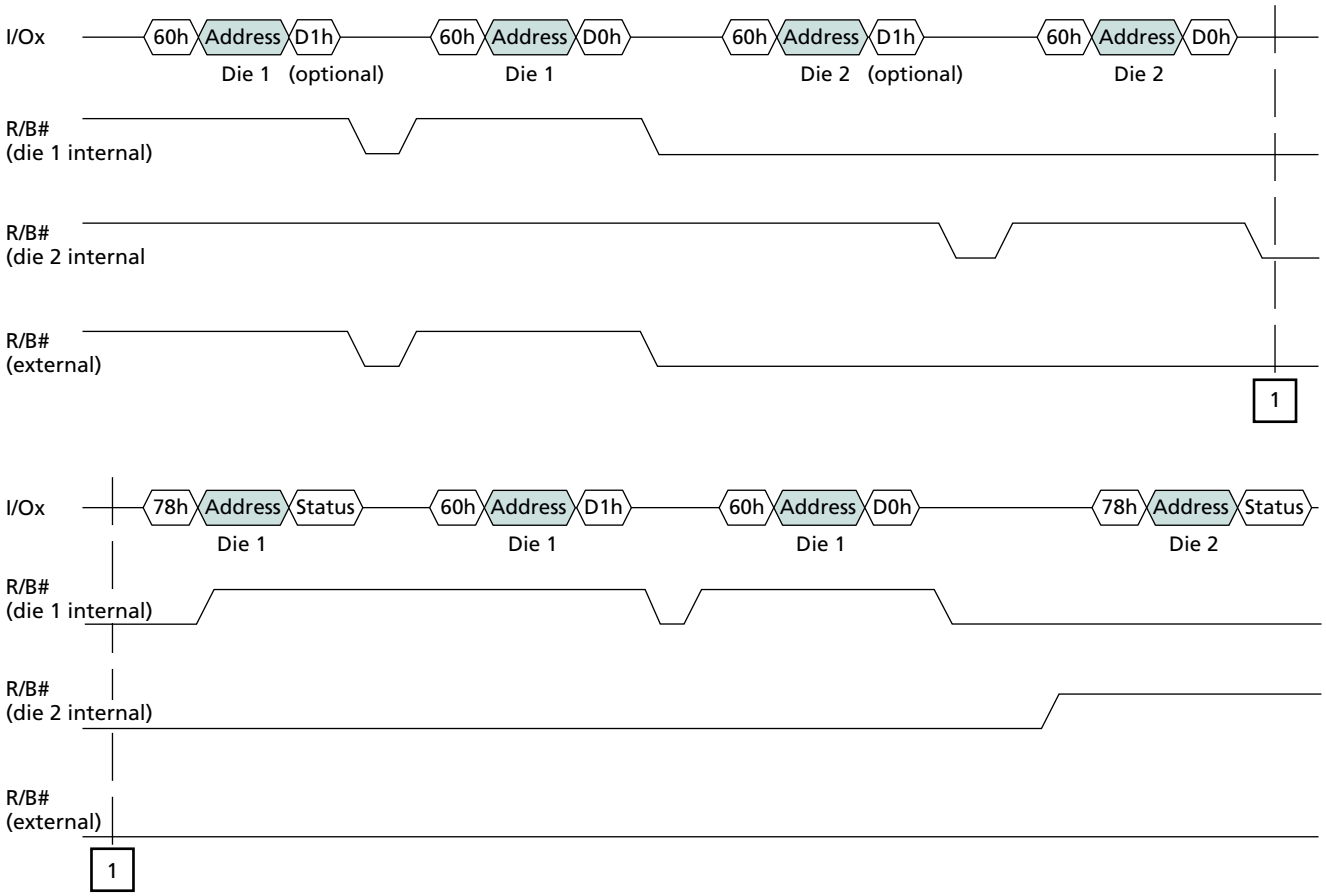


Interleaved TWO-PLANE BLOCK ERASE Operations

Figure 54 shows how to perform interleaved TWO-PLANE BLOCK ERASE operations. The TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command is used to monitor the status register for operation completion.

The interleaved TWO-PLANE BLOCK ERASE operation must meet two-plane addressing requirements. See "Two-Plane Addressing" on page 53 for details.

Figure 54: Interleaved TWO-PLANE BLOCK ERASE with Status Register Monitoring



Notes: 1. Two-plane addressing requirements apply.

RESET Operation

RESET FFh

The RESET (FFh) command is used to put the memory device into a known condition and to abort a command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes low for tRST after the RESET command is written to the command register (see Figure 55 and Table 16 on page 85).

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms. During and following the initial RESET command, and prior to issuing the next command, use of the TWO PLANE/MULTIPLE-DIE READ STATUS (78h) command is prohibited.

If the RESET command is issued during or following an interleaved-die operation then the TWO-PLANE/MULTIPLE-DIE READ STATUS (78h) command must be issued, once per die, to determine completion of the RESET operation. Use of the READ STATUS (70h) command is not permitted until the 78h command is issued.

Figure 55: RESET Operation

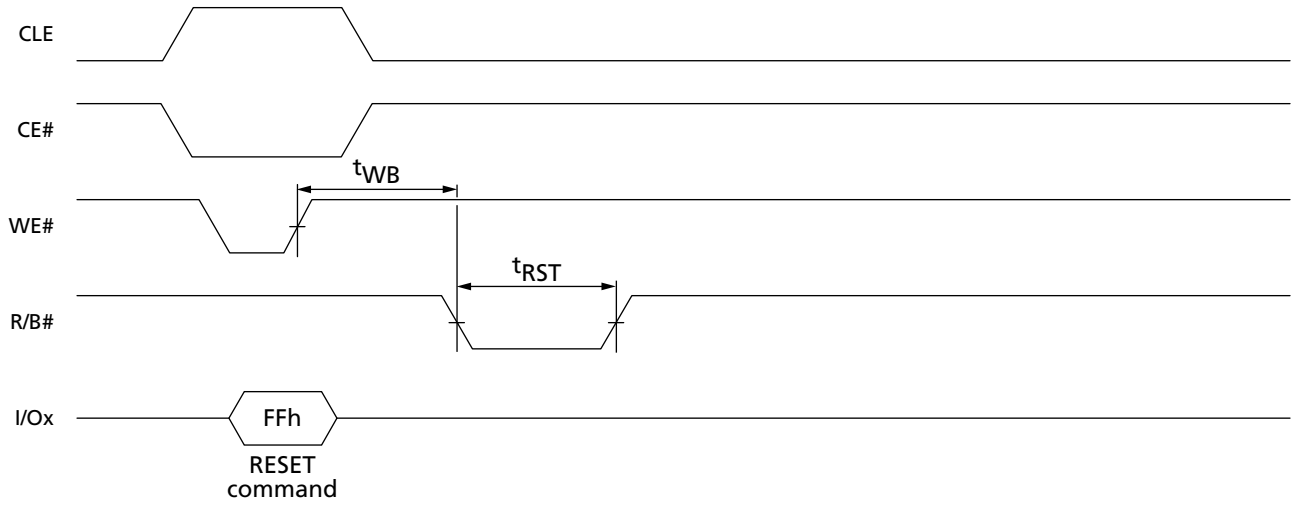


Table 16: Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using WP#. Figures 56 through 67 illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, WP# must not be toggled until the command is complete and the device is ready (status register bit 5 is "1").

Figure 56: ERASE Enable

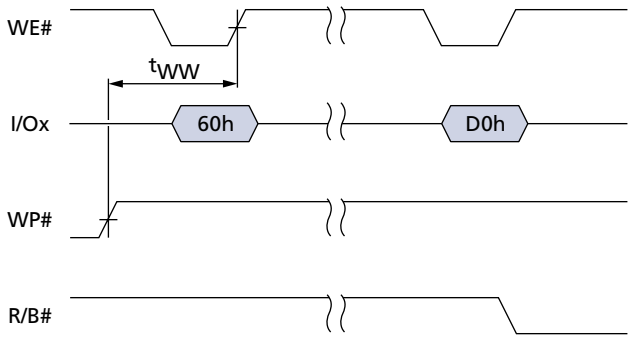


Figure 57: ERASE Disable

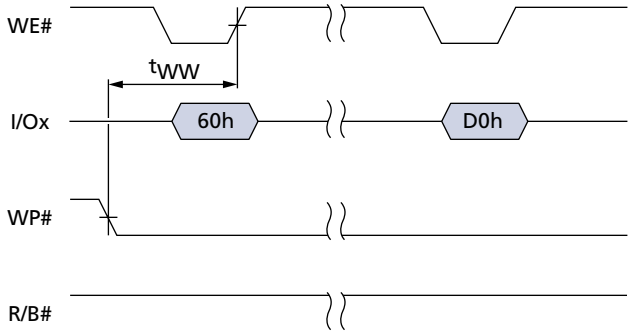


Figure 58: PROGRAM Enable

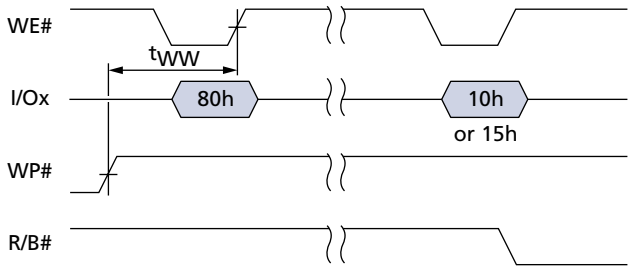


Figure 59: PROGRAM Disable

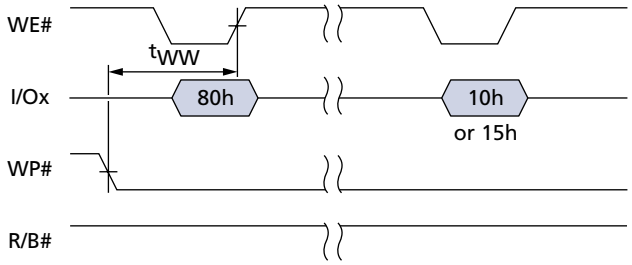


Figure 60: PROGRAM for INTERNAL DATA MOVE Enable

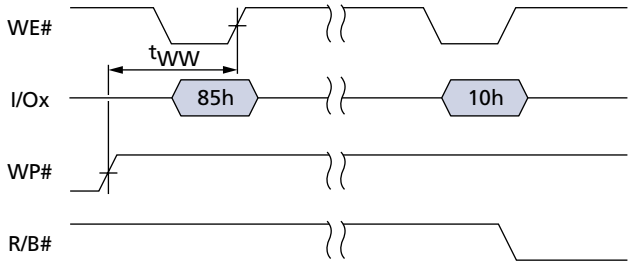


Figure 61: PROGRAM for INTERNAL DATA MOVE Disable

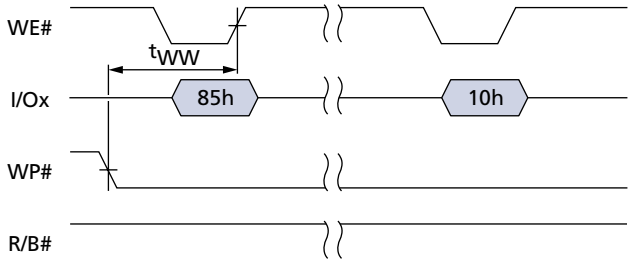


Figure 62: TWO-PLANE ERASE Enable

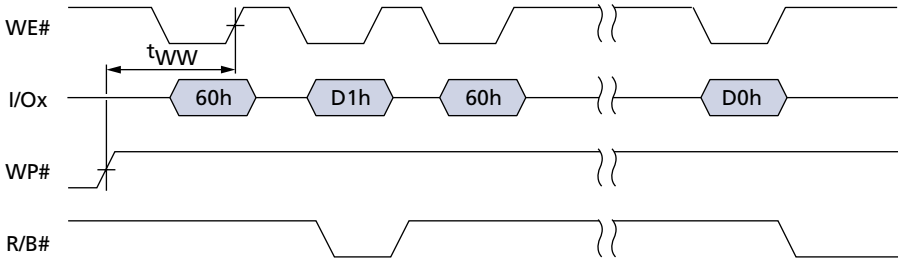


Figure 63: TWO-PLANE ERASE Disable

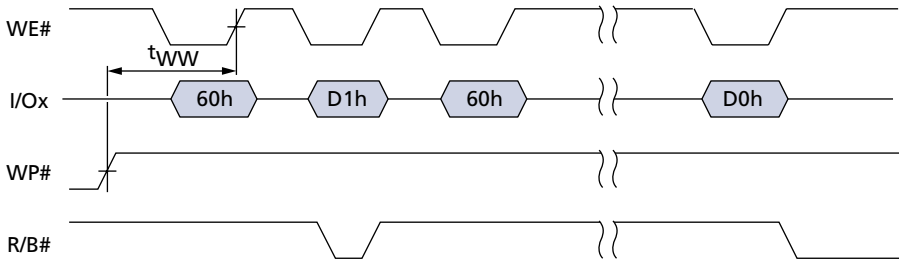


Figure 64: TWO-PLANE PROGRAM Enable

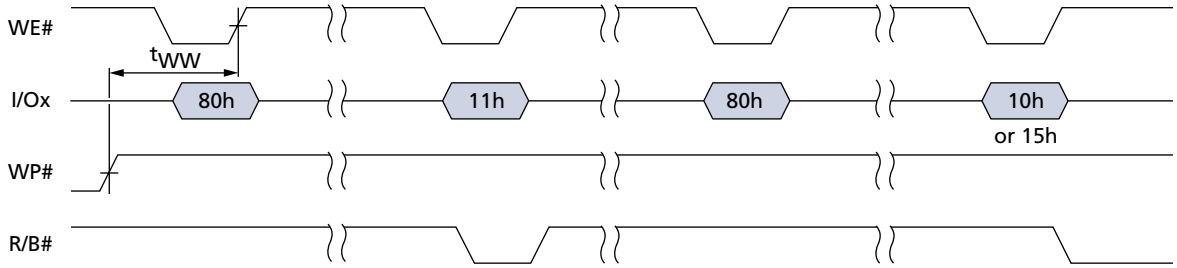


Figure 65: TWO-PLANE PROGRAM Disable

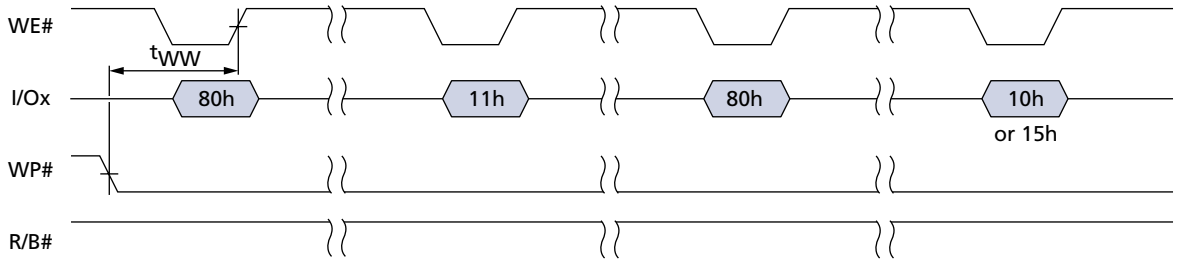


Figure 66: TWO-PLANE PROGRAM for INTERNAL DATA MOVE Enable

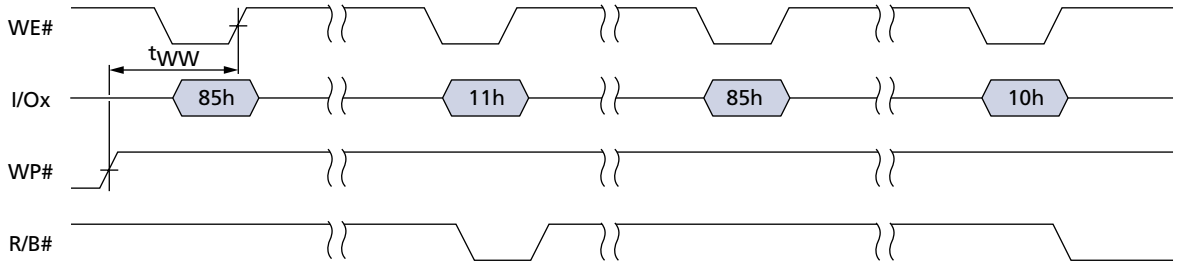
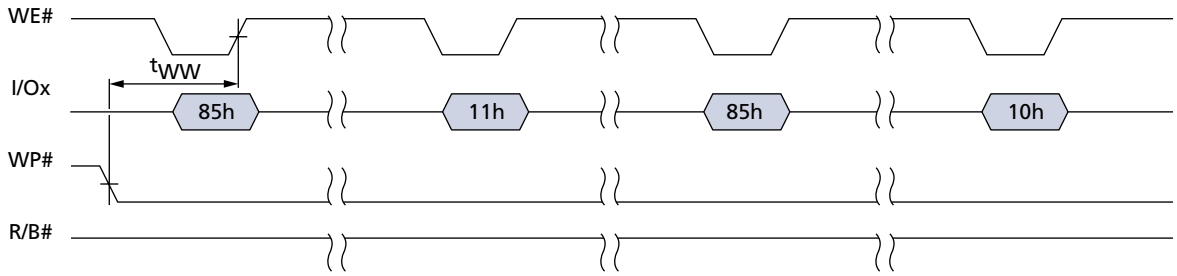


Figure 67: TWO-PLANE PROGRAM for INTERNAL DATA MOVE Disable



Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in Table 21 on page 93. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See Table 17 for the bad-block mark.

System software should initially check the first spare area location on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad- block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Check status after each PROGRAM and ERASE operation.
- Under typical conditions, use the minimum required ECC shown in Table 17.
- Use bad-block management and wear-leveling algorithms.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 17: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB)	4,016
Total available blocks per die	4,096
Minimum required ECC	4-bit ECC per 539 bytes of data
First spare area location	x8: byte 4,096
Bad-block mark	x8: 00h

Electrical Characteristics

Table 18: Absolute Maximum Ratings by Device
Voltage on any pin relative to Vss

Parameter/Condition	Symbol	Min	Max	Unit
Voltage input	VIN	–0.6	+4.6	V
Vcc supply voltage	Vcc	–0.6	+4.6	V
Storage temperature	T_{STG}	–65	+150	°C
Short circuit output current, I/Os		–	5	mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Extended		–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Ground supply voltage		Vss	0	0	0	V

Vcc Power Cycling

Micron NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored. (The WP# signal permits additional hardware protection during power transitions.) When VCC reaches 2.5V for a 3V device, a minimum of 100µs should be allowed for the Flash device to initialize before any commands are executed (see Figure 68 on page 92 for the states of signals during VCC power cycling).

Both of the following conditions must be satisfied before R/B# will be valid:

- 50µs have elapsed since Vcc started its ramp.
- 10µs have elapsed since Vcc reached ≈ 2.5V

The RESET command must be issued to all CE#s as the first command after the NAND Flash device is powered on. Each CE# will be busy for a maximum of 1ms after a RESET command is issued.

Each NAND die will draw no more than IST prior to execution of the first RESET command after the device is powered on.

Each NAND die will draw no more than 10mA of current during the execution of the first RESET command after the device is powered on.

Figure 68: AC Waveforms During Power Transitions

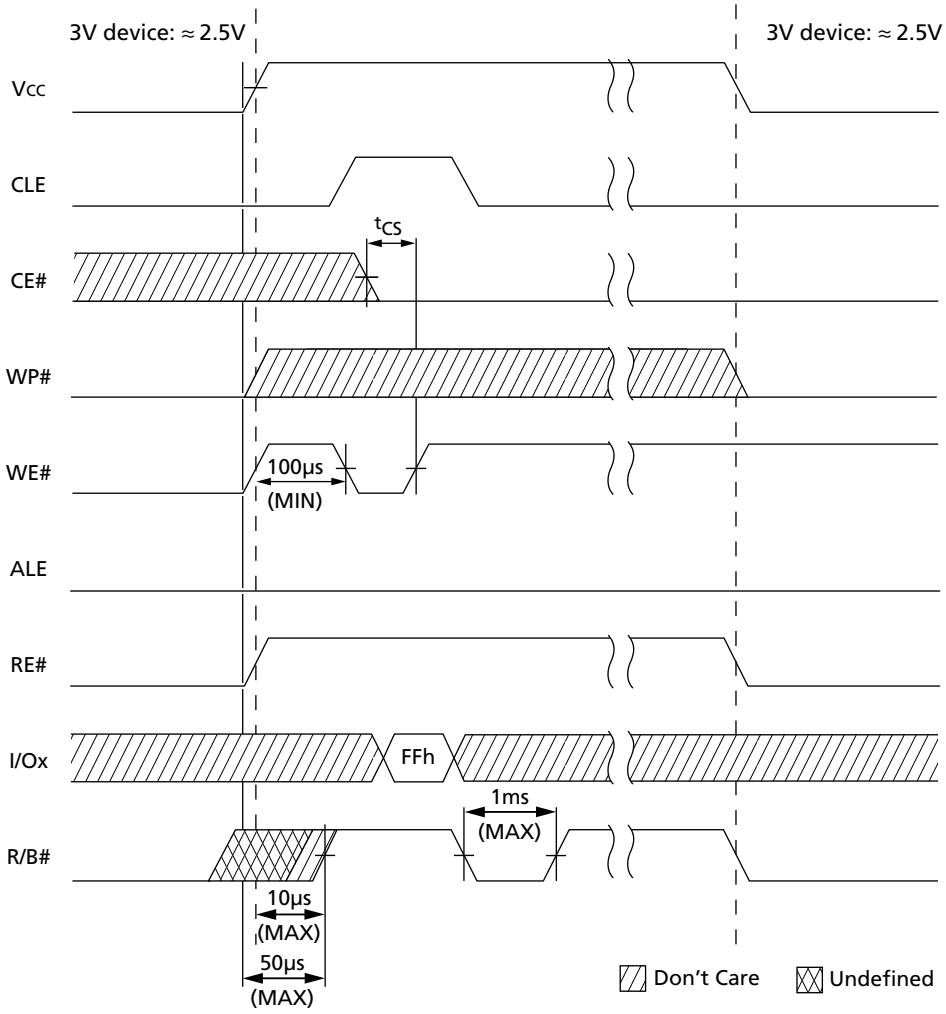


Table 20: Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential read current	$^{t}RC = {}^{t}RC$ (MIN); CE# = VIL; IOUT = 0mA	ICC1	–	20	30	mA	4
Program current	–	ICC2	–	20	30	mA	4
Erase current	–	ICC3	–	20	30	mA	4
Current during first RESET command after power-on	–	ICC4	–	–	10	mA	4
Standby current (TTL)	CE# = VIH; WP# = 0V/VCC	ISB1	–	–	1	mA	
Standby current (CMOS)	CE# = VCC – 0.2V; WP# = 0V/VCC	ISB2	–	10	50	µA	
Input leakage current	VIN = 0V to VCC	ILI	–	–	±10	µA	
Output leakage current	VOUT = 0V to VCC	ILO	–	–	±10	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	IST	–	–	10 per die	mA	3
Input high voltage	I/Ox, CE#, CLE, ALE, WE#, RE#, WP#	VIH	0.8 x VCC	–	VCC + 0.3	V	
Input low voltage (all inputs)	–	VIL	–0.3	–	0.2 x VCC	V	
Output high voltage	IOH = –400µA	VOH	0.67 x VCC	–	–	V	1
Output low voltage	IOL = 2.1mA	VOL	–	–	0.4	V	1
Output low current (R/B#)	VOL = 0.4V	IOL (R/B#)	8	10	–	mA	2

Notes:
1. Test conditions for VOH and VOL.
2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to "full." See Table 15 on page 51 for additional details.
3. Measurement is taken with 1ms averaging intervals and begins after VCC reaches VCC (MIN).
4. This is for single-die operations. It can be greater for interleaved die operations.

Table 21: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	MT29F8G	4,016	4,096	Blocks	1, 2
		MT29F16G	8,032	8,192	Blocks	1, 2, 3
		MT29F32G	16,064	16,384	Blocks	1, 2, 4
		MT29F64G	32,128	32,768	Blocks	1, 2, 4

Notes:
1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block per each chip enable) is guaranteed to be valid with ECC when shipped from the factory.
3. Each 8Gb section has a maximum of 80 invalid blocks.
4. Each 16Gb section has a maximum of 160 invalid blocks, not to exceed 80 invalid blocks for each NAND Flash die.

Table 22: Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	C_{IN}	MT29F8G	5	pF	1, 2
		MT29F16G	10		
		MT29F32G	20		
		MT29F64G	20		
Input/output capacitance (I/O)	C_{OUT}	MT29F8G	5	pF	1, 2
		MT29F16G	10		
		MT29F32G	20		
		MT29F64G	20		

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_c = 25°C; f = 1 MHz; V_{IN} = 0V.

Table 23: Test Conditions

Parameter		Value	Notes
Input pulse levels	MT29FxxG08xAA	0.0V to 3.3V	
Input rise and fall times		5ns	
Input and output timing levels		Vcc/2	
Output load	MT29FxxG08xAA (V_{CC} = 3.0V ± 10%)	1 TTL GATE and CL = 50pF	1
	MT29FxxG08xAA (V_{CC} = 3.3V ± 10%)	1 TTL GATE and CL = 100pF	1

Notes: 1. Verified in device characterization; not 100 percent tested.

Table 24: AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Min[1]	Max[1]	Unit	Notes
ALE to data start	^tADL	70	–	ns	2
ALE hold time	^tALH	5	–	ns	
ALE setup time	^tALS	10	–	ns	
CE# hold time	^tCH	5	–	ns	
CLE hold time	^tCLH	5	–	ns	
CLE setup time	^tCLS	10	–	ns	
CE# setup time	^tCS	15	–	ns	
Data hold time	^tDH	5	–	ns	
Data setup time	^tDS	7	–	ns	
WRITE cycle time	^tWC	20	–	ns	
WE# pulse width HIGH	^tWH	7	–	ns	
WE# pulse width	^tWP	10	–	ns	
WP# setup time	^tWW	30	–	ns	

Notes: 1. Operating-mode timings meet ONFI timing mode 5 parameters.
2. Timing for ^tADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.

Table 25: AC Characteristics: Normal Operation

Parameter	Symbol	Min[1]	Max[1]	Unit	Notes
ALE to RE# delay	tAR	10	–	ns	
Change column setup time	tCCS	70	–	ns	
CE# access time	tCEA	–	25	ns	
CE# HIGH to output High-Z	tCHZ	–	30	ns	2
CLE to RE# delay	tCLR	10	–	ns	
CE# HIGH to output hold	tCOH	15		ns	
Cache busy in page read cache mode (first 31h)	tDCBSYR1	–	5	µs	
Cache busy in page read cache mode (next 31h and 3Fh)	tDCBSYR2	tDCBSYR1	25	µs	
Output High-Z to RE# LOW	tIR	0	–	ns	
Data transfer from Flash array to data register	tR	–	25	µs	
READ cycle time	tRC	25	–	ns	
RE# access time	tREA	–	20	ns	3
RE# HIGH hold time	tREH	7	–	ns	3
RE# HIGH to output hold	tRHOH	15	–	ns	3
RE# HIGH to WE# LOW	tRHW	100	–		
RE# HIGH to output High-Z	tRHZ	–	100	ns	2, 3
RE# LOW to output hold	tRLOH	5		ns	
RE# pulse width	tRP	10	–	ns	
Ready to RE# LOW	tRR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	tRST	–	5/10/500	µs	4
WE# HIGH to busy	tWB	–	100	ns	5
WE# HIGH to RE# LOW	tWHR	60	–	ns	

Notes:
1. Operating-mode timings meet ONFI timing mode 4 parameters.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if I/O drive strength is not set to "full." See Table 14 on page 50 for additional details.
4. If RESET (FFh) command is loaded at ready state, the device goes busy for maximum 5µs.
5. Do not issue a new command during tWB, even if R/B# is ready.

Table 26: PROGRAM/ERASE Characteristics

Symbol	Parameter	Typ	Max	Unit	Notes
NOP	Number of partial-page programs	–	4	cycles	1
^{t}BERS	BLOCK ERASE operation time	0.7	3	ms	
^{t}CBSY	Busy time for CACHE PROGRAM operation	20	700	µs	2
^{t}DBSY	Dummy busy time for two-plane operations	0.5	1	µs	
^{t}FEAT	Busy time for SET FEATURES and GET FEATURES operations	–	1	µs	
^{t}LPROG	LAST PAGE PROGRAM operation time	–	–	–	3
^{t}OBSY	Busy time for OTP DATA PROGRAM operation if OTP is protected	–	25	µs	
^{t}PROG	PROGRAM PAGE operation time	250	700	µs	

Notes: 1. Four total to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

Timing Diagrams

Figure 69: COMMAND LATCH Cycle

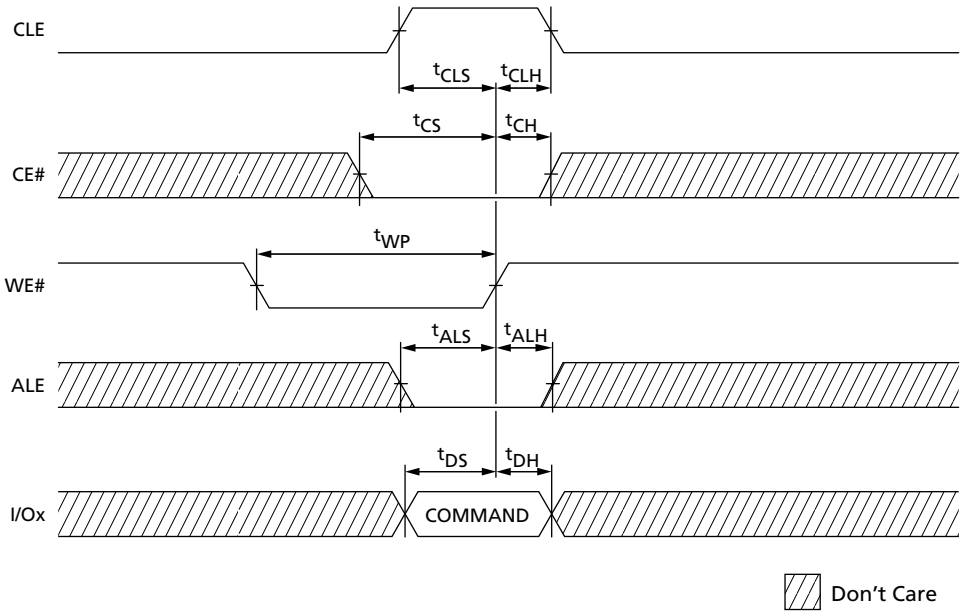


Figure 70: ADDRESS LATCH Cycle

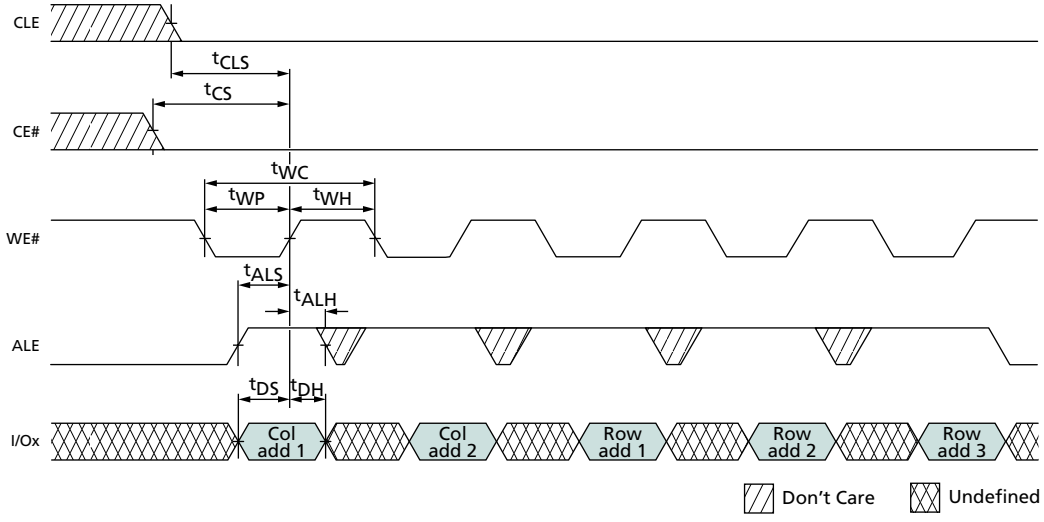
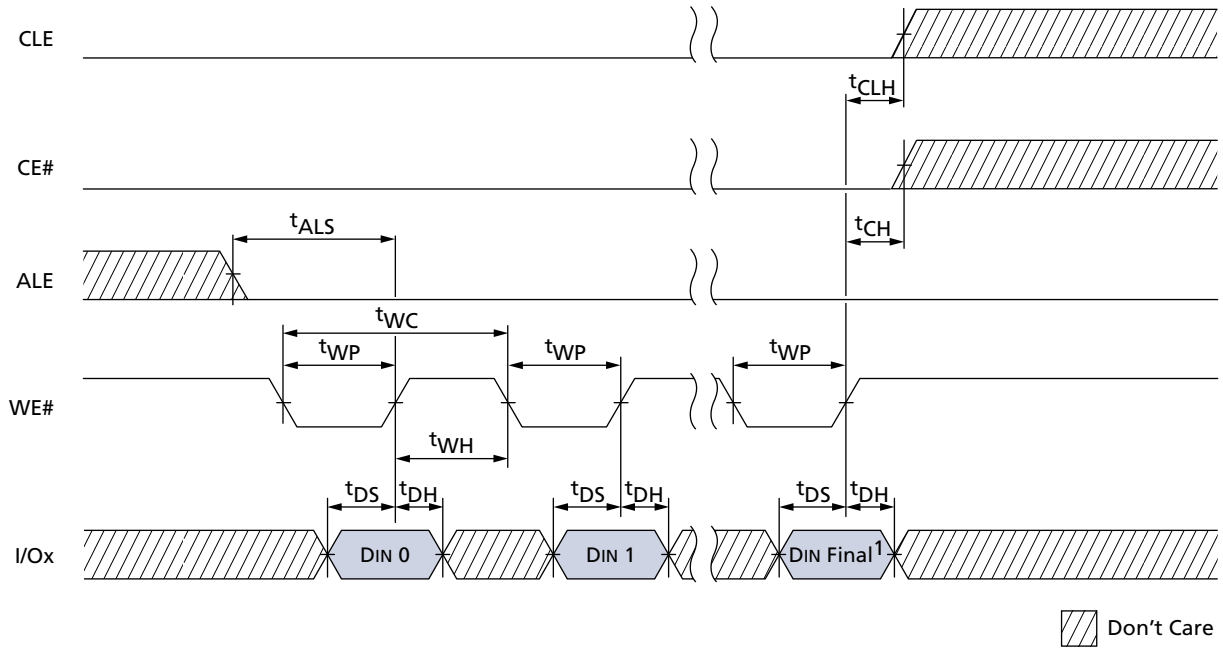
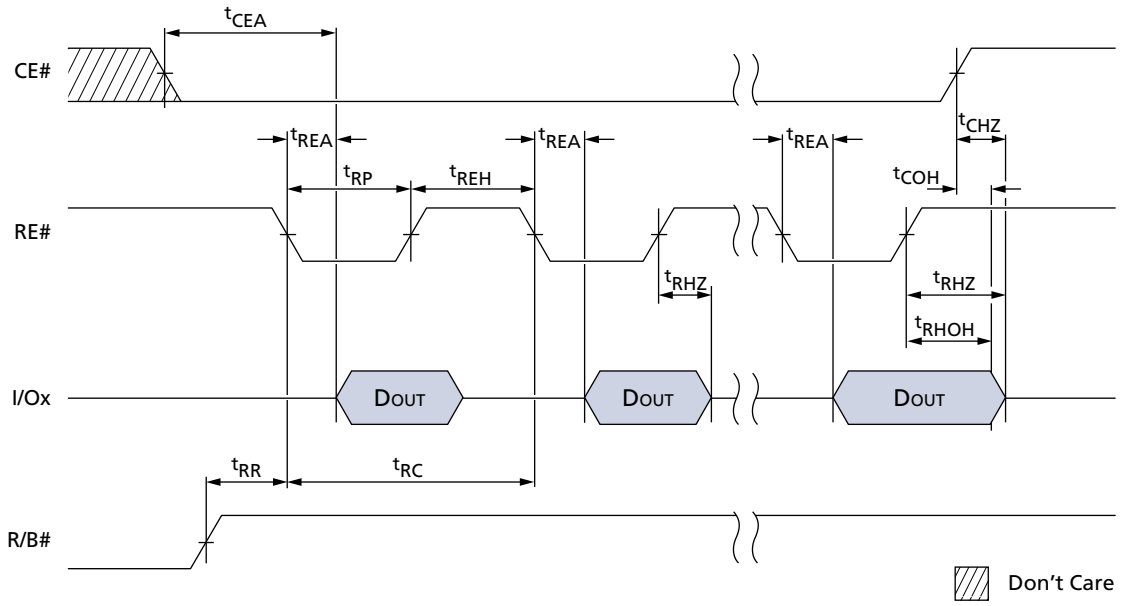


Figure 71: INPUT DATA LATCH Cycle



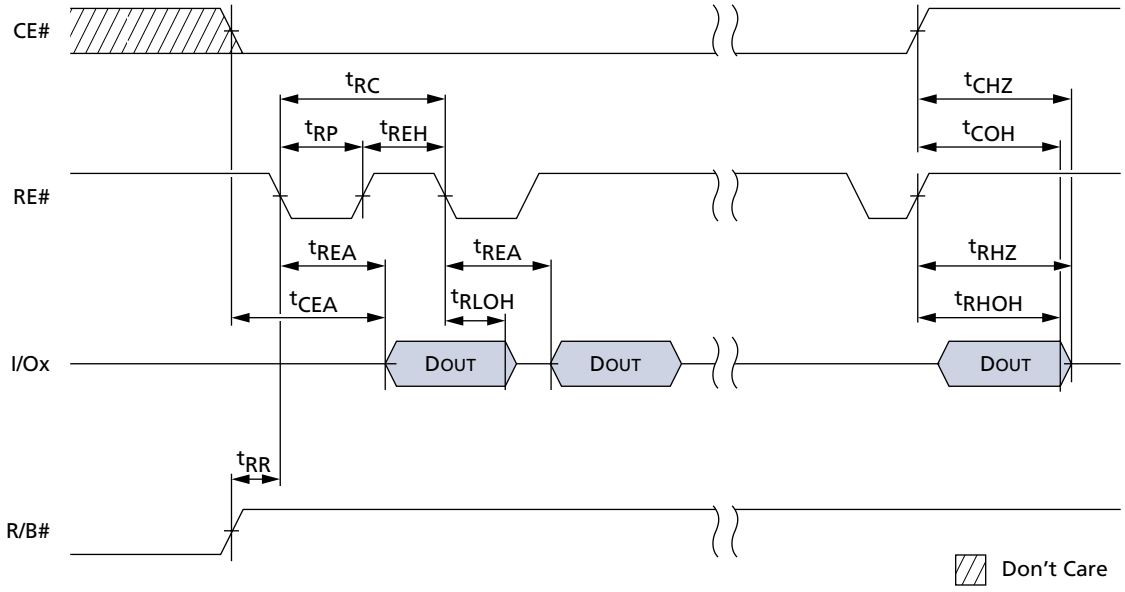
Notes: 1. DIN Final = 4,313 (x8)

Figure 72: SERIAL ACCESS Cycle After READ



Note: Use this timing diagram for $^{t}RC \geq 30ns$.

Figure 73: SERIAL ACCESS Cycle After READ (EDO Mode)



Note: Use this timing diagram for $^{t}RC < 30ns$.

Figure 74: READ STATUS Cycle

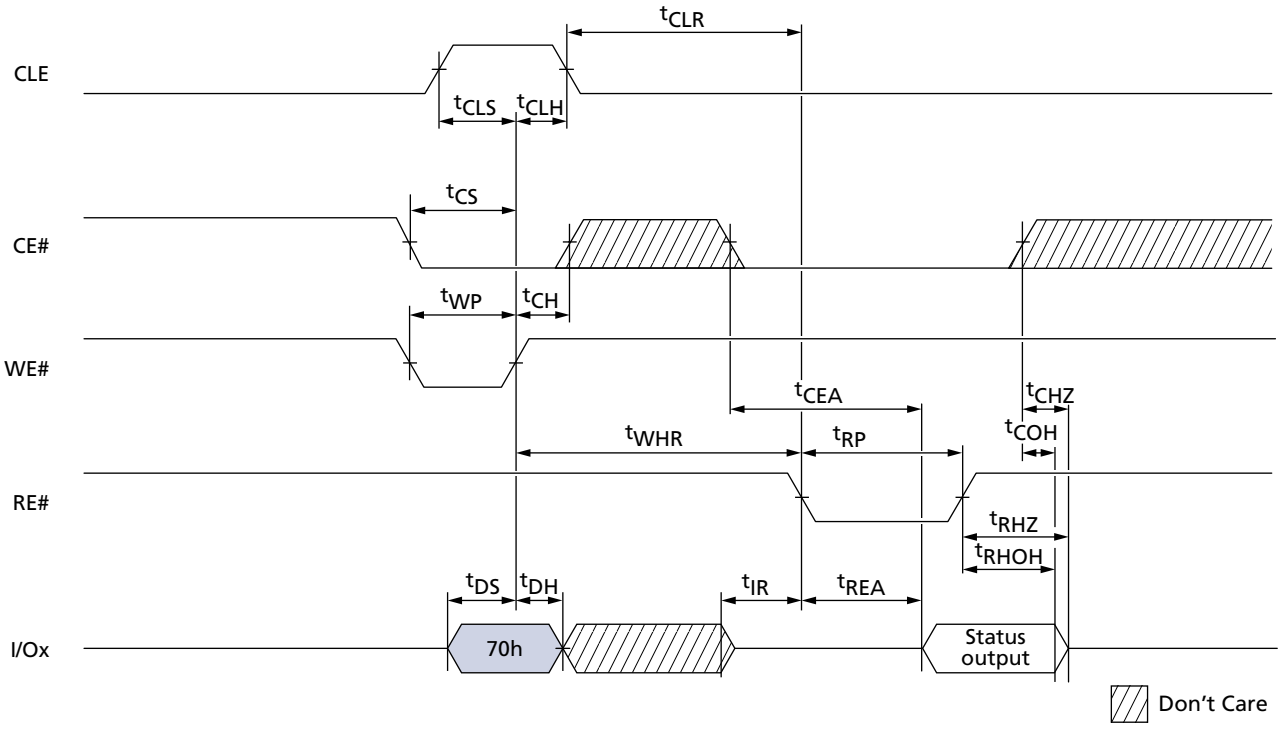


Figure 75: TWO-PLANE/MULTIPLE-DIE READ STATUS Operation

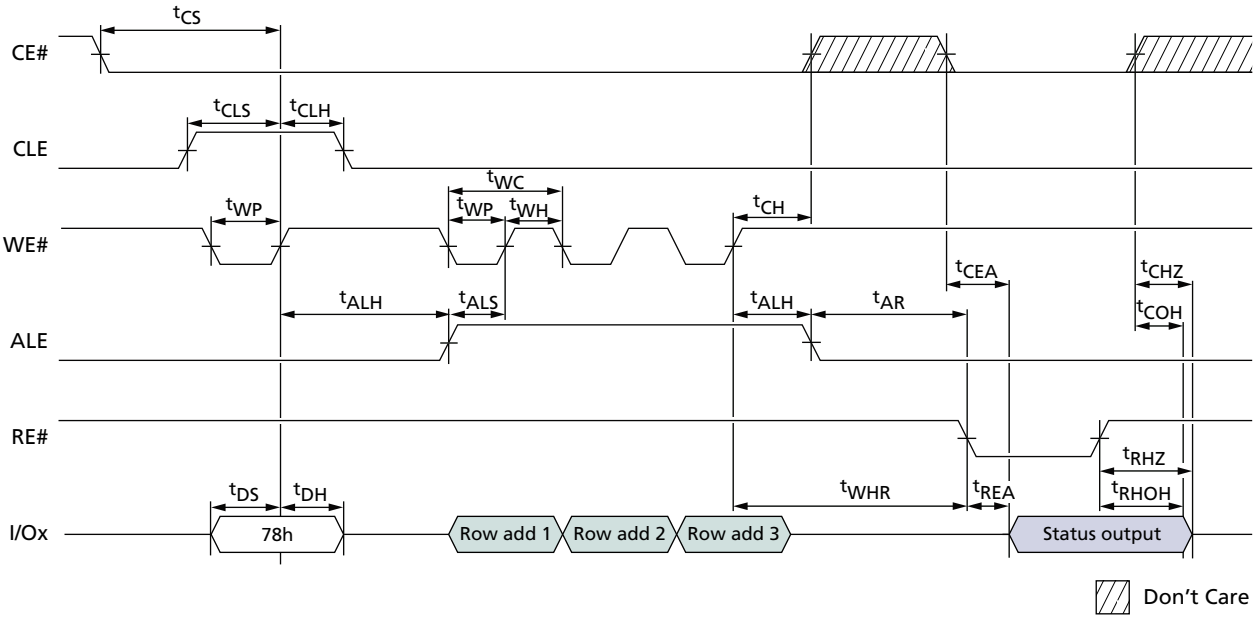


Figure 76: PAGE READ Operation

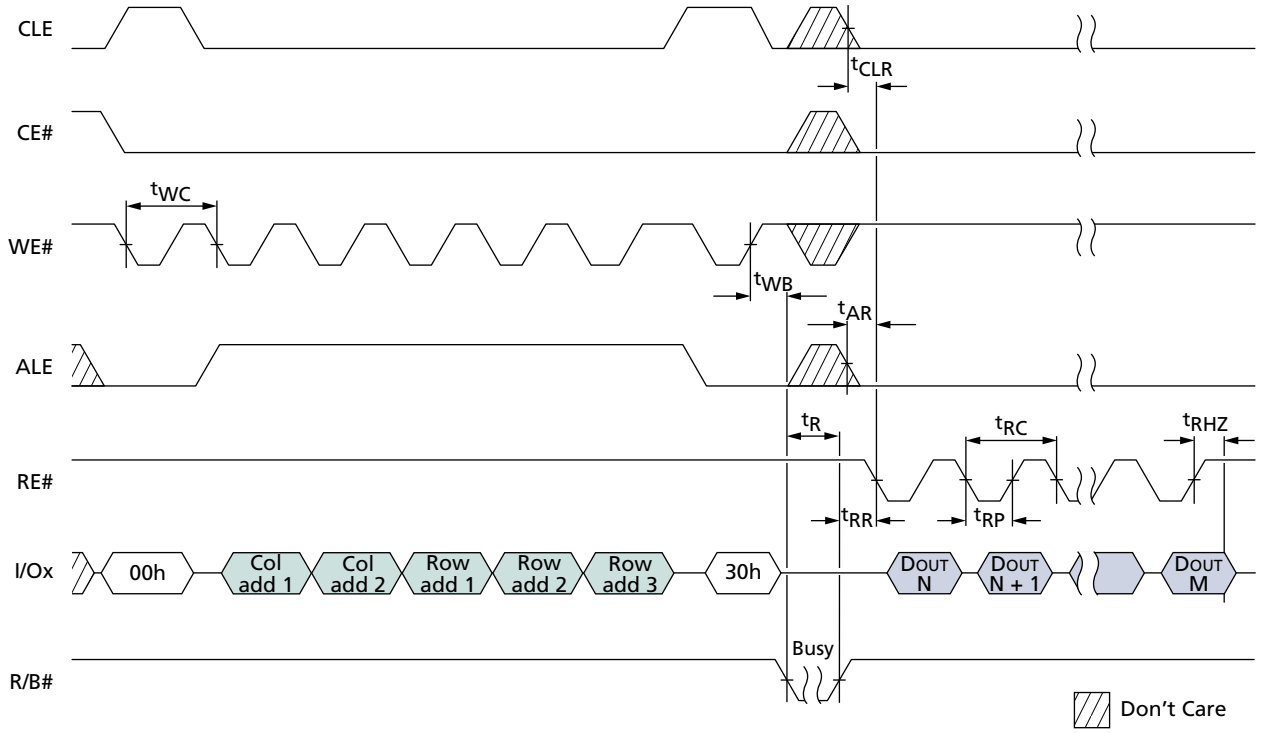


Figure 77: READ Operation with CE# "Don't Care"

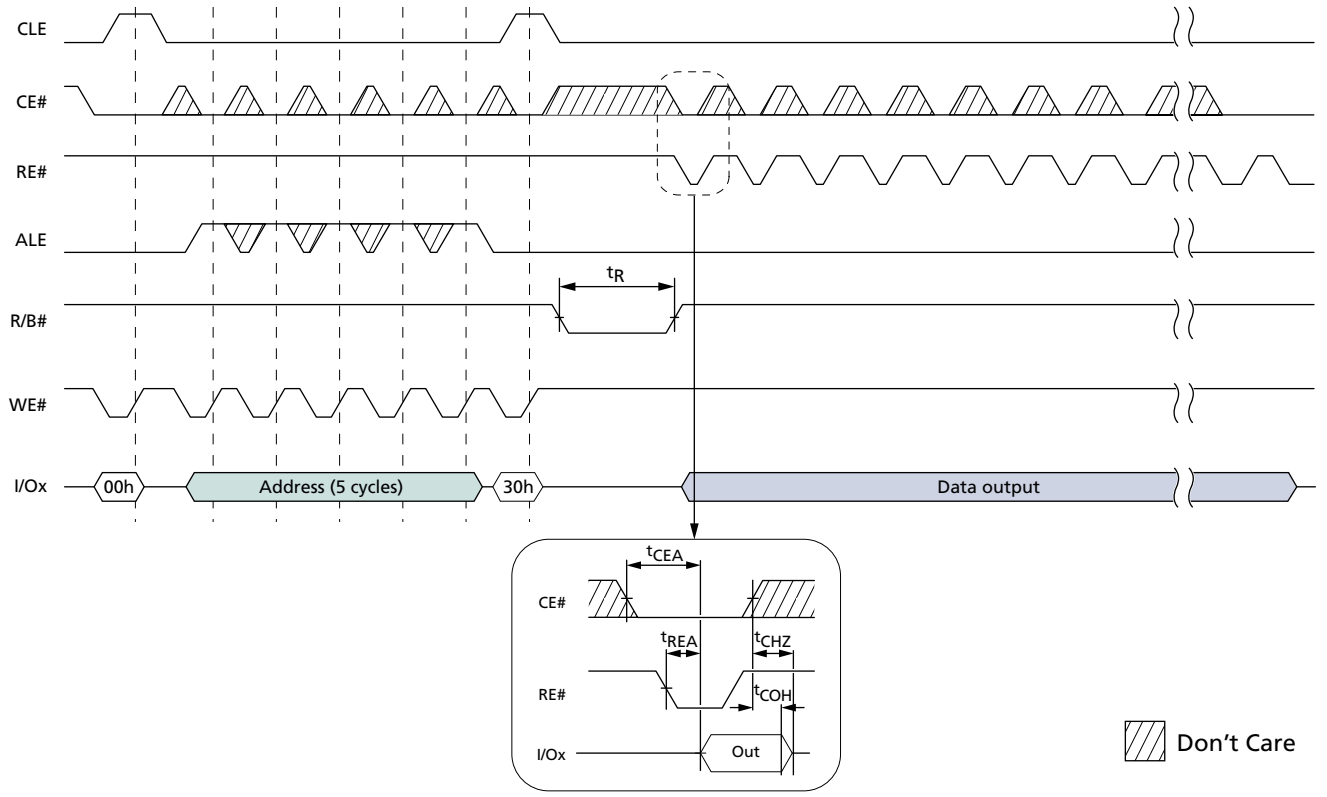
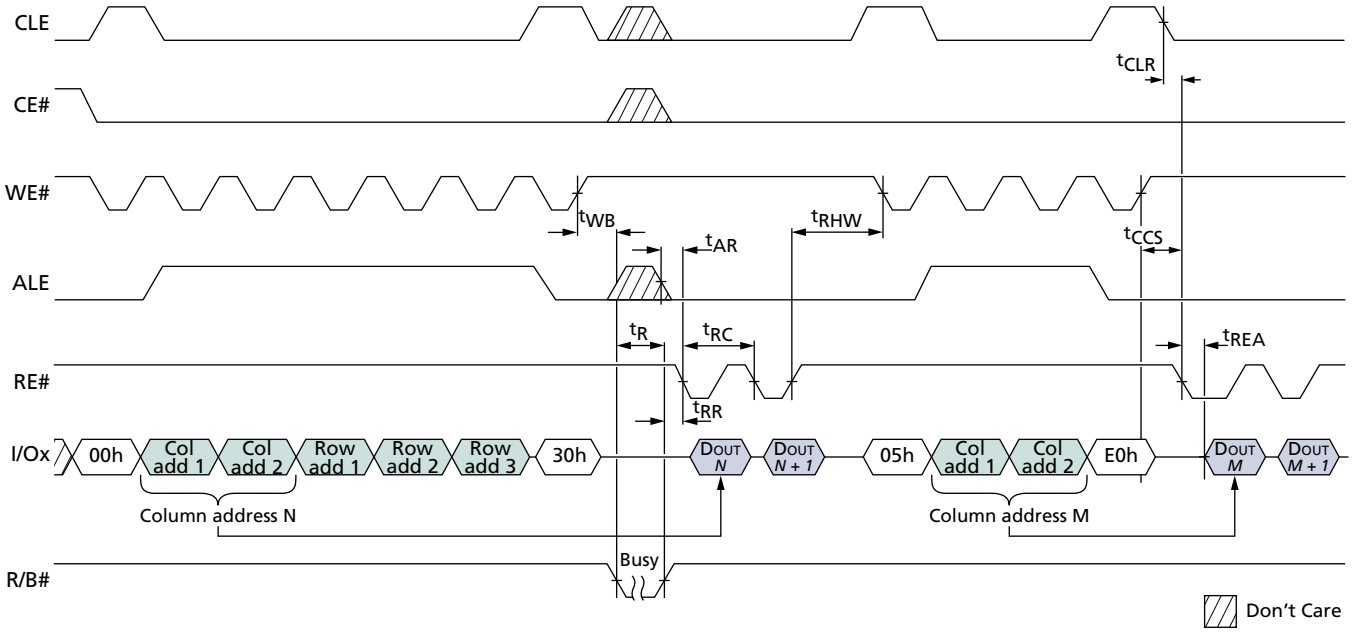


Figure 78: RANDOM DATA READ Operation



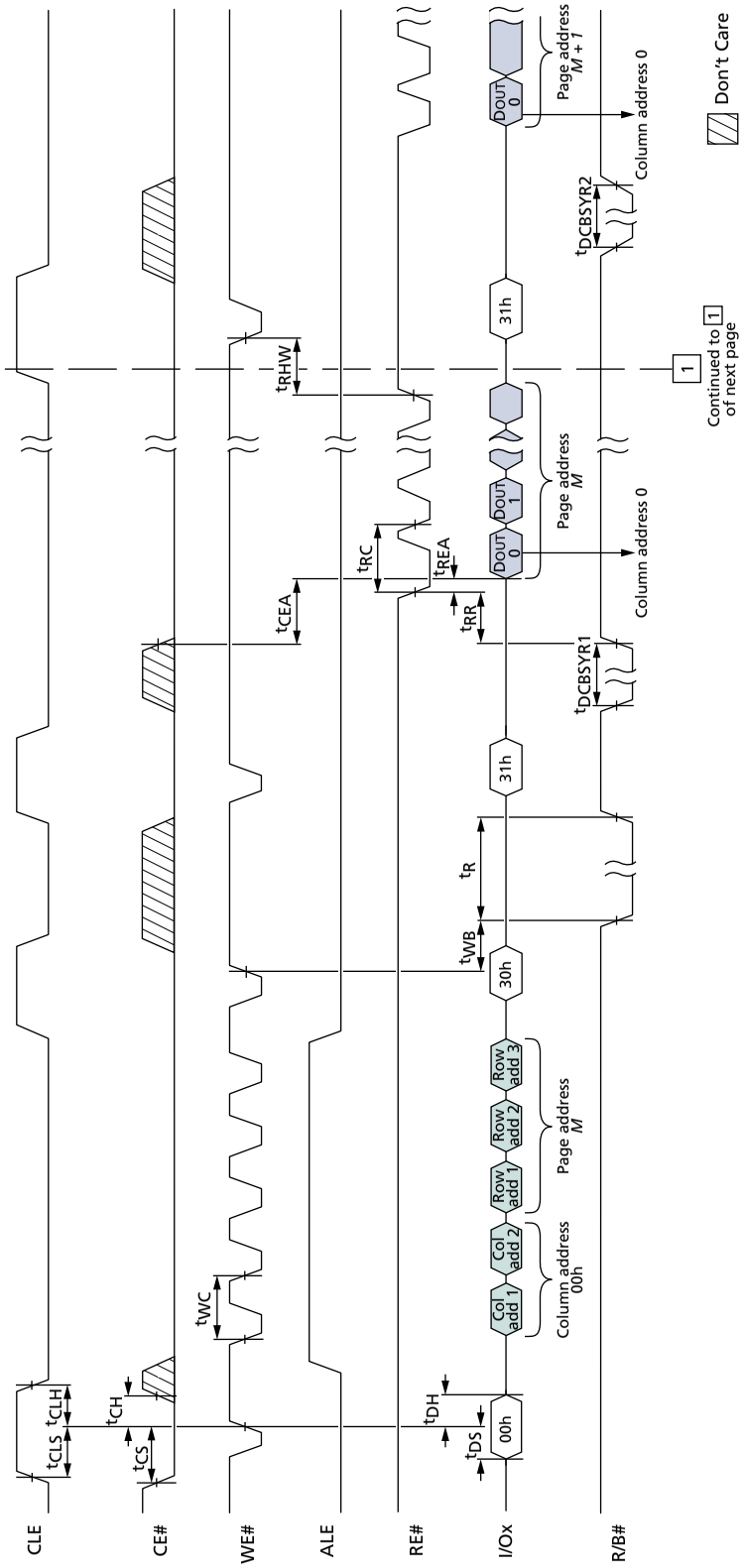


Figure 79: PAGE READ CACHE MODE Operation, Part 1 of 2

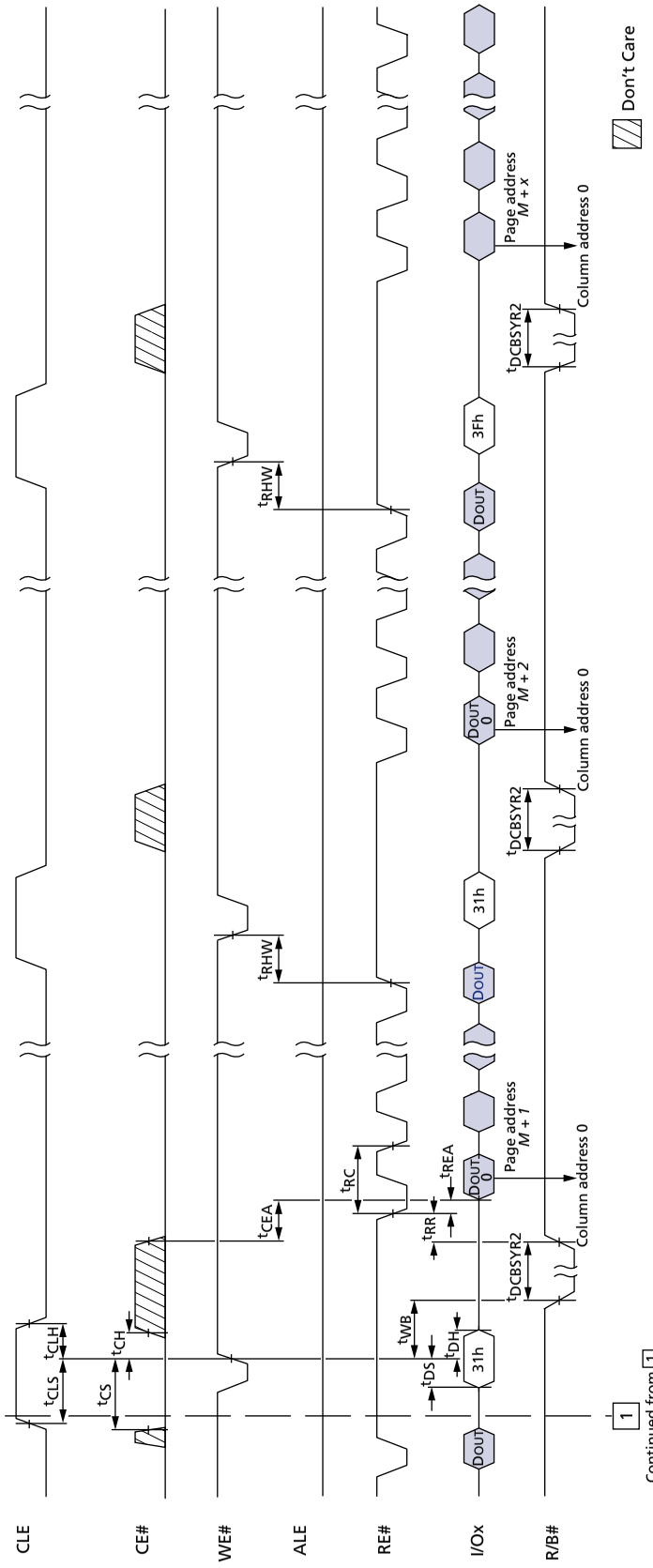


Figure 80: PAGE READ CACHE MODE Operation, Part 2 of 2

Figure 81: PAGE READ CACHE MODE Operation without R/B#, Part 1 of 2

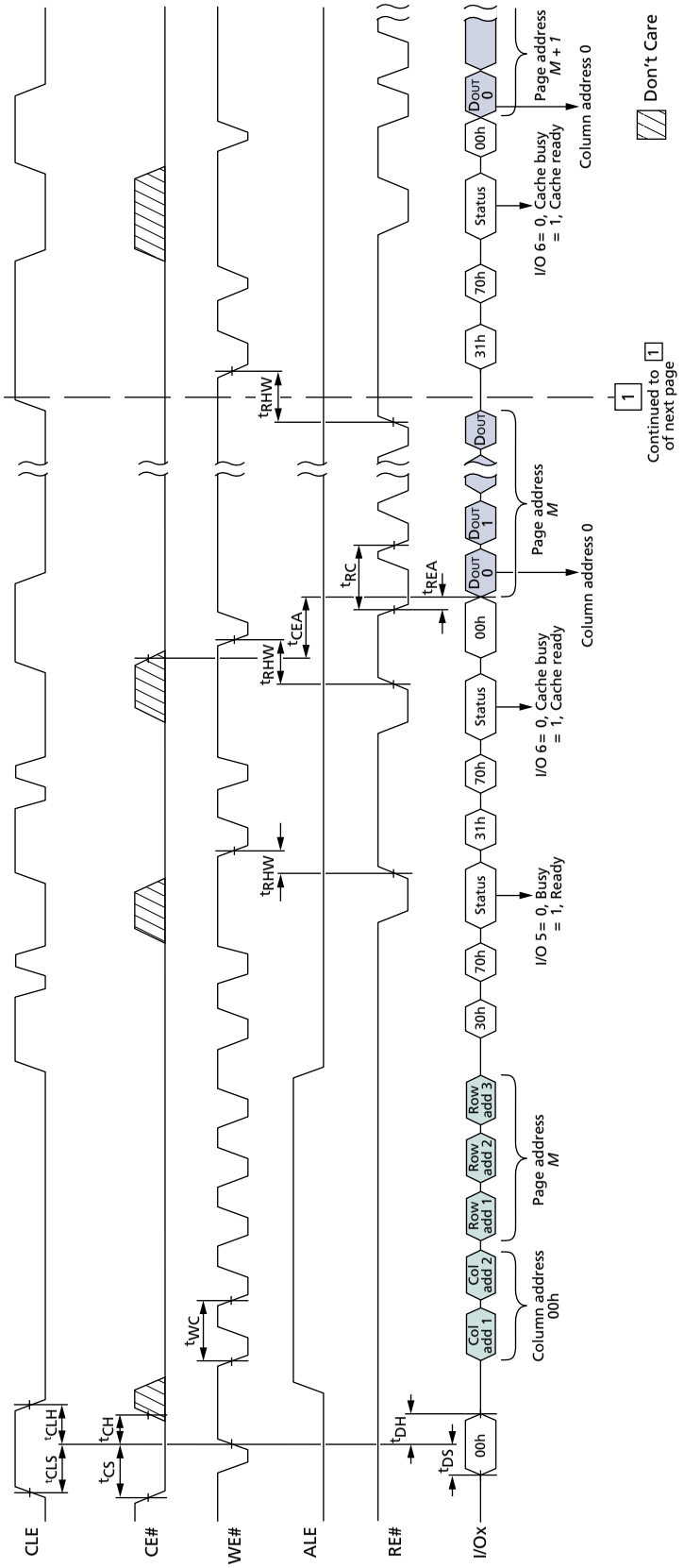
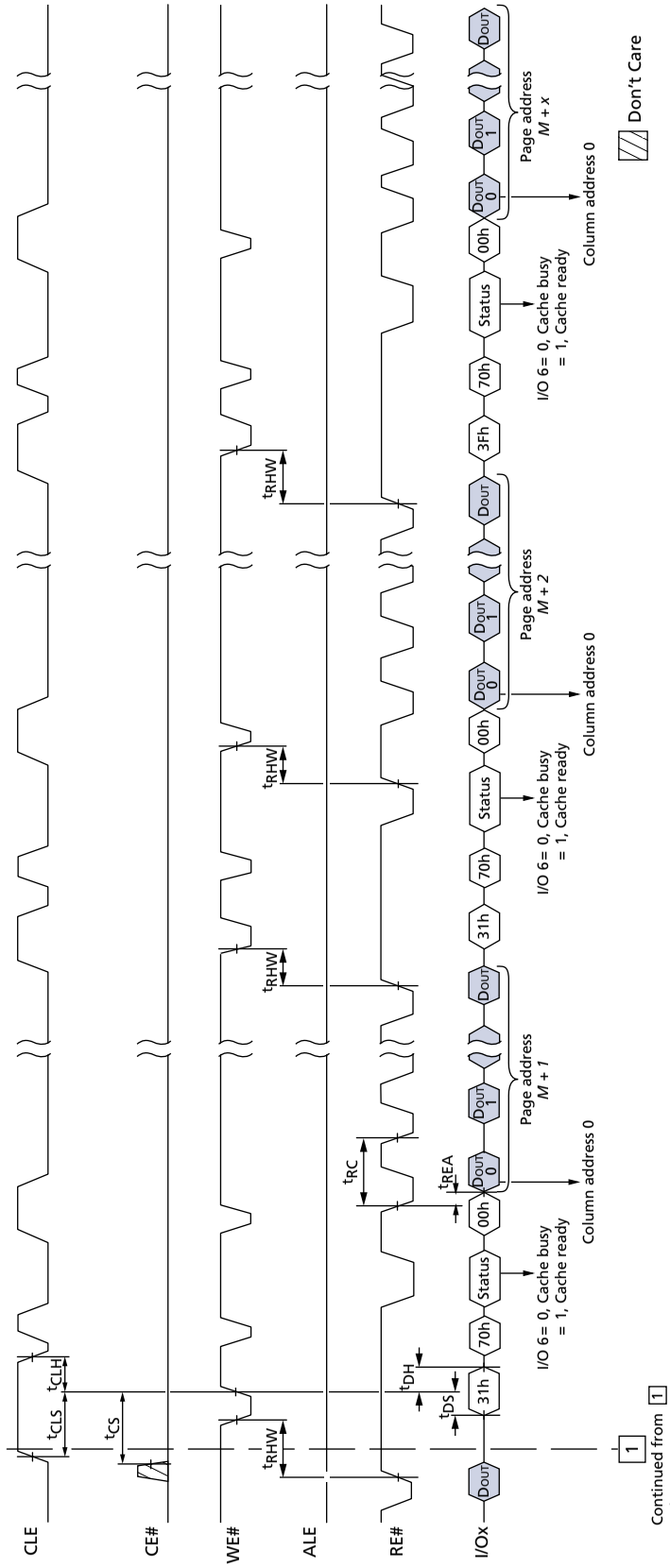
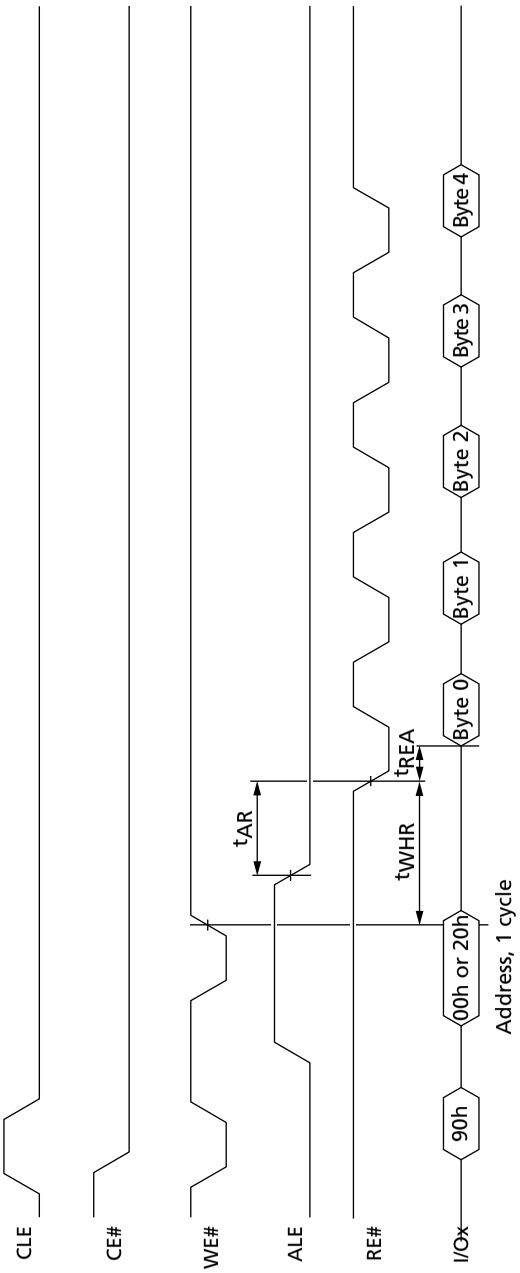


Figure 82: PAGE READ CACHE MODE Operation without R/B#, Part 2 of 2





Note: See Table 9 on page 27 for actual values.

Figure 83: READ ID Operation

Figure 84: PROGRAM PAGE Operation

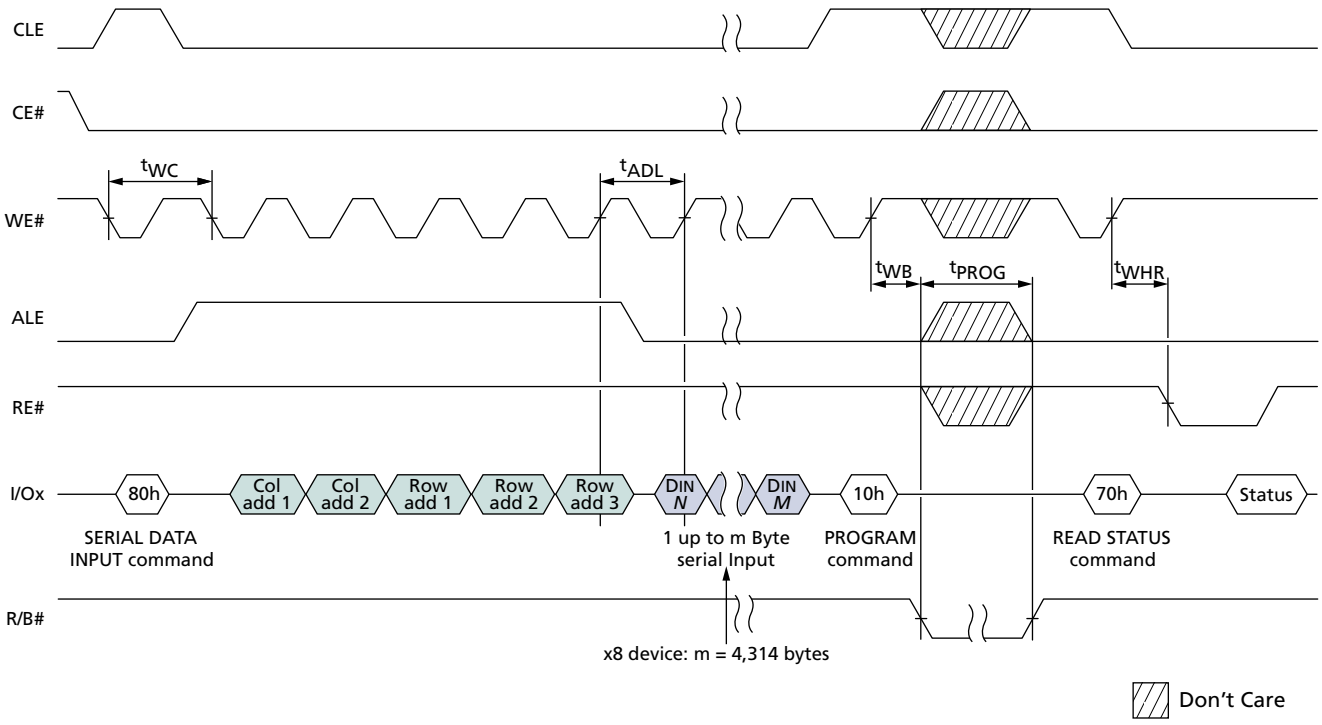


Figure 85: Program Operation with CE# "Don't Care"

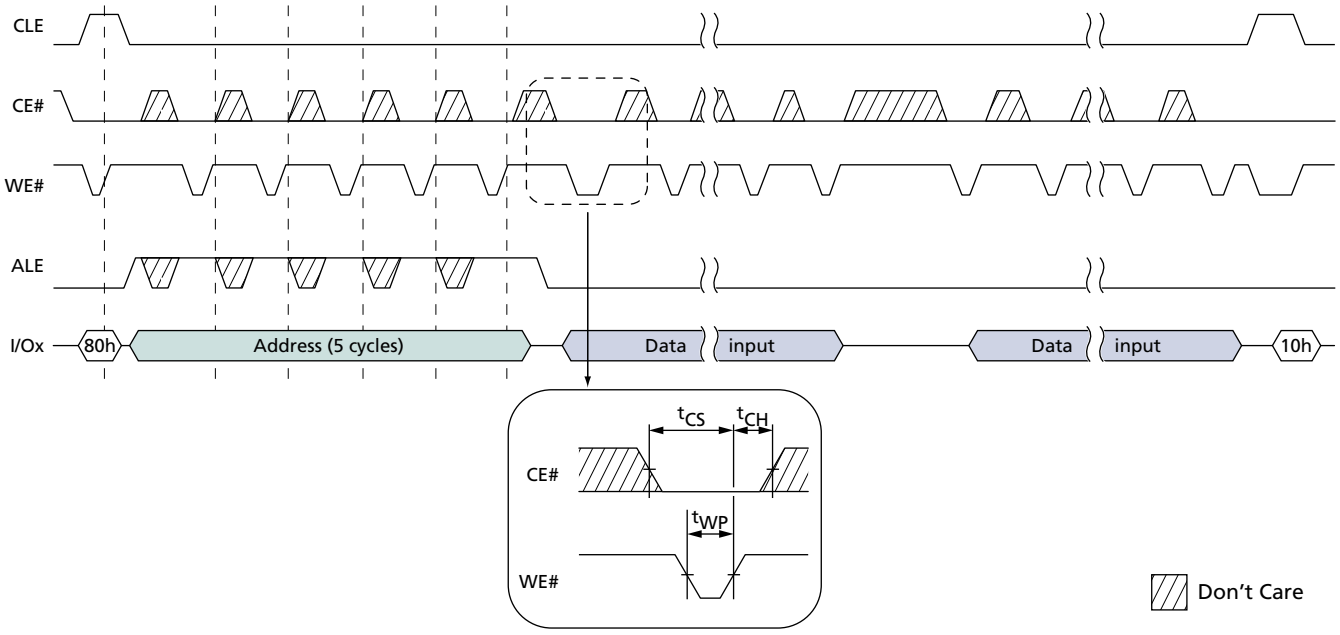


Figure 86: PROGRAM PAGE Operation with RANDOM DATA INPUT

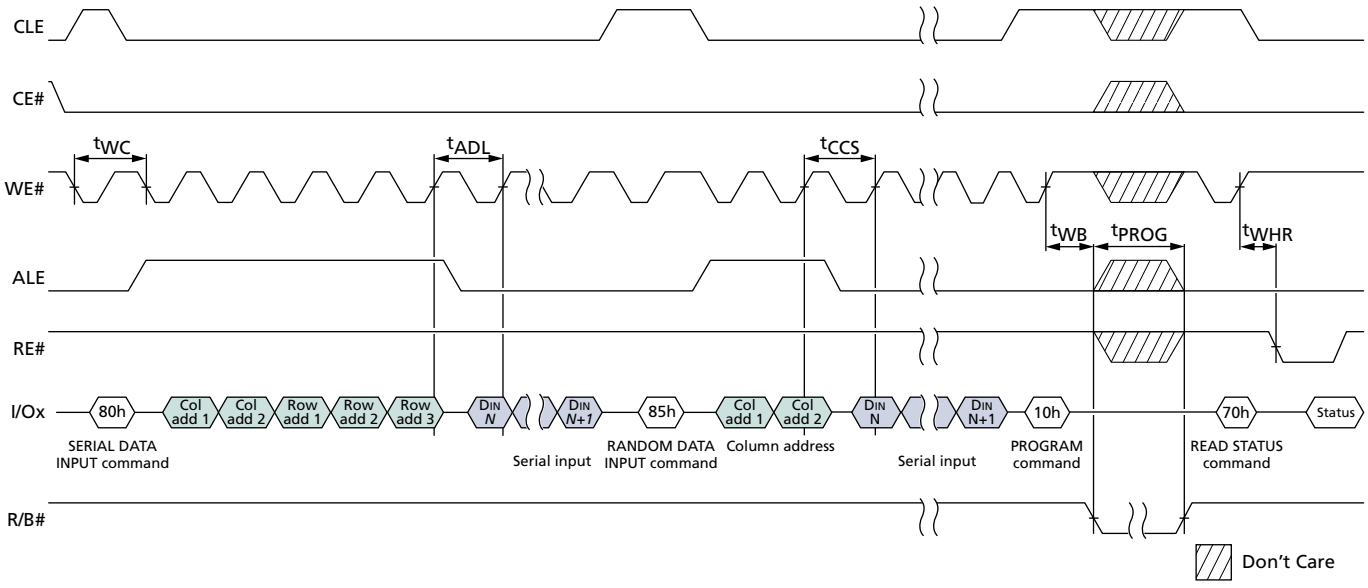


Figure 87: INTERNAL DATA MOVE Operation

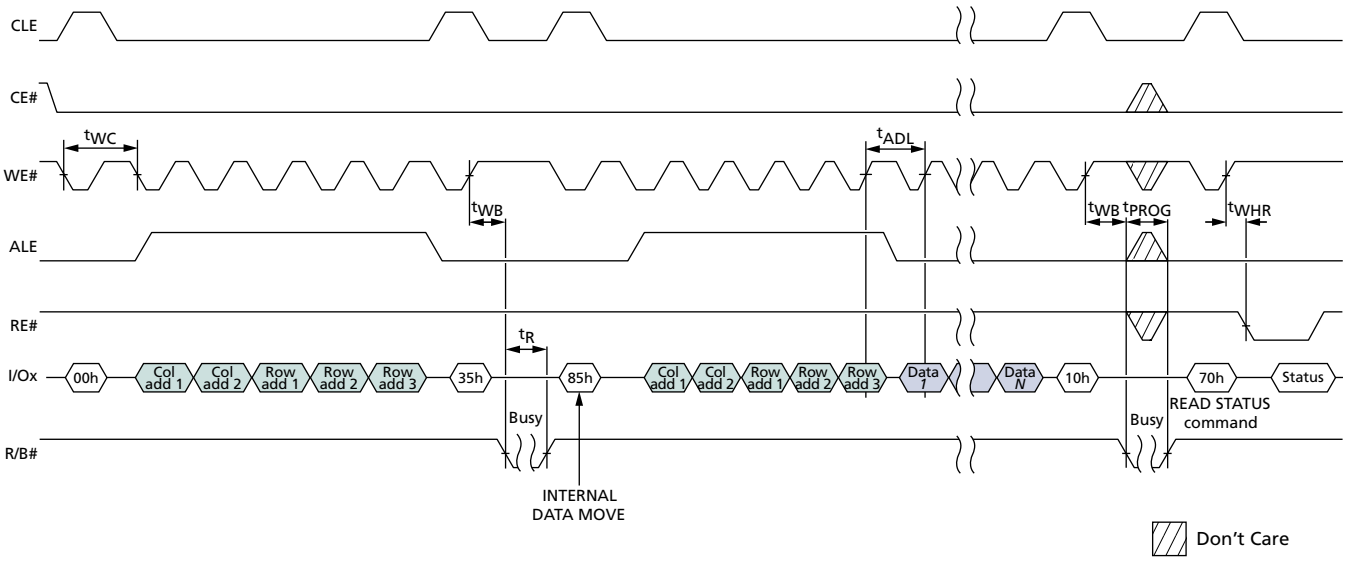


Figure 88: PROGRAM PAGE CACHE MODE Operation

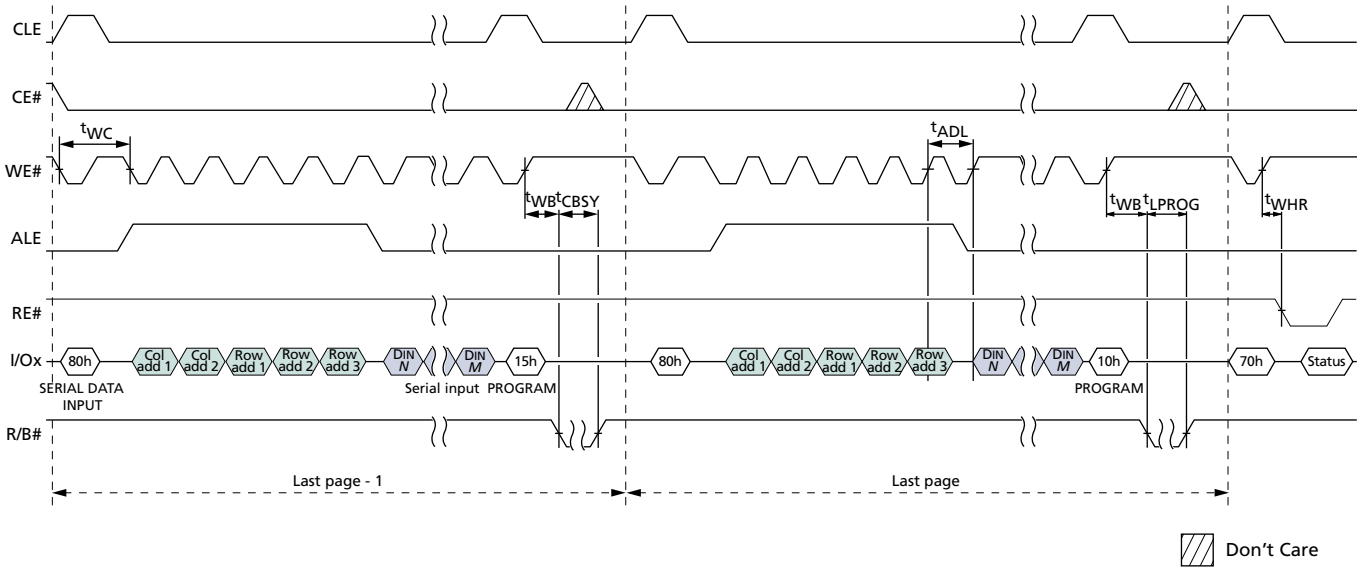


Figure 89: PROGRAM PAGE CACHE MODE Operation Ending on 15h

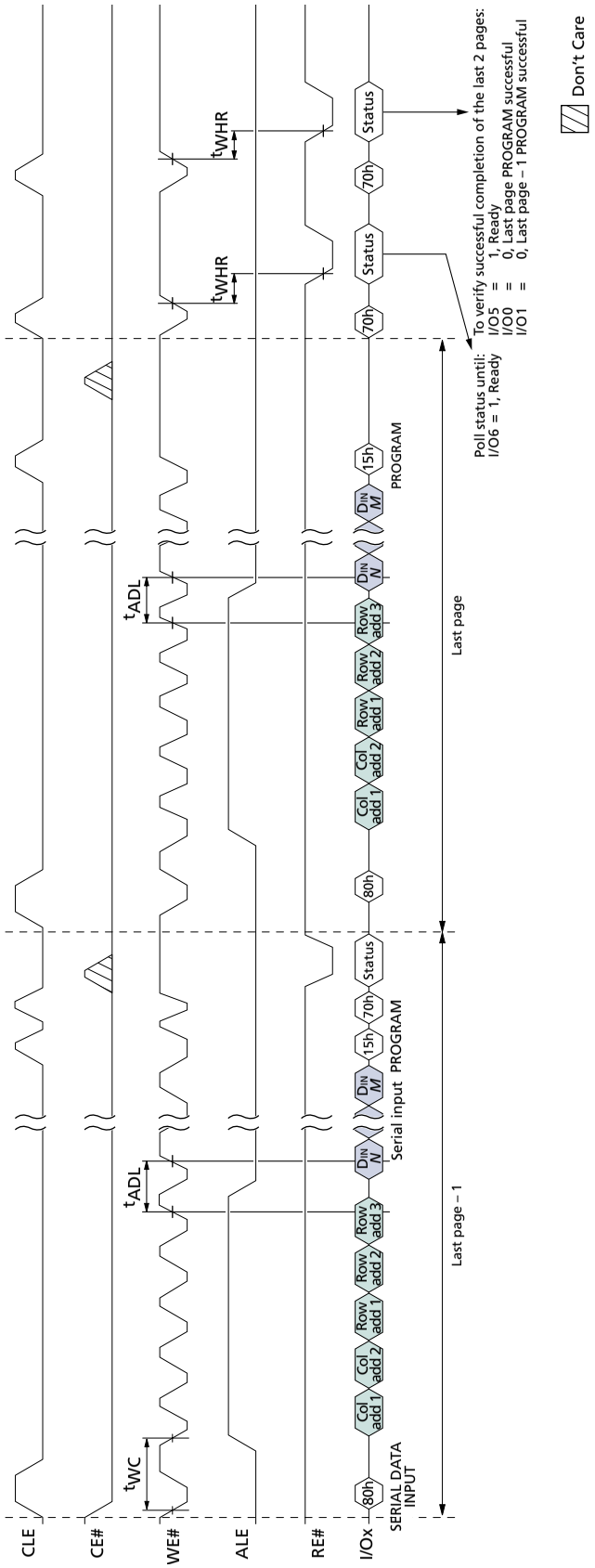


Figure 90: BLOCK ERASE Operation

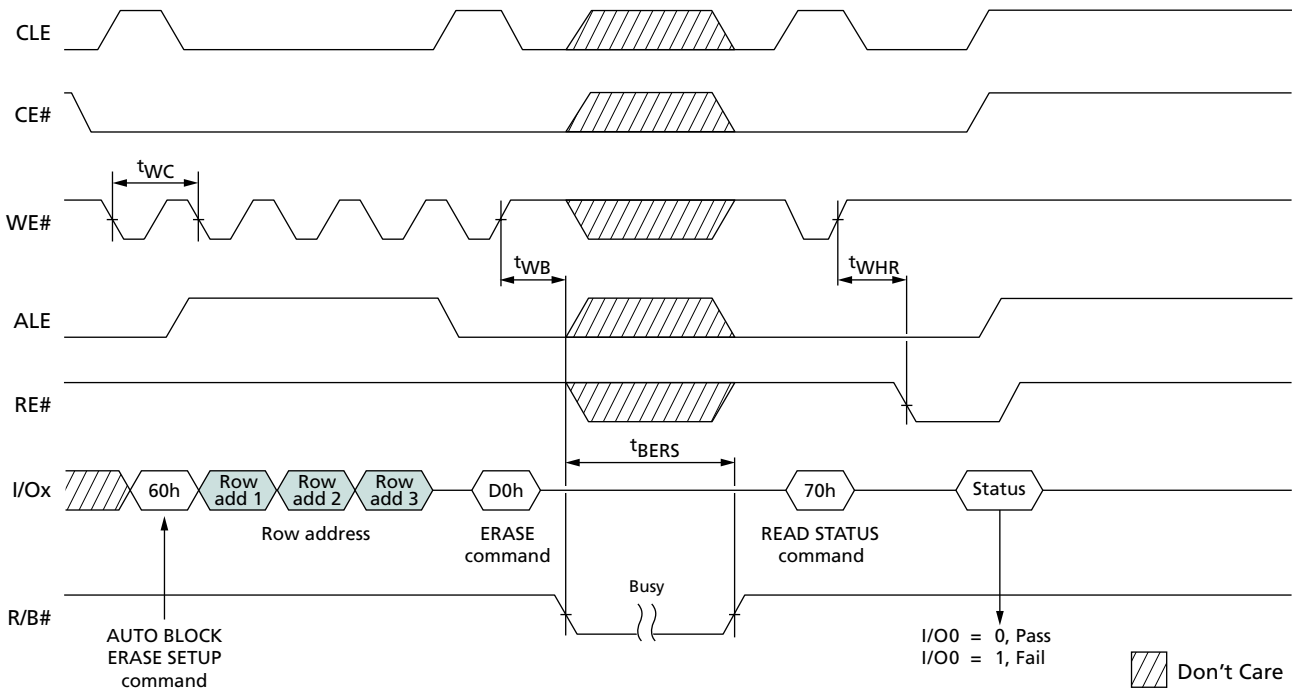
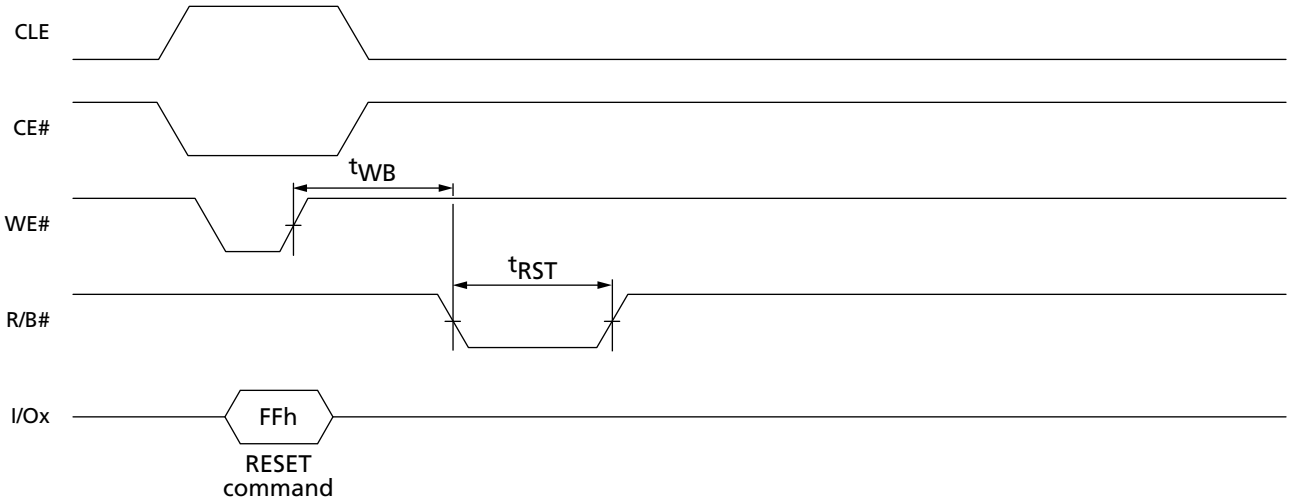
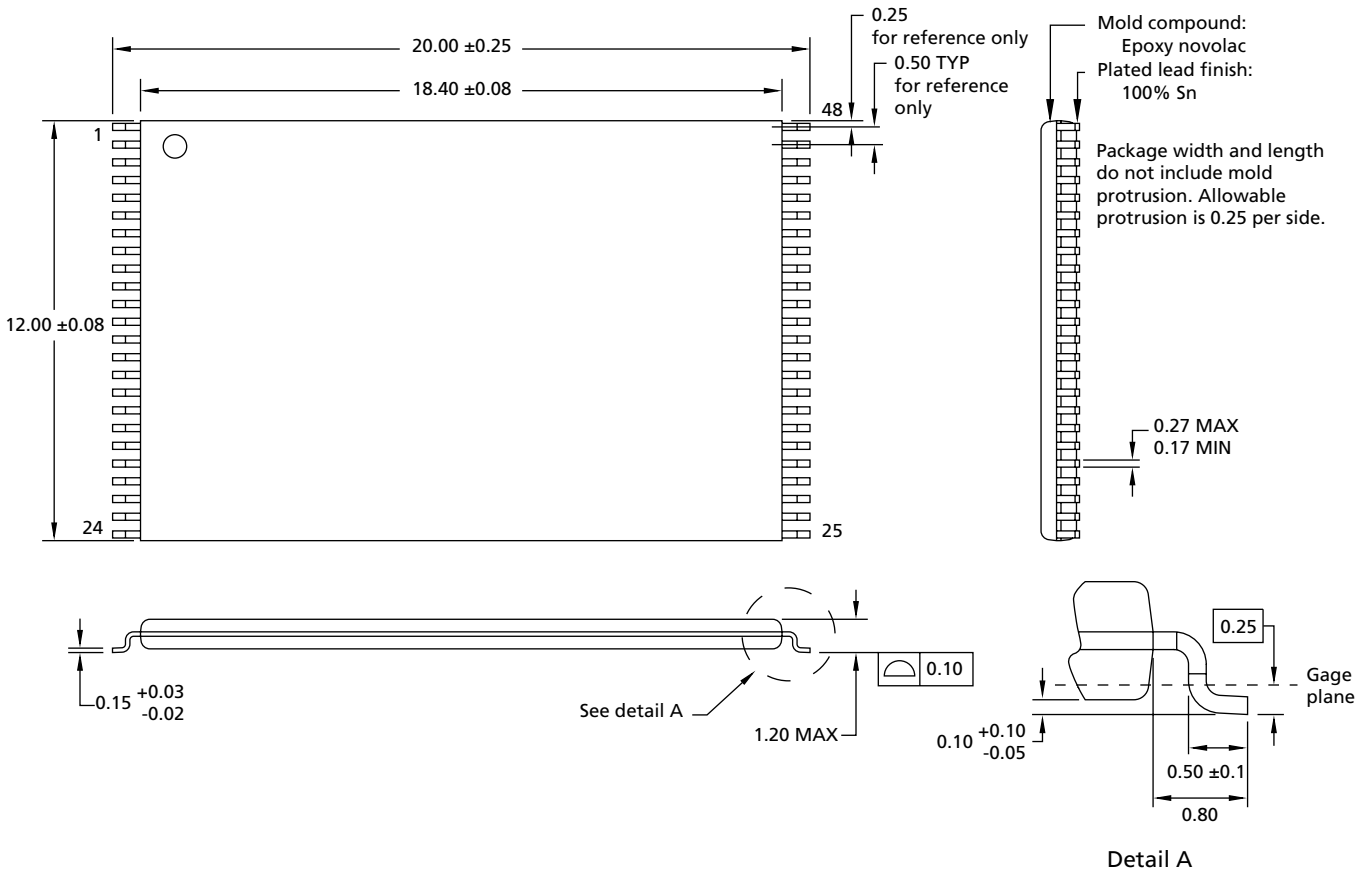


Figure 91: RESET Operation



TSOP Package Information

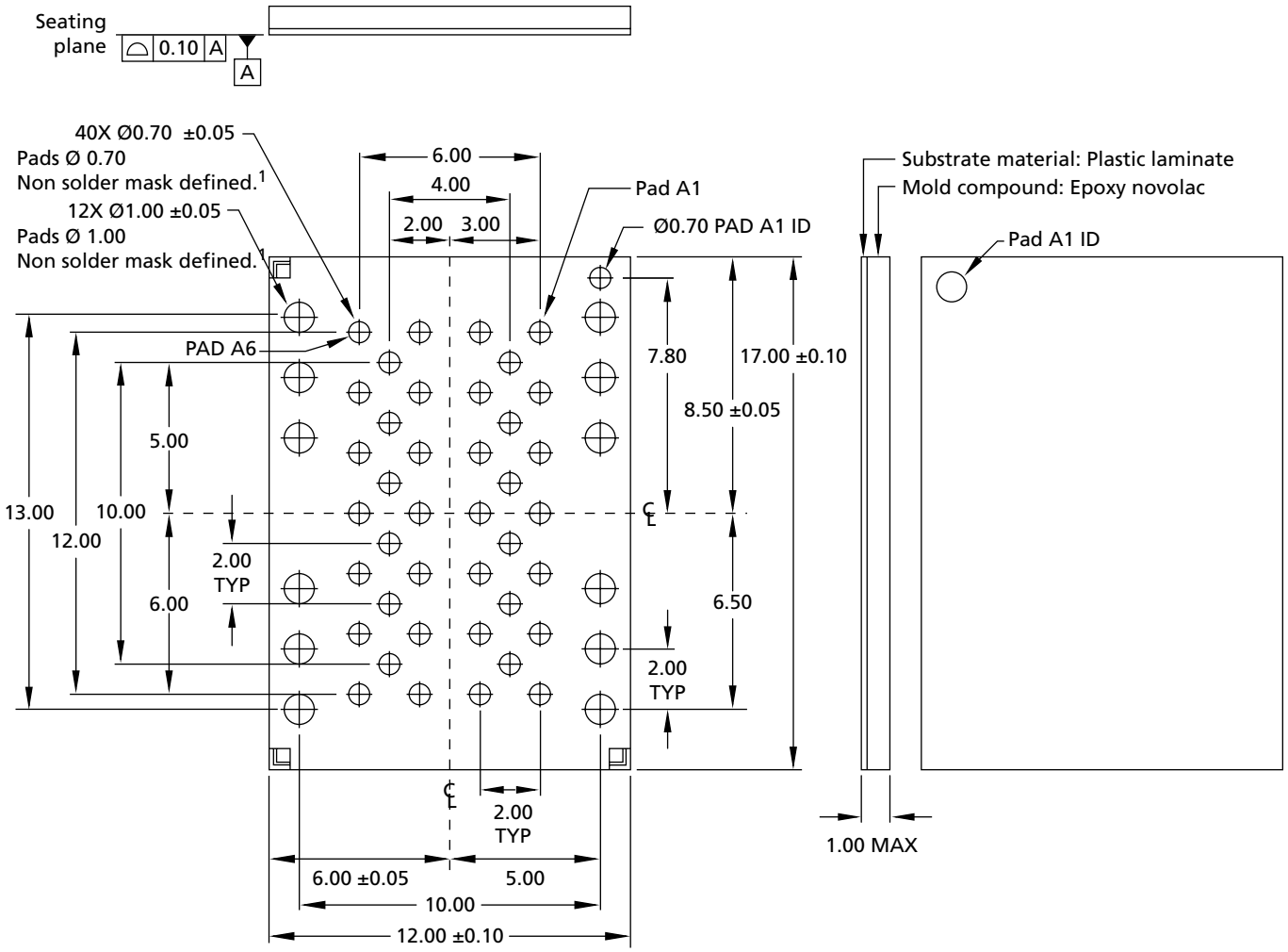
Figure 92: 48-Pin TSOP Type 1 (WP Package Code) Package Diagram



Note: All dimensions are in millimeters.

VLGA Package Information

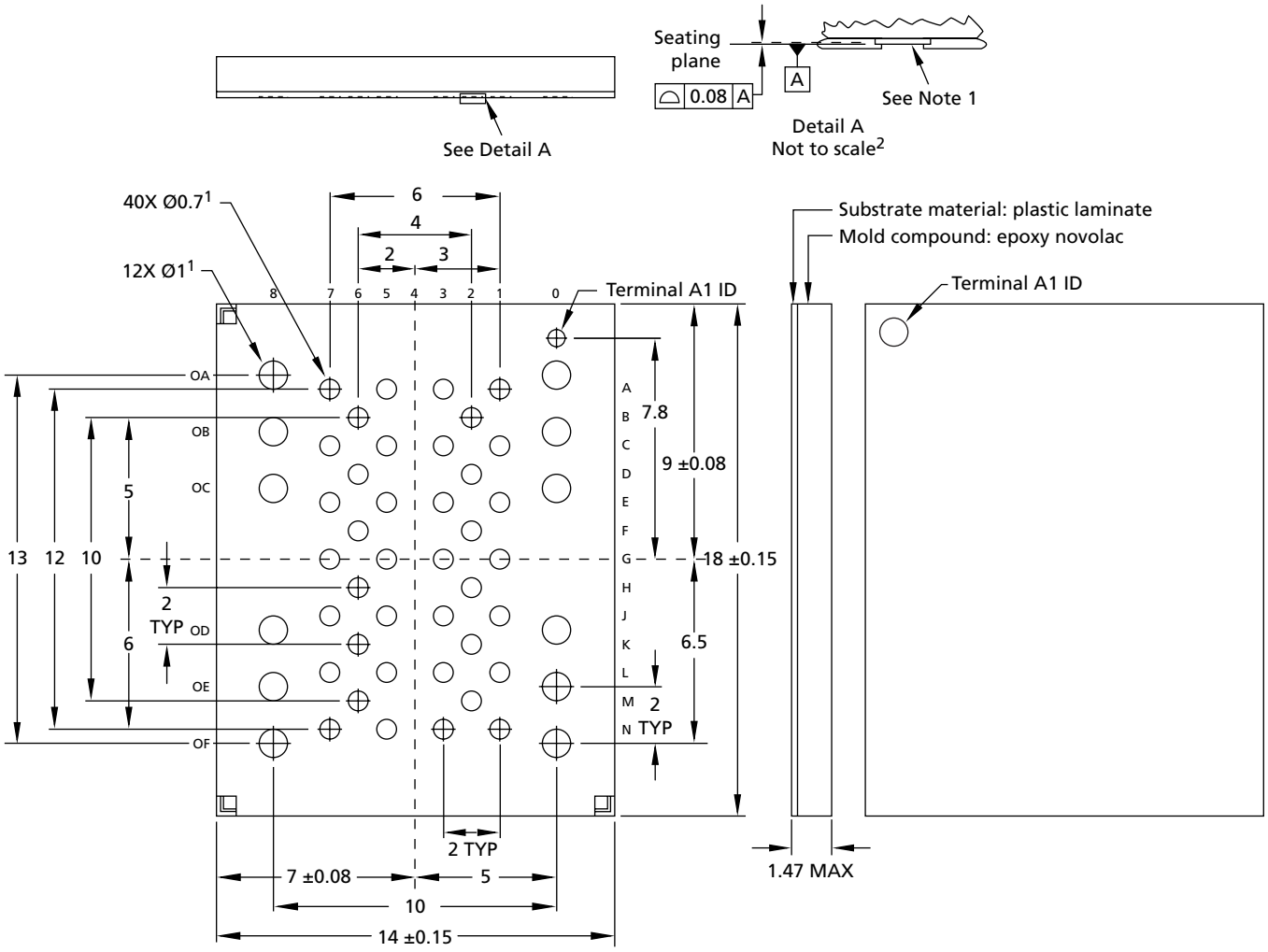
Figure 93: 52-Pad VLGA



Notes:
1. All dimensions are in millimeters.
2. Solder pads are plated with 5-16 microns of nickel followed by a minimum of 1.0 microns of soft wire bondable gold (99.9% pure).
3. Primary datum A (seating plane) is defined by the bottom terminal surface. Metallized test terminal lands or interconnect terminals need not extend below the package bottom surface.

LLGA Package Information

Figure 94: 52-Pad LLGA



Notes: 1. All dimensions are in millimeters.
2. Solder pads are plated with 5-16 microns of nickel followed by a minimum of 1.0 microns of soft wire bondable gold (99.9% pure).
3. Primary datum A (seating plane) is defined by the bottom terminal surface. Metallized test terminal lands or interconnect terminals need not extend below package bottom surface.

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Revision History

Rev. C, Production 11/08

- "Features" on page 1: Updated BLOCK ERASE time.
- Table 26: PROGRAM/ERASE Characteristics on page 96: Updated ^{t}BERS (TYP).

Rev. B, Production 9/08

- "Features" on page 1: Under the Endurance bullet, changed 1-bit ECC[1] to 4-bit ECC[1].
- Table 10, Parameter Page Data Structure, on page 28: Updated "Values" column for byte 112 and bytes 254-255.
- Table 17, Error Management Details, on page 90: Changed "Minimum required ECC" row value from 1-bit to 4-bit.

Rev. A, Production. 8/08

- Initial release.