PAH8002EP: Low Power Optical Heart Rate Detection Sensor

General Description

The PAH8002EP is a low power and high-performance CMOS-process optical sensor with three LEDs: two Green and one Infrared, and integrated DSP, targeted as a Heart Rate Detection (HRD) sensor. It is based on optical sensing technology that captures higher resolution image than the traditional photodiode. The images are then processed through our integrated DSP to attain processed PPG (Photoplethysmogram) data for use in deducing heart rate.

Key Features

- Heart rate detection function (HRD)
- SRAM buffer support
- Integrated ultra-low power mode, while in Sleep mode
- Adjustable sleep rate control
- Communication interface options
  - I^2C
  - Four-Wire SPI
- I^2C interface up to 1 Mbit/s
- SPI interface up to 2 Mbit/s
- Hardware reset support
- Integrated chip-on-board LEDs with wavelength of 525nm and 940nm

Applications

- Heart Rate Monitor Accessories
- Wearables: Smartwatch, Wrist Band

Key Parameters

Parameter	Value
Operating Temperature, Tj (°C)	-20 to +60
Array Size	1 pixel
Pixel Size (µm)	780 x 780
Max Frame Rate (fps)	50K
Dynamic Range (dB)	70
Supply Voltage (V)	VDDM: 3.3 – 3.6 VDD_LEDx: 3.3 – 3.6 VDDIO: 1.62 – 3.6 Analog: 2.8 Digital: 1.8
Power Consumption (mW) @3.3V Note: Including LED current, without I/O toggling, package only	Active: 4.95 with one LED 8.25 with two LEDs 0.165 with IR Touch Detection Sleep: 0.08
Heart Rate Measurement Range (bpm)	30 - 240
Package Size (mm)	3.6 x 6.36 x 1.0

Ordering Information

Part Number	Package Type
PAH8002EP-IP	22-Pin LGA

Lead (Pb) Free RoHS 6 fully compliant

For any additional inquiries, please contact us at http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

The PAH8002EP is a low power and high-performance CMOS-process optical sensor, targeted as a Heart Rate Detection (HRD) sensor. It is built-in with 2 Green LEDs, 1 Infrared LED and integrated DSP It comes with two communication interfaces, which are I^2C supporting up to 1 Mbit/s and Four-Wire SPI supporting up to 2 Mbit/s. SRAM buffer of 832 bytes is supported for the power saving at the host.

The Figure 1 shows the architecture block diagram of the device. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Note: Throughout this document PAH8002EP low power Optical CMOS Heart Rate Sensor is referred to as the sensor.

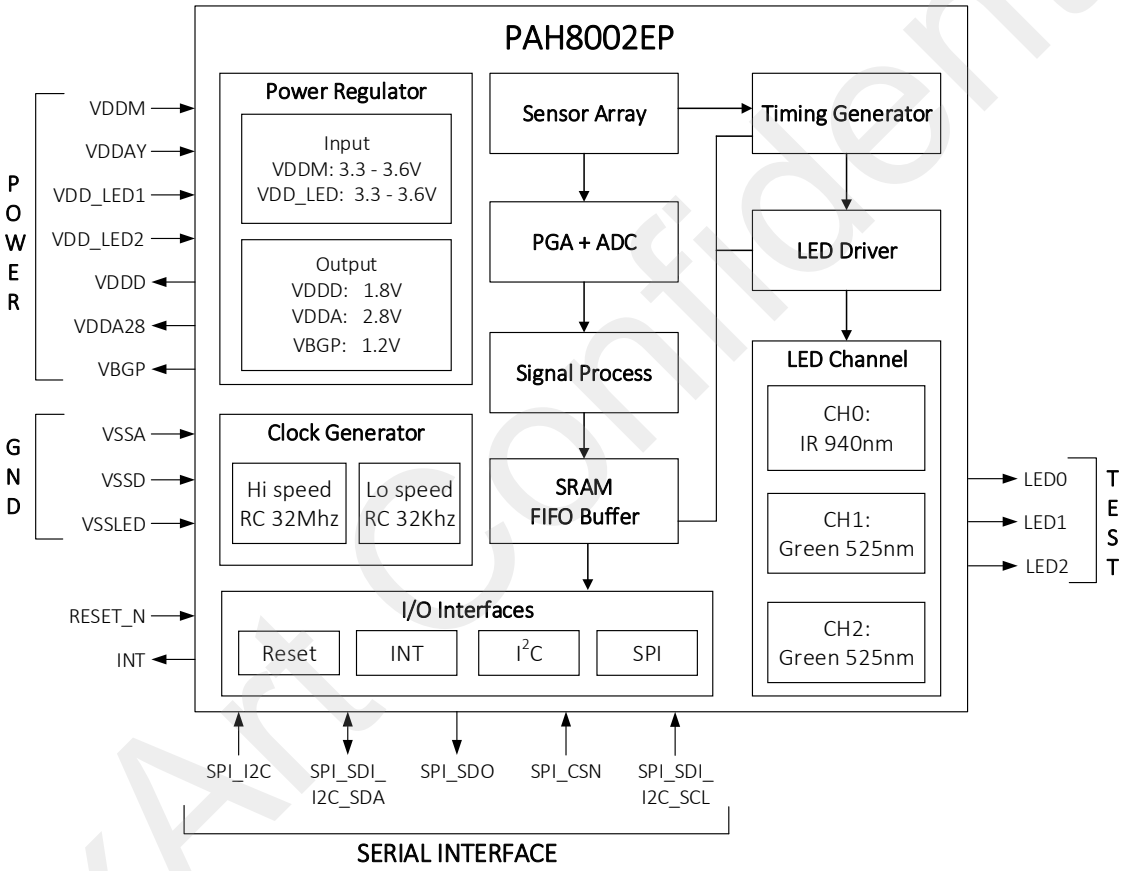

Figure 1. Functional Block Diagram

1.2 Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PPG	Photoplethysmogram
Touch	Touch detection for wear on or wear off
SW reset	Software reset by register

1.3 Signal Description

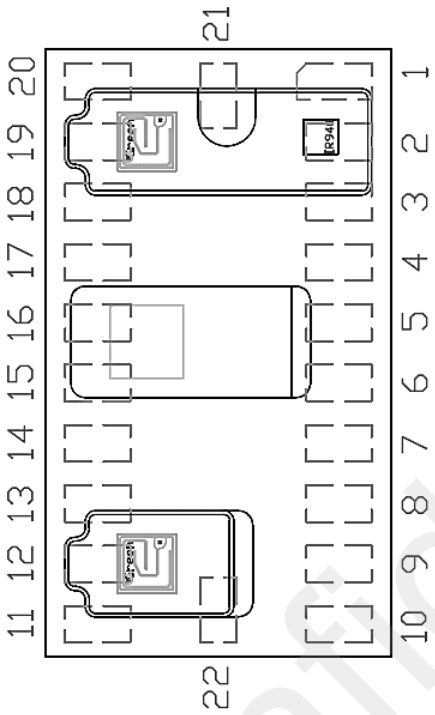

Figure 2. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
Functional Group:		Power Supplies	
1	VDD_LED01	Input	IR/Green LED Anode. Provide VDDM supply voltage
2	VDDAY	Input	Analog circuit power regulator input. Connect to VDDA28 or provide 2.8V voltage
3	VDDA28	Output	Analog circuit power regulator output. Must connect 1µF capacitor to GND
4	VDDD	Output	Digital circuit power regulator output. Must connect 1µF capacitor to GND
5	VBGP	Output	Reference regulator output. Must connect 0.1µF capacitor to GND
7	VDDM	Input	Power supply (3.3 - 3.6V) for internal power regulator
8	VSSLED	GND	LED Ground
15	VSSD	GND	Digital Ground
19	VDDIO	Input	I/O Power Supply (1.62 - 3.6V)
20	VSSA	GND	Analog Ground
22	VDD_LED2	Input	Green LED Anode. Provide VDDM supply voltage
Functional Group:		Interface	
11	SPI_SDI_I2C_SDA	BiDir	4-wire SPI: Data input I^2C: Data input-output
12	SPI_SDO	Output	4-wire SPI: Data output
13	SPI_CSN	Input	4-wire SPI: Chip Select. Active Low
14	SPI_SCLK_I2C_SCL	Input	4-wire SPI/ I^2C: Clock

Pin No.	Signal Name	Type	Description
Functional Group:		Functional I/O	
16	INT	Output	Data ready interrupt. Default is edge sensitive interrupt, can be changed to level sensitive interrupt (high active) in INT_Type register
17	SPI_I2C	Input	Interface Selection I^2C: Pull down (Tie to GND) 4-wire SPI: Pull high (Tie to VDDIO)
18	RESET_N	Input	Hardware control to enter Reset Mode. Connect to VDDIO when not used Level High: Leave Reset Mode Level Low: Enter Reset Mode
Functional Group:		Reserved	
9	LED0	RSV	Reserved for LED0 test pin
6	LED1	RSV	Reserved for LED1 test pin
10	LED2	RSV	Reserved for LED2 test pin
21	NC	RSV	Reserved. No Connection

1.4 Sensor Array

1.4.1 Array Size

Table 2. Array Information

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
X Dimension	X		780		µm	No optical filter
Y Dimension	Y		780		µm	
Pixel Size	Pix		1 x 1		pixel	

1.4.2 Against Ambient Light

Support HW background subtraction to reduce ambient light interference. PAH8002 can detect background brightness and subtract this background value. Refer to 10.2.2 and 10.3.2 registers section.

1.4.3 Conversion Gain

Support two types of sensitivity levels: 1x and 4x to improve the performance on different human skin colors and skin tones, for example on the darker skin tone. Digital circuit can control capacitor value to optimize Conversion Gain. Refer to 10.2.3 registers section.

1.5 ADC Normalized Mode

1.5.1 Normalized Mode

Write 0x00 to Bank0 Address 0x50 and 0x51 to enable normalized mode. Refer to 8.1 AEC section and 10.7, 10.13 registers section.

*ADC Data = ((AEC Range * Sampling Number * 2^20) / (PGA Gain * LED DAC * Exposure Time)) >> Normalized_Right_Shift*

1.5.2 Non-normalized Mode

Write 0x01 to Bank0 Address 0x50 and 0x51 is disable normalized mode. Refer to 8.1 AEC section and 10.7, 10.13 registers section.

*ADC Data = ((AEC Range * Sampling Number)*

1.6 Power Saving Mechanism

The sensor will enter into Sleep mode at most of the operating duration for power saving purpose. The low power timer will control clock source to reduce power consumption at Sleep mode. The sensor will wake up by itself during setting period. If three LED channels are used, these channels will be repeating in this sequence: CH0->CH1->CH2>CH0->CH1->CH2. Every channel will turn on each LED sampling number of exposure for better signal noise ratio. The sensor will get some raw data and save them into SRAM FIFO. Then the sensor will enter sleep mode for power saving and to be woke up by internal timer. Refer to 10.5 and 10.6 registers section.

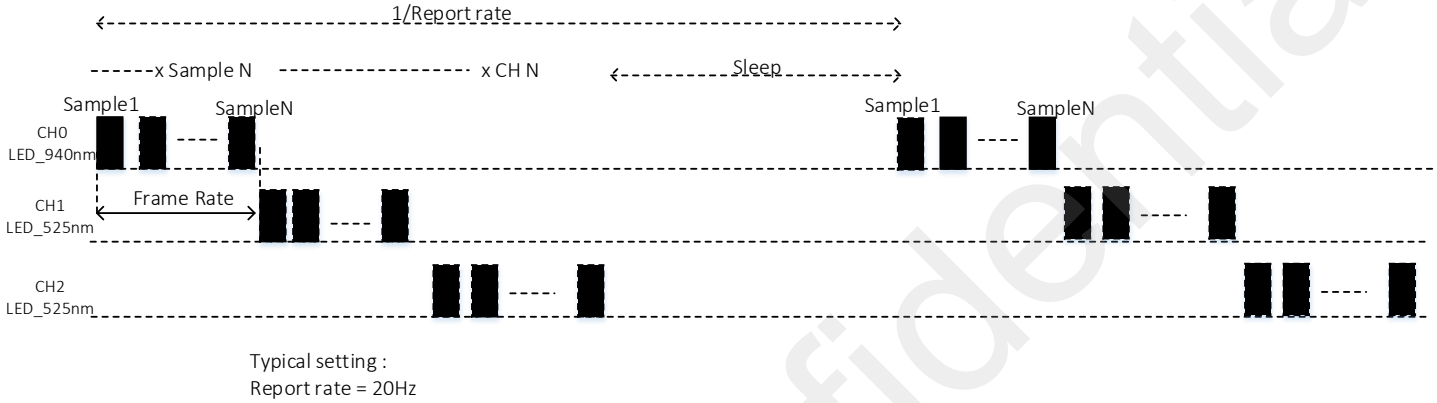

Figure 3. Three Channels LED Timing Diagram

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Analog Voltage	V_{DDM_MAX}	-0.4	V_{DDM} + 0.3	V	
I/O Voltage	V_{DDIO_MAX}	-0.4	V_{DDIO} + 0.3	V	
I/O Pin Input High Voltage	V_{DDIO_IN}	-0.4	V_{DDIO} + 0.3	V	All I/O pins
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T_A	-20	25	60	°C	
Operating Junction Temperature	T_J	-20	-	60	°C	
Power Supply Voltage	V_{DDM}	3.25	3.3	3.6	V	Power regulator input supply. Includes ripples
Analog Supply Voltage	V_{DDAY}	2.66	2.8	2.94	V	If supply from external power regulator. Includes ripples
I/O Supply Voltage	V_{DDIO}	1.62	1.8	3.6	V	Includes ripples
Power Regulator Output Voltage	V_{DDD}	1.62	1.8	1.98	V	For digital circuit. Includes ripples
	V_{DDA28}	2.52	2.8	3.08	V	For analog circuit to be connected to V_{DDAY}. Includes ripples
	V_{BGP}	1.08	1.2	1.32	V	For power regulator reference. Includes ripples
Supply Noise	V_{Npp}	-	-	100	mV_{p-p}	Peak to peak within 10K – 80 MHz
Serial Clock Frequency	SCK_SPI	-	-	2	MHz	
	SCK_I^2C	-	400[1]	1000[2]	KHz	1. Max value for Fast mode 2. Max value for Fast mode plus

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

2.3 Thermal Specifications

Table 5. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-25	-	125	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Package Handling Information document

2.4 DC Characteristics

Table 6. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Peak Power Supply Current	I_{DDM_MAX}	-	-	100	mA	For V_{DDM}
	I_{DDAY_MAX}	-	-	10	mA	For V_{DDAY}
Peak I/O Supply Current	I_{DDIO_MAX}	-	-	1	mA	For V_{DDIO}
Output Supply Current	I_{DDD_MAX}	-	-	80	mA	For V_{DDD}
Output Supply Current	I_{DDA28_MAX}	-	-	20	mA	For V_{DDA28}
Power Consumption						
Supply Current @ Sleep	I_{DDPD}	-	25	75	uA	For sensor only Wakeup by read register
Inrush Current	I_{INRUSH}	-	-	60	mA	
With One Green LED						
Supply Current @ HRD PPG mode	I_{DDHRD}	-	1.2	3.0	mA	For sensor only, not including LED current, without I^2C interface I/O toggle
LED current	I_{DDLED}	-	0.3	-	mA	20 report/sec, LED DAC = 50mA, on yellow skin color
With Two Green LEDs						
Supply Current @ HRD PPG mode	I_{DDHRD}	-	1.7	3.0	mA	For sensor only, not including LED current, without I^2C interface I/O toggle
LED current	I_{DDLED}	-	0.8	-	mA	20 report/sec, LED DAC = 50mA, on yellow skin color
With IR Touch Detection						
Supply Current @ Touch Detection mode	$I_{DDtouch}$		45		uA	For sensor only, not including LED current, without I^2C interface I/O toggle
LED current at touch	I_{DDLED}	-	5	-	uA	3.8 report/sec, LED DAC = 50mA, on yellow skin color
I/O						
Input High Voltage	V_{IH}	0.7* V_{DDIO}	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.3* V_{DDIO}	V	
Output High Voltage	V_{OH}	V_{DDIO} - 0.4	-	V_{DDIO} + 0.4	V	@I_{OH} = 2mA
Output Low Voltage	V_{OL}	-0.4	-	0.4	V	@I_{OL} = 2mA

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
LED						
Sink current	I_{LED}	40	50	60	mA	@ LED DAC = 50mA
LED cathode voltage	V_{LED-}	0.4		3.6	V	

Notes:
1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions: V_{DDM} = 3.3V, V_{DDIO} = 1.8 and 3.3V, T_A = 25°C

2.5 AC Characteristics

Table 7. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Up from V_{DD}↑	t_{PU}	200	300	400	ms	From V_{DD}↑ to valid interface communication
SDI/SDO Read Hold Time	T_{HOLD}	-	3	-	us	Minimum hold time for valid data.
Address and data delay time	t_{delay}	2.75			us	Refer to Serial Interface section
Sensor Pulse Interrupt Width	t_{INT}	0.00625	0.5	16	us	Default 0.5us, can be changed in INT_Pulse_Width register
Rise and Fall Times: SDI/SDO	t_r , t_f	-	30	-	ns	C_L = 30 pF
HW Reset Time	t_{reset}	200	300	400	ms	Reset_N from low to high period

Notes:
1. Electrical Characteristics are defined under recommended operating conditions
2. All the parameters are tested under operating conditions: T_A = 25°C, V_{DDM} = 3.3V, V_{DDIO} = 3.3V for 3.3V IO application and V_{DDIO} = 1.8 V for 1.8V IO application.

3.0 Mechanical Specifications

3.1 Mechanical Dimension

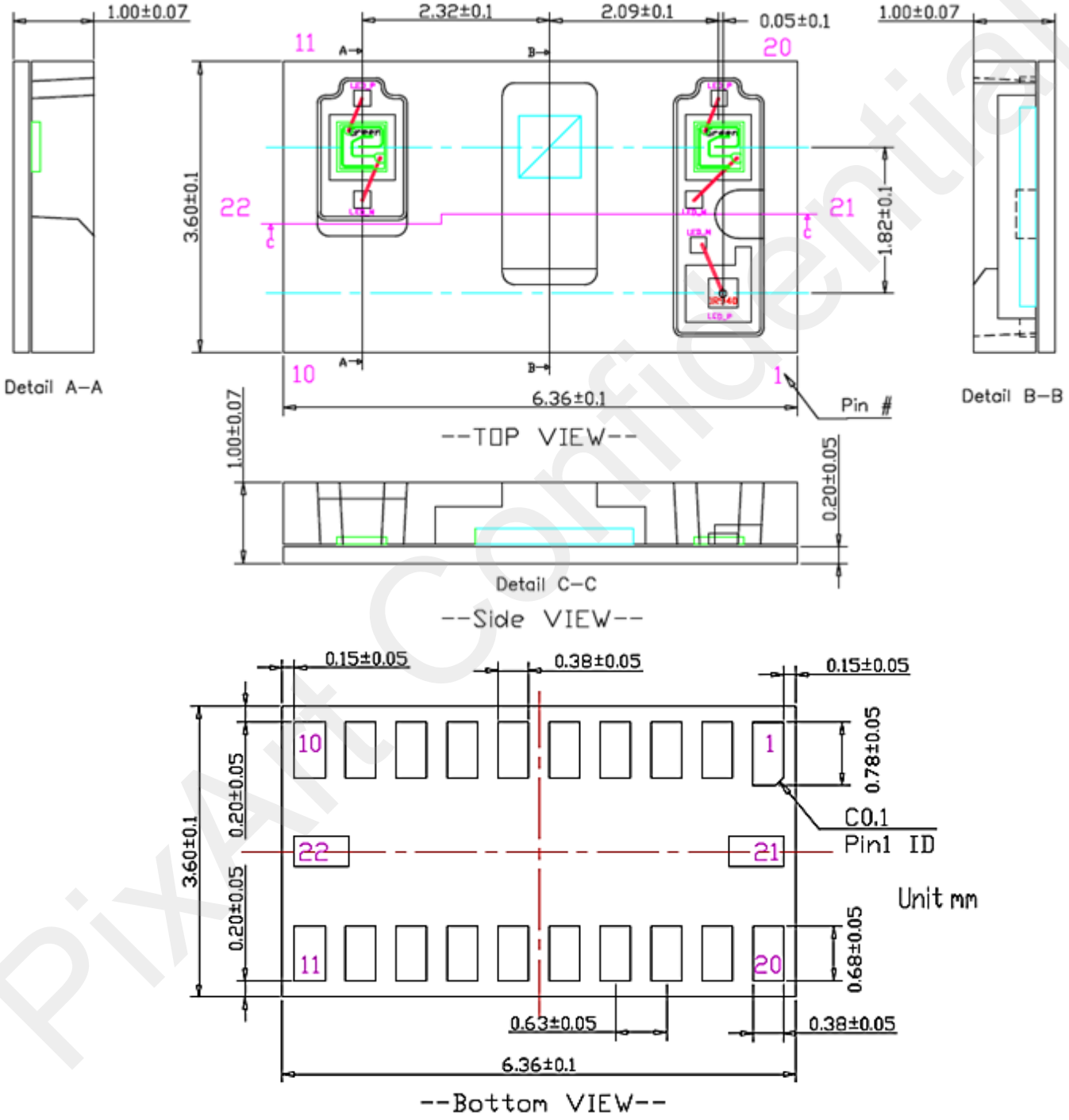

Figure 4. Package Outline Diagram

3.2 Package Marking

Refer to Figure 5. Package marking for the code marking location on the device package.

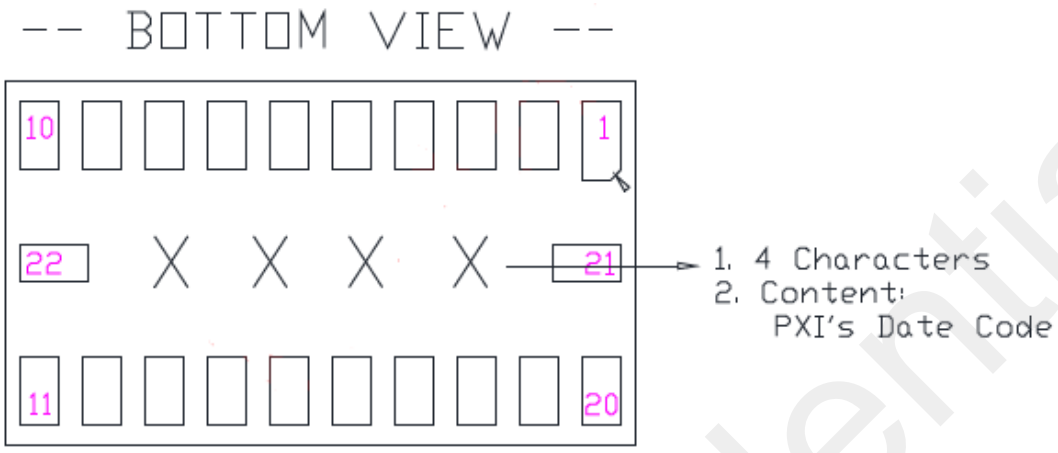

Figure 5. Package marking

Table 8. Code Identification

Marking	Description
XXXX	PixArt Date Code

4.0 System Level Description

4.1 System Overview

This section describes on how the sensor being used to make up a complete system including the explanation on the 3rd party components and how they work with the sensor.

The PAH8002 is based on CMOS image sensor technology. It is designed to meet the requirements as heart rate monitor accessories and wearables like smart watch or wrist band device. Figure 6 illustrates a system design for App Level diagram. The processor is accessing PPG data from 8002 sensor, then pass it to App level. APP level applies PixArt provided algorithm library to determine the heart rate data and waveform. Figure 7. System Design for Firmware Level illustrates a system design for Firmware Level diagram. The processor will also access PPG data from 8002 sensor, then perform heart rate calculation with PixArt algorithm library and send result to display or end device.

PAH8002 can be configured to generate different frame rate settings up to 50K fps.

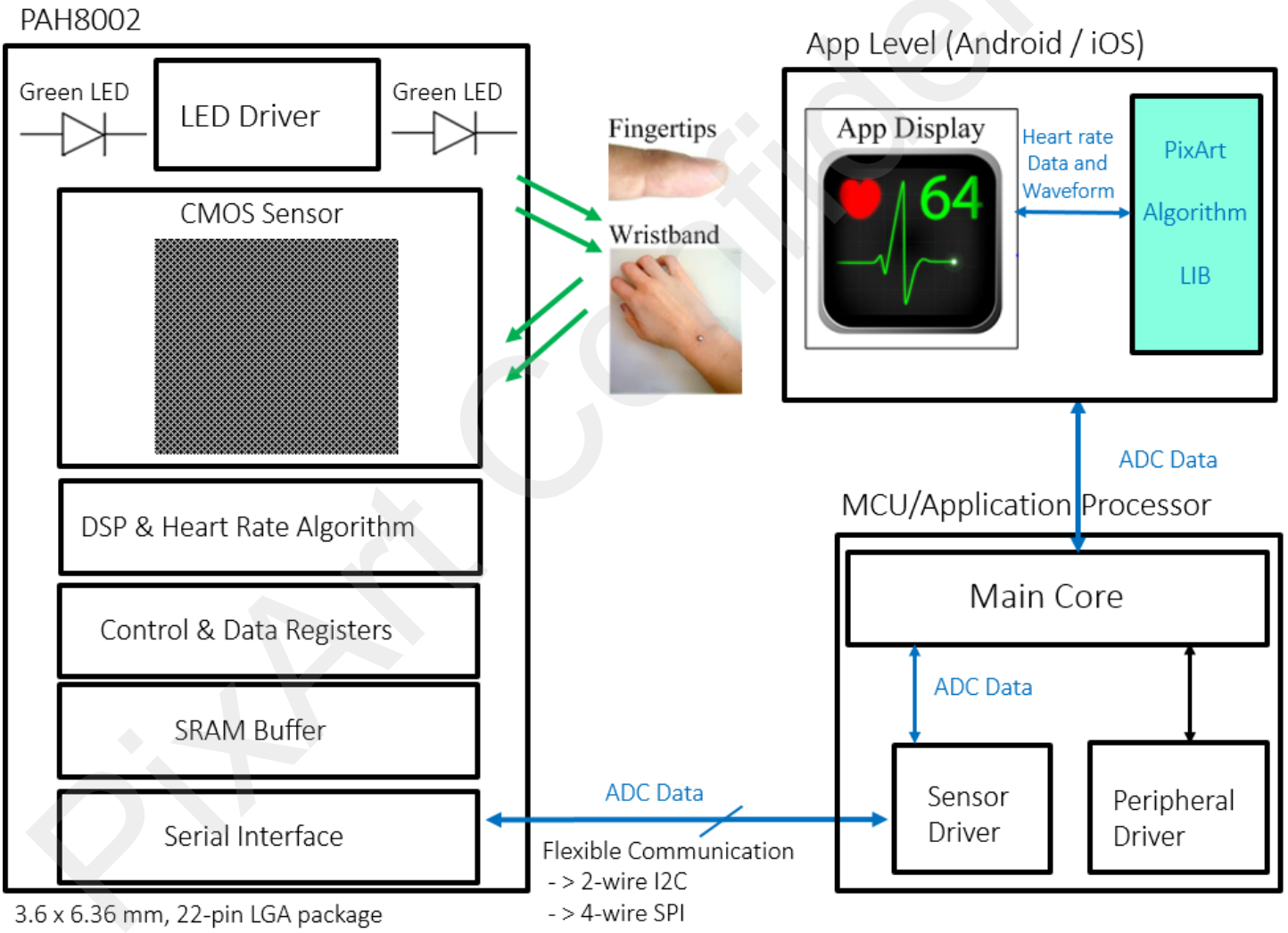

Figure 6. System Design for App Level

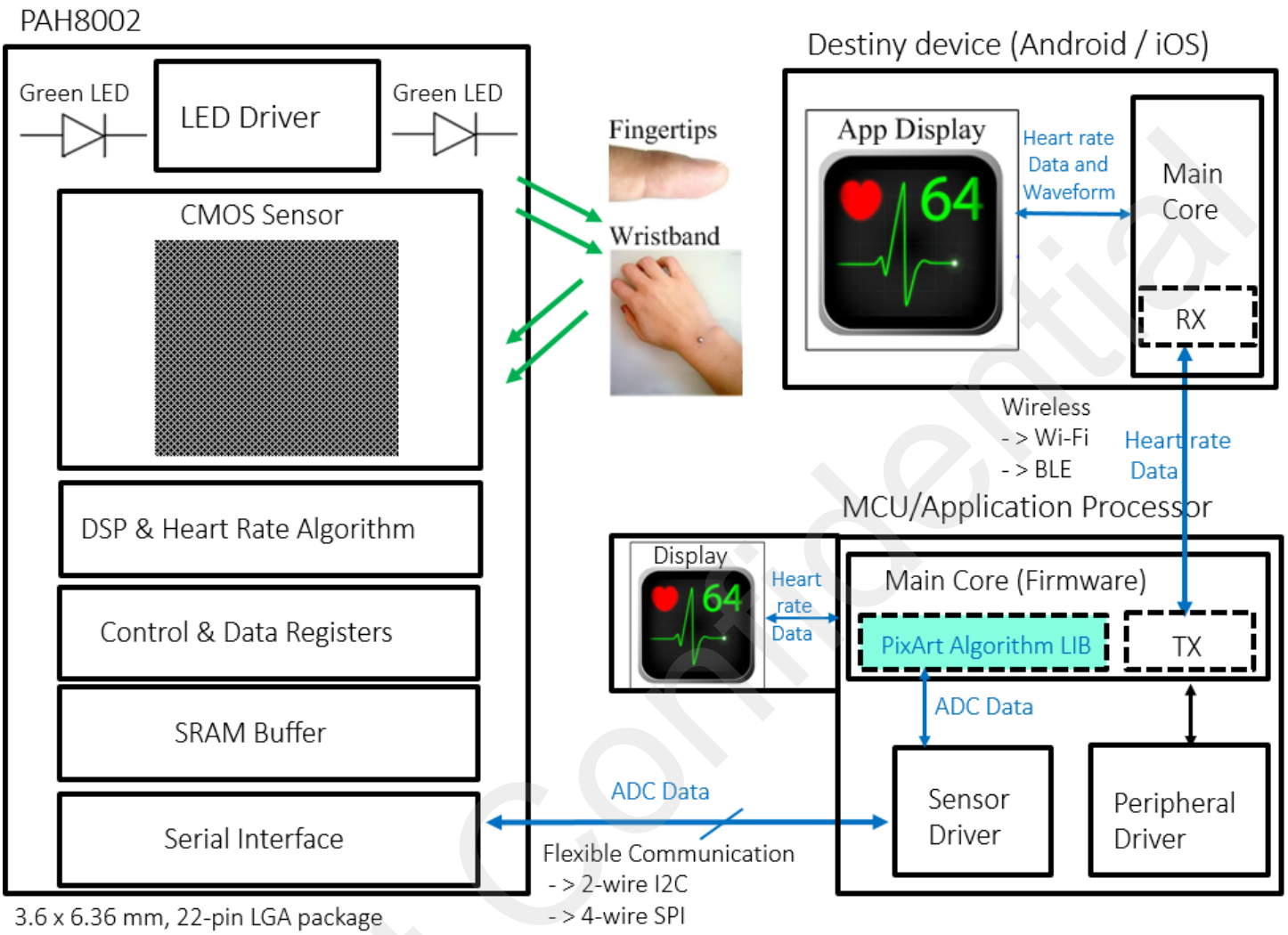

Figure 7. System Design for Firmware Level

4.2 Reference Schematic

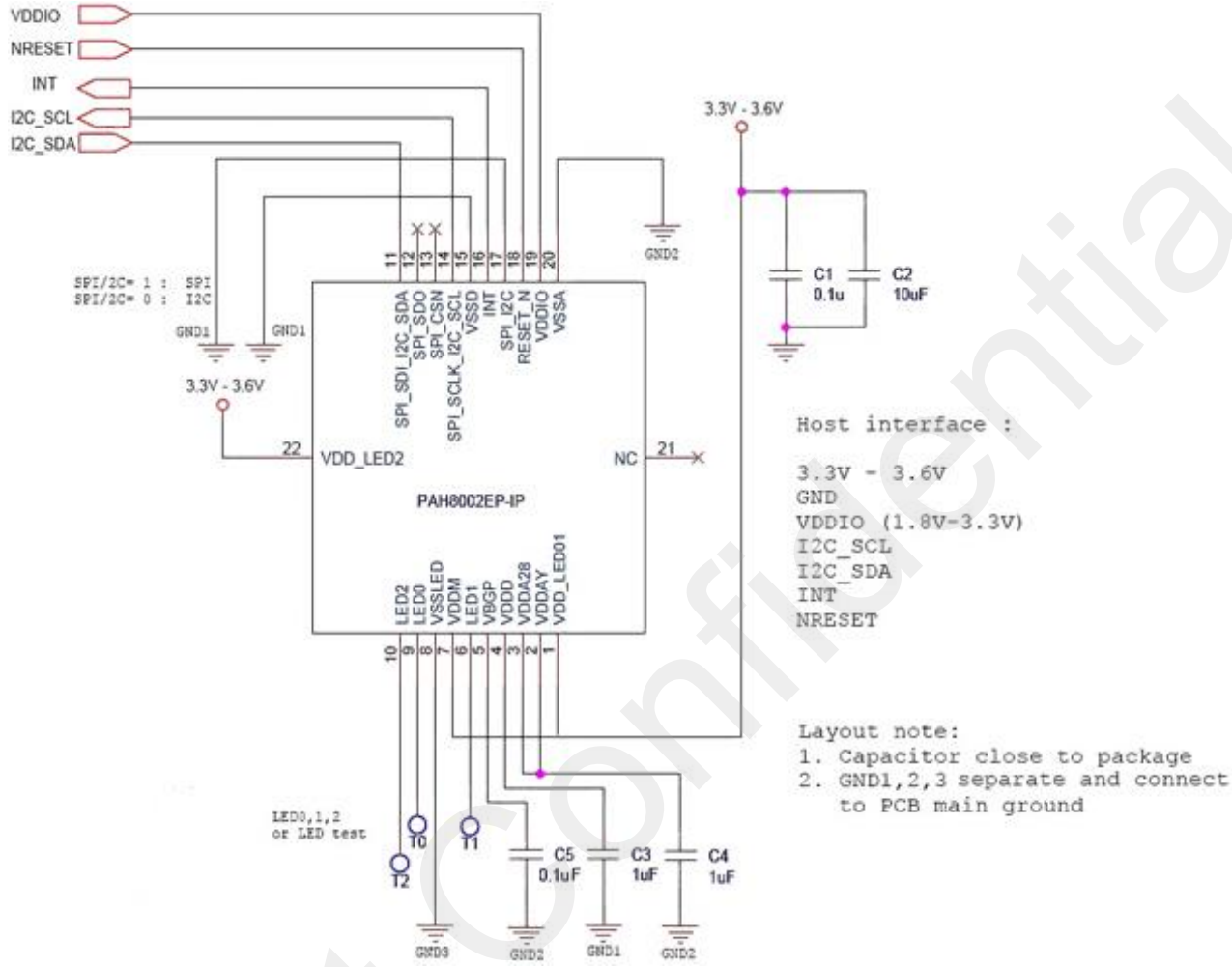

Figure 8. Reference Application Circuit

4.3 Design Guidelines

4.3.1 Schematic Design

1. VDDM & VDDIO: 3.3V~3.6V (for 3.3V System)
2. VDDM: 3.3V~3.6V, VDDIO: 1.62V~1.98V (for 1.8V System)
3. It is recommended to separate the power system for VDDM to avoid power interference.
4. SPI_SDI_I2C_SDA and SPI_SCLK_I2C_SCL pull high to VDDIO with resistor for I^2C Only
5. VDDD, VDDA28 must have 1µF and VBGP must have 0.1µF capacitor connecting to GND and place closely to 8002.
6. The GND1, GND2 and GND3 must be separated and connected to PCB main GND.
7. INT pin is recommended to be connected to MCU HW INT as data ready INT for power saving.
8. Ensure that the VDDM and VDDIO's power noise should be under 100mV (with 0.1µF and 10µF capacitor)
9. Tie SPI_I2C pin to VDDIO for SPI or tie to GND for I^2C.
10. At power on, VDDM and VDDIO must be powered on at the same time or VDDIO to be powered on first before VDDM.
11. At power off, VDDM and VDDIO must be powered off at the same time or VDDM to be powered off first before VDDIO.

4.3.2 PCB Layout Design

4.3.2.1 Recommend Layout PCB

Recommended Stencil Thickness: 0.1mm. PCB Layout can be refer to Figure 9. Recommend Layout PCB.

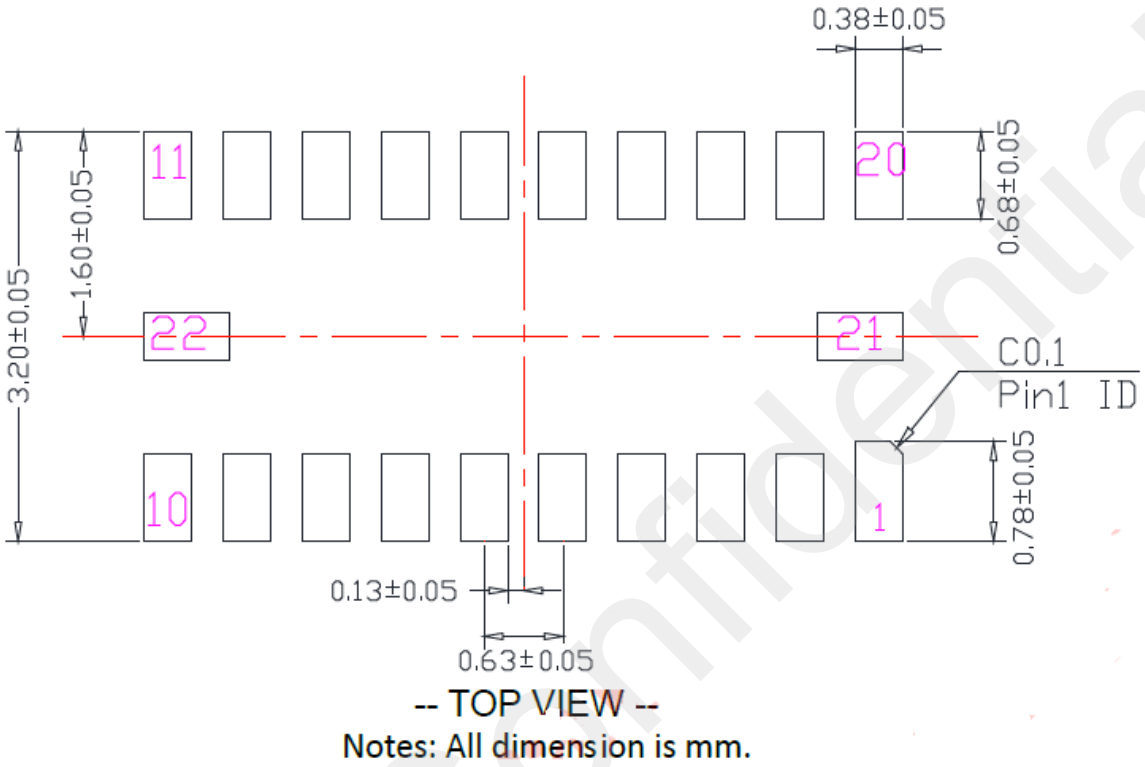

Figure 9. Recommend Layout PCB

4.3.2.2 Recommended Stiffener type for FPC (Flex) back-side (at Sensor package area)

1. If use FPC (Flex) board, need add stiffener onto the back - side to enhance the Flex strength.
2. Recommended Stiffener type: FR4 or stainless steel or equivalent material.

4.3.2.3 PCB Layout Guidelines

The following guidelines can be refer to Figure 10. PCB Layout Guide.

1. Capacitor 0.1μF and 1μF must be placed close to the sensor package.
2. The GND plane of GND of VSSA, VSSD and VSSLED must be layout separately and connected to the PCB's main GND.

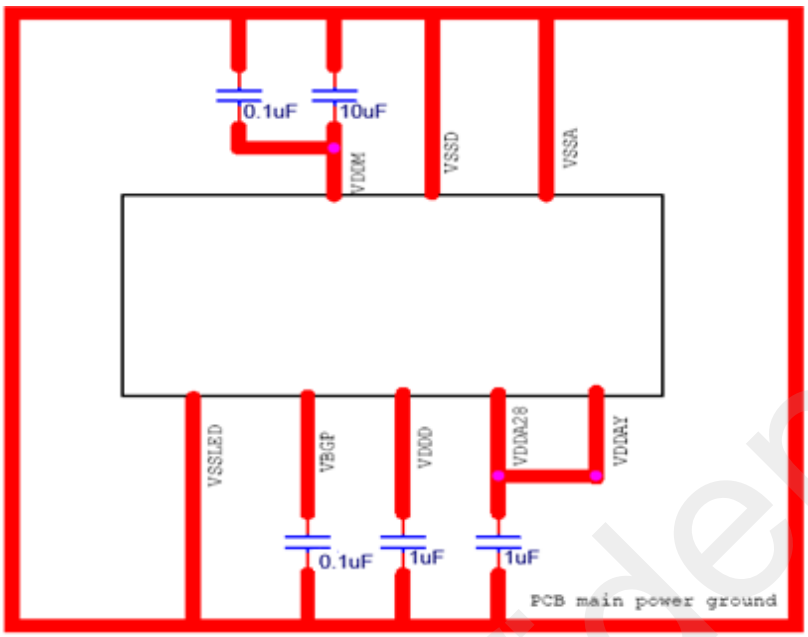

Figure 10. PCB Layout Guide

4.4 Recommend Guideline for PCB Assembly

Recommended vender and type for Pb-free solder paste

1. Almit LFM-48W TM-HP

2. Senju M705-GRN360-K

IR Reflow Soldering Profile can be refer to Figure 11. IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is:

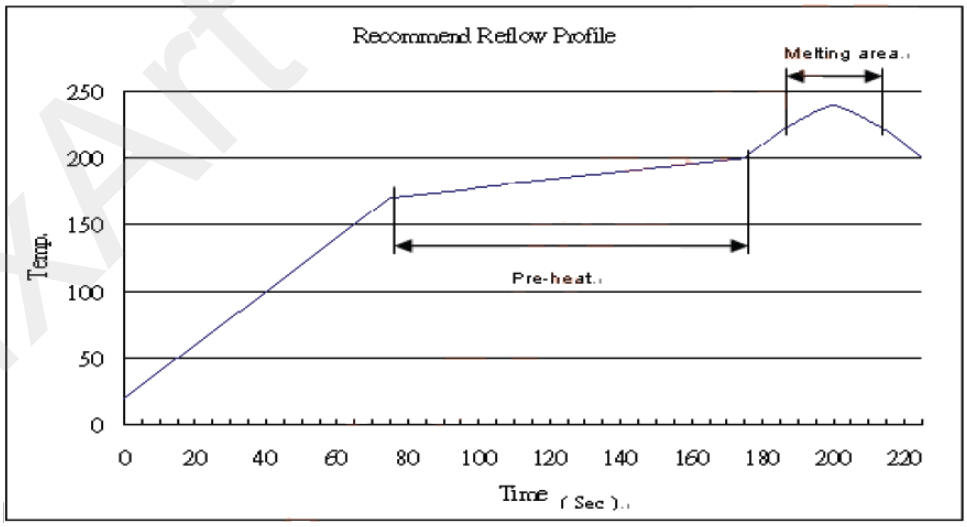

Figure 11. IR Reflow Soldering Profile

Note:

(1) Average Ramp-up Rate (30℃ to preheat zone): 1.5~2.5℃/Sec
(2) Preheat zone:
  (2.1) Temperature ramp from 170~200℃
  (2.2) Exposure time: 90 +/- 30 sec
(3) Melting zone:
  (3.1) Melting area temperature > 220℃ for at least 30~50sec
  (3.2) Peak temperature: 245℃
MS Level: MS Level 3

4.5 Package Information

4.5.1 Carrier Tape Drawing

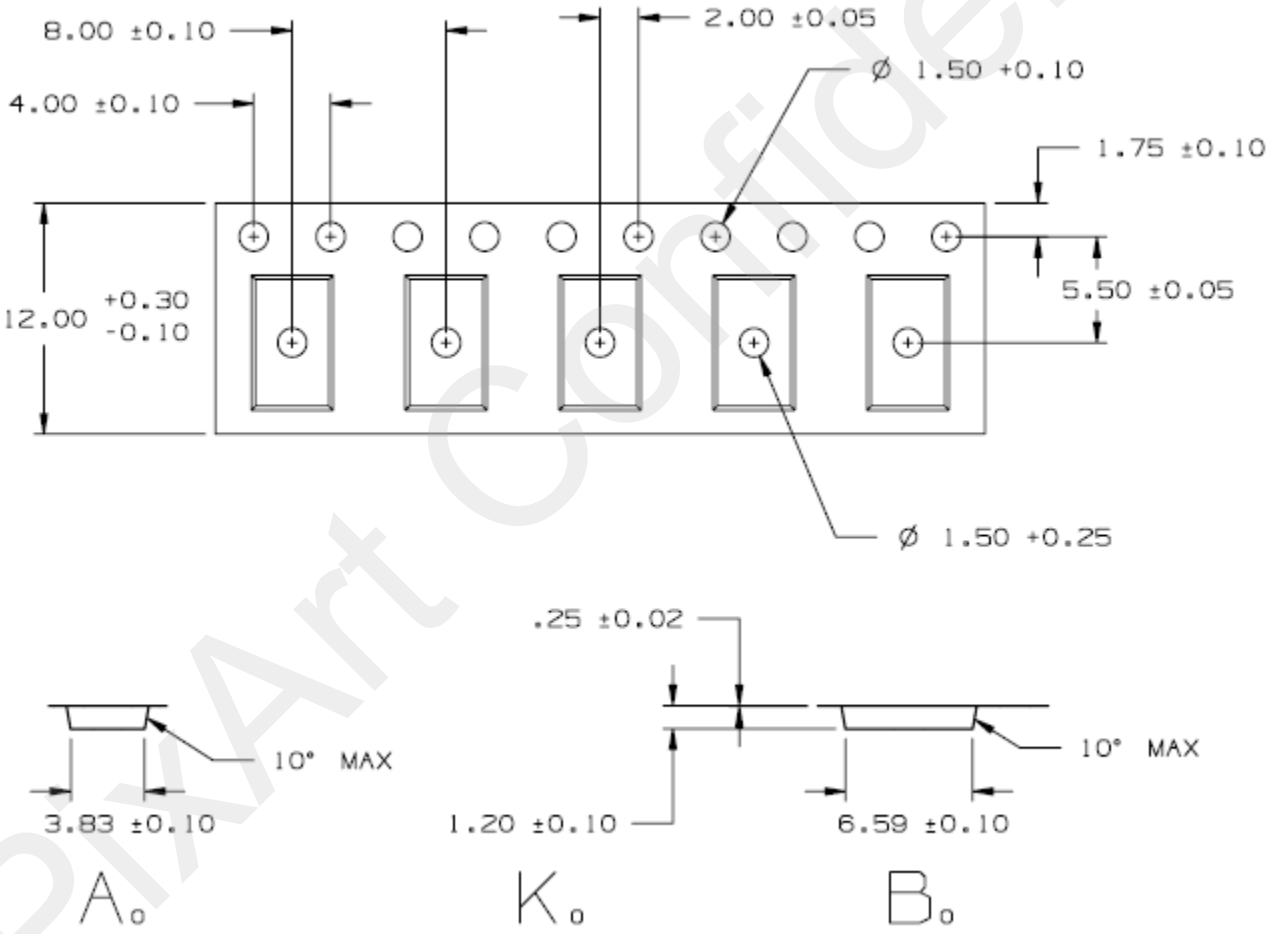

Figure 12. Carrier Tape Drawing

4.5.2 Unit Orientation

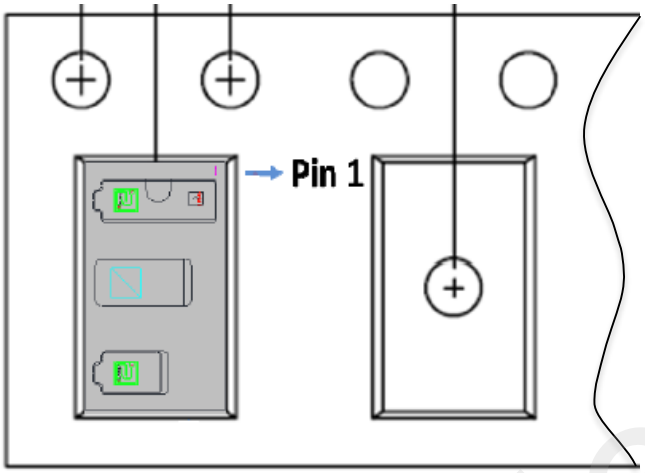

Figure 13. Unit Orientation

The maximum capacity of one packing box for PAH8002EP-IP: One Inner packing box = 2500 units
Note: The Tape and Reel packing with vacuum pack is 1year storage available @ 25℃, 50%RH

5.0 Power States & Sequence

5.1 Power States

State	Functional Description
OFF	No power supply, all the voltage rails and clocks are gated.
RESET	This mode is entered when power-up sequence is executed and RESET_N is held low. The sensor stays in this state as long as RESET_N is held low. High on RESET_N will transition the sensor to Ready mode. After power up, when the sensor is waiting for RESET_N to go high, all the rails to the individual functional blocks shall be internally gated. Any time the RESET_N is pulled low the sensor shall enter this mode.
READY	The sensor is transitioned to this mode when RESET_N is set to high or SW reset by register. This mode can be thought of as a mode for re-initialization of the registers if they are different from the default register settings. All the rails and clocks are enabled. There is no capture or transmission of data on the SPI/I^2C lanes. All the functional blocks are enabled.
SLEEP[1]	This mode is entered from Ready mode either by using I^2C or SPI. When I^2C or SPI is used the user will transition by setting Sleep Sequence. The sensor stays in this mode until the user transitions back to PPG mode or Touch mode by read ID and write 0x00 to bank2 addr0x70, then SW reset and setting PPG initial setting or Touch initial setting.
PPG[2]	This mode is obtaining Heart rate PPG raw data from Sleep mode by using I2C or SPI. When I^2C or SPI is used the user will transition by setting PPG Sequence. The sensor stays in this mode until the user transitions back to Sleep mode for power saving by read ID and write 0x00 to bank2 addr0x70, then SW reset and setting Sleep initial setting.
Touch[3]	This mode is touch detection from Sleep mode by using I2C or SPI. When I^2C or SPI is used the user will transition by setting Touch Detection Sequence. The sensor stays in this mode until the user transitions back to Sleep mode for power saving by read ID and write 0x00 to bank2 addr0x70, then SW reset and setting Sleep initial setting.

Notes:

1. Refer to Sleep Mode Sequence for Power Saving section.
2. Refer to Obtaining Heart Rate PPG Raw Data Sequence section.
3. Refer to IR Touch Detection Sequence section.

5.2 Power-up and Power-off Sequence

The power up and power off sequence is illustrated in Figure 14. Please note:

1. There is no specific power supply voltage rise or fall time requirement.
2. Toggling RESET_N with steady supply voltages triggering a Reset.
3. I^2C slave address will take effect only after a Reset.

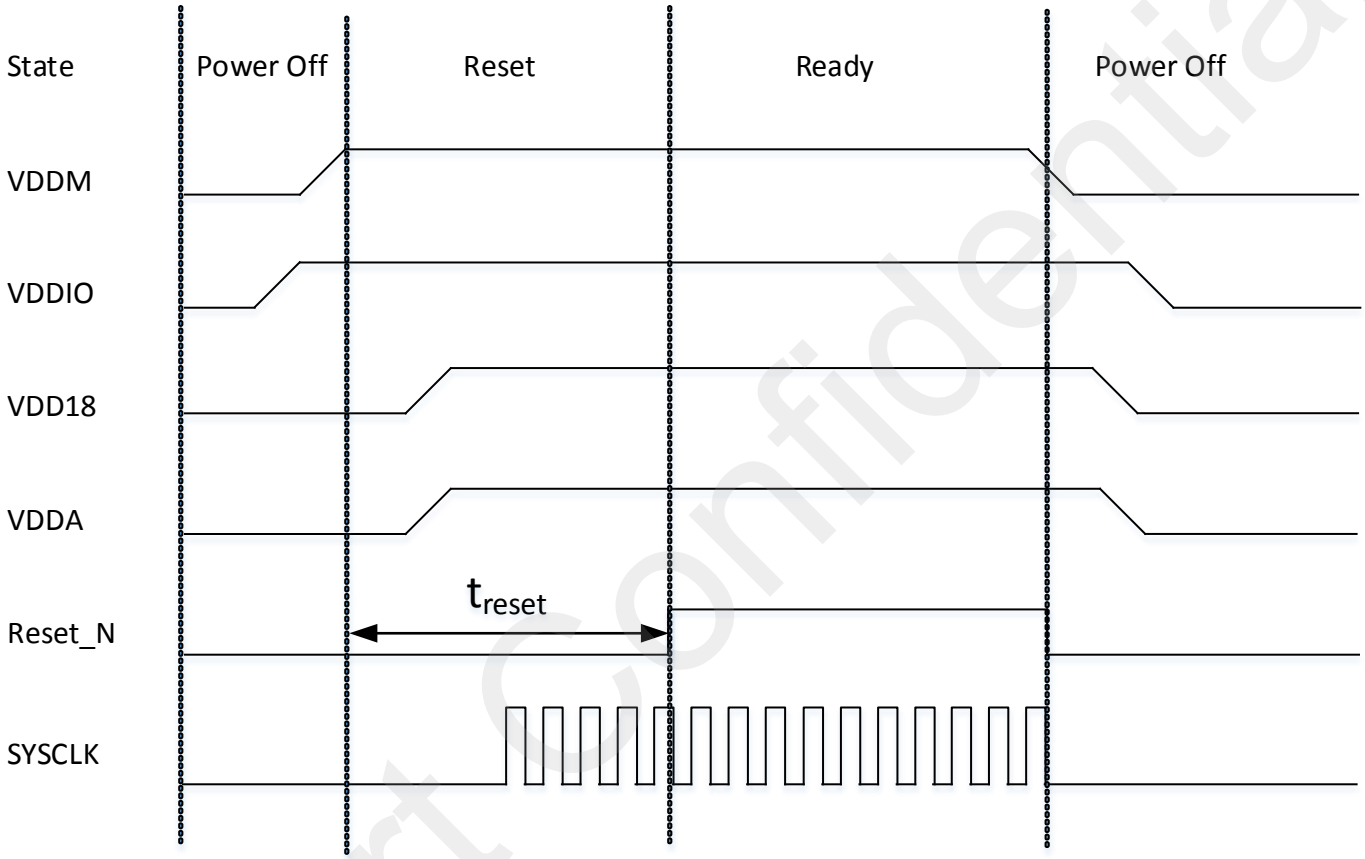

Figure 14. Power-up and Power-off Sequence Timing Diagram

6.0 I²C Serial Interface Communication

6.1 Signal Description

The two wires used for interface communication in PAH8002 are SCL (clock) and SDA (data). The PAH8002 is implemented as a slave-only device, so it never drives SCL, and only drives SDA during read cycles and transfer acknowledge bits. PAH8002 uses 7-bit 0x15 addressing and does not support clock stretching.

Table 9. I²C Signals Description

Signal Name	Label	Type	Reset State	Description
Serial Clock	SPI_SCLK_I2C_SCL	Input	Input	The SCL signal is always driven by the master. SCL synchronizes the serial transmission of data bits on SDA. The frequency of SCL may vary throughout a transfer, as long as it meets all timing requirements.
Serial Data	SPI_SDI_I2C_SDA	Bi-Directional	Pull-up with 10K resistor	The SDA signal is for the host (master) to read from or write to the PAH8002. The host (typically a microcontroller) drives SCL and SDA in a write operation to, or when requesting information from the PAH8002. PAH8002 drives the SDA under two conditions: ▪ When responding with an acknowledge (ACK) bit after receiving data from the host, or ▪ When sending data to the host at the host's request. Data is sent in eight-bit packets

6.2 Start and Stop of Synchronous Operation

All communications take 9 clocks to complete, 8 for the data and the 9th bit is for acknowledge. Transfers are initiated with an S condition and terminated with the P condition. During the 8 bits of data transmissions, SDA may change while clock is low. SDA changing while clock is high is the S or P condition.

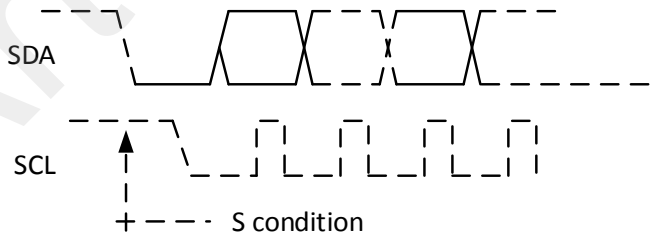

Figure 15. I²C S Conditions

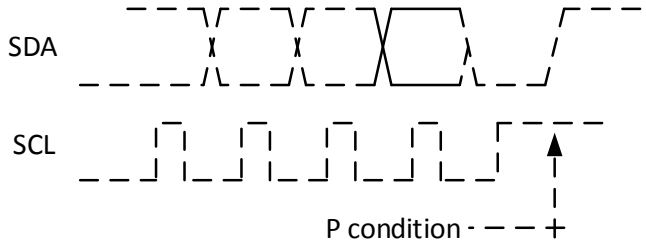

Figure 16. I²C P Conditions

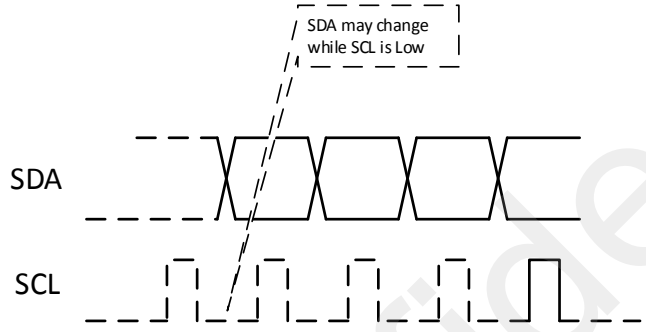

Figure 17. Data may change when SCL is low

Bytes that are transferred from the master to the slave are acknowledged by the slave. The slave acknowledges by driving a 0 on SDA during the 9th clock. This includes write data and slave address packets. When a byte is transferred from the slave to the master (read data), the slave ignores the SDA pin during the 9th clock.

When packets are sent over the I²C interface, they are generally of the format. The rnw (read_not_write) bit defines the direction of all data bytes after the S condition. In other words, it is not possible to initiate a write operation, and then switch to a read operation without completing the write.

S, <slave address, rnw>, A, data, A, data, A, ... , P

After a start condition, a single acknowledge/not acknowledge bit follows each eight-bit data packet. The device receiving the data drives the acknowledge/not acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not acknowledge (NAK) is defined as 1.

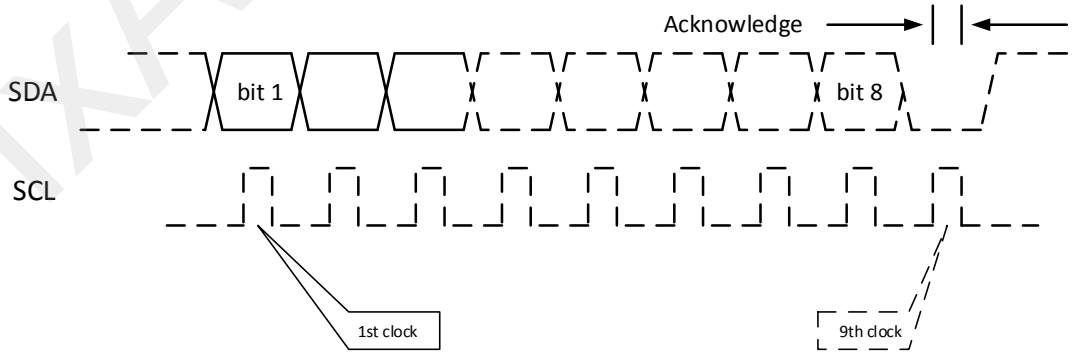

Figure 18. I²C Acknowledge bit

6.3 Packet Formats

Read and write operations between the host and the PAH8002 use three types of host driven packets. All packets are eight bits long, with the most significant bit first, followed by an acknowledge bit.

- Slave Device Address (DA): Command packets contain a 7-bit device address and an read/write bit (R/W)
- Register Address Packets (RA): The address packets contain an 8-bit register address
- Data Packet (DP): Contains 8 data bits, and may be sent by the host or the PAH8002

Table 10. Packet Formats

Slave Device Address							
DA[6]	DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	0: Write 1: Read
Register Address							
RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
Register Data							
DP[7]	DP[6]	DP[5]	DP[4]	DP[3]	DP[2]	DP[1]	DP[0]

6.4 Driven Packets

For a host driven packet, the host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the PAH8002 then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first. To terminate the transfer of host driven packets, the host follows the PAH8002's ACK with a STOP condition. The host can also issue a START condition after the PAH8002's ACK, if it wants to start a new data transfer.

Figure 19. I²C Host Driven Packet (Write)

For a PAH8002 driven packet, by request of the host, the PAH8002 acknowledges a read request, and then outputs a data byte transmitting the most significant bit (7) first. If the host intends to continue the data transfer, the host acknowledges the PAH8002. If the host intends to terminate the transfer, it responds with not acknowledge (SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition, if it wants to begin a new data transfer with the same PAH8002.

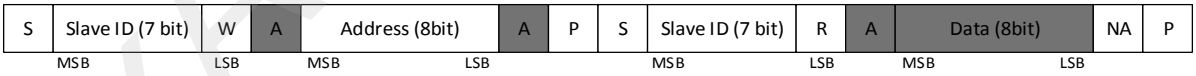

Figure 20. I²C Slave Driven Packet (Read)

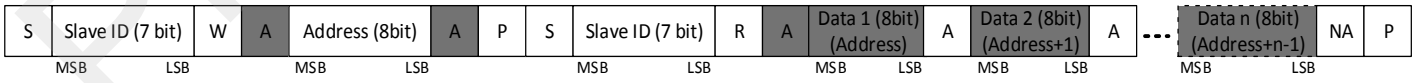

Figure 21. I²C slave driven packet (burst read)

6.5 I²C Timing

Table 11. I²C Timing Specifications

Parameters	Symbol	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency.	f_{scl}	10	100	10	400	kHz
Hold time for Start/Repeat Start. After this period, the first clock pulse is generated.	$t_{HD.STA}$	4		0.6		µs
Set-up time for a repeated Start.	$t_{SU.STA}$	4.7		0.6		µs
Low period of SCL clock.	t_{LOW}	4.7		1.3		µs
High period of SCL clock.	t_{HIGH}	0.75		0.6		µs
Data hold time.	$t_{HD.DAT}$	0		0		µs
Data set-up time.	$t_{SU.DAT}$	250		100		ns
Rise time of both SDA and SCL signals.	t_r		1000	-	300	ns
Fall time of both SDA and SCL signals.	t_f		300	-	300	ns
Set-up time for STOP condition.	$t_{SU.STO}$	4		0.6		µs
Bus free time between a STOP and START.	t_{BUF}	4.7		1.3		µs

Notes:

1. Maximum current is 5mA and capacitance load spec. =100pF

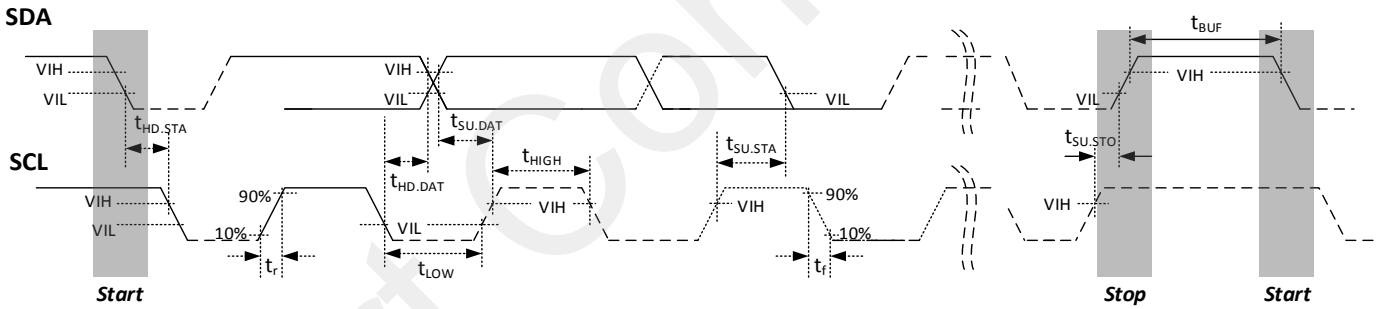

Figure 22. I²C Timing Diagram

7.0 Four-Wire SPI Serial Interface Communication

7.1 Signal Description

The four wires used for interface communication in PAH8002 are CSN (chip select), SCLK (clock), SDI (MOSI data) and SDO (MISO data). The PAH8002 is implemented as a slave-only device, so it never drives SCLK, and only drives SDO during read cycles.

Table 12. SPI Signals Description

Signal Name	Label	Type	Reset State	Description
Chip Select	SPI_CSN	Input	Input	The CSN signal is always driven by the master and active low.
Serial Clock	SPI_SCLK_I2C_SCL	Input	Input	The SCLK signal is always driven by the master. All data changes on SPI_SDI/SPI_SDO are latched at SCLK rising edge. The frequency of SCLK may vary throughout a transfer, as long as it meets all timing requirements.
Serial Data	SPI_SDI_I2C_SDA	Input	Input	The SDI (MOSI) signal is for the host (master) to write to the PAH8002. The host (master) drives SCLK and SDI (MOSI) in a write operation to the PAH8002.
Serial Data	SPI_SDO	Output	Output	The SDO (MISO) signal is for the host (master) to read from the PAH8002. The host (master) drives SCLK and SDI when requesting information from SDO of the PAH8002.

7.2 Packet Formats

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has bit-7 as its MSB to indicate data direction. The second byte contains the data.

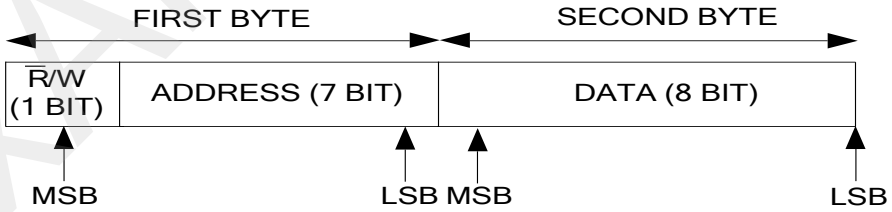

Figure 23. Four-wire SPI Transmission protocol

7.3 Driven Packets

7.3.1 Write Operation

A write operation is always initiated by the host controller and consists of two bytes, which the data is going from the host controller to the sensor. The first byte contains the 7 bits address and has a "1" as its MSB to indicate data direction. The second byte contains the full 8 bits data. This transfer is synchronized by SPI_SCLK_I2C_SCL. The host controller changes SPI_SDI_I2C_SDA at the falling edge of SPI_SCLK_I2C_SCL, while the sensor reads SPI_SDI_I2C_SDA at the rising edge of SPI_SCLK_I2C_SCL.

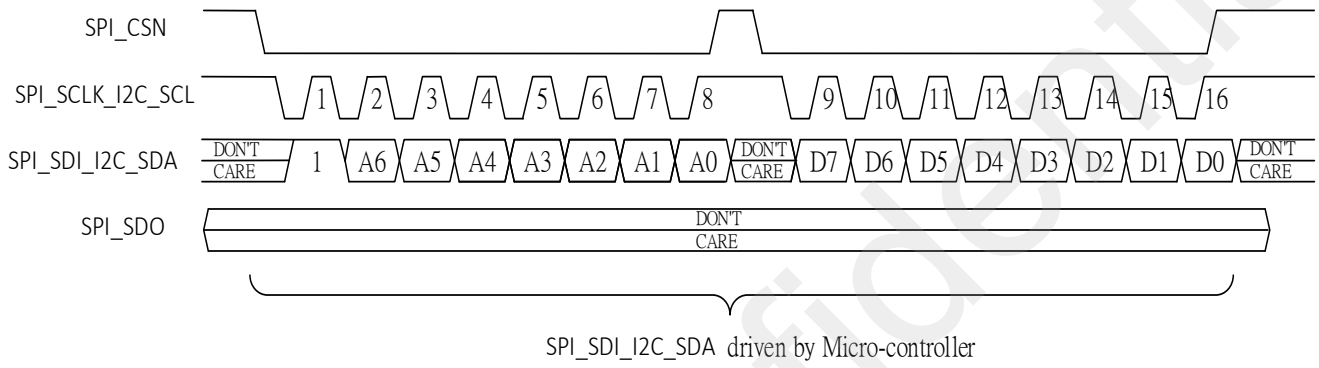

Figure 24. Four-wire SPI Write operation

7.3.2 Read Operation

A read operation is always initiated by the host controller and consists of two bytes, which the data is going from the sensor to the host controller. The first byte contains the 7 bits address that is written by the controller, and has a "0" as its MSB to indicate data direction. The second byte contains the full 8 bits data and is driven by the sensor. This transfer is synchronized by SPI_SCLK_I2C_SCL.

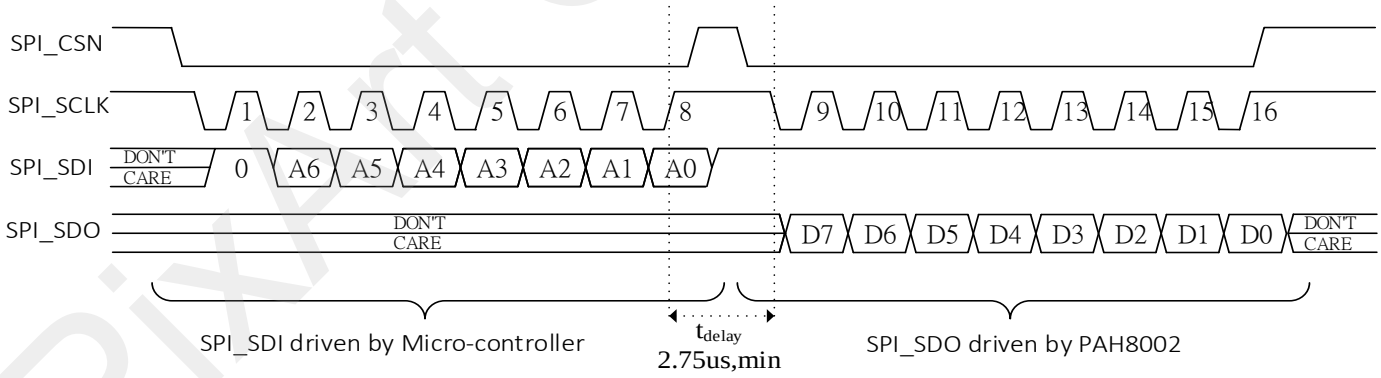

Figure 25. Four-wire SPI Read Operation

7.3.3 Switch Bank

For four-wire SPI interface, when the Read/Write Register addressing is beyond 0x7F in the Bank0, Bank1 and Bank2, the Switch Bank rule of (X+4) must be followed, where X is the bank number = 0, 1 and 2.

For example:

To read the data of Bank0 Addr0xE1, the following sequence shows the rule of bank switching from Bank0 to Bank4.

1. Write 0x04 to Addr0x7F //switch to Bank4
2. Read Addr0xE1 data

7.4 SPI Timing

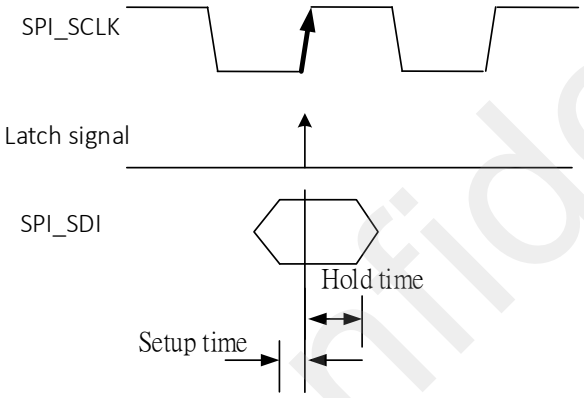

Figure 26. SPI Timing

Table 13. SPI Timing

Parameters	Symbol	Min	Max	Unit
Serial Host Write data bus setup time	Setup time	1/8 T		ns
Serial Host Write data bus hold time	Hold time	1/4 T		ns

Note：T = SPI clock (SPI_SCLK)

8.0 Digital SOC Function Control

8.1 Auto Exposure Control (AEC)

For the coverage of different human skin colors and tones, the sensor self-adjusts the exposure time and LED DAC current to optimize for the best brightness operating range.

- Three LED channels are controlled independently and output continuous signals. Refer to 0 registers section on the LED channels setting.
- Maximum exposure time is the value of AE_CHx_Max register and minimum exposure time is the value of AE_CHx_Min register. Refer to 10.3.3 registers section for the exposure time configuration.
- Maximum LED DAC current is set in LEDx_DAC_Code register and minimum LED DAC current is set in AE_LEDx_DAC_Min register. Refer to 10.6.5 and 10.6.6 registers section.

Example of Operating Range for Ch0 with bank0 0x77-0x7E registers and 1 sampling number.

- Bank0 0x77 and 0x78 is Outer Hi Bound, set value is 3072.
- Bank0 0x79 and 0x7A is Outer Low Bound, set value is 2048.
- Bank0 0x7B and 0x7C is Inner Hi Target, set value is 2816.
- Bank0 0x7D and 0x7E is Inner Low Target, set value is 2304.

Thus, ADC data convergence range is between 2048 and 3072. (2560 ± 512)

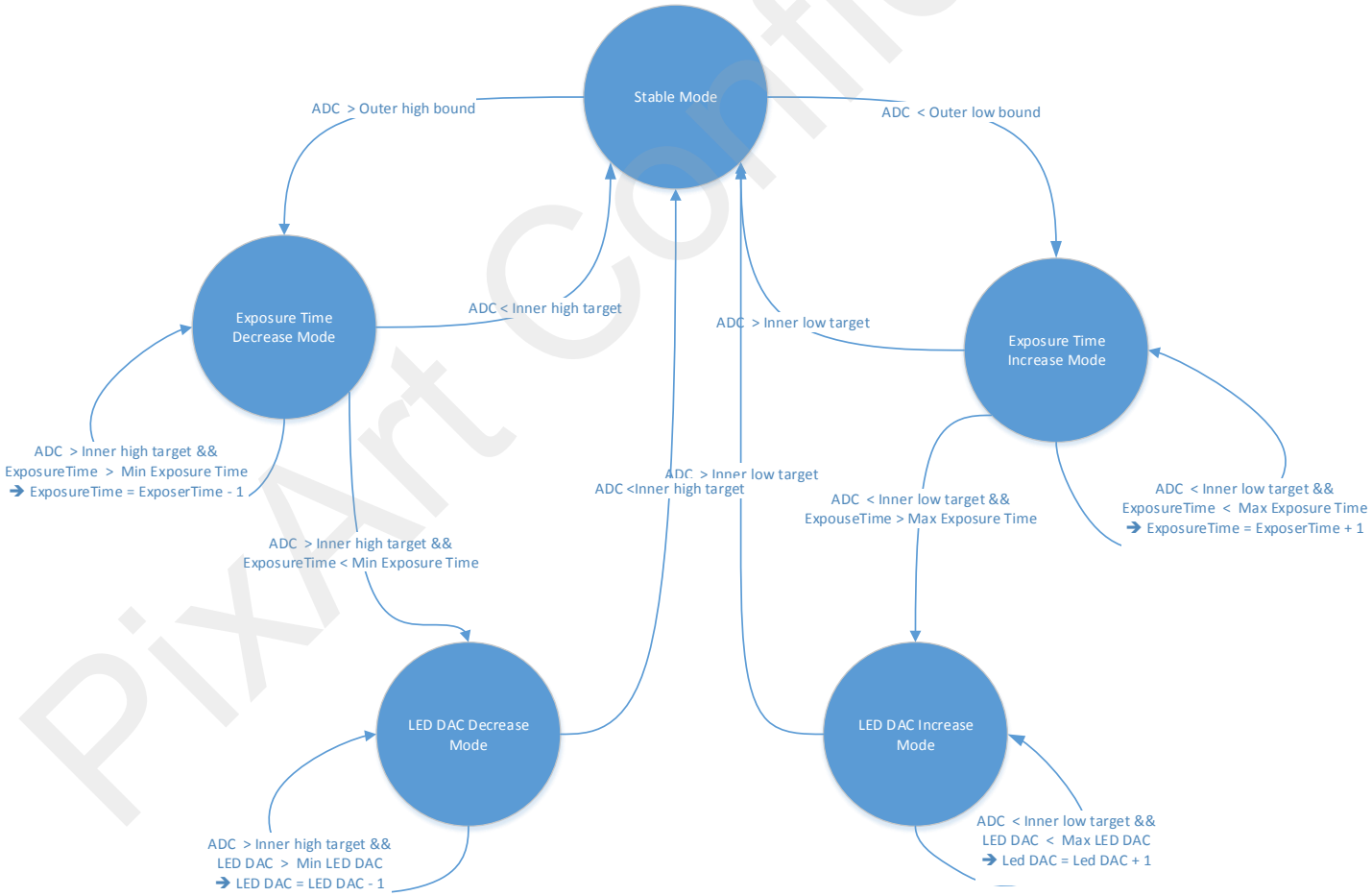

Figure 27. Auto Exposure Control Diagram

Table 14. Register Reference of Enabling AEC

Bank	Address	Register Name	Description
0	0x77, 0x78	AE_CH0_Outerbound_Hi	Auto exposure outer high bound of CH0/1/2
	0x9A, 0x9B	AE_CH1_Outerbound_Hi	
	0xBC, 0xBD	AE_CH2_Outerbound_Hi	
	0x7B, 0x7C	AE_CH0_Innertarget _Hi	Auto exposure inner high target of CH0/1/2
	0x9E, 0x9F	AE_CH1_Innertarget _Hi	
	0xC0, 0xC1	AE_CH2_Innertarget _Hi	
	0x7D, 0x7E	AE_CH0_Innertarget_Lo	Auto exposure inner low target of CH0/1/2
	0xA0, 0xA1	AE_CH1_Innertarget_Lo	
	0xC2, 0xC3	AE_CH2_Innertarget_Lo	
	0x79, 0x7A	AE_CH0_Outerbound_Lo	Auto exposure outer low bound of CH0/1/2
	0x9C, 0x9D	AE_CH1_Outerbound_Lo	
	0xBE, 0xBF	AE_CH2_Outerbound_Lo	
	0x6F, 0x70	AE_CH0_Max	Auto exposure time for the maximum bound of CH0/1/2
	0x92, 0x93	AE_CH1_Max	
	0xB4, 0xB5	AE_CH2_Max	
	0x71, 0x72	AE_CH0_Min	Auto exposure time for the minimum bound of CH0/1/2
	0x94, 0x95	AE_CH1_Min	
	0xB6, 0xB7	AE_CH2_Min	
	0x85	AE_LED0_DAC_Min	Auto LED DAC control for the minimum bound of CH0/1/2
	0xA7	AE_LED1_DAC_Min	
	0xC9	AE_LED2_DAC_Min	
1	0xBA	LED0_DAC_Code	Auto LED DAC control for the maximum bound of CH0/1/2
	0xBB	LED1_DAC_Code	
	0xBC	LED2_DAC_Code	

Table 15. Register Reference of Disabling AEC

Bank	Address	Register Name	Description
0	0x6C	AE_CH0_EnH	Disable Auto Exposure for CH0/1/2
	0x8F	AE_CH1_EnH	
	0xB1	AE_CH2_EnH	
	0x0D, 0x0E	Ch0_Man_ET	Manual set of fixed exposure time for CH0/1/2
	0x0F, 0x10	Ch1_Man_ET	
	0x11, 0x12	Ch2_Man_ET	
1	0xBA	LED0_DAC_Code	Manual set of fixed LED DAC current for CH0/1/2
	0xBB	LED1_DAC_Code	
	0xBC	LED2_DAC_Code	

Note: When disabling AE, the sensor will be fixed LED DAC current and exposure time. Refer to 10.3.3, 10.6.6 and 10.3.1 registers section.

8.2 Heart Rate Detection

Heart rate detection is an optical measurement technique that uses a light source and a detector to detect cardiovascular pulse wave that propagates through the body. The detected signal (pulse wave) called photoplethysmography and it is known as PPG/PTG. The PPG signal reflects the blood movement in the vessel, which goes from the heart to the fingertips through the blood vessels in a wave-like motion. Therefore, we can use this PPG signal to calculate heart rate.

This optical based technology could offer significant benefits in healthcare application as it is noninvasive, yet accurate and simple to use.

8.2.1 Applications

- Heart rate detection in general healthcare (Perfusion Index : Typ.1%)
- PPG Waveform

8.2.2 Heart Rate Detection Performance

Parameters	Value	Unit	Conditions
Heart Rate Measurement Range	30 - 240	bpm	
Heart Rate Tolerance of Root Mean Square (RMS)	±3	bpm	@ Room temperature for steady state: 0 km/hr.
	±5	bpm	@ Room temperature for motion state: 0 – 9 km/hr on the treadmill.
Response Time	8 - 10	second	@ Heart Rate = 72/bpm

Notes:

- PAH8002EP can provide heart rate measurement. However, it is not for medical device usage.
- For usage of heart rate detection sensor on the wearable device that to be put on the wrist, finger or palm,
  - The sensor must be placed securely and in-contact with the skin surface as well as keeping it stable without any motion during measurement in acquiring accurate heart rate measurement.
  - Do not wear the device on the wrist bone. It should be wear on the higher position of, especially for those with a smaller wrist.
- Sensor's performance is optimized with good blood flow. It is recommended to have light exercise for a few minutes to increase your blood flow before turning on the heart rate monitor.
- On cold weather condition or user is having poor blood circulation (e.g.: cold hands, fingers and feet), the sensor performance (heart rate accuracy) could be effected as the blood flow is slower in the measuring spot position. It is recommended to activate the heart rate monitor in indoor use.
- If the sensor is having problem to read heart rate, may try to swap it on the other side of hand wrist to repeat the measurement.
- For continuous heart rate measurement, do minimize hand movement and extreme bending of the wrist.

8.3 IR Touch Detection

To enable IR Touch Detection function, configure the touch detection upper threshold, lower threshold and count registers in the PAH8002EP. Touch detection count period is the same as report rate period. A Touch action is reported when ADC data is more than both the touch detection upper threshold and count thresholds. HW INT will be triggered when change status from No Touch to Touch and from Touch to No Touch. A No Touch action is reported when ADC data is lower than touch detection lower threshold but above count threshold. Refer to 10.8 registers section.

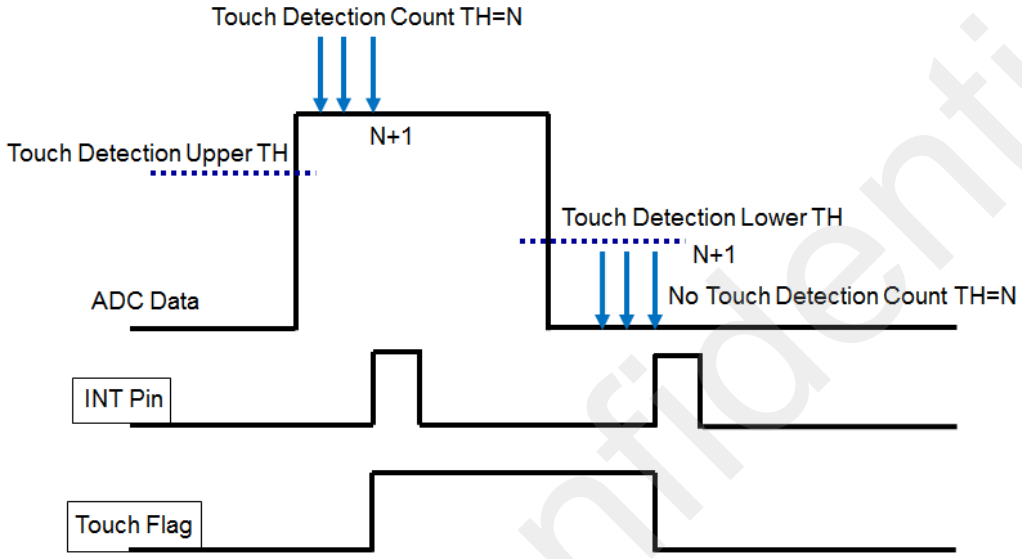

Figure 28. Touch Detection for INT Application

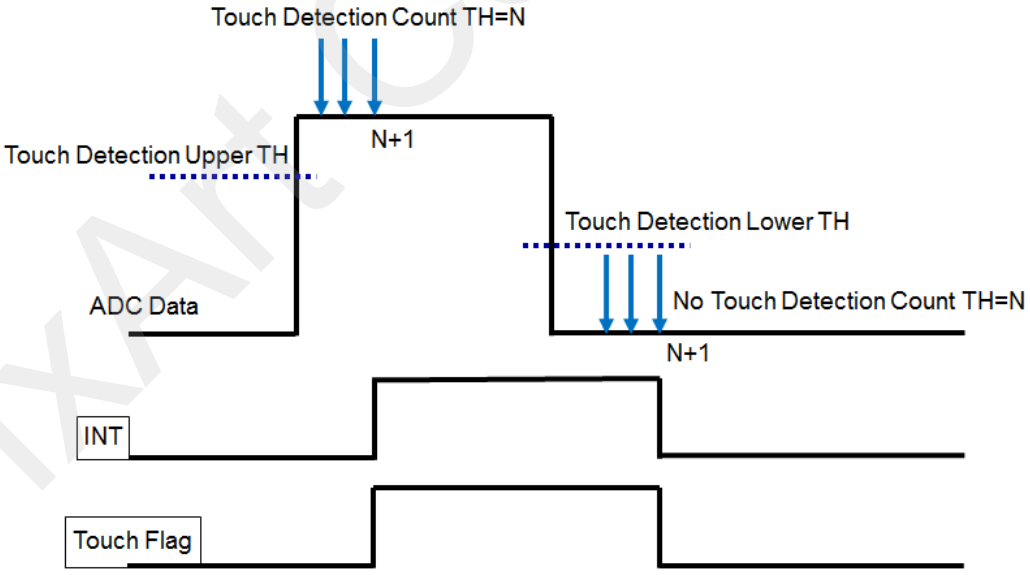

Figure 29. Touch Detection for Touch Flag Application

9.0 Operation Examples

9.1 IR Touch Detection Sequence

The following illustrates the steps to be in Touch mode.

1. Wake up Sensor (Read ID bank0 Addr0x00=0x02, Write 0x00 to Bank2 Addr0x70)
2. Run SW Reset (Write 0x00 to Bank0 Addr0xE1)
3. Load Touch setting for Touch mode. Refer to 11.1 and 11.2 appendix section.
4. Enable MCU interrupt.
5. Write 0x01 to Bank1 Addr0xD5 enable sensor.
6. Wait for touch interrupt.
7. When getting interrupt, execute (1.) action, then report touch status to MCU.

9.2 Obtaining Heart Rate PPG Raw Data Sequence with SRAM Buffer Mode

The following illustrates the steps to be in PPG mode.

1. Wake up Sensor (Read ID bank0 Addr0x00=0x02, Write 0x00 to Bank2 Addr0x70)
2. Run SW Reset (Write 0x00 to Bank0 Addr0xE1)
3. Load PPG setting of 20Hz for PPG mode. Refer to 11.3 appendix section.
4. Enable MCU interrupt.
5. Write 0x3D to Bank1 Addr0xEA set each 20 ADC data of three channels. Total is 3*20*4=240 bytes. FIFO data ready interval is 1 second for 20Hz report rate. Refer to 10.11 registers section.
6. Write 0x01 to Bank1 Addr0xD5 enable sensor.
7. Wait for FIFO interrupt.
8. When getting interrupt, execute (1.) action, then read out Bank3 Addr0x00 to get raw data from FIFO and clear interrupt (Write 0x01 to Bank2 Addr0x75, then Write 0x00 to Bank2 Addr0x75).
9. Exclusive or (XOR) FIFO data and compare with check sum register (burst read from bank2 Addr0x80~ Addr0x83)
10. Compare raw data and touch threshold to determine touch status.
11. Report PPG raw data and touch status to MCU.

9.3 Sleep Mode Sequence for Power Saving

The following illustrates the steps to be in sleep mode.

1. Wake up Sensor (Read ID bank0 Addr0x00=0x02, Write 0x00 to Bank2 Addr0x70)
2. Run SW Reset (Write 0x00 to Bank0 Addr0xE1)
3. Load Sleep setting for Sleep mode. Refer to 11.4 appendix section.
4. Write 0x01 to Bank1 Addr0xD5 enable sensor.

10.0 Registers

10.1 Registers List

Table 16. Register Bank0

Note: Switch to Register Bank0 by writing 0x00 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x00	Product_ID_LB	RO	0x02	0x6E	AE_Ch0_Mid_HB	R/W	0x00
0x01	Product_ID_HB	RO	0x80	0x6F	AE_Ch0_Max_LB	R/W	0xF0
0x02	Version_ID	RO	0xDx	0x70	AE_Ch0_Max_HB	R/W	0x00
0x0D	Ch0_Man_ET_LB	R/W	0xC8	0x71	AE_Ch0_Min_LB	R/W	0x52
0x0E	Ch0_Man_ET_HB	R/W	0x00	0x72	AE_Ch0_Min_HB	R/W	0x00
0x0F	Ch1_Man_ET_LB	R/W	0xA0	0x77	AE_Ch0_Outerbound_Hi_LB	R/W	0x00
0x10	Ch1_Man_ET_HB	R/W	0x00	0x78	AE_Ch0_Outerbound_Hi_HB	R/W	0x06
0x11	Ch2_Man_ET_LB	R/W	0x78	0x79	AE_Ch0_Outerbound_Lo_LB	R/W	0x00
0x12	Ch2_Man_ET_HB	R/W	0x00	0x7A	AE_Ch0_Outerbound_Lo_HB	R/W	0x02
0x16	Ana_BG	R/W	0x00	0x7B	AE_Ch0_Innertarget_Hi_LB	R/W	0x00
0x3B	Ch0_Samp_Num	R/W	0x32	0x7C	AE_Ch0_Innertarget_Hi_HB	R/W	0x05
0x3C	Ch1_Samp_Num	R/W	0x20	0x7D	AE_Ch0_Innertarget_Lo_LB	R/W	0x00
0x3D	Ch2_Samp_Num	R/W	0x20	0x7E	AE_Ch0_Innertarget_Lo_HB	R/W	0x03
0x47	Ch0_Global_EnH	R/W	0x01	0x85	AE_LED0_DAC_Min	R/W	0x01
0x48	Ch1_Global_EnH	R/W	0x00	0x8E	AE_LED0_DAC_EnH	R/W	0x01
0x49	Ch2_Global_EnH	R/W	0x00	0x8F	AE_Ch1_EnH	R/W	0x01
0x4A	LED0_Sub_EnH	R/W	0x00	0x90	AE_Ch1_Mid_LB	R/W	0xA0
0x4B	LED1_Sub_EnH	R/W	0x01	0x91	AE_Ch1_Mid_HB	R/W	0x00
0x4C	LED2_Sub_EnH	R/W	0x01	0x92	AE_Ch1_Max_LB	R/W	0xF0
0x4D	LED_OnOff_Swap	R/W	0x01	0x93	AE_Ch1_Max_HB	R/W	0x00
0x50	Normalized_Mode_EnL_1	R/W	0x00	0x94	AE_Ch1_Min_LB	R/W	0x52
0x51	Normalized_Mode_EnL_2	R/W	0x00	0x95	AE_Ch1_Min_HB	R/W	0x00
0x56	Normalized_Right_Shift	R/W	0x07	0x9A	AE_Ch1_Outerbound_Hi_LB	R/W	0x00
0x5A	Touch_Detect_EnH	R/W	0x00	0x9B	AE_Ch1_Outerbound_Hi_HB	R/W	0x06
0x5C	TouchDetection_Upper_TH_1	R/W	0x00	0x9C	AE_Ch1_Outerbound_Lo_LB	R/W	0x00
0x5D	TouchDetection_Upper_TH_2	R/W	0x02	0x9D	AE_Ch1_Outerbound_Lo_HB	R/W	0x02
0x5E	TouchDetection_Upper_TH_3	R/W	0x00	0x9E	AE_Ch1_Innertarget_Hi_LB	R/W	0x00
0x5F	TouchDetection_Upper_TH_4	R/W	0x00	0x9F	AE_Ch1_Innertarget_Hi_HB	R/W	0x05
0x60	TouchDetection_Lower_TH_1	R/W	0x80	0xA0	AE_Ch1_Innertarget_Lo_LB	R/W	0x00
0x61	TouchDetection_Lower_TH_2	R/W	0x00	0xA1	AE_Ch1_Innertarget_Lo_HB	R/W	0x03
0x62	TouchDetection_Lower_TH_3	R/W	0x00	0xA7	AE_LED1_DAC_Min	R/W	0x01
0x63	TouchDetection_Lower_TH_4	R/W	0x00	0xB0	AE_LED1_DAC_EnH	R/W	0x01
0x64	TouchDetection_Count_TH	R/W	0x0A	0xB1	AE_Ch2_EnH	R/W	0x01
0x65	NoTouchDetection_Count_TH	R/W	0x0A	0xB2	AE_Ch2_Mid_LB	R/W	0xA0
0x6C	AE_Ch0_EnH	R/W	0x01	0xB3	AE_Ch2_Mid_HB	R/W	0x00
0x6D	AE_Ch0_Mid_LB	R/W	0xA0	0xB4	AE_Ch2_Max_LB	R/W	0xF0

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0xB5	AE_Ch2_Max_HB	R/W	0x00	0xC1	AE_Ch2_Innertarget_Hi_HB	R/W	0x05
0xB6	AE_Ch2_Min_LB	R/W	0x52	0xC2	AE_Ch2_Innertarget_Lo_LB	R/W	0x00
0xB7	AE_Ch2_Min_HB	R/W	0x00	0xC3	AE_Ch2_Innertarget_Lo_HB	R/W	0x03
0xBC	AE_Ch2_Outerbound_Hi_LB	R/W	0x00	0xC9	AE_LED2_DAC_Min	R/W	0x01
0xBD	AE_Ch2_Outerbound_Hi_HB	R/W	0x06	0xD2	AE_LED2_DAC_EnH	R/W	0x01
0xBE	AE_Ch2_Outerbound_Lo_LB	R/W	0x00	0xDE	PGAgain_Sel	R/W	0x01
0xBF	AE_Ch2_Outerbound_Lo_HB	R/W	0x02	0xE1	SW_Reset_N	R/W	0x01
0xC0	AE_Ch2_Innertarget_Hi_LB	R/W	0x00	0xE6	LED_DAC_Change_Flag_EnH	R/W	0x00

Table 17. Register Bank1

Note: Switch to Register Bank1 by writing 0x01 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x7A	BG_Sub_EnH	R/W	0x00	0xBB	LED1_DAC_Code	R/W	0x40
0x7C	Congain_Sel	R/W	0x00	0xBC	LED2_DAC_Code	R/W	0x40
0x80	PS_Ctrl_EnH	R/W	0x01	0xC0	LPT_EnH	R/W	0x01
0xB4	LED0_Man_EnH	R/W	0x00	0xC3	OSC_EnL	R/W	0x00
0xB5	LED1_Man_EnH	R/W	0x00	0xD5	TIMER_Gen_Enable	R/W	0x00
0xB6	LED2_Man_EnH	R/W	0x00	0xD6	TIMER_Gen_Period_LB	R/W	0x40
0xB7	LED0_DAC_EnL	R/W	0x00	0xD7	TIMER_Gen_Period_HB	R/W	0x01
0xB8	LED1_DAC_EnL	R/W	0x00	0xE6	IF_Wakeup_Interval_LB	R/W	0x05
0xB9	LED2_DAC_EnL	R/W	0x00	0xE7	IF_Wakeup_Interval_HB	R/W	0x00
0xBA	LED0_DAC_Code	R/W	0x40	0xEA	SetFIFO_RptNum	R/W	0x03

Table 18. Register Bank2

Note: Switch to Register Bank2 by writing 0x02 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x25	INT_Mode_Sel	R/W	0x00	0x83	Readout_FIFO_Checksum_4	RO	0x00
0x29	INT_Output_EnL	R/W	0x01	0x8C	INT_SramFIFO_Overflow_Clear	R/W	0x00
0x45	Touch_Flag	RO	0x00	0x8D	INT_SramFIFO_Overflow_Mask	R/W	0x00
0x73	INT_Reg_Array	RO	0x00	0x8E	INT_SramFIFO_Underflow_Clear	R/W	0x00
0x74	INT_SramFIFO_DR_Mask	R/W	0x00	0x8F	INT_SramFIFO_Underflow_Mask	R/W	0x00
0x75	INT_SramFIFO_DR_Clear	R/W	0x00	0xA0	CH0_Exposure_Time_LB	RO	0x00
0x76	INT_TouchDet_Mask	R/W	0x00	0xA1	CH0_Exposure_Time_HB	RO	0x00
0x77	INT_TouchDet_Clear	R/W	0x00	0xA2	CH1_Exposure_Time_LB	RO	0x00
0x78	All_INT_Mask	R/W	0x00	0xA3	CH1_Exposure_Time_HB	RO	0x00
0x7A	INT_Type	R/W	0x01	0xA4	CH2_Exposure_Time_LB	RO	0x00
0x7B	INT_Pulse_Width	R/W	0x08	0xA5	CH2_Exposure_Time_HB	RO	0x00
0x80	Readout_FIFO_Checksum_1	RO	0x00	0xA6	LED0_DAC_Value	RO	0x00
0x81	Readout_FIFO_Checksum_2	RO	0x00	0xA7	LED1_DAC_Value	RO	0x00
0x82	Readout_FIFO_Checksum_3	RO	0x00	0xA8	LED2_DAC_Value	RO	0x00

10.2 Sensor Array Controls

Table 19. Sensor Array Controls Registers Usage Reference

Usage	Register Addresses
PGA Gain	Bank0: 0xDE
Background Subtraction	Bank1: 0x7A
Conversion Gain	Bank1: 0x7C

10.2.1 PGAgain_Sel Register

Register Name	PGAgain_Sel							
Bank	0			Address		0xDE		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							PGA Gain
Description	Bit[0] is used for PGA gain factor control.							

Field	Access	Reset	Value	Description
PGA Gain	R/W	1	0	1x
			1	2x

10.2.2 BG_Sub_EnH Register

Register Name	BG_Sub_EnH							
Bank	1			Address		0x7A		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							BG_Sub
Description	Bit[0] is used to enable background subtraction.							

Field	Access	Reset	Value	Description
BG_Sub	R/W	0	0	Disable
			1	Enable

10.2.3 Congain_Sel Register

Register Name	Congain_Sel							
Bank	1			Address		0x7C		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							Congain
Description	Bit[0] is used for conversion gain factor control.							

Field	Access	Reset	Value	Description
Congain	R/W	0	0	4x
			1	1x

10.3 Image Sensor Core Digital Controls

Table 20. Image Sensor Core Digital Registers Usage Reference

Usage	Register Addresses
Channel Exposure Time	Bank0: 0x0D – 0x12,
Analog Background Subtraction Mode	Bank0: 0x16
Auto Exposure Controls	Bank0: 0x6C – 0x72, 0x8F – 0x95, 0xB1 – 0xB7
Auto Exposure Convergence Range	Bank0: 0x77-0x7E, 0x9A-0xA1, 0xBC-0xC3

10.3.1 Channel Exposure time

10.3.1.1 CH0_Man_ET Register

Register Name	Ch0_Man_ET_LB							
Bank	0			Address		0x0D		
Access	R/W			Reset Value		0xC8		
Bit	7	6	5	4	3	2	1	0
Field	Ch0_Man_ET[7:0]							
Register Name	**Ch0_Man_ET_HB**							
Bank	0			Address		0x0E		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Ch0_Man_ET[15:8]							
Description	Manual set of exposure time for LED0 Channel. Ch0_Man_ET[7:0] are the lower 8bits and Ch0_Man_ET[15:8] are the upper 8bits.Each bit step is 62.5ns. Reset value: 0x00C8 = 200 Default exposure time = 62.5ns x 200 = 12500ns = 12.5µs							

10.3.1.2 CH1_Man_ET Register

Register Name	Ch1_Man_ET_LB							
Bank	0			Address		0x0F		
Access	R/W			Reset Value		0xA0		
Bit	7	6	5	4	3	2	1	0
Field	Ch1_Man_ET[7:0]							
Register Name	**Ch1_Man_ET_HB**							
Bank	0			Address		0x10		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Ch1_Man_ET[15:8]							
Description	Manual set of exposure time for LED1 Channel. Ch1_Man_ET[7:0] are the lower 8bits and Ch1_Man_ET[15:8] are the upper 8bits. Each bit step is 62.5ns. Reset value: 0x00A0 = 160 Default exposure time: 62.5ns x 160 = 10000ns = 10.0µs							

10.3.1.3 CH2_Man_ET Register

Register Name	Ch2_Man_ET_LB							
Bank	0			Address		0x11		
Access	R/W			Reset Value		0x78		
Bit	7	6	5	4	3	2	1	0
Field	Ch2_Man_ET[7:0]							
Register Name	**Ch2_Man_ET_HB**							
Bank	0			Address		0x12		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Ch2_Man_ET[15:8]							
Description	Manual set of exposure time for LED2 Channel. Ch2_Man_ET[7:0] are the lower 8bits and Ch2_Man_ET[15:8] are the upper 8bits. Each bit step is 62.5ns. Reset value: 0x0078 = 120 Default exposure time: 62.5ns x 120 = 7500ns = 7.5µs							

10.3.2 Analog Background Subtraction

10.3.2.1 Analog Background Subtraction Mode Register

Register Name	Ana_BG							
Bank	0			Address		0x16		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							Ana_BG
Description	Bit[0] is used to enable the Analog background subtraction mode. If Analog background subtraction mode is enabled, user must set LED_Swap bit to 1 manually. Refer to 10.6.4.							

Field	Access	Reset	Value	Description
Ana_BG	R/W	0	0	Disable
			1	Enable

10.3.3 Auto Exposure Control

10.3.3.1 AE_CH0_EnH Register

Register Name	AE_CH0_EnH							
Bank	0			Address		0x6C		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							AE_CH
Description	Bit[0] is used to enable Auto Exposure for Channel 0.							

Field	Access	Reset	Value	Description
AE_CH	R/W	1	0	Disable
			1	Enable

10.3.3.2 AE_CH0_Mid Register

Register Name	AE_CH0_Mid_LB							
Bank	0			Address		0x6D		
Access	R/W			Reset Value		0xA0		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Mid[7:0]							
Register Name	**AE_CH0_Mid_HB**							
Bank	0			Address		0x6E		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Mid[15:8]							
Description	Set the AE control exposure time for the middle bound of Channel 0. AE_CH0_Mid[7:0] are the lower 8bits and AE_CH0_Mid[15:8] are the upper 8bits.							

10.3.3.3 AE_CH0_Max Register

Register Name	AE_CH0_Max_LB							
Bank	0			Address		0x6F		
Access	R/W			Reset Value		0xF0		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Max[7:0]							
Register Name	**AE_CH0_Max_HB**							
Bank	0			Address		0x70		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Max[15:8]							
Description	Set the AE control exposure time for the maximum bound of Channel 0. AE_CH0_Max[7:0] are the lower 8bits and AE_CH0_Max[15:8] are the upper 8bits.							

10.3.3.4 AE_CH0_Min Register

Register Name	AE_CH0_Min_LB							
Bank	0			Address		0x71		
Access	R/W			Reset Value		0x52		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Min[7:0]							
Register Name	**AE_CH0_Min_HB**							
Bank	0			Address		0x72		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Min[15:8]							
Description	Set the AE control exposure time for the minimum bound of Channel 0. AE_CH0_Min[7:0] are the lower 8bits and AE_CH0_Min[15:8] are the upper 8bits.							

10.3.3.5 AE_CH1_EnH Register

Register Name	AE_CH1_EnH							
Bank	0			Address		0x8F		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							AE_CH1
Description	Bit[0] is used to enable Auto Exposure for Channel 1.							

Field	Access	Reset	Value	Description
AE_CH1	R/W	1	0	Disable
			1	Enable

10.3.3.6 AE_CH1_Mid Register

Register Name	AE_CH1_Mid_LB							
Bank	0			Address		0x90		
Access	R/W			Reset Value		0xA0		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Mid[7:0]							
Register Name	**AE_CH1_Mid_HB**							
Bank	0			Address		0x91		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Mid[15:8]							
Description	Set the AE control exposure time for the middle bound of Channel 1. AE_CH1_Mid[7:0] are the lower 8bits and AE_CH1_Mid[15:8] are the upper 8bits.							

10.3.3.7 AE_CH1_Max Register

Register Name	AE_CH1_Max_LB							
Bank	0			Address		0x92		
Access	R/W			Reset Value		0xF0		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Max[7:0]							
Register Name	**AE_CH1_Max_HB**							
Bank	0			Address		0x93		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Max[15:8]							
Description	Set the AE control exposure time for the maximum bound of Channel 1. AE_CH1_Max[7:0] are the lower 8bits and AE_CH1_Max[15:8] are the upper 8bits.							

10.3.3.8 AE_CH1_Min Register

Register Name	AE_CH1_Min_LB							
Bank	0			Address		0x94		
Access	R/W			Reset Value		0x52		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Min[7:0]							
Register Name	**AE_CH1_Min_HB**							
Bank	0			Address		0x95		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Min[15:8]							
Description	Set the AE control exposure time for the minimum bound of Channel 1. AE_CH1_Min[7:0] are the lower 8bits and AE_CH1_Min[15:8] are the upper 8bits.							

10.3.3.9 AE_CH2_EnH Register

Register Name	AE_CH2_EnH							
Bank	0			Address		0xB1		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							AE_CH2
Description	Bit[0] is used to enable Auto Exposure for Channel 2.							

Field	Access	Reset	Value	Description
AE_CH2	R/W	1	0	Disable
			1	Enable

10.3.3.10 AE_CH2_Mid Register

Register Name	AE_CH2_Mid_LB							
Bank	0			Address		0xB2		
Access	R/W			Reset Value		0xA0		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Mid[7:0]							
Register Name	**AE_CH2_Mid_HB**							
Bank	0			Address		0xB3		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Mid[15:8]							
Description	Set the AE control exposure time for the middle bound of Channel 2. AE_CH2_Mid[7:0] are the lower 8bits and AE_CH2_Mid[15:8] are the upper 8bits.							

10.3.3.11 AE_CH2_Max Register

Register Name	AE_CH2_Max_LB							
Bank	0			Address		0xB4		
Access	R/W			Reset Value		0xF0		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Max[7:0]							
Register Name	**AE_CH2_Max_HB**							
Bank	0			Address		0xB5		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Max[15:8]							
Description	Set the AE control exposure time for the maximum bound of Channel 2. AE_CH2_Max[7:0] are the lower 8bits and AE_CH2_Max[15:8] are the upper 8bits.							

10.3.3.12 AE_CH2_Min Register

Register Name	AE_CH2_Min_LB							
Bank	0			Address		0xB6		
Access	R/W			Reset Value		0x52		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Min[7:0]							
Register Name	**AE_CH2_Min_HB**							
Bank	0			Address		0xB7		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Min[15:8]							
Description	Set the AE control exposure time for the minimum bound of Channel 2. AE_CH2_Min[7:0] are the lower 8bits and AE_CH2_Min[15:8] are the upper 8bits.							

10.3.4 Auto Exposure Convergence Range

10.3.4.1 AE_CH0_Outerbound_Hi Register

Register Name	AE_CH0_Outerbound_Hi_LB							
Bank	0			Address		0x77		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Outerbound_Hi[7:0]							
Register Name	**AE_CH0_Outerbound_Hi_HB**							
Bank	0			Address		0x78		
Access	R/W			Reset Value		0x06		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Outerbound_Hi[15:8]							
Description	Set the AE convergence range for the outer high bound of Channel 0. AE_CH0_Outerbound_Hi [7:0] are the lower 8bits and AE_CH0_Outerbound_Hi [15:8] are the upper 8bits.							

10.3.4.2 AE_CH0_Outerbound_Lo Register

Register Name	AE_CH0_Outerbound_Lo_LB							
Bank	0			Address		0x79		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Outerbound_Lo[7:0]							
Register Name	**AE_CH0_Outerbound_Lo_HB**							
Bank	0			Address		0x7A		
Access	R/W			Reset Value		0x02		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Outerbound_Lo[15:8]							
Description	Set the AE convergence range for the outer low bound of Channel 0. AE_CH0_Outerbound_Lo [7:0] are the lower 8bits and AE_CH0_Outerbound_Lo [15:8] are the upper 8bits.							

10.3.4.3 AE_CH0_Innertarget_Hi Register

Register Name	AE_CH0_Innertarget_Hi_LB							
Bank	0			Address		0x7B		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Innertarget_Hi[7:0]							
Register Name	**AE_CH0_Innertarget_Hi_HB**							
Bank	0			Address		0x7C		
Access	R/W			Reset Value		0x05		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Innertarget _Hi[15:8]							
Description	Set the AE convergence range for the inner high target of Channel 0. AE_CH0_Innertarget _Hi [7:0] are the lower 8bits and AE_CH0_Innertarget _Hi [15:8] are the upper 8bits.							

10.3.4.4 AE_CH0_Innertarget_Lo Register

Register Name	AE_CH0_Innertarget_Lo_LB							
Bank	0			Address		0x7D		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Innertarget_Lo[7:0]							
Register Name	**AE_CH0_Innertarget_Lo_HB**							
Bank	0			Address		0x7E		
Access	R/W			Reset Value		0x03		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH0_Innertarget _Lo[15:8]							
Description	Set the AE convergence range for the inner low target of Channel 0. AE_CH0_Innertarget _Lo [7:0] are the lower 8bits and AE_CH0_Innertarget _Lo [15:8] are the upper 8bits.							

10.3.4.5 AE_CH1_Outerbound_Hi Register

Register Name	AE_CH1_Outerbound_Hi_LB							
Bank	0			Address		0x9A		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Outerbound_Hi[7:0]							
Register Name	**AE_CH1_Outerbound_Hi_HB**							
Bank	0			Address		0x9B		
Access	R/W			Reset Value		0x06		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Outerbound_Hi[15:8]							
Description	Set the AE convergence range for the outer high bound of Channel 1. AE_CH1_Outerbound_Hi [7:0] are the lower 8bits and AE_CH1_Outerbound_Hi [15:8] are the upper 8bits.							

10.3.4.6 AE_CH1_Outerbound_Lo Register

Register Name	AE_CH1_Outerbound_Lo_LB							
Bank	0			Address		0x9C		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Outerbound_Lo[7:0]							
Register Name	**AE_CH1_Outerbound_Lo_HB**							
Bank	0			Address		0x9D		
Access	R/W			Reset Value		0x02		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Outerbound_Lo[15:8]							
Description	Set the AE convergence range for the outer low bound of Channel 1. AE_CH1_Outerbound_Lo [7:0] are the lower 8bits and AE_CH1_Outerbound_Lo [15:8] are the upper 8bits.							

10.3.4.7 AE_CH1_Innertarget_Hi Register

Register Name	AE_CH1_Innertarget_Hi_LB							
Bank	0			Address		0x9E		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Innertarget_Hi[7:0]							
Register Name	**AE_CH1_Innertarget_Hi_HB**							
Bank	0			Address		0x9F		
Access	R/W			Reset Value		0x05		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Innertarget _Hi[15:8]							
Description	Set the AE convergence range for the inner high target of Channel 1. AE_CH1_Innertarget _Hi [7:0] are the lower 8bits and AE_CH1_Innertarget _Hi [15:8] are the upper 8bits.							

10.3.4.8 AE_CH1_Innertarget_Lo Register

Register Name	AE_CH1_Innertarget_Lo_LB							
Bank	0			Address		0xA0		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Innertarget_Lo[7:0]							
Register Name	**AE_CH1_Innertarget_Lo_HB**							
Bank	0			Address		0xA1		
Access	R/W			Reset Value		0x03		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH1_Innertarget _Lo[15:8]							
Description	Set the AE convergence range for the inner low target of Channel 1. AE_CH1_Innertarget _Lo [7:0] are the lower 8bits and AE_CH1_Innertarget _Lo [15:8] are the upper 8bits.							

10.3.4.9 AE_CH2_Outerbound_Hi Register

Register Name	AE_CH2_Outerbound_Hi_LB							
Bank	0			Address		0xBC		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Outerbound_Hi[7:0]							
Register Name	**AE_CH2_Outerbound_Hi_HB**							
Bank	0			Address		0xBD		
Access	R/W			Reset Value		0x06		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Outerbound_Hi[15:8]							
Description	Set the AE convergence range for the outer high bound of Channel 2. AE_CH2_Outerbound_Hi [7:0] are the lower 8bits and AE_CH2_Outerbound_Hi [15:8] are the upper 8bits.							

10.3.4.10 AE_CH2_Outerbound_Lo Register

Register Name	AE_CH2_Outerbound_Lo_LB							
Bank	0			Address		0xBE		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Outerbound_Lo[7:0]							
Register Name	**AE_CH2_Outerbound_Lo_HB**							
Bank	0			Address		0xBF		
Access	R/W			Reset Value		0x02		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Outerbound_Lo[15:8]							
Description	Set the AE convergence range for the outer low bound of Channel 2. AE_CH2_Outerbound_Lo [7:0] are the lower 8bits and AE_CH2_Outerbound_Lo [15:8] are the upper 8bits.							

10.3.4.11 AE_CH2_Innertarget_Hi Register

Register Name	AE_CH2_Innertarget_Hi_LB							
Bank	0			Address		0xC0		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Innertarget_Hi[7:0]							
Register Name	**AE_CH2_Innertarget_Hi_HB**							
Bank	0			Address		0xC1		
Access	R/W			Reset Value		0x05		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Innertarget _Hi[15:8]							
Description	Set the AE convergence range for the inner high target of Channel 2. AE_CH2_Innertarget _Hi [7:0] are the lower 8bits and AE_CH2_Innertarget _Hi [15:8] are the upper 8bits.							

10.3.4.12 AE_CH2_Innertarget_Lo Register

Register Name	AE_CH2_Innertarget_Lo_LB							
Bank	0			Address		0xC2		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Innertarget_Lo[7:0]							
Register Name	**AE_CH2_Innertarget_Lo_HB**							
Bank	0			Address		0xC3		
Access	R/W			Reset Value		0x03		
Bit	7	6	5	4	3	2	1	0
Field	AE_CH2_Innertarget _Lo[15:8]							
Description	Set the AE convergence range for the inner low target of Channel 2. AE_CH2_Innertarget _Lo [7:0] are the lower 8bits and AE_CH2_Innertarget _Lo [15:8] are the upper 8bits.							

10.4 Reset

10.4.1.1 SW_Reset Register

Register Name	SW_Reset_N							
Bank	0			Address		0xE1		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							SW_Reset_N
Description	Software reset for all digital blocks. Signal is Active Low.							

Field	Access	Reset	Value	Description
SW_Reset_N	R/W	1	0	Reset all digital blocks
			1	In current use-mode

10.5 Power Saving

10.5.1 PS_Ctrl_EnH Register

Register Name	PS_Ctrl_EnH							
Bank	1			Address		0x80		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							PS_Ctrl
Description	Bit[0] is used to enable power saving mechanism for reducing power consumption of analog and digital block. Refer to Power Saving Mechanism section.							

Field	Access	Reset	Value	Description
PS_Ctrl	R/W	0	0	Disable
			1	Enable

10.5.2 Wakeup Interval Registers

Register Name	IF_Wakeup_Interval_LB							
Bank	1			Address		0xE6		
Access	R/W			Reset Value		0x05		
Bit	7	6	5	4	3	2	1	0
Field	IF_Wakeup_Interval [7:0]							
Register Name	**IF_Wakeup_Interval_HB**							
Bank	1			Address		0xE7		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	IF_Wakeup_Interval [15:8]							
Description	While in power saving mode, once I^2C/SPI goes to idle state and after Sleep Time period, the chip will go to Sleep mode. Sleep Time = IF_Wakeup_Interval [15:0] x 31.25µs Default Time = 5 x 31.25µs =156.25µs							

10.6 LED Controls

10.6.1 Channel Sampling Number

10.6.1.1 CH0_Sampling_Number Register

Register Name	CH0_Sampling_Number							
Bank	0			Address		0x3B		
Access	R/W			Reset Value		0x32		
Bit	7	6	5	4	3	2	1	0
Field	CH0_Sampling_Number[7:0]							
Description	Set the LED0 sampling number of Channel 0.							

10.6.1.2 CH1_Sampling_Number Register

Register Name	CH0_Sampling_Number							
Bank	0			Address		0x3C		
Access	R/W			Reset Value		0x20		
Bit	7	6	5	4	3	2	1	0
Field	CH1_Sampling_Number[7:0]							
Description	Set the LED1 sampling number of Channel 1.							

10.6.1.3 CH2_Sampling_Number Register

Register Name	CH0_Sampling_Number							
Bank	0			Address		0x3D		
Access	R/W			Reset Value		0x20		
Bit	7	6	5	4	3	2	1	0
Field	CH2_Sampling_Number[7:0]							
Description	Set the LED2 sampling number of Channel 2.							

10.6.2 Channel Main Switch Enable

Sensor can support three channels and user can select to use either one, two or three channels.

10.6.2.1 CH0_Global_EnH Register

Register Name	CH0_Global_EnH							
Bank	0			Address		0x47		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							CH0_Glob
Description	Bit[0] is used for main switch enable of Channel 0							

Field	Access	Reset	Value	Description
CH0_Glob	R/W	1	0	Disable
			1	Enable

10.6.2.2 CH1_Global_EnH Register

Register Name	CH1_Global_EnH							
Bank	0			Address		0x48		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							CH1_Glob
Description	Bit[0] is used for main switch enable of Channel 1							

Field	Access	Reset	Value	Description
CH0_Glob	R/W	0	0	Disable
			1	Enable

10.6.2.3 CH2_Global_EnH Register

Register Name	CH2_Global_EnH							
Bank	0			Address		0x49		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							CH2_Glob
Description	Bit[0] is used for main switch enable of Channel 2							

Field	Access	Reset	Value	Description
CH2_Glob	R/W	0	0	Disable
			1	Enable

10.6.3 LED Frame Cycle Control

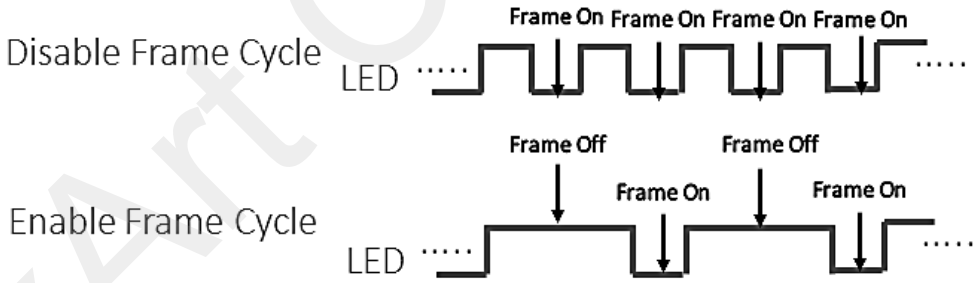

Figure 30. LED Frame Cycle Diagram

10.6.3.1 LED0_Sub_EnH Register

Register Name	LED0_Sub_EnH							
Bank	0			Address		0x4A		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED0_Sub
Description	Bit[0] is used to enable frame cycle of Channel 0							

Field	Access	Reset	Value	Description
LED0_Sub	R/W	0	0	Disable. LED0 is always On for each frame.
			1	Enable. LED0 is On and Off cycle in turn.

10.6.3.2 LED1_Sub_EnH Register

Register Name	LED1_Sub_EnH							
Bank	0			Address		0x4B		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED1_Sub
Description	Bit[0] is used to enable frame cycle of Channel 1.							

Field	Access	Reset	Value	Description
LED1_Sub	R/W	1	0	Disable. LED1 is always On for each frame.
			1	Enable. LED1 is On and Off cycle in turn.

10.6.3.3 LED2_Sub_EnH Register

Register Name	LED2_Sub_EnH							
Bank	0			Address		0x4C		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED2_Sub
Description	Bit[0] is used to enable frame cycle of Channel 2.							

Field	Access	Reset	Value	Description
LED2_Sub	R/W	1	0	Disable. LED2 is always On for each frame.
			1	Enable. LED2 is On and Off cycle in turn.

10.6.4 LED Frame Cycle Swap

10.6.4.1 LED_OnOff_Swap Register

Register Name	LED_OnOff_Swap							
Bank	0			Address		0x4D		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED_Swap
Description	Bit[0] is used to enable LED On/Off frame swapping mode. If Analog background subtraction mode in section 10.3.2 is enabled, user must set this bit to 1 manually.							

Field	Access	Reset	Value	Description
LED_Swap	R/W	0	0	Disable. On frame first then Off frame.
			1	Enable. Off frame first then On frame.

10.6.5 LED DAC AE Controls

10.6.5.1 AE_LED0_DAC Registers

Register Name	AE_LED0_DAC_Min							
Bank	0			Address		0x85		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	AE_LED0_DAC_Min[6:0]						
Description	This is the minimum bound of AE control for LED0 DAC.							

Register Name	AE_LED0_DAC_EnH							
Bank	0			Address		0x8E		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							AE_LED0_DAC
Description	Bit[0] is to enable AE control for LED0 DAC.							

Field	Access	Reset	Value	Description
AE_LED0_DAC	R/W	1	0	Disable
			1	Enable

10.6.5.2 AE_LED1_DAC Registers

Register Name	AE_LED1_DAC_Min							
Bank	0			Address		0xA7		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	AE_LED1_DAC_Min[6:0]						
Description	This is the minimum bound of AE control for LED1 DAC.							

Register Name	AE_LED1_DAC_EnH							
Bank	0			Address		0xB0		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							AE_LED1_DAC
Description	Bit[0] is to enable AE control for LED1 DAC.							

Field	Access	Reset	Value	Description
AE_LED1_DAC	R/W	1	0	Disable
			1	Enable

10.6.5.3 AE_LED2_DAC Registers

Register Name	AE_LED2_DAC_Min							
Bank	0			Address		0xC9		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	AE_LED2_DAC_Min[6:0]						
Description	This is the minimum bound of AE control for LED2 DAC.							

Register Name	AE_LED2_DAC_EnH							
Bank	0			Address		0xD2		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							AE_LED2_DAC
Description	Bit[0] is to enable AE control for LED2 DAC.							

Field	Access	Reset	Value	Description
AE_LED2_DAC	R/W	1	0	Disable
			1	Enable

10.6.5.4 LED_DAC_Change_Flag_EnH Registers

Register Name	LED_DAC_Change_Flag_EnH							
Bank	0			Address		0xE6		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved					LED2_DAC_CH_ Flag	LED1_DAC_CH_ Flag	LED0_DAC_CH_ Flag
Description	The LED DAC Change Flag for the respective LED0, LED1 and LED2 channel is set via this register.							

Field	Access	Reset	Value	Description
LED0_DAC_CH_ Flag	R/W	0	0	Disable
			1	Enable
LED1_DAC_CH_ Flag	R/W	0	0	Disable
			1	Enable
LED2_DAC_CH_ Flag	R/W	1	0	Disable
			1	Enable

10.6.6 LED DAC Controls

10.6.6.1 LED_Man_EnH Registers

Register Name	LED0_Man_EnH							
Bank	1			Address		0xB4		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED0_Man
Description	Bit[0] is to enable LED0 manual mode. This bit is active high.							

Field	Access	Reset	Value	Description
LED0_Man	R/W	0	0	Disable
			1	Enable

Register Name	LED1_Man_EnH							
Bank	1			Address		0xB5		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED1_Man
Description	Bit[0] is to enable LED1 manual mode. This bit is active high.							

Field	Access	Reset	Value	Description
LED1_Man	R/W	0	0	Disable
			1	Enable

Register Name	LED2_Man_EnH							
Bank	1			Address		0xB6		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED2_Man
Description	Bit[0] is to enable LED2 manual mode. This bit is active high.							

Field	Access	Reset	Value	Description
LED2_Man	R/W	0	0	Disable
			1	Enable

10.6.6.2 LED_DAC_EnL Registers

Register Name	LED0_DAC_EnL							
Bank	1			Address		0xB7		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED0_DAC
Description	Bit[0] is to enable AE control for LED0 DAC. This bit is active low.							

Field	Access	Reset	Value	Description
LED0_DAC	R/W	0	0	Enable
			1	Disable

Register Name	LED1_DAC_EnL							
Bank	1			Address		0xB8		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED1_DAC
Description	Bit[0] is to enable AE control for LED1 DAC. This bit is active low.							

Field	Access	Reset	Value	Description
LED1_DAC	R/W	0	0	Enable
			1	Disable

Register Name	LED2_DAC_EnL							
Bank	1			Address		0xB9		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LED2_DAC
Description	Bit[0] is to enable AE control for LED2 DAC. This bit is active low.							

Field	Access	Reset	Value	Description
LED2_DAC	R/W	0	0	Enable
			1	Disable

10.6.6.3 LED DAC Code Registers

Register Name	LED0_DAC_Code							
Bank	1			Address		0xBA		
Access	R/W			Reset Value		0x40		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	LED0_DAC_Code[6:0]						
Description	Bit[6:0] is used to adjust LED0 driving current. Drive Current = 0.7mA x LED0_DAC_Code[6:0] value. If AE_LED0_DAC_EnH = 1 (bank0), LED0_DAC_Code is at the maximum current for AE adjust. If AE_LED0_DAC_EnH = 0 (bank0), LED0_DAC drive current is set according to LED0_DAC_Code[6:0].							

Register Name	LED1_DAC_Code							
Bank	1			Address		0xBB		
Access	R/W			Reset Value		0x40		
Bit		6	5	4	3	2	1	0
Field	Reserved	LED1_DAC_Code[6:0]						
Description	Bit[6:0] is used to adjust LED1 driving current. Drive Current = 0.7mA x LED1_DAC_Code[6:0] value. If AE_LED1_DAC_EnH = 1 (bank0), LED1_DAC_Code is at the maximum drive current for AE adjust. If AE_LED1_DAC_EnH = 0 (bank0), LED1_DAC drive current is set according to LED1_DAC_Code[6:0].							

Register Name	LED2_DAC_Code							
Bank	1			Address		0xBC		
Access	R/W			Reset Value		0x40		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	LED2_DAC_Code[6:0]						
Description	Bit[6:0] is used to adjust LED2 driving current. Drive Current = 0.7mA x LED2_DAC_Code[6:0] value. If AE_LED2_DAC_EnH = 1 (bank0), LED2_DAC_Code is at the maximum current for AE adjust. If AE_LED2_DAC_EnH = 0 (bank0), LED0_DAC drive current is set according to LED2_DAC_Code[6:0].							

10.7 ADC Normalized Mode

10.7.1 Normalized_Mode_EnL Registers

Register Name	Normalized_Mode_EnL_1							
Bank	0			Address		0x50		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							Normalized

Register Name	Normalized_Mode_EnL_2							
Bank	0			Address		0x51		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							Normalized
Description	Bit[0] are used to enable ADC normalized mode.							

Field	Access	Reset	Value	Description
Normalized	R/W	0	0	Enable
			1	Disable

10.7.2 Normalized_Right_Shift Register

Register Name	Normalized_Right_Shift							
Bank	0			Address		0x56		
Access	R/W			Reset Value		0x07		
Bit	7	6	5	4	3	2	1	0
Field	Reserved			Normalized_Right_Shift[4:0]				
Description	Bit[4:0] is used to right shift ADC Normalized value when enable Normalized Mode.							

10.8 Touch Detection Controls

10.8.1 Touch_Detect_EnH Registers

Register Name	Touch_Detect_EnH							
Bank	0			Address		0x5A		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							Touch_Det
Description	Bit[0] is used to enable the Touch Detection mode.							

Field	Access	Reset	Value	Description
Touch_Det	R/W	0	0	Disable
			1	Enable

10.8.2 Touch Detection Upper Threshold Registers

Register Name	TouchDetection_Upper_TH_1							
Bank	0			Address		0x5C		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Upper_TH[7:0]							
Register Name	**TouchDetection_Upper_TH_2**							
Bank	0			Address		0x5D		
Access	R/W			Reset Value		0x02		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Upper_TH[15:8]							
Register Name	**TouchDetection_Upper_TH_3**							
Bank	0			Address		0x5E		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Upper_TH[23:16]							
Register Name	**TouchDetection_Upper_TH_4**							
Bank	0			Address		0x5F		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Upper_TH[31:24]							
Description	These are the registers to set the touch detection upper threshold. The threshold width is 32-bits. Refer to Figure 28.							

10.8.3 Touch Detection Lower Threshold Registers

Register Name	TouchDetection_Lower_TH_1							
Bank	0			Address		0x60		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Lower_TH[7:0]							
Register Name	**TouchDetection_Lower_TH_2**							
Bank	0			Address		0x61		
Access	R/W			Reset Value		0x02		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Lower_TH[15:8]							
Register Name	**TouchDetection_Lower_TH_3**							
Bank	0			Address		0x62		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Lower_TH[23:16]							
Register Name	**TouchDetection_Lower_TH_4**							
Bank	0			Address		0x63		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	TouchDetection_Lower_TH[31:24]							
Description	These are the registers to set the touch detection Lower threshold. The threshold width is 32-bits. Refer to Figure 28.							

10.8.4 Touch Detection Count Registers

10.8.4.1 Touch Detection Count Threshold Register

Register Name	TouchDetection_Count_TH							
Bank	0			Address		0x64		
Access	R/W			Reset Value		0x0A		
Bit	7	6	5	4	3	2	1	0
Field	Reserved			TouchDetection_Count_TH[4:0]				
Description	This register is the Touch Count Threshold in Touch Detection. Count value is from 0 to 30. Touch flag and INT pin will be asserted when counting number > TouchDetection_Count_TH. Counting period is one data report interval.							

10.8.4.2 No Touch Detection Count Threshold Register

Register Name	NoTouchDetection_Count_TH							
Bank	0			Address		0x65		
Access	R/W			Reset Value		0x0A		
Bit	7	6	5	4	3	2	1	0
Field	Reserved			NoTouchDetection_Count_TH[4:0]				
Description	This register is the No-touch Count Threshold in Touch Detection. Count value is from 0 to 30. Touch flag will be de-asserted when counting number >TouchDetection_Count_TH. Counting period is one data report interval.							

10.8.5 Touch Detection Interrupt Register

Register Name	INT_TouchDet_Mask							
Bank	2			Address		0x76		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							TouchDet_Mask
Description	Bit [0] is to mask touch detection interrupt.							

Field	Access	Reset	Value	Description
TouchDet_Mask	R/W	0	0	Unmask
			1	Mask

Register Name	INT_TouchDet_Clear							
Bank	2			Address		0x77		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							TouchDet_Clear
Description	A High to Low transition of TouchDet_Clear bit will clear the touch detection interrupt. 1. Set Bit[0] to 1 2. Then set Bit[0] to 0							

Field	Access	Reset	Value	Description
TouchDet_Clear	R/W	0	0	Low
			1	High

10.9 Clock/Timer Controls

10.9.1 Low Power Timer Register

Register Name	LPT_EnH							
Bank	1			Address		0xC0		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							LPT
Description	Bit[0] is to enable the 32kHz low power timer.							

Field	Access	Reset	Value	Description
LPT	R/W	1	0	Disable
			1	Enable

10.9.2 Oscillator Register

Register Name	OSC_EnL							
Bank	1			Address		0xC3		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							OSC
Description	Bit[0] is to enable the 32MHz internal oscillator.							

Field	Access	Reset	Value	Description
OSC	R/W	0	0	Enable
			1	Disable

10.10 Timing Generator Controls

10.10.1 TIMER_Gen_Enable Register

Register Name	TIMER_Gen_Enable							
Bank	1			Address		0xD5		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							TIMER_Gen
Description	Bit[0] is to enable the timing generator in the sensor.							

Field	Access	Reset	Value	Description
TIMER_Gen	R/W	0	0	Disable
			1	Enable

10.10.2 TIMER_Gen_Period Registers

Register Name	TIMER_Gen_Period_LB							
Bank	1			Address		0xD6		
Access	R/W			Reset Value		0x40		
Bit	7	6	5	4	3	2	1	0
Field	TIMER_Gen_Period[7:0]							
Register Name	**TIMER_Gen_Period_HB**							
Bank	1			Address		0xD7		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	TIMER_Gen_Period[15:8]							
Description	TIMER_Gen_Period[15:0] is 16-bit width used to report the period of timing generator. 1-bit step is 31.25µs. Period = TIMER_Gen_Period[15:0] x 31.25 µs Default setting = 0x140 = 320 Default Period = 320 x 31.25 µs = 10000 µs = 10ms Thus, Default Report Rate = 1/10ms = 100Hz							

10.11 FIFO Buffer Registers

10.11.1 Set FIFO Report Number Register

Register Name	SetFIFO_RptNum							
Bank	1			Address		0xEA		
Access	R/W			Reset Value		0x03		
Bit	7	6	5	4	3	2	1	0
Field	SetFIFO_RptNum[7:0]							
Description	SetFIFO_RptNum[7:0] sets the Number of FIFO entry valid for data ready report interrupt. SetFIFO_RptNum[7:0] = report number +1 Default value is 0x03 and report number is 2.							

10.11.2 FIFO Checksum Registers

Register Name	Readout_FIFO_Checksum_1							
Bank	2			Address		0x80		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	FIFO_Checksum [7:0]							
Register Name	**Readout_FIFO_Checksum_2**							
Bank	2			Address		0x81		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	FIFO_Checksum [15:8]							
Register Name	**Readout_FIFO_Checksum_3**							
Bank	2			Address		0x82		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	FIFO_Checksum [23:16]							
Register Name	**Readout_FIFO_Checksum_4**							
Bank	2			Address		0x83		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	FIFO_Checksum [31:24]							
Description	Checksum [31:0] contains 32-bit FIFO data_read_out. Chip hardware will automatic sum all burst data for Host (MCU) checking.							

10.11.3 FIFO Interrupts Registers

10.11.3.1 INT_SramFIFO_DR Registers

Register Name	INT_SramFIFO_DR_Mask							
Bank	2			Address		0x74		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							DR_Mask
Description	Bit [0] is to mask the data ready interrupt of SDRAM FIFO buffer							

Field	Access	Reset	Value	Description
DR_Mask	R/W	0	0	Unmask
			1	Mask

Register Name	INT_SramFIFO_DR_Clear							
Bank	2			Address		0x75		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							DR_Clear
Description	A High to Low transition of DR_Clear bit will clear the data ready interrupt of SDRAM FIFO buffer. 1. Set Bit[0] to 1 2. Then set Bit[0] to 0							

Field	Access	Reset	Value	Description
DR_Clear	R/W	0	0	Low
			1	High

10.11.3.2 INT_SramFIFO_Overflow Registers

Register Name	INT_SramFIFO_Overflow_Clear							
Bank	2			Address		0x8C		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							OVF_Clear
Description	A High to Low transition of OVF_Clear bit will clear the FIFO Overflow interrupt. 1. Set Bit[0] to 1 2. Then set Bit[0] to 0							

Field	Access	Reset	Value	Description
OVF_Clear	R/W	0	0	Low
			1	High

Register Name	INT_SramFIFO_Overflow_Mask							
Bank	2			Address		0x8D		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							OVF_Mask
Description	Bit [0] is to mask the FIFO Overflow interrupt.							
Field	**Access**	**Reset**	**Value**	**Description**				
OVF_Mask	R/W	0	0	Unmask				
			1	Mask				

10.11.3.3 INT_SdramFIFO_Underflow Registers

Register Name	INT_SramFIFO_Underflow_Clear							
Bank	2			Address		0x8E		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							UDF_Clear
Description	A High to Low transition of UDF_Clear bit will clear the FIFO Underflow interrupt. 1. Set Bit[0] to 1 2. Then set Bit[0] to 0							
Field	**Access**	**Reset**	**Value**	**Description**				
OVF_Clear	R/W	0	0	Low				
			1	High				

Register Name	INT_SramFIFO_Underflow_Mask							
Bank	2			Address		0x8F		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							UNF_Mask
Description	Bit [0] is to mask the FIFO Underflow interrupt.							
Field	**Access**	**Reset**	**Value**	**Description**				
UNF_Mask	R/W	0	0	Unmask				
			1	Mask				

10.12 Interrupt Controls

10.12.1 Interrupt Setting

10.12.1.1 Interrupt Mode Selection Register

Register Name	INT_Model_Sel							
Bank	2			Address		0x25		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved					INT_Mode_Sel [2:0]		
Description	Interrupt Mode Selection							

Field	Access	Reset	Value	Description
INT_Mode_Sel	R/W	000	010	INT Register Array
			100	Touch Flag readout
			Others	Reserved

10.12.1.2 Interrupt Direction Register

Register Name	INT_Output_EnL							
Bank	2			Address		0x29		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							INT_Out
Description	Interrupt Output Direction							

Field	Access	Reset	Value	Description
INT_Output	R/W	0	0	Output
			1	Input

10.12.1.3 Interrupt Mask All Register

Register Name	All_INT_Mask							
Bank	2			Address		0x78		
Access	R/W			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							All_Mask
Description	Bit [0] is to mask all the interrupts.							

Field	Access	Reset	Value	Description
All_Mask	R/W	0	0	Unmask
			1	Mask

10.12.1.4 Interrupt Type Register

Register Name	INT_Type							
Bank	2			Address		0x7A		
Access	R/W			Reset Value		0x01		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							INT_Type
Description	Bit [0] is to select the types of interrupt for triggering.							

Field	Access	Reset	Value	Description
INT_Type	R/W	1	0	Level Sensitive
			1	Edge (Pulse) Sensitive

10.12.1.5 Interrupt Pulse Width Register

Register Name	INT_Pulse_Width							
Bank	2			Address		0x7B		
Access	R/W			Reset Value		0x08		
Bit	7	6	5	4	3	2	1	0
Field	INT_Pulse_Width [7:0]							
Description	INT_Pulse_Width [7:0] sets the width of edge/pulse of an interrupt as triggering signal. Pulse Width = INT_Pulse_Width [7:0] x62.5ns Default = 8 x 62.5ns = 500ns = 0.5µs							

10.12.2 Interrupt Mode Status

10.12.2.1 Touch Flag Register

Register Name	Touch_Flag_readout							
Bank	2			Address		0x45		
Access	Read only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved							Touch
Description	Bit [0] reports the readout of touch flag status							

Field	Access	Reset	Value	Description
Touch	R/W	0	0	No Touch
			1	Touch

10.12.2.2 Interrupt Status Array Register

Register Name	INT_Reg_Array							
Bank	2			Address		0x73		
Access	Read only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FIFO_UND	FIFO_OVF	Touch_Det	FIFO_DR
Description	Bit[3:0] report the Interrupt Status Array status							

Field	Access	Reset	Value	Description
FIFO_UND	R	0	X	INT_SramFIFO_Underflow
FIFO_OVF	R	0	X	INT_SramFIFO_Overflow
Touch_Det	R	0	X	INT_Touch_Detection
FIFO_DR	R	0	X	INT_SramFIFO_Data_Ready

10.13 Read AE Information

10.13.1 Exposure Time Registers

Register Name	CH0_Exposure_Time_LB							
Bank	2			Address		0xA0		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CH0_Expusure_Time[7:0]							
Register Name	CH0_Exposure_Time_HB							
Bank	2			Address		0xA1		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CH0_Expusure_Time [15:8]							
Description	Read exposure time of Channel 0. CH0_Expusure_Time [7:0] are the lower 8bits and CH0_Expusure_Time [15:8] are the upper 8bits.							

Register Name	CH1_Exposure_Time_LB							
Bank	2			Address		0xA2		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CH1_Expusure_Time[7:0]							
Register Name	CH1_Exposure_Time_HB							
Bank	2			Address		0xA3		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CH1_Expusure_Time [15:8]							
Description	Read exposure time of Channel 1. CH1_Expusure_Time [7:0] are the lower 8bits and CH1_Expusure_Time [15:8] are the upper 8bits.							

Register Name	CH2_Exposure_Time_LB							
Bank	2			Address		0xA4		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CH2_Expusure_Time[7:0]							
Register Name	**CH2_Exposure_Time_HB**							
Bank	2			Address		0xA5		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	CH2_Expusure_Time [15:8]							
Description	Read exposure time of Channel 2. CH2_Expusure_Time [7:0] are the lower 8bits and CH2_Expusure_Time [15:8] are the upper 8bits.							

10.13.2 LED DAC

Register Name	LED0_DAC_Value							
Bank	2			Address		0xA6		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	LED0_DAC_Value[6:0]						
Description	Read DAC value of LED Channel 0.							

Register Name	LED1_DAC_Value							
Bank	2			Address		0xA7		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	LED1_DAC_Value[6:0]						
Description	Read DAC value of LED Channel 1.							

Register Name	LED2_DAC_Value							
Bank	2			Address		0xA8		
Access	Read Only			Reset Value		0x00		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	LED2_DAC_Value[6:0]						
Description	Read DAC value of LED Channel 2.							

11.0 Appendix

11.1 Touch Setting of 3.8Hz for INT Application

7f	01 //switch to bank1
E6	C8
E7	00
F1	00
07	01
AE	06
AF	07
BA	7C
6C	10
6D	10
7A	01
6F	10
7F	00 //switch to bank0
08	FF
09	03
5A	01
5C	58
5D	02
60	00
61	02
64	01
65	01
35	80
36	02
8C	00
8E	00
DE	00
D9	01
DD	04
3B	01
43	00
47	01
48	00
49	00
4A	01
4D	01
16	01
13	01
14	01
15	01
50	01
51	01
59	00

```
57      00
6B      00
6C      00
3E      00
0D      78
0E      00
7F      02 //switch to bank2
25      02
29      00
2d      01
4F      0C
66      01
67      01
68      01
69      01
6A      01
//6B     01
//6C     01
6D      01
6E      01
6F      01
70      01
74      01
76      00
7A      01
7B      FF
8D      01
8F      01
92      00
7F      01 //switch to bank1
A2      40
7C      01
4C      01
4F      07
3F      04
0C      05
4D      05
52      05
86      50
92      1C
98      1D
9A      42
81      01
3B      00
EA      C9
A4      50
```

A5	00
A6	52
A7	00
A8	53
A9	00
D6	FF
D7	1F
D8	01
D9	00
DA	10
DB	00
DC	16
DD	00
DE	17
DF	00
E0	FE
E1	1F

11.2 Touch Setting of 3.8Hz for Touch Flag Application

7f	01 //switch to bank1
4C	00
E6	C8
E7	00
F1	00
07	01
AE	06
AF	07
BA	7C
6C	10
6D	10
7A	01
6F	10
7F	00 //switch to bank0
08	FF
09	03
5A	01
5C	58
5D	02
60	00
61	02
64	01
65	01
35	80
36	02
84	78
8C	00
8E	00
DE	00
D9	01
DD	04
3B	01
43	00
47	01
48	00
49	00
4A	01
4D	01
16	01
13	01
14	01
15	01
50	01
51	01
59	00

```
57      00
6B      00
6C      00
3E      00
0D      78
0E      00
7F      02 //switch to bank2
25      04
29      00
2d      01
4F      0C
66      01
67      01
68      01
69      01
6A      01
//6B     01
//6C     01
6D      01
6E      01
6F      01
70      01
74      01
76      01
8D      01
8F      01
92      00
7F      01 //switch to bank1
A2      40
7C      01
4F      07
3F      04
0C      05
4D      05
52      05
86      50
92      1C
98      1D
9A      42
81      01
3B      00
EA      C9
A4      50
A5      00
A6      52
A7      00
```

A8	53
A9	00
D6	FF
D7	1F
D8	01
D9	00
DA	10
DB	00
DC	16
DD	00
DE	17
DF	00
E0	FE
E1	1F

11.3 PPG Setting of 20Hz

7f	01 //switch to bank1
E6	C8
E7	00
07	01
AE	06
AF	07
4D	00
BA	7C
BB	7C
BC	7C
BD	06
BE	06
BF	06
B1	06
B2	06
B3	06
6A	00
6B	01
6C	10
6D	10
7A	00
6F	10
7F	00 //switch to bank0
08	FF
09	03
4F	0C
E6	07
8C	00
AE	01
D0	01
8E	00
D2	01
B0	01
27	80
28	12
35	C0
36	12
37	C0
38	12
39	C0
3A	12
DE	00
D9	01
DD	04
3B	01

3C	15
3D	15
47	01
48	01
49	01
4A	01
4B	00
4C	00
4D	00
16	00
13	01
14	01
15	01
50	00
59	00
56	00
57	00
6B	01
6C	00
8F	01
B1	01
3E	02
3F	04
40	04
0D	78
0E	00
0F	F0
10	00
11	F0
12	00
6D	F0
6E	00
6F	00
70	02
71	10
72	00
77	00
78	0C
79	00
7A	08
7B	00
7C	0B
7D	00
7E	09
80	00
81	0D

82	00
83	07
85	01
90	F0
91	00
92	20
93	12
94	10
95	00
9A	00
9B	0C
9C	00
9D	08
9E	00
9F	0B
A0	00
A1	09
A2	00
A3	0D
A4	00
A5	07
A7	01
B2	F0
B3	00
B4	20
B5	12
B6	10
B7	00
BC	00
BD	0C
BE	00
BF	08
C0	00
C1	0B
C2	00
C3	09
C4	00
C5	0D
C6	00
C7	07
C9	01
7F	02 //switch to bank2
25	02
29	00
2d	01
4F	10

```
66      01
67      01
68      01
69      01
6A      01
//6B    01
//6C    01
6D      01
6E      01
70      01
7B      FF
7F      01 //switch to bank1
A2      40
7C      01
4F      07
3F      04
0C      05
4D      05
52      05
86      50
92      1C
98      1D
9A      42
81      01
3B      00
EA      C9
A4      50
A5      00
A6      52
A7      00
A8      53
A9      00
D6      40
D7      06
D8      01
D9      00
DA      11
DB      00
DC      84
DD      02
DE      85
DF      02
E0      3F
E1      06
```

11.4 PPG Setting of 20Hz Long Exposure Time

7f	01 //switch to bank1
E6	C8
E7	00
07	01
AE	06
AF	07
4D	00
BA	7C
BB	7C
BC	7C
BD	06
BE	06
BF	06
B1	06
B2	06
B3	06
6A	00
6B	01
6C	10
6D	10
7A	00
6F	10
7F	00 //switch to bank0
08	FF
09	03
4F	0C
E6	07
8C	00
AE	01
D0	01
8E	00
D2	01
B0	01
27	40
28	25
35	80
36	25
37	80
38	25
39	80
3A	25
DE	00
D9	01
DD	04
3B	01

3C	0A
3D	0A
47	01
48	01
49	01
4A	01
4B	00
4C	00
4D	00
16	00
13	01
14	01
15	01
50	00
59	00
56	00
57	00
6B	01
6C	00
8F	01
B1	01
3E	02
3F	02
40	02
0D	78
0E	00
0F	C0
10	12
11	C0
12	12
6D	F0
6E	00
6F	00
70	02
71	10
72	00
77	00
78	0C
79	00
7A	08
7B	00
7C	0B
7D	00
7E	09
80	00
81	0D

82	00
83	07
85	01
90	F0
91	00
92	00
93	25
94	10
95	00
9A	00
9B	0C
9C	00
9D	08
9E	00
9F	0B
A0	00
A1	09
A2	00
A3	0D
A4	00
A5	07
A7	01
B2	F0
B3	00
B4	00
B5	25
B6	10
B7	00
BC	00
BD	0C
BE	00
BF	08
C0	00
C1	0B
C2	00
C3	09
C4	00
C5	0D
C6	00
C7	07
C9	01
7F	02 //switch to bank2
25	02
29	00
2d	01
4F	10

```
66      01
67      01
68      01
69      01
6A      01
//6B    01
//6C    01
6D      01
6E      01
70      01
7B      FF
7F      01 //switch to bank1
A2      40
7C      01
4F      07
3F      04
0C      05
4D      05
52      05
86      50
92      1C
98      1D
9A      42
81      01
3B      00
EA      C9
A4      50
A5      00
A6      52
A7      00
A8      53
A9      00
D6      40
D7      06
D8      01
D9      00
DA      11
DB      00
DC      C4
DD      02
DE      C5
DF      02
E0      3F
E1      06
```

11.5 PPG Setting of 200Hz

7f	01//switch to bank1
E6	C8
E7	00
07	01
AE	06
AF	07
4D	00
BA	7C
BB	7C
BC	7C
BD	06
BE	06
BF	06
B1	06
B2	06
B3	06
6A	00
6B	01
6C	10
6D	10
7A	00
6F	08
7F	00//switch to bank0
08	FF
09	03
4F	0C
E6	07
8C	00
AE	01
D0	01
8E	00
D2	01
B0	01
27	60
28	0F
35	A0
36	0F
37	A0
38	0F
39	A0
3A	0F
DE	00
D9	01
DD	04
3B	01

3C	02
3D	02
43	00
44	00
45	00
47	01
48	01
49	01
4A	01
4B	00
4C	00
4D	00
16	00
13	01
14	01
15	01
50	00
59	00
56	00
57	00
6B	01
6C	00
8F	01
B1	01
3E	00
3F	00
40	00
0D	78
0E	00
0F	F0
10	00
11	F0
12	00
6D	F0
6E	00
6F	00
70	02
71	10
72	00
77	00
78	0C
79	00
7A	08
7B	00
7C	0B
7D	00

7E	09
80	00
81	0D
82	00
83	07
85	01
90	F0
91	00
92	40
93	0F
94	10
95	00
9A	00
9B	0C
9C	00
9D	08
9E	00
9F	0B
A0	00
A1	09
A2	00
A3	0D
A4	00
A5	07
A7	01
B2	F0
B3	00
B4	40
B5	0F
B6	10
B7	00
BC	00
BD	0C
BE	00
BF	08
C0	00
C1	0B
C2	00
C3	09
C4	00
C5	0D
C6	00
C7	07
C9	01
7F	02//switch to bank2
25	02

29	00
2d	01
4F	0C
66	01
67	01
68	01
69	01
6A	01
6D	01
6E	01
70	01
7B	FF
7F	01//switch to bank1
22	50
48	50
A2	40
7C	01
4F	07
3F	04
0C	05
4D	05
52	05
86	50
92	1C
98	1D
9A	42
81	01
3B	00
EA	C9
A4	50
A5	00
A6	52
A7	00
A8	53
A9	00
D6	A0
D7	00
D8	01
D9	00
DA	2C
DB	00
DC	8B
DD	00
DE	8C
DF	00
E0	9F
E1	00

11.6 Sleep Setting

```
7f      01 //switch to bank1
09      01
23      01
B4      01
B7      01
E6      C8
E7      00
F1      00
07      01
AE      06
AF      07
BA      7C
6C      10
6D      10
7A      00
6F      10
7F      00 //switch to bank0
08      FF
09      03
D6      01
5C      00
5D      05
60      00
61      03
64      05
65      05
35      80
36      02
8C      00
8E      00
DE      00
D9      01
DD      04
3B      01
47      01
48      00
49      00
4A      00
4D      00
16      00
13      01
14      01
15      01
50      01
51      01
```

```
59    00
57    00
6B    00
6C    00
3E    00
43    00
0D    78
0E    00
7F    02 //switch to bank2
17    00
18    00
1F    00
29    00
2D    01
2B    00
2C    00
31    00
4F    10
66    01
67    01
68    01
69    01
6A    01
6B    01
6C    01
6D    01
6E    01
6F    01
70    01
74    00
76    01
78    01
7A    01
7B    FF
8D    01
8F    01
92    00
7F    01 //switch to bank1
A2    40
7C    01
4C    01
4F    07
3F    04
0C    05
4D    05
52    05
```

86	50
92	1C
98	1D
9A	42
81	01
3B	00
EA	C9
A4	50
A5	00
A6	52
A7	00
A8	53
A9	00
D6	FF
D7	1F
D8	01
D9	00
DA	10
DB	00
DC	13
DD	00
DE	14
DF	00
E0	FE
E1	1F

Document Revision History

Revision Number	Date	Description
1.2	13 Mar 2015	1st Creation, Preliminary version
1.4	21 May 2015	1. Updated parameters in Section 2.0 Operating Specifications 2. Added Section 1.5 ADC Normalized Mode 3. Added Section 1.6 Power Saving Mechanism 4. Added Section 3.2 Package Marking 5. Added Section 5.0 Power States & Sequence 6. Updated Section 8.1 Auto Exposure Control (AEC) 7. Updated registers in Section 10.0 Registers 8. Added code settings in Section 11.0 Appendix
1.5	12 Jun 2015	1. Update Figure 10 Power-up and Power-off Sequence Timing Diagram 2. Modify power up time from V_{DD} 3. Modify SetFIFO_RptNum register description 4. Modify sleep setting 5. Added PPG setting of 200Hz
1.6	01 Jul 2015	1. Update Sleep setting, Touch setting and PPG setting 2. Update Package Marking 3. Update PCB Layout Design 4. Added Recommend Guideline for PCB Assembly 5. Added Package Information 6. Update Auto Exposure Control Diagram
1.7	15 Jul 2015	1. Update PPG setting of 20Hz and 200Hz
1.8	27 Aug 2015	1. Update PPG setting of 20Hz and 200Hz and Touch Setting and Sleep Setting 2. Modify IR Touch Detection current 3. Modify VBGP Capacitor value to 0.1µF 4. Modify Power Up From V_{DD} Time
1.9	02 Sep 2015	1. Modify Power Up From V_{DD} Time
2.0	15 Sep 2015	1. Update Figure 12. Carrier Tape Drawing 2. Add Section 11.4 PPG setting of 20Hz Long Exposure Time Setting 3. Modify the setting value of LED0 DAC (Bank1 0xBA) to 7C in the Appendix
2.1	08 Oct 2015	1. Update Table 1. Signal Pins Description 2. Mask bank2 0x6B and 0x6C of Touch Setting and PPG Setting of 20Hz
2.2	03 Dec 2015	1. Update HW Reset Time t_{reset} 2. Update Figure 31. Power-up and Power-off Sequence Timing Diagram