

## SRPS021A – D2920, JUNE 1986 – REVISED DECEMBER 2010

- TIBPAL20L8'**  
**C SUFFIX . . . JT OR NT PACKAGE**  
**M SUFFIX . . . JT OR W PACKAGE**

Pinout diagram for the 28-pin DIP package of the 74VHC04. The package is shown with pins numbered 1 to 24 on the left and 25 to 48 on the right. The pins are connected to various signals: VCC (pin 24), I (pin 23), O (pin 22), I/O (pin 21), I/O (pin 20), I/O (pin 19), I/O (pin 18), I/O (pin 17), I/O (pin 16), O (pin 15), I (pin 14), and I (pin 13). The GND pin is labeled 'GND'.

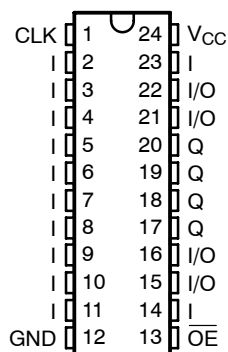
1

# TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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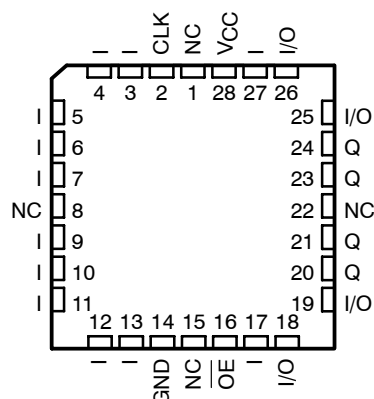
**TIBPAL20R4'**  
C SUFFIX ... JT OR NT PACKAGE  
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



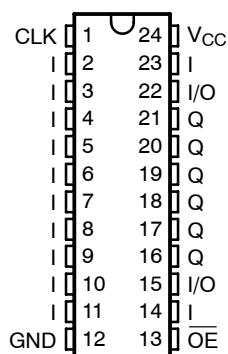
**TIBPAL20R4'**  
C SUFFIX ... FN PACKAGE  
M SUFFIX ... FK PACKAGE

(TOP VIEW)



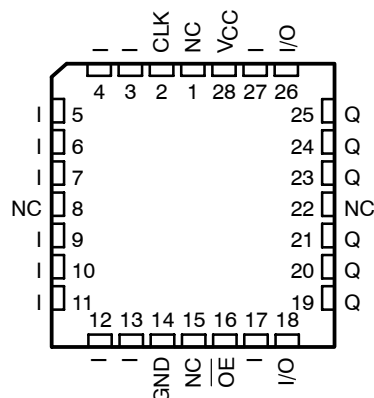
**TIBPAL20R6'**  
C SUFFIX ... JT OR NT PACKAGE  
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



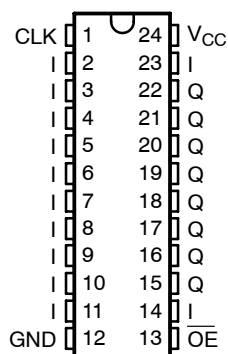
**TIBPAL20R6'**  
C SUFFIX ... FN PACKAGE  
M SUFFIX ... FK PACKAGE

(TOP VIEW)



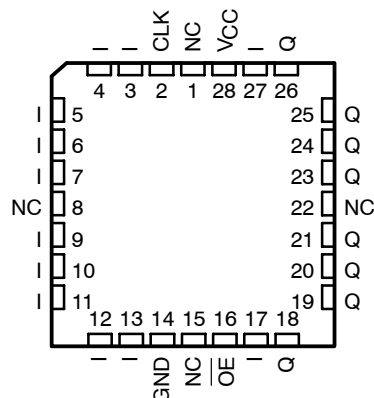
**TIBPAL20R8'**  
C SUFFIX ... JT OR NT PACKAGE  
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



**TIBPAL20R8'**  
C SUFFIX ... FN PACKAGE  
M SUFFIX ... FK PACKAGE

(TOP VIEW)



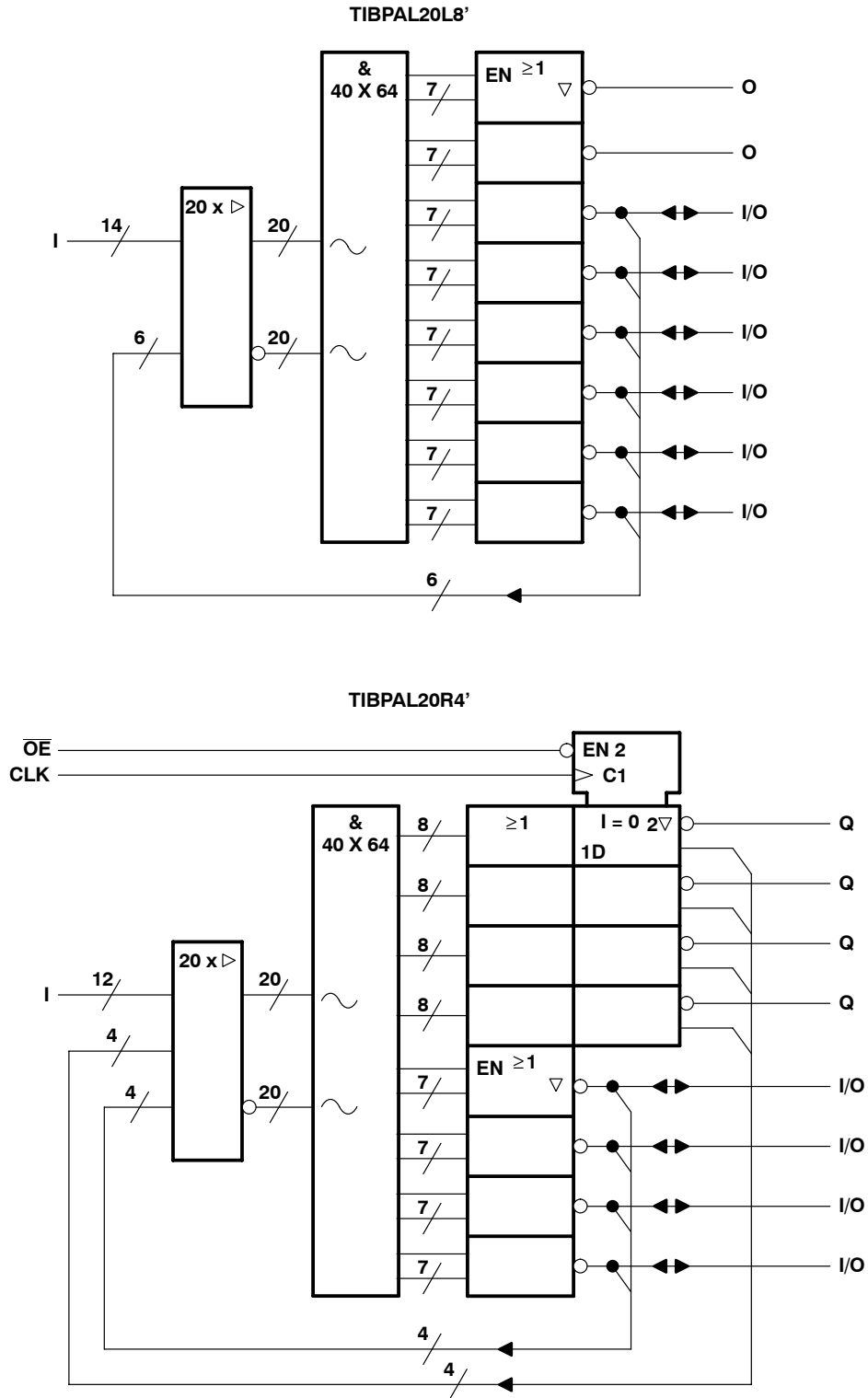
Pin assignments in operating mode

NC – No internal connection



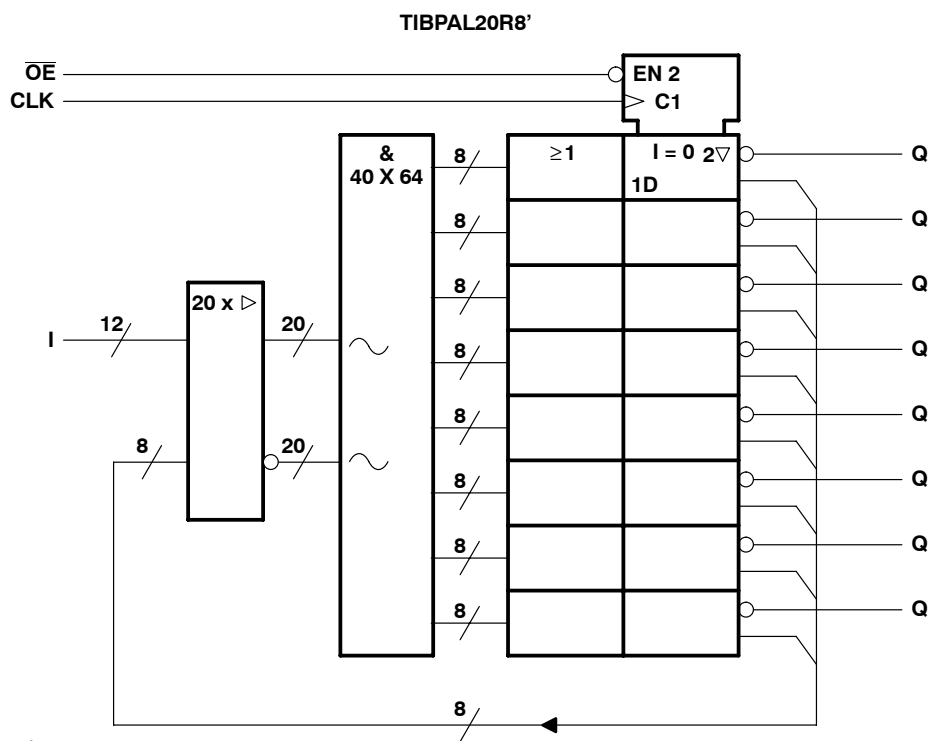
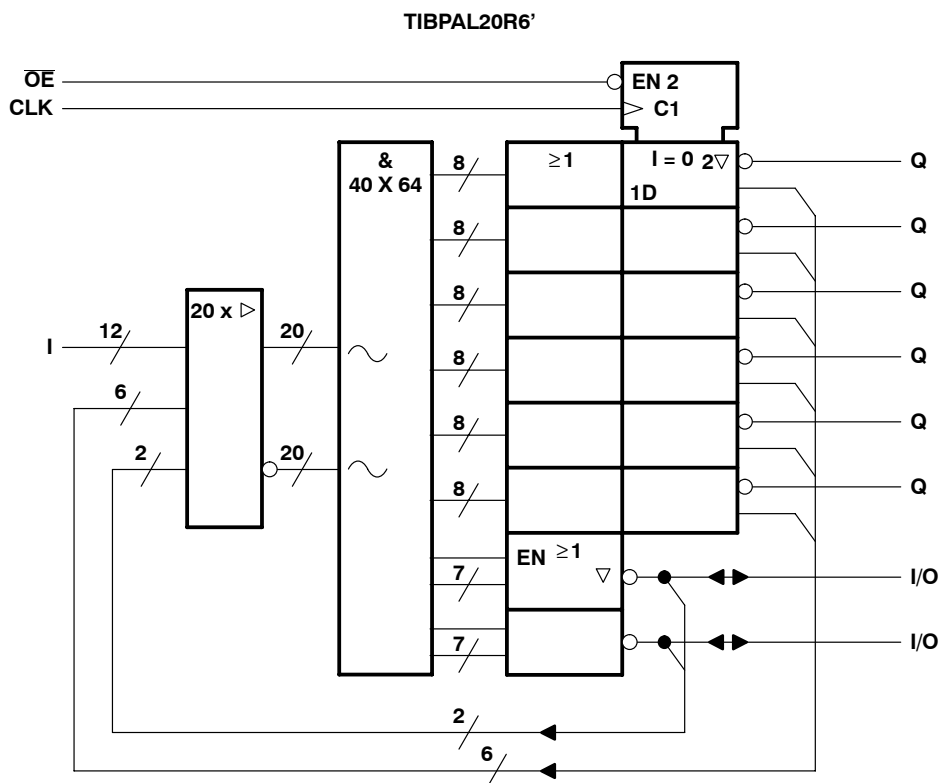
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**functional block diagrams (positive logic)**



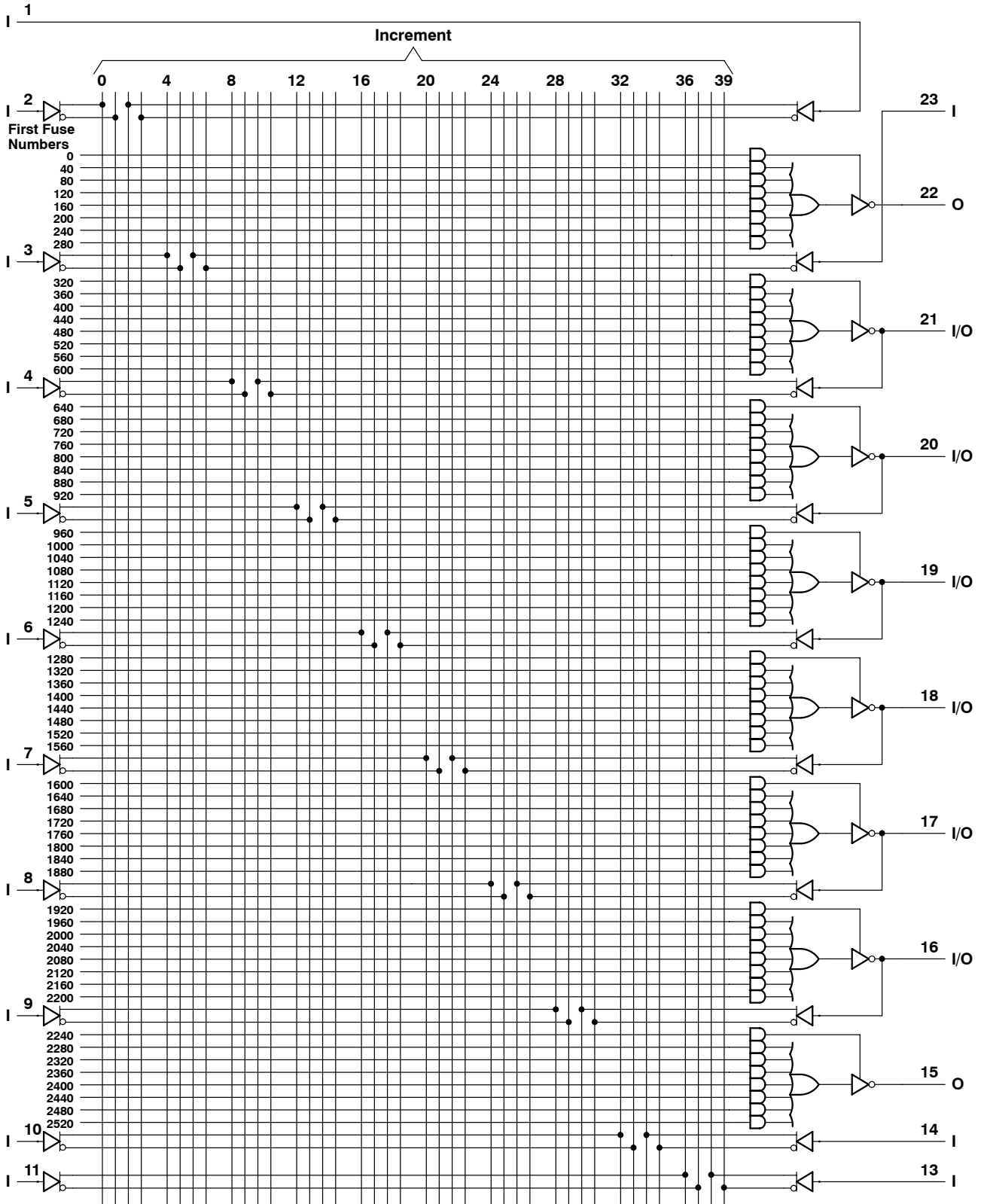
**TIBPAL20R6-15C, TIBPAL20R8-15C**  
**TIBPAL20R6-20M, TIBPAL20R8-20M**  
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**functional block diagrams (positive logic)**



~ denotes fused inputs

**logic diagram (positive logic)**

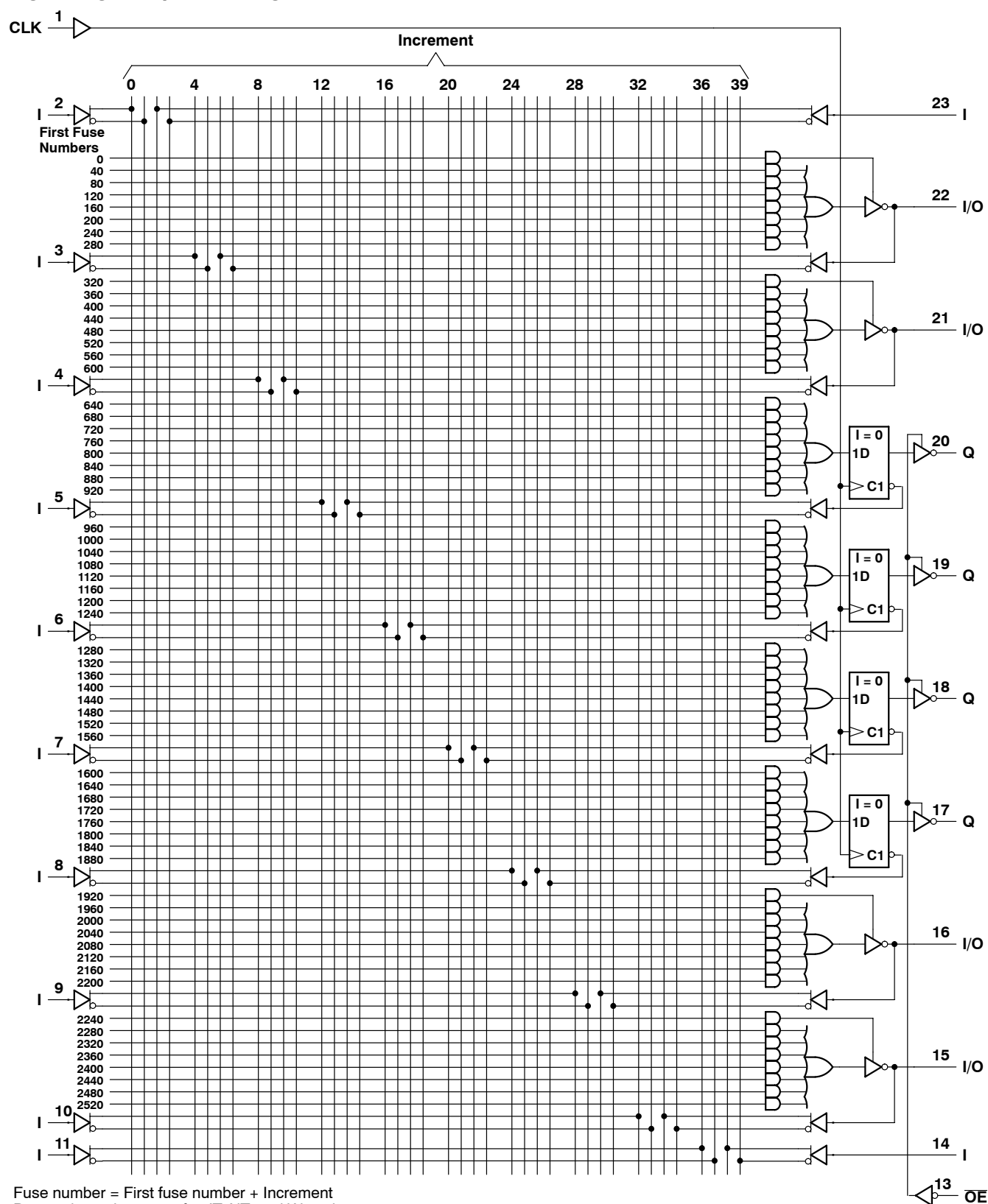


Fuse number = First fuse number + Increment  
 Pin numbers shown are for JT, NT, and W packages.

# TIBPAL20R4-15C TIBPAL20R4-20M HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

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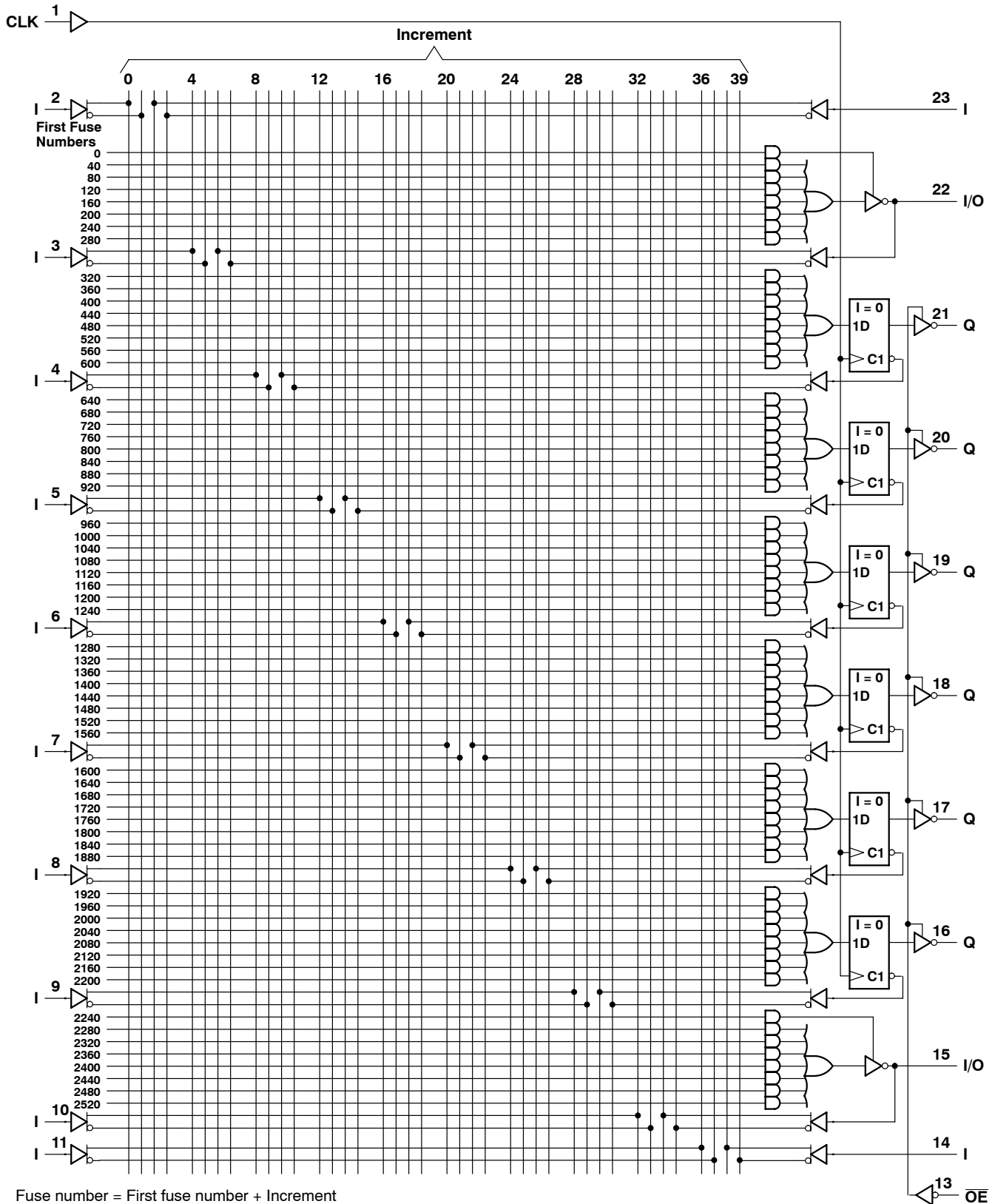
## logic diagram (positive logic)



TEXAS  
INSTRUMENTS

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**logic diagram (positive logic)**



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Diagram illustrating the 1024-bit fuse array for the 70V10 device. The array is organized into 10 columns (I=0 to I=11) and 1024 rows (First Fuse Numbers 0 to 2520). The horizontal axis is labeled "Increment" with values from 0 to 39. The vertical axis is labeled "First Fuse Numbers" with values from 0 to 2520 in increments of 40. Each intersection in the grid contains a small dot representing a fuse. To the right of the array, the output logic is shown: each column I has a 1024-to-1 multiplexer (represented by a wavy line) that selects a fuse value based on the "Increment" signal. The selected value is then passed through a 1D-to-1D decoder (labeled "I=0 1D") and a C1 counter to produce the output Q. The output lines are labeled 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, and 13 (OE).

Fuse number = First fuse number + Increment

Fuse number = First fuse number + Increment  
Pin numbers shown are for JT, NT, and W packages.



# TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage (see Note 1)                      | 5.5 V          |
| Voltage applied to disabled output (see Note 1) | 5.5 V          |
| Operating free-air temperature range            | 0°C to 75°C    |
| Storage temperature range                       | –65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

## recommended operating conditions

|                       |   | MIN  | NOM | MAX  | UNIT |
|-----------------------|---|------|-----|------|------|
| $V_{CC}$              | Supply voltage  | 4.75 | 5   | 5.25 | V    |
| $V_{IH}$              | High-level input voltage                              | 2    |     | 5.5  | V    |
| $V_{IL}$              | Low-level input voltage                               |      |     | 0.8  | V    |
| $I_{OH}$              | High-level output current                             |      |     | –3.2 | mA   |
| $I_{OL}$              | Low-level output current                              |      |     | 24   | mA   |
| $f_{clock}^{\dagger}$ | Clock frequency                                       | 0    |     | 45   | MHz  |
| $t_w^{\dagger}$       | Pulse duration, clock                                 | High |     | 10   | ns   |
|                       |   | Low  |     | 12   |      |
| $t_{su}^{\dagger}$    | Setup time, input or feedback before clock $\uparrow$ | 15   |     |      | ns   |
| $t_h^{\dagger}$       | Hold time, input or feedback after clock $\uparrow$   | 0    |     |      | ns   |
| $T_A$                 | Operating free-air temperature                        | 0    | 25  | 75   | °C   |

$^{\dagger} f_{clock}$ ,  $t_w$ ,  $t_{su}$ , and  $t_h$  do not apply for TIBPAL20L8'.



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# TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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## electrical characteristics over recommended operating free-air temperature range

| PARAMETER         |              | TEST CONDITIONS                             |  | MIN | TYP† | MAX   | UNIT          |
|-------------------|--------------|---|--|-----|------|-------|---------------|
| $V_{IK}$          |              | $V_{CC} = 4.75\text{ V}$ ,                  | $I_I = -18\text{ mA}$                      |     | -0.8 | -1.5  | V             |
| $V_{OH}$          |              | $V_{CC} = 4.75\text{ V}$ ,                  | $I_{OH} = -3.2\text{ mA}$                  | 2.4 |      |       | V             |
| $V_{OL}$          |              | $V_{CC} = 4.75\text{ V}$ ,                  | $I_{OL} = 24\text{ mA}$                    |     | 0.3  | 0.5   | V             |
| $I_{OZH}$         | O, Q outputs | $V_{CC} = 5.25\text{ V}$ ,                  | $V_O = 2.7\text{ V}$                       |     |      | 20    | $\mu\text{A}$ |
|                   | I/O ports    |   |  |     |      | 100   |               |
| $I_{OZL}$         | O, Q outputs | $V_{CC} = 5.25\text{ V}$ ,                  | $V_O = 0.4\text{ V}$                       |     |      | -20   | $\mu\text{A}$ |
|                   | I/O ports    |   |  |     |      | -250  |               |
| $I_I$             |              | $V_{CC} = 5.25\text{ V}$ ,                  | $V_I = 5.5\text{ V}$                       |     |      | 0.1   | mA            |
| $I_{IH}^\ddagger$ |              | $V_{CC} = 5.25\text{ V}$ ,                  | $V_I = 2.7\text{ V}$                       |     |      | 25    | $\mu\text{A}$ |
| $I_{IL}^\ddagger$ |              | $V_{CC} = 5.25\text{ V}$ ,                  | $V_I = 0.4\text{ V}$                       |     |      | -0.25 | mA            |
| $I_{OS}^\S$       |              | $V_{CC} = 5.25\text{ V}$ ,                  | $V_O = 0.5\text{ V}$                       | -30 | -70  | -130  | mA            |
| $I_{CC}$          |              | $V_{CC} = 5.25\text{ V}$ ,<br>Outputs open, | $V_I = 0$ ,<br>$\overline{OE}$ at $V_{IH}$ |     | 120  | 180   | mA            |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                     | FROM<br>(INPUT)  | TO<br>(OUTPUT) | TEST CONDITION                             | MIN | TYP† | MAX | UNIT |
|-------------------------------|------------------|----------------|--|-----|------|-----|------|
| f <sub>max</sub> <sup>¶</sup> | With feedback    |                | R1 = 200 Ω,<br>R2 = 390 Ω,<br>See Figure 3 | 37  | 40   |     | MHz  |
|                               | Without feedback |                |  | 45  | 50   |     |      |
| t <sub>pd</sub>               | I, I/O           | O, I/O         |  |     | 12   | 15  | ns   |
| t <sub>pd</sub>               | CLK↑             | Q              |  |     | 8    | 12  | ns   |
| t <sub>en</sub>               | OE               | Q              |  |     | 10   | 15  | ns   |
| t <sub>dis</sub>              | OE↑              | Q              |  |     | 8    | 12  | ns   |
| t <sub>en</sub>               | I, I/O           | O, I/O         |  |     | 12   | 18  | ns   |
| t <sub>dis</sub>              | I, I/O           | O, I/O         |  |     | 12   | 15  | ns   |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

$$^\P f_{\max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, \quad f_{\max}(\text{without feedback}) = \frac{1}{t_{w\text{ high}} + t_{w\text{ low}}},$$

$f_{\max}$  does not apply for TIBPAL20L8.



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# TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage (see Note 1)                      | 5.5 V          |
| Voltage applied to disabled output (see Note 1) | 5.5 V          |
| Operating free-air temperature range            | –55°C to 125°C |
| Storage temperature range                       | –65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

## recommended operating conditions

|                       |   | MIN  | NOM | MAX  | UNIT |
|-----------------------|---|------|-----|------|------|
| $V_{CC}$              | Supply voltage  | 4.5  | 5   | 5.5  | V    |
| $V_{IH}$              | High-level input voltage                              | 2    |     | 5.5  | V    |
| $V_{IL}$              | Low-level input voltage                               |      |     | 0.8  | V    |
| $I_{OH}$              | High-level output current                             |      |     | –2   | mA   |
| $I_{OL}$              | Low-level output current                              |      |     | 12   | mA   |
| $f_{clock}^{\dagger}$ | Clock frequency                                       | 0    |     | 41.6 | MHz  |
| $t_w^{\dagger}$       | Pulse duration, clock                                 | High |     | 12   | ns   |
|                       |   | Low  |     | 12   |      |
| $t_{su}^{\dagger}$    | Setup time, input or feedback before clock $\uparrow$ | 20   |     |      | ns   |
| $t_h^{\dagger}$       | Hold time, input or feedback after clock $\uparrow$   | 0    |     |      | ns   |
| $T_A$                 | Operating free-air temperature                        | –55  | 25  | 125  | °C   |

$^{\dagger} f_{clock}$ ,  $t_w$ ,  $t_{su}$ , and  $t_h$  do not apply for TIBPAL20L8'.



# TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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## electrical characteristics over recommended operating free-air temperature range

| PARAMETER          |              | TEST CONDITIONS                            |                              | MIN | TYP† | MAX   | UNIT          |
|--------------------|--------------|--|------------------------------|-----|------|-------|---------------|
| $V_{IK}$           |              | $V_{CC} = 4.5\text{ V}$ ,                  | $I_I = -18\text{ mA}$        |     | -0.8 | -1.5  | V             |
| $V_{OH}$           |              | $V_{CC} = 4.5\text{ V}$ ,                  | $I_{OH} = -2\text{ mA}$      | 2.4 | 3.2  |       | V             |
| $V_{OL}$           |              | $V_{CC} = 4.5\text{ V}$ ,                  | $I_{OL} = 12\text{ mA}$      |     | 0.3  | 0.5   | V             |
| $I_{OZH}$          |              | $V_{CC} = 5.5\text{ V}$ ,                  | $V_O = 2.7\text{ V}$         |     |      | 100   | $\mu\text{A}$ |
| $I_{OZL}^\ddagger$ | O, Q outputs | $V_{CC} = 5.5\text{ V}$ ,                  | $V_O = 0.4\text{ V}$         |     |      | -20   | $\mu\text{A}$ |
|                    | I/O ports    |  |                              |     |      | -250  |               |
| $I_I$              |              | $V_{CC} = 5.5\text{ V}$ ,                  | $V_I = 5.5\text{ V}$         |     |      | 1     | mA            |
| $I_{IH}^\ddagger$  | I/O ports    | $V_{CC} = 5.5\text{ V}$ ,                  | $V_I = 2.7\text{ V}$         |     |      | 100   | $\mu\text{A}$ |
|                    | All others   |  |                              |     |      | 25    |               |
| $I_{IL}^\ddagger$  |              | $V_{CC} = 5.5\text{ V}$ ,                  | $V_I = 0.4\text{ V}$         |     |      | -0.25 | mA            |
| $I_{OS}^\S$        |              | $V_{CC} = 5.5\text{ V}$ ,                  | $V_O = 0.5\text{ V}$         | -30 | -70  | -250  | mA            |
| $I_{CC}$           |              | $V_{CC} = 5.5\text{ V}$ ,<br>Outputs open, | $V_I = 0$ ,<br>$OE = V_{IH}$ |     | 120  | 180   | mA            |

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                     | FROM<br>(INPUT)         | TO<br>(OUTPUT) | TEST CONDITION                             | MIN  | TYP† | MAX | UNIT |
|-------------------------------|-------------------------|----------------|--|------|------|-----|------|
| f <sub>max</sub> <sup>¶</sup> | With feedback           |                | R1 = 390 Ω,<br>R2 = 750 Ω,<br>See Figure 3 | 28.5 | 40   |     | MHz  |
|                               | Without feedback        |                |  | 41.6 | 50   |     |      |
| t <sub>pd</sub>               | I, I/O                  | O, I/O         |  |      | 12   | 20  | ns   |
| t <sub>pd</sub>               | CLK↑                    | Q              |  |      | 8    | 15  | ns   |
| t <sub>en</sub>               | $\overline{OE}$         | Q              |  |      | 10   | 20  | ns   |
| t <sub>dis</sub>              | $\overline{OE}\uparrow$ | Q              |  |      | 8    | 20  | ns   |
| t <sub>en</sub>               | I, I/O                  | O, I/O         |  |      | 12   | 25  | ns   |
| t <sub>dis</sub>              | I, I/O                  | O, I/O         |  |      | 12   | 20  | ns   |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. Set  $V_O$  at 0.5 V to avoid test equipment ground degradation.

$$^\P f_{\max(\text{with feedback})} = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}, \quad f_{\max(\text{without feedback})} = \frac{1}{t_{w\text{ high}} + t_{w\text{ low}}},$$

$f_{\max}$  does not apply for TIBPAL20L8.

## programming information

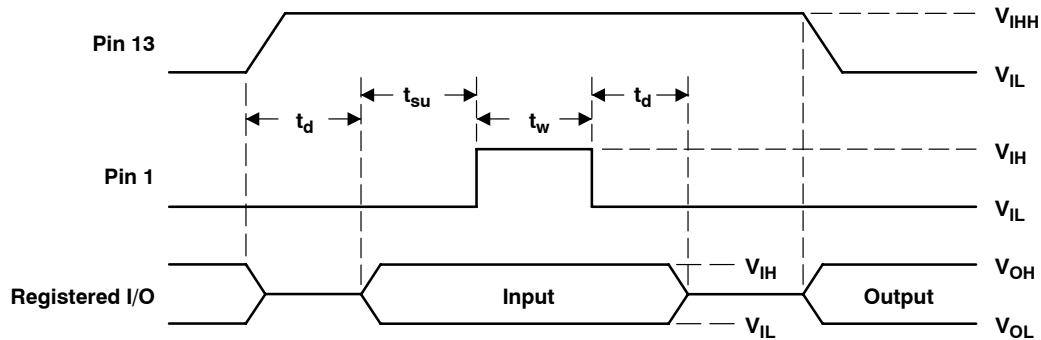
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

## preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With  $V_{CC}$  at 5 volts and Pin 1 at  $V_{IL}$ , raise Pin 13 to  $V_{IHH}$ .
- Step 2. Apply either  $V_{IL}$  or  $V_{IH}$  to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 13 to  $V_{IL}$ . Preload can be verified by observing the voltage level at the output pin.



**Figure 1. Preload Waveforms**

NOTES: 2. Pin numbers shown are for JT, NT, and W packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

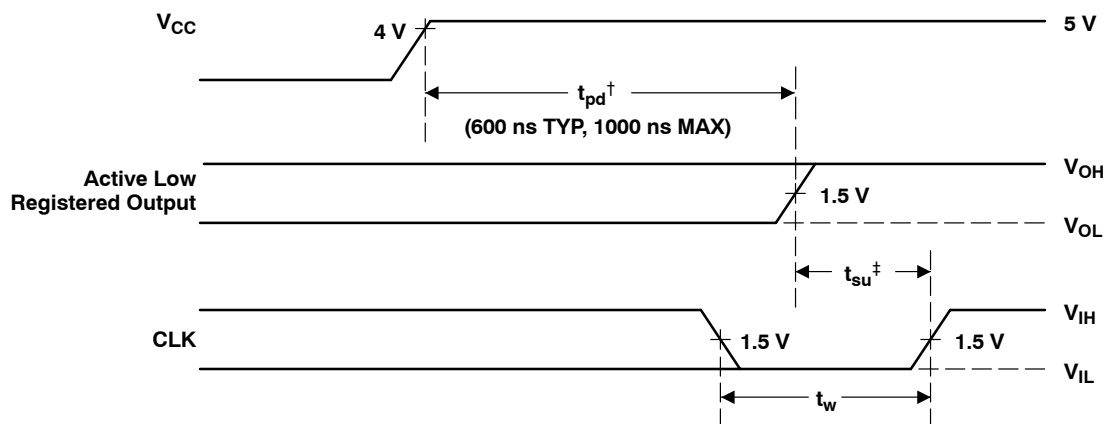
3.  $t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns}$   $V_{IHH} = 10.25 \text{ V to } 10.75 \text{ v}$

**TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C**  
**TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M**  
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**power-up reset (see Figure 2)**

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of  $V_{CC}$  be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

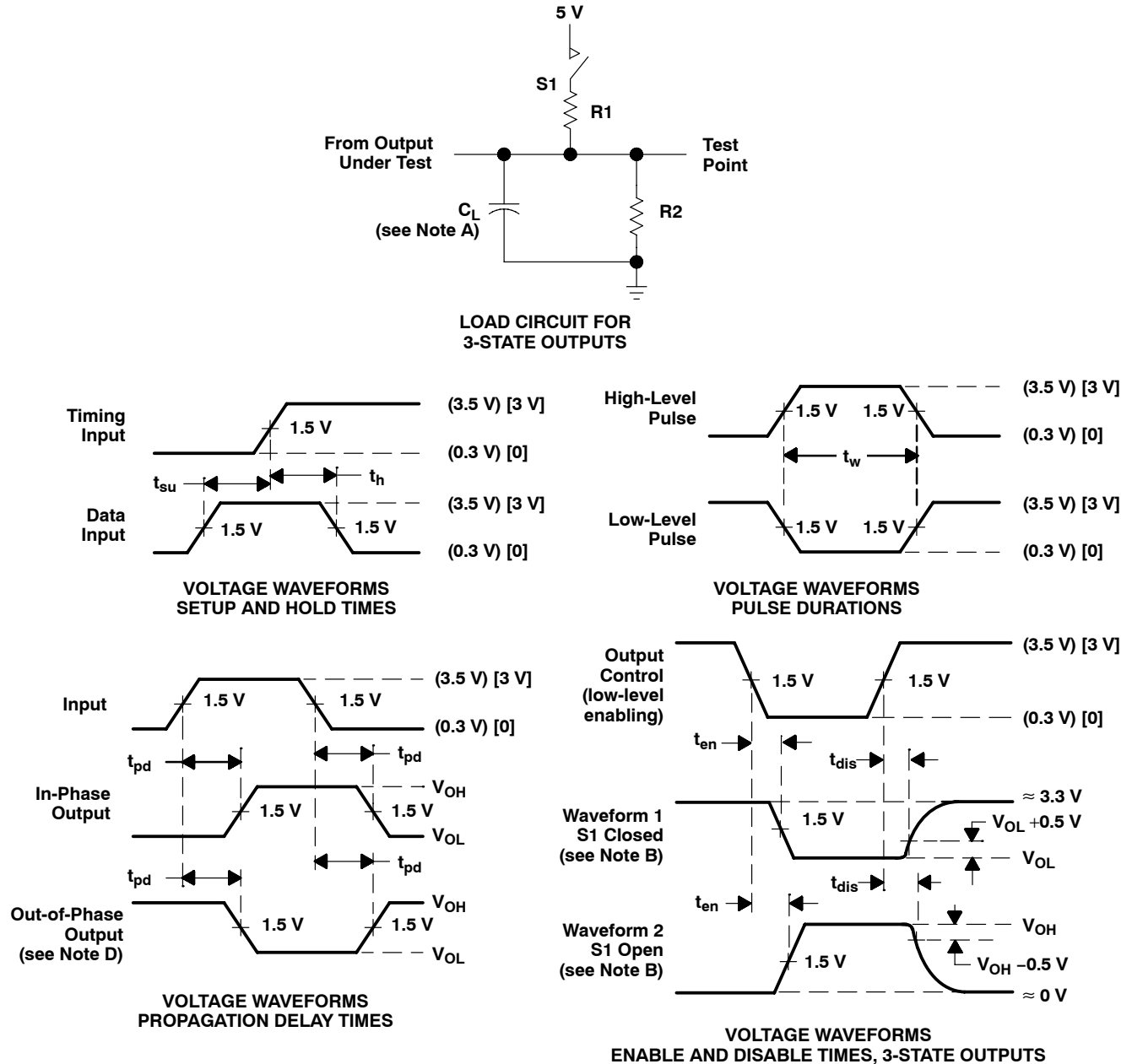


<sup>†</sup> This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

<sup>‡</sup> This is the setup time for input or feedback.

**Figure 2. Power-Up Reset Waveforms**

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR  $\leq$  1 MHz,  $t_r = t_f \leq 2$  ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR  $\leq$  10 MHz,  $t_r$  and  $t_f \leq 2$  ns, duty cycle = 50%.  
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.  
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

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D0892



**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                         |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| <a href="#">5962-87671013A</a> | Active        | Production           | LCCC (FD)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87671013A<br>TIBPAL20<br>L8-20MFDB |
| 5962-87671013A.A               | Active        | Production           | LCCC (FD)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87671013A<br>TIBPAL20<br>L8-20MFDB |
| <a href="#">5962-87671043A</a> | Active        | Production           | LCCC (FD)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87671043A<br>TIBPAL20<br>R4-20MFDB |
| 5962-87671043A.A               | Active        | Production           | LCCC (FD)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87671043A<br>TIBPAL20<br>R4-20MFDB |
| <a href="#">5962-8767104LA</a> | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8767104LA<br>TIBPAL20R4-20M<br>JTB     |
| 5962-8767104LA.A               | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8767104LA<br>TIBPAL20R4-20M<br>JTB     |
| <a href="#">8412901XA</a>      | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8412901XA<br>TIBPAL20<br>L8-20MFKB          |
| 8412901XA.A                    | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8412901XA<br>TIBPAL20<br>L8-20MFKB          |
| <a href="#">8412902LA</a>      | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8412902LA<br>TIBPAL20R8-20M<br>JTB          |
| 8412902LA.A                    | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8412902LA<br>TIBPAL20R8-20M<br>JTB          |

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                     |
|-----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| <a href="#">8412904LA</a>         | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8412904LA<br>TIBPAL20R4-20M<br>JTB      |
| 8412904LA.A                       | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8412904LA<br>TIBPAL20R4-20M<br>JTB      |
| <a href="#">JM38510/50501BLA</a>  | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50501BLA                    |
| JM38510/50501BLA.A                | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50501BLA                    |
| <a href="#">JM38510/50502BLA</a>  | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50502BLA                    |
| JM38510/50502BLA.A                | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50502BLA                    |
| <a href="#">JM38510/50504BLA</a>  | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50504BLA                    |
| JM38510/50504BLA.A                | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50504BLA                    |
| <a href="#">M38510/50501BLA</a>   | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50501BLA                    |
| <a href="#">M38510/50502BLA</a>   | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50502BLA                    |
| <a href="#">M38510/50504BLA</a>   | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>50504BLA                    |
| <a href="#">TIBPAL20R4-20MJT</a>  | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | TIBPAL20R4-20M<br>JT                    |
| TIBPAL20R4-20MJT.A                | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | TIBPAL20R4-20M<br>JT                    |
| <a href="#">TIBPAL20R4-20MJTB</a> | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8767104LA<br>TIBPAL20R4-20M<br>JTB |
| TIBPAL20R4-20MJTB.A               | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8767104LA<br>TIBPAL20R4-20M<br>JTB |

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                     |
|-----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| <a href="#">TIBPAL20R8-20MJTB</a> | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8767102LA<br>TIBPAL20R8-20M<br>JTB |
| TIBPAL20R8-20MJTB.A               | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8767102LA<br>TIBPAL20R8-20M<br>JTB |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

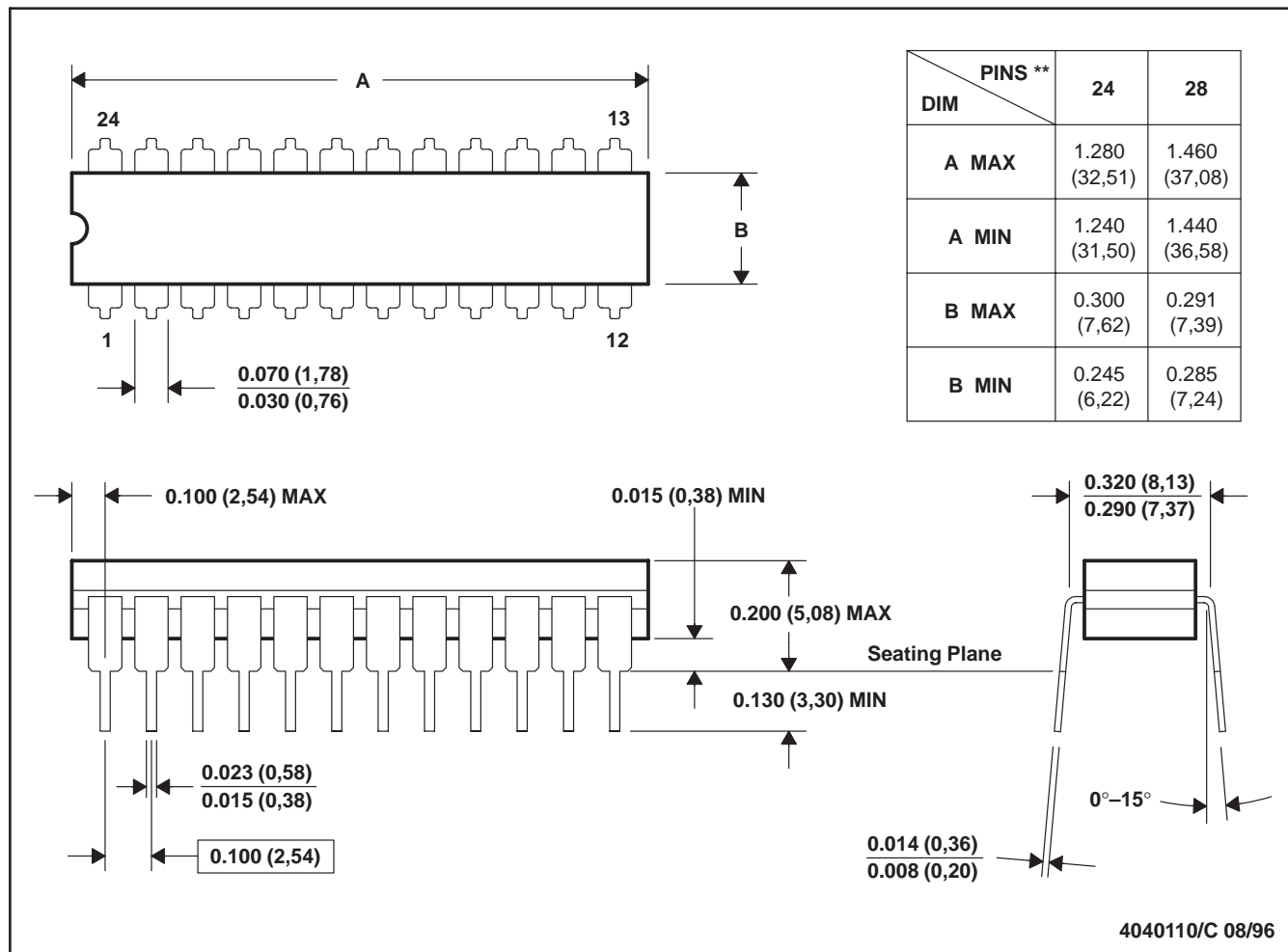
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## JT (R-GDIP-T\*\*)

## CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



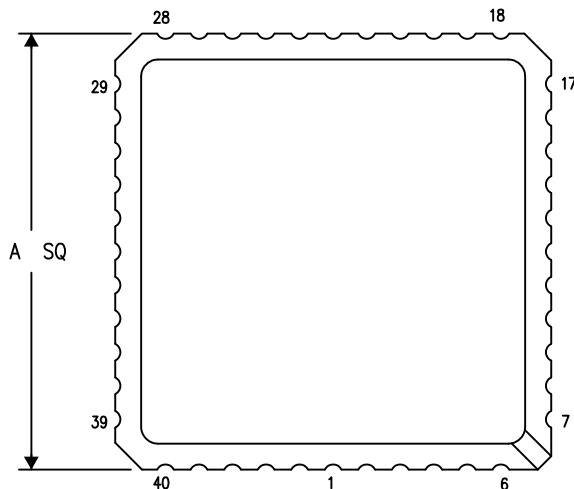
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

# MECHANICAL DATA

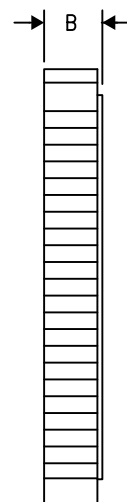
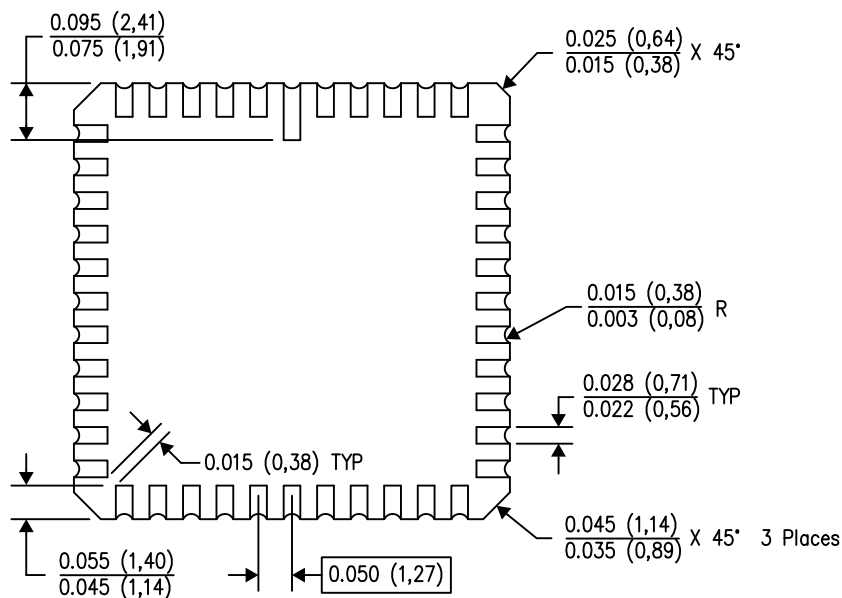
FD (S-CQCC-N\*\*)

44 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



| NO. OF<br>TERMINALS<br>** | A                |                  | B               |                 |
|---------------------------|------------------|------------------|-----------------|-----------------|
|                           | MIN              | MAX              | MIN             | MAX             |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.064<br>(1,63) | 0.080<br>(2,03) |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.064<br>(1,63) | 0.080<br>(2,03) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.069<br>(1,75) | 0.120<br>(3,05) |
| 52                        | 0.739<br>(18,78) | 0.761<br>(19,33) | 0.082<br>(2,08) | 0.120<br>(3,05) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.082<br>(2,08) | 0.120<br>(3,05) |
| 84                        | 1.135<br>(28,83) | 1.165<br>(29,59) | 0.082<br>(2,08) | 0.120<br>(3,05) |



4040136/C 08/12

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals will be gold plated.
  - E. Falls within JEDEC MS-004.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

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