Sun P4 Video

Architecture Description

Version 1.0
July 21, 1987

Sun Microsystems, Inc.
2550 Garcia Avenue
Mountain View,
California 94043
(415) 960–1300

P4 BUS SPECIFICATION

Rev 1.0 – 7/10/87

Introduction and Overview

This document provides a specification for a local expansion bus called P4. This bus provides a framework upon which universal frame buffers (with or without graphics acceleration capability) may be developed for existing and future SUN workstations. Other applications may utilize the P4 bus for connection to SUN workstations providing they adhere to the specifications provided in this document.

This specification covers the physical design, signal description, power constraints, loading characteristics, and timing for connection to this bus.

Masters and Slaves

The P4 bus defines the concept of master and slave as follows: A P4 master is defined as the host workstation where the main processor which executes the operating system resides. A P4 slave is the auxillary card which resides on top of or adjacent to the master card. See the Physical Design section for the precise physical constraints. The P4 slave may contain its own local processor(s).

Physical Design

The P4 bus supports three options for the P4 slave card sizes. One is the "standard size" P4 slave card. The width and length of this card are: 144.78 mm +-.13 mm and 195.58 mm +-.13 mm respectively (5.70 in. x 7.70 in. or 43.89 sq. in.). This standard card supports 4 BNC connectors for red, green blue, and sync and/or a 9 pin "D" connector.

The second size is the "intermediate size" P4 slave card. The width and length of this card are: 220.98 mm +-.13 mm and 195.58 mm +-.13 mm respectively (8.70 in. x 7.70 in. or 66.99 sq. in.). This intermediate card supports 4 BNC connectors for red, green, blue, and sync and/or a 9 pin "D" connector. The intermediate card allows an additional 25 pin "D" connector to be used.

The third size is the "extended" P4 slave card. This card shall have a width dimension of: 366.7 mm +.0 -.3 and a length dimension of: 195.58 mm +- .13 mm (14.44 in. x 7.70 in. or 111 sq. in.) . All dimensions are card edge to card edge. This extended card allows an additional 25 pin "D" connector to be used. All P4 compatible workstations shall support both the standard and intermediate card types. Not all P4 masters will support the extended card type.

The thickness of all board types shall be 1.6 +- .2mm thick (.063 + - .008) thick. The length and width dimensions for all three cards types are provided below. Please reference the fab drawing. (SUN part #270-1288-01) .

Introduction

This document describes the daughter card video software architecture for Sun-3 and Sun-4 systems equipped with Sun's P4 bus. Daughter card P4 video devices may range from simple monochrome or color frame buffers to high performance graphics accelerators. The organization of current P4 devices is included in the appendices.

P4 Device Space

P4 Device Space Allocation

On Sun-3 systems all P4 devices will be located within a 16 MB area of memory which is host-dependent. Each Sun-3 host CPU board will be responsible for decoding the upper 8 bits of a 32-bit physical address (leaving 24 bits = 16 MB) to indicate an access to the P4 device. The Sun 3/60 has allocated its 16 MB beginning at 0xFF000000 ('0x' indicates hex notation) in type 0 space, but the first two megabytes are occupied by its on-board frame buffer. Hence, the 3/60 actually has only 14 MB available for any P4 device.   *on board I/o*

Sun-4 systems, on the other hand, will have 32 MB of P4 device space available. The Sun-4 host must decode an access into this 32 MB space. Sun-4 systems will allocate 0xFB000000 and 0xFC000000 in type 1 device space as the P4 device space.   *on board memory*

P4 Register

Within the P4 device space there is a 32-bit read/write register which is used as the ID register, interrupt register, and enable register for the particular P4 device. Bytes 0 (D31:D24) and 1 (D23:D16) are dedicated for the ID number of the P4 device and bytes 2 (D15:D8) and 3 (D7:D0) are used for interrupt and enable information. The P4 register is located at 0x300000 within the P4 device space and may repeat within its 1 MB space, but it must be guaranteed to exist at its base. See Appendix A for a list of current P4 ID number assignments.

Port Size
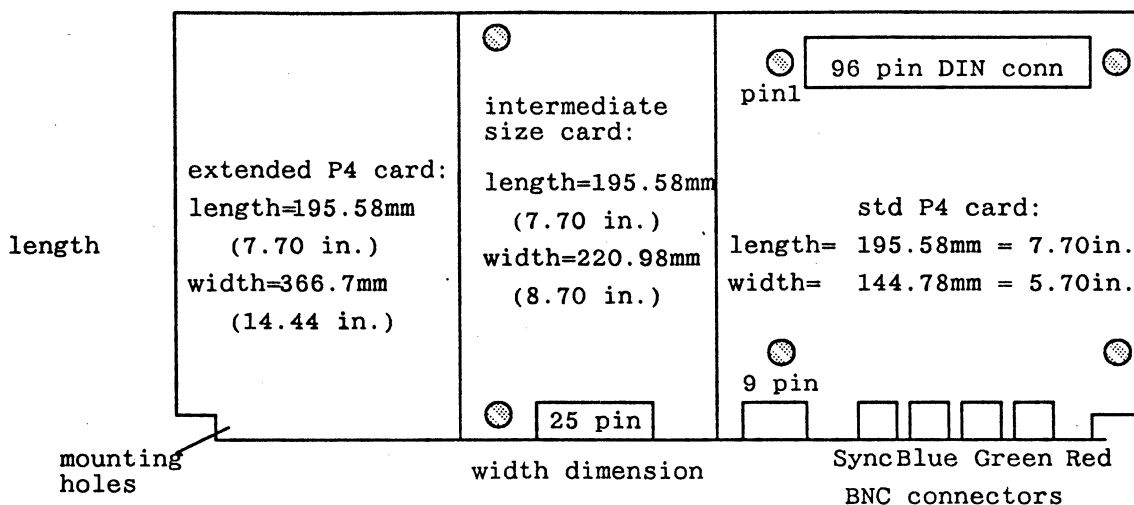
All P4 devices will have 32-bit ports only.

No P4 Device

An attempted access to a non–existing P4 device or an unused area within the P4 device space will result in a time-out. It is up to each host CPU to handle such a time-out appropriately.

Future Video Devices
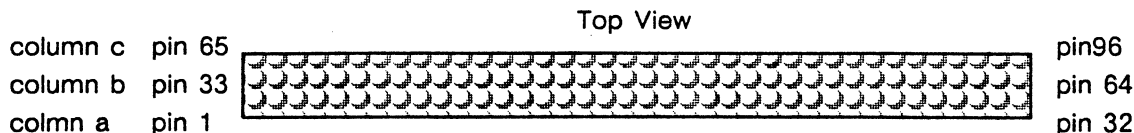
There is a broad range of future video devices which may exist within the P4 device space of Sun-3 and Sun-4 systems. It should be insured, however, that the P4 register of these future devices remains in the same location to allow the CPU host to detect it properly.

```
                    ┌─────────────────┬─────────────────┬──────────────────────────┐
                    │                 │        ◎        │  ◎  ┌──────────────┐  ◎   │
                    │                 │                 │ pin1│ 96 pin DIN conn│      │
                    │                 │  intermediate   │     └──────────────┘      │
                    │                 │  size card:     │                           │
                    │  extended P4 card:│               │                           │
                    │  length=195.58mm │ length=195.58mm│     std P4 card:          │
 length             │      (7.70 in.) │     (7.70 in.)  │  length= 195.58mm = 7.70in.│
                    │  width=366.7mm   │ width=220.98mm │  width=  144.78mm = 5.70in.│
                    │     (14.44 in.)  │    (8.70 in.)   │                           │
                    │                  │                 │        ◎            ◎     │
                    │                  │                 │     9 pin                 │
                    └───┐              │    ◎ ┌──────┐   │  ┌──┐ ┌─┐ ┌─┐ ┌─┐ ┌─┐    │
                        └──            │      │25 pin│   │  └──┘ └─┘ └─┘ └─┘ └─┘──   │
```

mounting   width dimension   SyncBlue Green Red
holes   BNC connectors

back edge of workstation
connectors to board must reside along this edge

P4 masters along with their slaves can be mounted in horizontal or vertical chassis arrangements. The height of all P4 slave cards above (adjacent to) the P4 master shall be equivalent to that specified by VMEbus specification (rev C.1). This dimension is specified by three parameters. The first is the interboard separation plane distance, 20.32 mm (.8 in.). The second is the distance from the centerline of the board (master or slave) to the interboard separation plane, 3.27mm (.129 in.). The third is the distance from the tallest component above the board to the interboard separation plane, 2.54mm (.1 in.). Please reference the VMEbus specification for further details

All signal and power connection to the P4 bus shall be made through the IEC 603–2–IEC–C096xx–xxx 96 pin DIN connector diagrammed below. This is the same connector called out for in the VMEbus specification (rev C.1). The male version of this connector resides on the slave card while the female version resides on the master card. Ground connections will be made via DIN connector pins and metallic standoffs to the mounting holes. See the attached drawing for pin assignments.

Top View

column c pin 65   pin96
column b pin 33   pin 64
colmn a   pin 1   pin 32

Signal Loading

The drive characteristics for P4 bus signals fall into 4 catagories: CLASS1, CLASS2, CLASS3 and CLASS4.

CLASS1

CLASS 1 signals are outputs from the P4 master to the P4 slave.

P4 SLAVE CHARACTERISTICS (receiver)

signals	A[0-24], SIZE, WRITE_,P4AS_,P4DS_,RESET_, OSC
Iil@Vil	-.8ma @ .4 V
Iih@Vih	80uA @ 2.4V
max load capacitance	25 pf. on P4 slave
recommended device family	ALS, FCT; MMI, AMD, TI Pals
trace length allowed on slave card	4"
max # of loads	2

CLASS2

CLASS2 signals are tri-state inputs active low to the P4 master, driven from the P4 slave. These signals must be tri-stated when inactive.   A pullup resistor is provided on the P4 master.

P4 SLAVE CHARACTERISTICS (driver)

signals	DSACK0_,DSACK1_
Iol@Vol	16 ma. @ .4V
Ioh@Voh	-400uA @ 2.4 V
max load capacitance	25 pf. on P4 slave, 120 pf. on P4 master
recommended device family	ALS, FCT; MMI, AMD, TI Pals
trace length allowed on master card	4"

CLASS 3

CLASS 3 signals are inputs to the P4 master driven from the P4 slave.
P4 SLAVE CHARACTERISTICS (driver)

signals	IBUSY_,P4INT_
Iol@Vol	1.6 ma @ .4 V
Ioh@Voh	−400 uA @ 2.4 V
max load capacitance	25 pf. P4 slave, 25 pf. P4 master
recommended device family	FCT, ALS; MMI, AMD TI (Pals)
trace length allowed on slave card	4"

CLASS 4

CLASS 4 signals are bi-directional signals with respect to the P4 master and slave.
P4 SLAVE CHARACTERISTICS (receiver)

signals	DATA D[0-31]
Iil@Vil	−.8ma @ .4V
Iih@Vih	80uA @ 2.4 V
max load capacitance	25 pf. on slave, 130 pf on master
recommended device family	ALS or FCT
trace length allowed on slave card	4"
max # of loads	2

P4 SLAVE CHARACTERISTICS (driver)

signals	DATA D[0–31]
Iol@Vol	1.6 ma @ .4 V
Ioh@Voh	–400 uA @ 2.4 V
max load capacitance	25 pf. on slave, 130 pf. on master
recommended device family	ALS or FCT
trace length allowed on master card	4"

Note that the recommended device families specified in the classes above are ones that we have experience with, to date, for the P4 interface. This does not imply that other logic families or manufacturers will not function properly in the same application. The designer should use the loading and timing characteristics as a guide for selection of alternate devices.

Signal Descriptions

DATA D[0–31]

The P4 bus supports a full 32 bit bi-directional data bus. Data bits D[0–31] are defined as CLASS 4 (see signal loading characteristics) D[0] is the least significant bit. The data bus supports byte (8 bits), word (16 bits) three byte (24 bits) or longword (32 bits) reads or writes. Byte, word, and three byte writes to any byte, word, or three byte group within a longword are permitted. The width of the current bus transaction is indicated by the SIZE 0 and SIZE1 pins. The size of the port for the current bus transaction as indicated by the DSACK0_ and DSACK1_ pins must always be 32 bits. Data must be memory aligned.

ADDRESS A[0–24]

Address bits A[0:24] are TTL compatible signals defined as CLASS 1. A[0] is the least significant bit.

OSC

This frequency of this signal is P4 master dependant and as such can be anywhere between 15–40 Mhz. OSC is a CLASS 1 signal.

IBUSY_

This signal, called interface busy, is used by the P4 master to determine when the P4 slave is available for the next bus cycle (see write cycle description). For a write to a P4 slave by the master, the slave should return DSACK0_ and 1_ as soon as possible since this will result in the minimum bus cycle for any P4 master. There are no references to the IBUSY signal on a read cycle. IBUSY may be generated by the P4 slave on a read but it will be ignored by the P4 master. IBUSY is active low, CLASS 3.

DSACK_

The two DSACK signals: DSACK0_ and DSACK1_, are used to indicate the speed of the P4 slave device. Wait states will be added by the P4 master to accomodate the speed of the P4 slave. DSACK0_ and 1_ are CLASS 2 signals (they must be tri-stated when inactive). The two DSACK lines cannot be tied together on the P4 slave device but must be driven individually to meet the timing specifications provided below. There is only one permissable DSACK encoding.

DSACK1	DSACK0	
H	H	insert wait states
L	L	port size 32 bits

SIZE

The two size signals: SIZE0 and SIZE1 are used to indicate the width of the current transaction on the data bus. SIZE0 and 1 are CLASS 1 signals.

SIZE0	SIZE1	
L	H	byte
H	L	word
H	H	three byte
L	L	longword

WRITE_

This signal is used to indicate whether the current bus transaction is a read or write. It is active along with the address. If H, then it is a read cycle, if L, then it is a write cycle. WRITE_ is a CLASS 1 signal.

P4.INT_

This signal is used by the P4 slave to interrupt the master. Assertion of this signal will create an auto-vectored interrupt. The interrupt level is not specified. The P4 slave must hold P4.INT_ active until it is serviced. This is accomplished by setting a bit in a register on the P4 slave upon P4.INT_ assertion which is then cleared during the interrupt service routine. This interrupt will typically be used by the P4 slave to tell the master when a video blanking interval is occurring, to allow new data to be written to the frame buffer or DAC at that time. P4.INT_ is a CLASS 3 signal.

P4AS_

This signal indicates the start of the P4 bus cycle. The ADDRESS, WRITE_, and SIZE signals are valid prior to this falling edge. P4AS_ will typically be used by the P4 slave to latch the address and control information. P4AS_ is a CLASS 1 signal.

P4DS_

This signal indicates that data is valid a setup time prior to its falling edge on a write. Data will be held valid as per the hold time spec.. There are no references to this signal on a read cycle. It may or may not be generated by the P4 master on a read. P4DS_ is a CLASS 1 signal.

RESET_

This signal is generated by the P4 master at powerup and is valid for a period of not less than 2usec. after the system power reaches Vcc.   It is to be used by the P4 slave to reset its own devices. RESET_ is a CLASS 1 signal.

RESERVED

There are three P4 bus pins that are reserved. These pins must not be used by either the P4 master or slave to insure compatibility across all P4 machines.
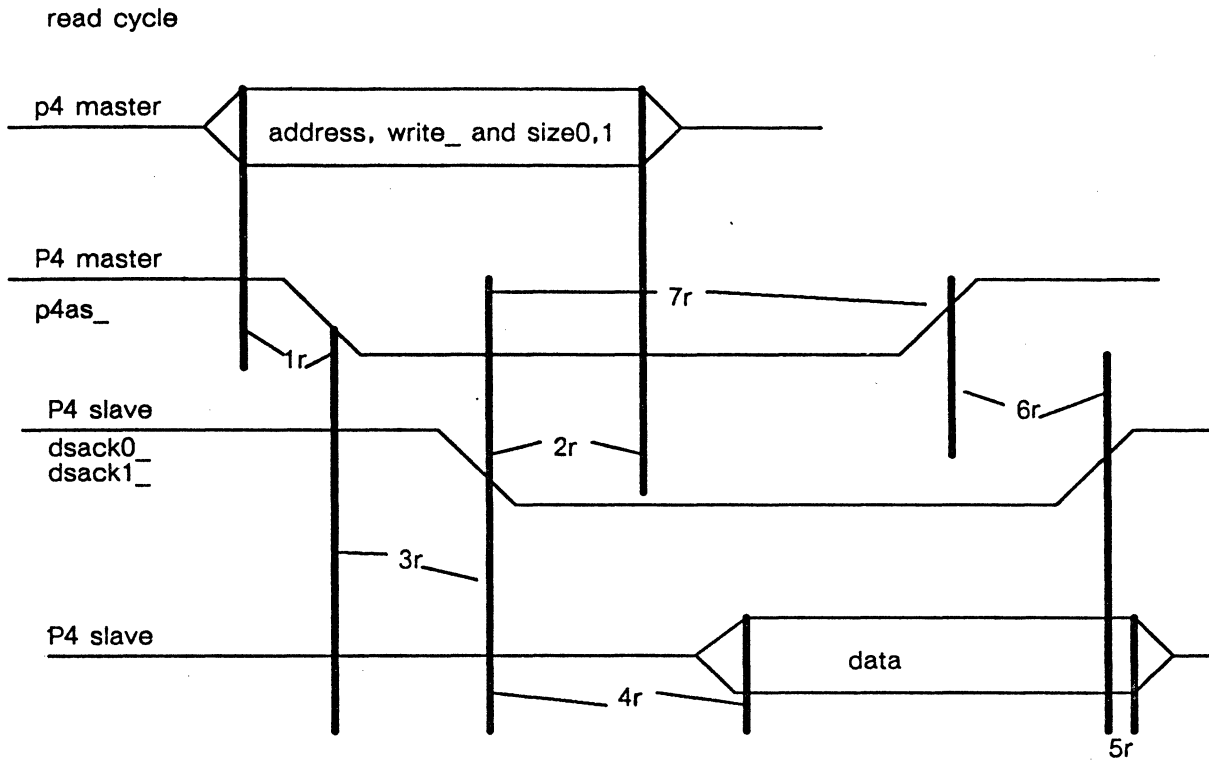
Power Supply

The power is supplied to the P4 bus through the 96 pin DIN connector.   There are 16 gnd. and 7 +5V(+ − 5%) power pins.   The −5.2V(+ − 5%) is delivered via 2 pins (maximum current 2 amps). There is no +12V or −12V on the P4 bus. Ground connections may also be made through the mounting holes on the board. Maximum current is 10 amps on the +5V. Certain processor / package configurations may not be able to supply 10 amps. at 5 volts. Consult the individual processor data sheets for power available in a given configuration.

P4 Timing Specs
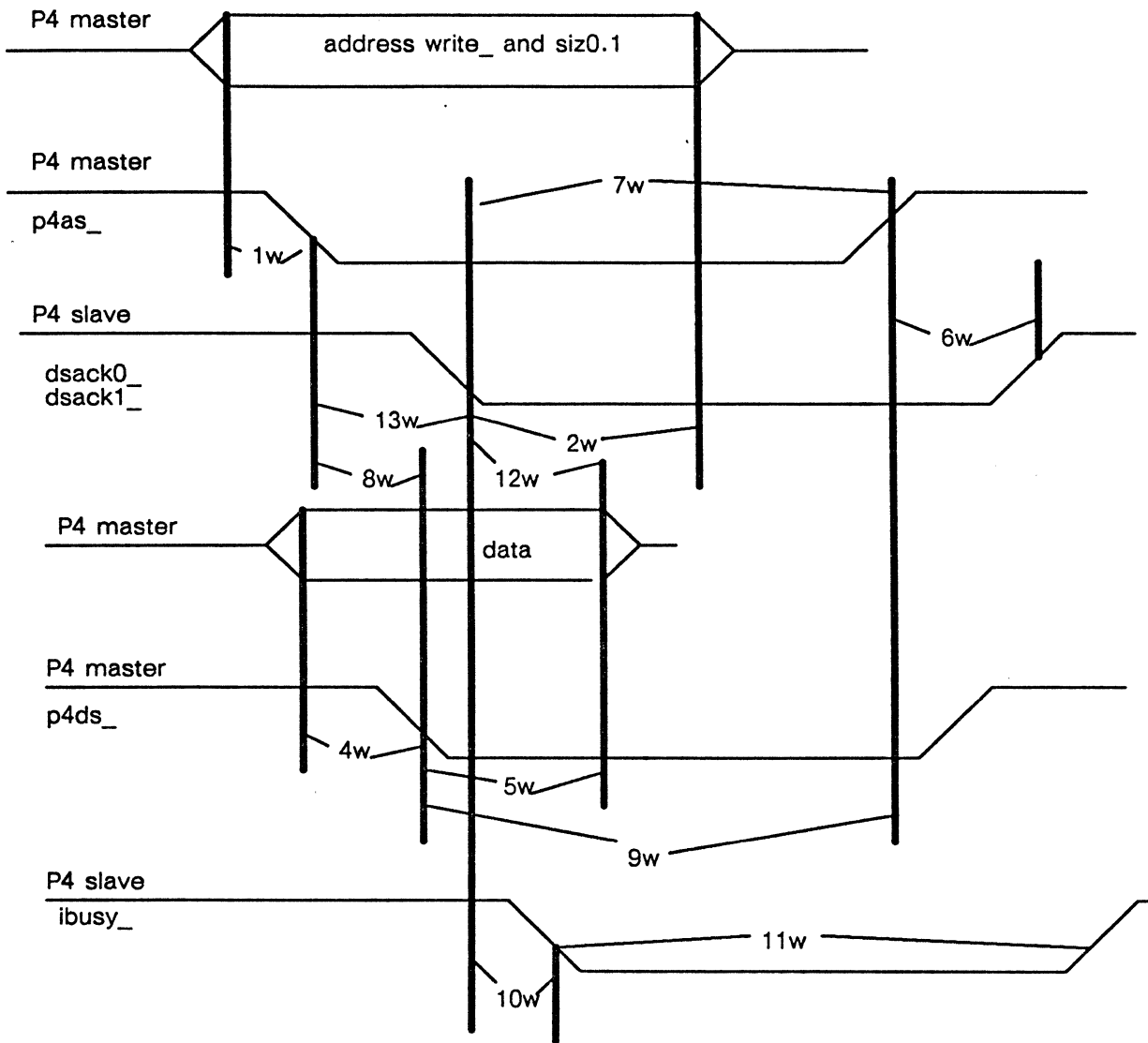
This bus is intended to provide a machine independent specification which will work across RISC and 68XXX machines of different clock cycles.   Note that the relationship between OSC and the P4 signal will not be specified.

The following set of specifications provides the set of signals and timing specifications for read and write cycles necessary for the machine independent asynchronous P4 bus. Descriptions of the cycles are provided after the diagrams.

read cycle

spec#	nsec		nsec	
1r) address setup to p4as_ active	15	min		
2r) address hold from dsack_ active	30	min		
3r) p4as_ active to dsack_ active	0	min	2 usec	max
4r) dsack_ active to data valid on read			45	max
5r) data hold from dsack_ inactive	0	min		
6r) dsack_ tristate after p4as_ inactive	0	min	15	max
7r) p4as_ hold from dsack_ active	45	min		

- 8 -
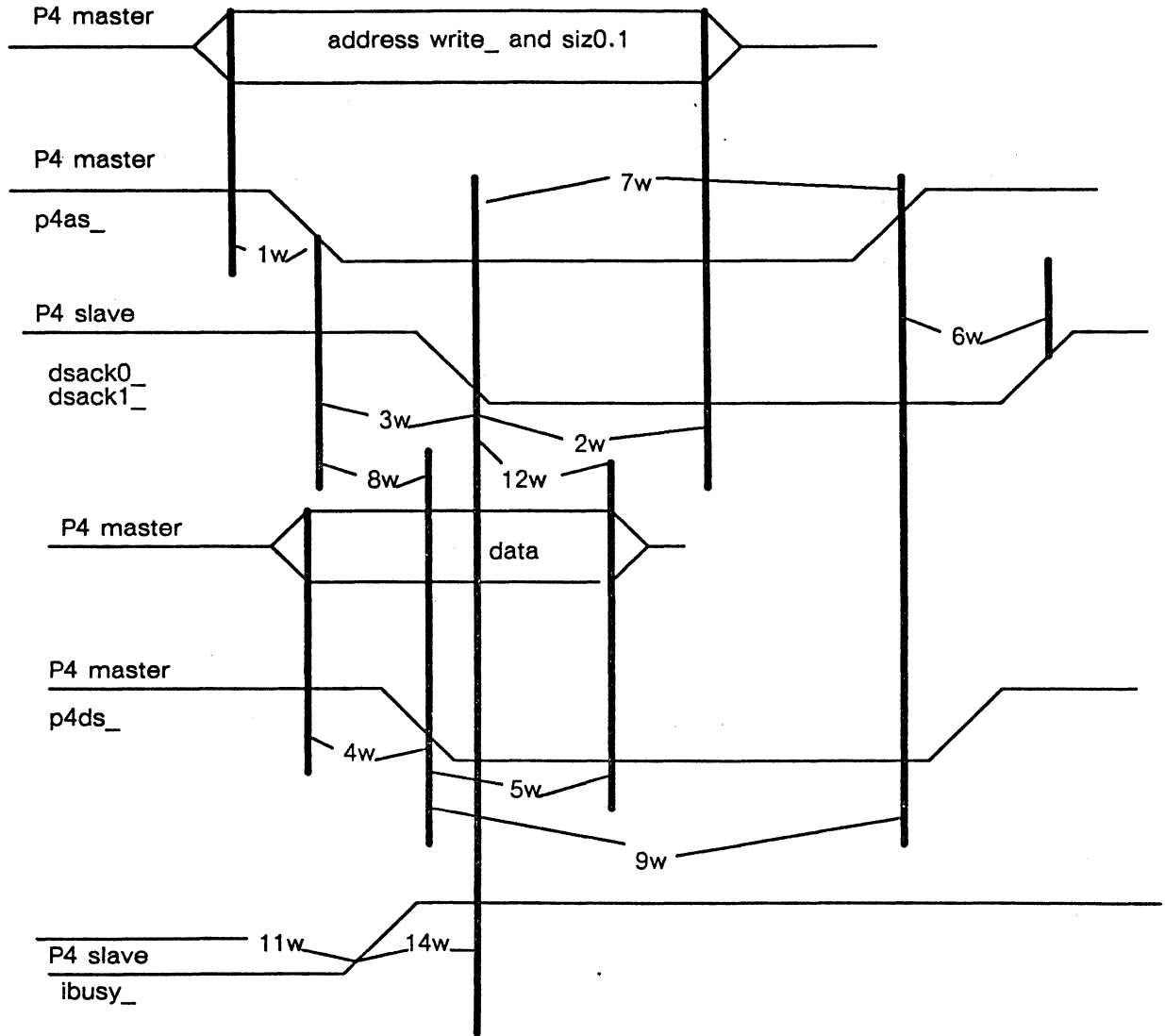
write cycle (P4 slave not busy)

P4 master

address write_ and siz0.1

P4 master

p4as_

1w

P4 slave

dsack0_
dsack1_

7w

6w

13w
2w

8w
12w

P4 master

data

P4 master

p4ds_

4w

5w

9w

P4 slave
ibusy_

11w

10w

spec#	nsec		nsec	
1w)= 1r)address setup to p4as_ active	15	min		
2w)= 2r)address hold from dsack_ active	30	min		
4w)data setup to p4ds_ active	15	min		
5w)data hold after p4ds_ active	15	min		
6w)= 6r)dsack_ tri-state after p4as_ inactive	0	min	15	max
7w)= 7r)p4as_ hold from dsack_ active	45	min		
8w)p4as_ active to p4ds_ active	0	min	75	max
9w)p4as_ hold from p4ds_ active	30	min		
10w)dsack_ active to ibusy_ active			30	max
11w)ibusy_ assertion time	0	min	2 usec max	
12w)dsack_ active to data hold	50	min		

- 9 -

13w) p4as_ active to dsack_ active   0   min   15   max

write cycle (P4 slave busy at address)

spec#		nsec		nsec	
1w)= 1r) address setup to p4as_ active		15	min		
2w)= 2r) address hold from dsack_ active		30	min		
3w)=3r) p4as_ active to dsack_ active		0	min	2usec max	
4w) data setup to p4ds_ active		15	min		
5w) data hold after p4ds_ active		15	min		
6w)= 6r) dsack_ tri-state after p4as_ inactive		0	min	15	max
7w)= 7r) p4as_ hold from dsack_ active		45	min		
8w) p4as_ active to p4ds_ active		0	min	75	max
9w) p4as_ hold from p4ds_ active		30	min		
11w) ibusy_ assertion time		0	min	2 usec max	

12w) dsack_ active to data hold	50	min
14w) ibusy_ inactive to dsack_ active	0	min

Read Cycle

On a read, the P4 master puts out the address, write and size information a minimum of spec 1r with respect to P4AS_.   The address, write, and size information will be held out by 2r past when DSACK0_ and 1_ are returned. Typically, the P4 slave will latch the address. The P4 slave then returns DSACK0 and DSACK1 (spec 3r) based upon the speed (spec 4r) of the device being accessed. For example, if the P4 slave device was a bank of 40 nsec. fast static RAM, it should return DSACKs as soon as it can after receiving P4AS_.   This is because it can return data within spec 4r (45nsec). The width of the bus cycle will vary depending upon the speed of the P4 master and slave. DSACK0_ and 1_ must be held by spec 6r past p4as- inactive. Data must be held by spec 5r past DSACK0_ and 1_ inactive.

Write Cycle

The address setup and hold times are the same for a write as a read. But on a write, a separate asynchronous signal called P4DS_ is generated to indicate when data is valid. Data is setup by spec 4w with respect to data strobe, and held by spec 5w. Typically the P4 slave will latch the address and data.   The bus cycle can then be terminated sooner than if it the P4 master had to wait until the slave was free. As before, DSACK0_ and 1_ must be held by spec 6w (= 6r) past P4AS_ inactive.

IBUSY_ must be driven active by spec 10w after p4as_ if it is not already busy from the previous cycle. It must be held until the P4 slave is ready to accept new data and address. IBUSY_ remains active for a duration of spec 11w. DSACK_ must not be issued until spec. 14w after IBUSY_ is inactive. IBUSY_ is synchronized and sampled by a SUN4 P4 master prior to the issuance of a write operation to the P4 slave. If IBUSY_ is not asserted, the P4 master will assume that DSACK0_ and 1_ will be asserted within spec. 13w of the assertion of P4AS_. If IBUSY_ is asserted when P4AS_ is asserted, the master must wait until DSACK0_ and 1_ is asserted.   IBUSY_ should also be used by the P4 slave to prevent the address and data on the second cycle of a back to back write-read or write-write from getting latched until IBUSY_ goes inactive.

There is no advantage to be gained from the P4 slave's point of view in delaying DSACK_ assertion, since in the P4 spec., data is vaild the same setup time prior to P4DS_ and held the same hold after P4DS_ regardless of when DSACK_ is asserted.   So the P4 slave can be very slow and the P4 master will go off on its way since the address and data are typically latched. Consequently, the writes to the P4 slave can be pipelined. The IBUSY_ signal is necessary since the P4 master may decide to do another read or write immediately after the current write. If so, the next bus cycle must be held off until the current cycle completes. Cycle termination is accomplished via the DSACK0_ and DSACK1_ signals.

P4
DIN CONNECTOR

1 — D[0]	33 — GND	65 — D[16]
2 — D[1]	34 — OSC	66 — D[17]
3 — D[2]	35 — GND	67 — D[18]
4 — D[3]	36 — IBUSY-	68 — D[19]
5 — D[4]	37 — GND	69 — D[20]
6 — D[5]	38 — GND	70 — D[21]
7 — D[6]	39 — GND	71 — D[22]
8 — D[7]	40 — GND	72 — D[23]
9 — D[8]	41 — GND	73 — D[24]
10 — D[9]	42 — DSACK0-	74 — D[25]
11 — D[10]	43 — DSACK1-	75 — D[26]
12 — D[11]	44 — GND	76 — D[27]
13 — D[12]	45 — VCC	77 — D[28]
14 — D[13]	46 — VCC	78 — D[29]
15 — D[14]	47 — VCC	79 — D[30]
16 — D[15]	48 — VCC	80 — D[31]
17 — GND	49 — GND	81 — GND
18 — A[0]	50 — SIZE0	82 — A[13]
19 — A[1]	51 — SIZE1	83 — A[14]
20 — A[2]	52 — WRITE-	84 — A[15]
21 — A[3]	53 — GND	85 — A[16]
22 — A[4]	54 — P4.INT-	86 — A[17]
23 — A[5]	55 — RESERVED	87 — A[18]
24 — A[6]	56 — GND	88 — A[19]
25 — A[7]	57 — P4AS-	89 — A[20]
26 — A[8]	58 — GND	90 — A[21]
27 — A[9]	59 — GND	91 — A[22]
28 — A[10]	60 — RESERVED	92 — A[23]
29 — A[11]	61 — P4DS-	93 — A[24]
30 — A[12]	62 — RESET-	94 — GND
31 — VEE	63 — VEE	95 — RESERVED
32 — VCC	64 — VCC	96 — VCC

sun microsystems

BACKPLANE

BOARD

COMPONENT

1.52 MAX

2.54   2.54
3.27   3.27
20.32   20.32

INTERBOARD SEPARATION PLANES

PRELIMINARY

366.7 +0.0 -0.3

220.98±0.13

144.78±0.13

210.03

90.18

0

160.02

96 PIN DIN CONN

195.58±0.13

EXTENDED CARD

INTERMEDIATE CARD

STANDARD CARD

3.96±0.08 DIA PLATED 6PL

0

13.97
19.05

26.42

25 PIN   9 PIN

DO NOT CONNECT
CHASSIS GND TO
SIGNAL GND

161.41

100.98
88.28
70.50
52.72
34.94
12.20
4.81

SYNC BLU GRN RED
BNC CONNECTORS

0
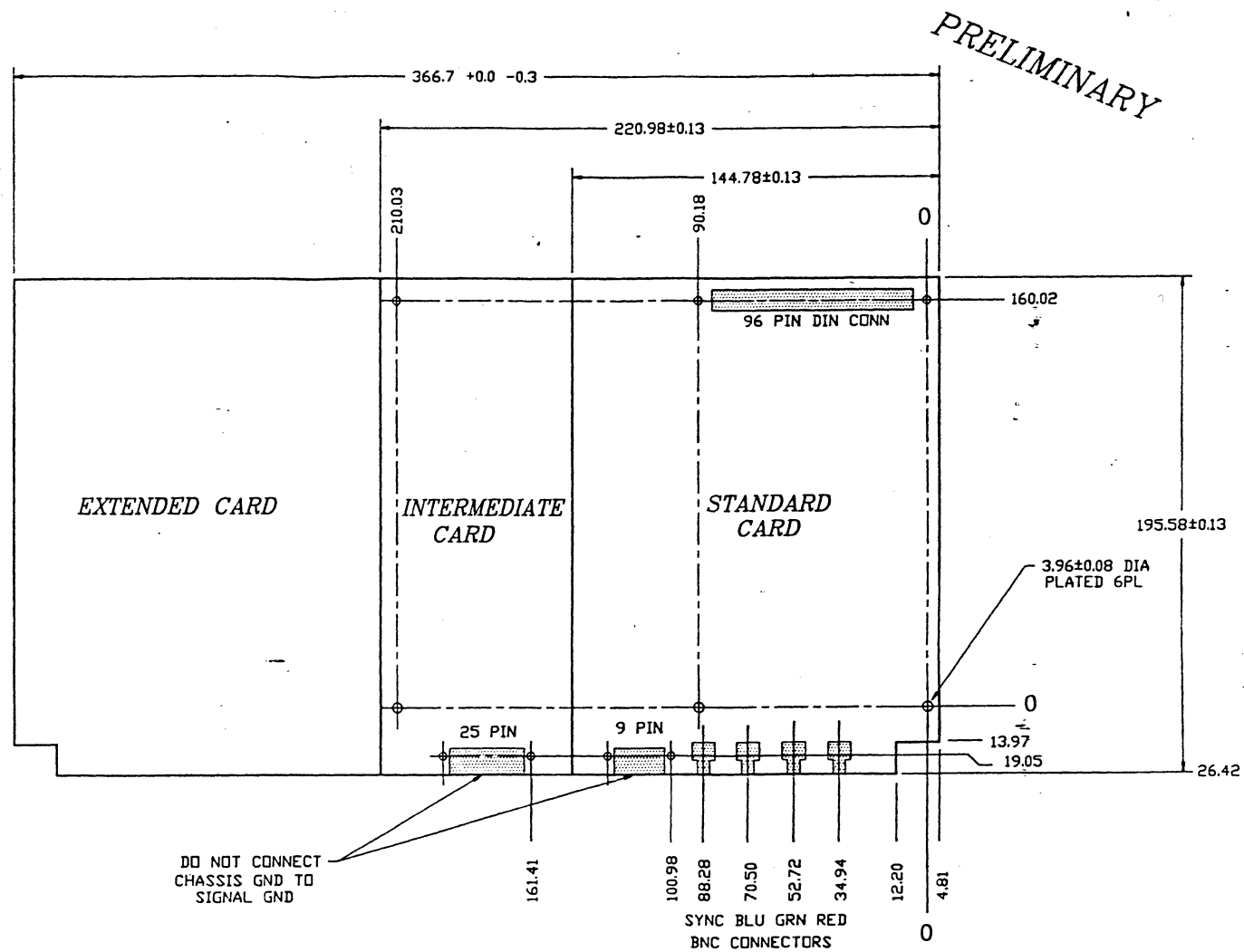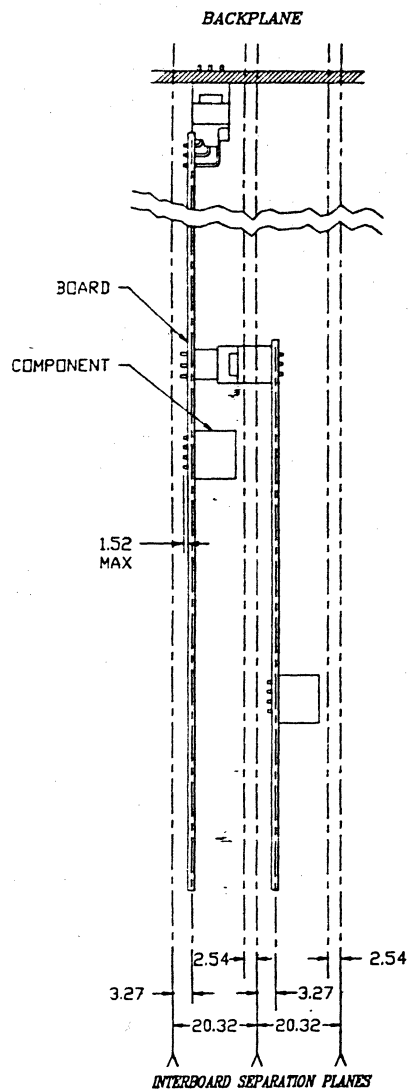
P4 SLAVE CARD
P/N 270-1288-01

Appendix A

Current P4 ID Number Assignments

Video Device Type*		ID Number
Monochrome FB (1600x1280)		0x00FF
Monochrome FB (1152x900)		0x01FF
Monochrome FB (1024x1024)		0x02FF
Monochrome FB (1280x1024)		0x03FF
Monochrome FB (1440x1440)		0x04FF
Dual Monochrome FB (640x480 x 2)		0x05FE
Monochrome FB (640x480)		0x05FF
unused		0x0600
:		:
unused		0x40FE
Color FB (1600x1280)		0x40FF
Color FB (1152x900)	(CG4)	0x41FF
Color FB (1024x1024)		0x42FF
Color FB (1280x1024)		0x43FF
Color FB (1440x1440)		0x44FF
unused		0x4500
:		:
unused		0xFFFF

*Future device IDs can be added as these devices are developed.
All new devices must obtain an unique ID from Sun Microsystems. Note that Sun does not currently offer all of the above devices, but has reserved their ID numbers.

Appendix B

Frame Buffer Type 0x00FF or 0x01FF Organization

This monochrome frame buffer begins at 0x400000 of the P4 device space and extends until 0x5FFFFF (2 MB total). It has a 32-bit interface to the CPU.

Current high-res monochrome frame buffers (1600x1280) require only 256 KB of video-RAM. Thus, there will be an additional 1.75 MB available for future higher resolution monochrome frame buffers. The following table shows the memory location of the monochrome video memory and the P4 register:

Physical Address*	Type	Meaning
0x300000	Read-Write	P4 Register
0x400000	Read-Write	Begin Monochrome
0x5FFFFF	Read-Write	End Monochrome

*In Sun-4 systems, these locations may repeat in the second 16 MB allocated for P4 devices.

P4 Register Assignment

The bytes within the 32-bit P4 register on this device are defined as follows:

Byte 0	(D31:D24)	ID number (returns 0x00 or 0x01)
Byte 1	(D23:D16)	ID number (returns 0xFF)
Byte 2	(D15:D8)	unused (returns 0xFF)
Byte 3	(D7:D0)	interrupt and enable information

Byte 3 which contains the interrupt and enable information for this frame buffer is organized as follows:

Bit 7	(D7)		unused
Bit 6	(D6)		unused
Bit 5	(D5)	video enable	enable monochrome video : writing a '1' will enable the video screen
Bit 4	(D4)		unused
Bit 3	(D3)		unused
Bit 2	(D2)	video interrupt	monochrome interrupt bit : reading

			a '1' indicates a monochrome inter-rupt has occurred. Writing a '1' will clear this interrupt.
Bit 1	(D1)	*interrupt enable*	enable interrupt bit : writing a '1' enables monochrome interrupt. Writing a '0' disables interrupts.
Bit 0	(D0)		unused

It should be noted that zeroes should be written to all unused bits of bytes 2 and 3 in the P4 register.

Data Organization of Frame Buffer Type 0x00FF or 0x01FF

The data organization for the monochrome video memory is as follows. Data bit 31 of word 0 of the frame buffer is the first visible pixel in the upper left corner of the display. Consecutive words are displayed along the horizontal scanline left to right. After <display-width> number of pixels have been displayed, the next word is displayed at the beginning of the next horizontal line, up to <display-height> number of lines. A type 0x00FF frame buffer has <display-width>=1600 and <display-height>=1280 whereas a type 0x01FF frame buffer has <display-width>=1152 and <display-height>=900. The display data polarity is such that "1" bits are black on the screen and "0" bits are white.

Monochrome Video Data Organization

```
N = <display-width> / 32
M = <display-height>

31                0 31              0 31      0 31                0
--------------------------------------------------------------------
| word 0           | word 1          |   ...  | word N-1           |
--------------------------------------------------------------------
| word N           | word N+1        |   ...  | word 2*N-1         |
--------------------------------------------------------------------
|       ...        |       ...       |  ...   |       ...          |
--------------------------------------------------------------------
| word (M-1)*N     |       ...       |  ...   | word M*N-1         |
--------------------------------------------------------------------
```

Appendix C

Frame Buffer Type 0x40FF or 0x41FF Organization

This color frame buffer is located beginning at 0x400000 of the P4 device space and extends until 0xFFFFFF (12 MB). The color frame buffer consists of 8 color planes, an enable plane, and an overlay plane. Each pixel on the screen will have 8 bits of color, 1 bit of overlay, and 1 bit of enable associated with it. All 3 planes will have a 32-bit interface to the CPU. Both the overlay and enable planes will have 2 MB allocated from the P4 device space whereas the color planes will have 8 MB allocated. Current low-res (1152x900) color frame buffers use only 128 KB for the overlay and enable planes and 1 MB for the color planes. Thus, there is additional address space in all planes to accommodate future higher resolution color frame buffers. Addressing of this color frame buffer is as follows:

Physical Address*	Type	Meaning
0x200000	Read-Write	Begin Color Map
0x2FFFFF	Read-Write	End Color Map
0x300000	Read-Write	P4 Register
0x400000	Read-Write	Begin Overlay
0x5FFFFF	Read-Write	End Overlay
0x600000	Read-Write	Begin Enable
0x7FFFFF	Read-Write	End Enable
0x800000	Read-Write	Begin Color
0xFFFFFF	Read-Write	End Color

In Sun-4 systems, these locations may repeat in the second 16 MB allocated for P4 devices.

P4 Register Assignment

The bytes within the 32-bit P4 register on this device are defined as follows:

Byte 0	(D31:D24)	ID number (returns 0x40 or 0x41)
Byte 1	(D23:D16)	ID number (returns 0xFF)
Byte 2	(D15:D8)	unused (returns 0xFF)
Byte 3	(D7:D0)	interrupt and enable information

Byte 3 which contains the interrupt and enable information for this frame buffer will be organized as follows:

Bit 7	(D7)		unused
Bit 6	(D6)		unused
Bit 5	(D5)	*video enable*	enable color video : writing a '1' will enable the video screen
Bit 4	(D4)		unused
Bit 3	(D3)		unused
Bit 2	(D2)	*video interrupt*	color interrupt bit : reading a '1' indicates a color interrupt has oc-curred. Writing a '1' will clear this interrupt.
Bit 1	(D1)	*interrupt enable*	enable interrupt bit : writing a '1' en-ables color interrupt. Writing a '0' disables interrupts.
Bit 0	(D0)		unused

It should be noted that zeroes should be written to all unused bits of bytes 2 and 3 in the P4 register.

Data Organization of Color Frame Buffer Type 0x40FF or 0x41FF

Color Video Memory

The data organization for color video memory on this device is as follows. Each byte of color video data corresponds to one display pixel. Each bit within the byte corresponds to a memory plane; eight planes are supported. By convention, bit 0 refers to plane 0, bit 1 to plane 1, etc.

The high order byte in color video memory (byte 0) maps to the first visible pixel in the upper left corner of the display. Consecutive bytes are displayed as consecutive pixels along the horizontal scanline left to right. After <display-width> number of bytes are mapped to pixels, the next byte maps to a pixel at the beginning of the next horizontal line, up to <display-height> number of lines. A type 0x40FF frame buffer has <display-width>=1600 and <display-height>=1280 whereas a type 0x41FF frame buffer has <display-width>=1152 and <display-height>=900.

Color Video Data Organization

```
N = <display-width>
M = <display-height>


7                   0 7              0 7    0 7                0
----------------------------------------------------------------
| byte 0 (pix 0)    |   byte 1       |   ... |   byte N-1       |
----------------------------------------------------------------
| byte N (pix N)    |   byte N+1     |   ... |   byte 2*N-1     |
----------------------------------------------------------------
|       ...         |      ...       |  ...  |      ...         |
----------------------------------------------------------------
| byte (M-1)*N      |      ...       |  ...  |   byte M*N-1     |
----------------------------------------------------------------
```

Overlay and Enable Video Memory

      The data organization for the overlay and enable memory is as follows. In order for the overlay data to be displayed the corresponding enable bits must be a "1". Data bit 31 of word 0 of both overlay and enable memory corresponds to the first visible pixel in the upper left corner of the display. Consecutive words of overlay data are displayed along the horizontal scanline left to right. After <display-width> number of pixels have been displayed, the next word is displayed at the beginning of the next horizontal line, up to <display-height> number of lines. A type 0x40FF frame buffer has <display-width>=1600 and <display-height>=1280 whereas a type 0x41FF frame buffer has <display-width>=1152 and <display-height>=900. The overlay data polarity is such that "1" bits are black on the screen and "0" bits are white.

Overlay and Enable Video Data Organization

N = <display-width> / 32
M = <display-height>

31 0	31 0	31 0	31 0
word 0	word 1	...	word N-1
word N	word N+1	...	word 2*N-1
...	...	...	...
word (M-1)*N	...	...	word M*N-1

Color Map Organization

In addition to all the planes needed for this color frame buffer, a color map is needed to map the bytes in the color, enable, and overlay memory into display pixels. The third megabyte of the P4 device space is reserved for this color map. The color map will reside on byte 0 (D31:D24). Current implementations of P4 device type 0x41FF use the Brooktree Bt458 RAMDAC (or compatible) which contains an on-board color palette.

Internal to the RAMDAC there is an address register, color palette RAM, overlay palette RAM, and control registers. These registers and RAM are located at the following addresses within the 1 MB space set aside for this color map:

Physical Address*	Type	Meaning
0x2XXXX0	*Read-Write*	*RAMDAC Address Register*
0x2XXXX4	*Read-Write*	*Color Palette RAM*
0x2XXXX8	*Read-Write*	*RAMDAC control registers*
0x2XXXXC	*Read-Write*	*Overlay palette RAM*

*Note how locations are allowed to repeat within this allocated megabyte.

Address Register

The internal 10-bit address register (ADDR9-0) is used for addressing color palette RAM, the overlay palette RAM, and the control registers. When reading or writing this register, D31-D24 are latched into ADDR9-2 and ADDR1,0 are reset.

Color and Overlay Palette RAM

The two least significant bits of the address register (ADDR1,0) count modulo 3 when accessing the color palette RAM or the overlay palette RAM. This RAM is addressed by ADDR9-0 as follows:

Physical Address	ADDR9-2	ADDR1	ADDR0*	Color
0x2XXXX4	0x00	0	0	red value for col palette RAM loc 0
0x2XXXX4	0x00	0	1	green value for col palette RAM loc 0
0x2XXXX4	0x00	1	1	blue value for col palette RAM loc 0
0x2XXXX4	0x01	0	0	red value for col palette RAM loc 1
0x2XXXX4	0x01	0	1	green value for col palette RAM loc 1
0x2XXXX4	0x01	1	1	blue value for col palette RAM loc 1
.	.	.	.	.
.	.	.	.	.
0x2XXXX4	0xFF	0	0	red value for col palette RAM loc 255
0x2XXXX4	0xFF	0	1	green value for col palette RAM loc 255
0x2XXXX4	0xFF	1	1	blue value for col palette RAM loc 255
0x2XXXXC	0x00	0	0	red value for overlay color 0
0x2XXXXC	0x00	0	1	green value for overlay color 0
0x2XXXXC	0x00	1	1	blue value for overlay color 0
0x2XXXXC	0x01	0	0	red value for overlay color 1
0x2XXXXC	0x01	0	1	green value for overlay color 1
0x2XXXXC	0x01	1	1	blue value for overlay color 1
.	.	.	.	.
.	.	.	.	.
0x2XXXXC	0x03	0	0	red value for overlay color 3
0x2XXXXC	0x03	0	1	green value for overlay color 3
0x2XXXXC	0x03	1	1	blue value for overlay color 3

After each blue read or write ADDR1,0 are reset and ADDR9-2 are incremented so the next RAM location can be accessed.

The enable plane data directly becomes the OL0 inputs into the RAMDAC whereas the overlay data is ANDed with the enable data prior to becoming the OL1 inputs. Thus, only the following combinations exist for overlay color selection:

	OL1 (overlay & enable)	OL0 (enable)
	0	0
	0	1
	1	1

Refer to the Bt458 specification (Appendix D) for further information on these inputs.

Control Registers

There are 4 control registers on the RAMDAC which are found at the following locations:

Physical Address	ADDR9–2	ADDR1	ADDR0**	Register
0x2XXXX8	0x04	X	X	Read Mask Register
0x2XXXX8	0x05	X	X	Blink Mask Register
0x2XXXX8	0x06	X	X	Command Register
0x2XXXX8	0x07	X	X	Test Register

**ADDR9–2 are not incremented and ADDR1,0 are ignored during accesses to any control register.*

All the registers can be read or written to at any time and are not initialized. Refer to the Bt458 specification (Appendix D) for further details on each of these registers. It should be noted, however, that bit 7 of the command register (CR7) always be set to a "0" to select 4:1 multiplexing for type 0x41FF frame buffers.

Bt458/451

Preliminary Information

This document contains information on a new product. The pinout and functional operation of the device are fully defined. The parametric information, although not fully characterized, is the result of testing initial devices.

125 MHz

Monolithic CMOS

256 x 24/12 Color Palette

RAMDAC™

Distinguishing Features

- 125 MHz Pipelined Operation
- Multiplexed TTL Pixel Ports
- Triple 8/4-bit D/A Converters
- 256 x 24/12 Dual Port Color Palette
- 4 x 24/12 Dual Port Overlay Registers
- RS-343A Compatible RGB Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- +5v CMOS Monolithic Construction
- 84-pin Ceramic PGA Package
- Typical Power Dissipation: 1600 mW

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction

Available Clock Speeds

- 125 MHz
- 100 MHz
- 75 MHz

Product Description
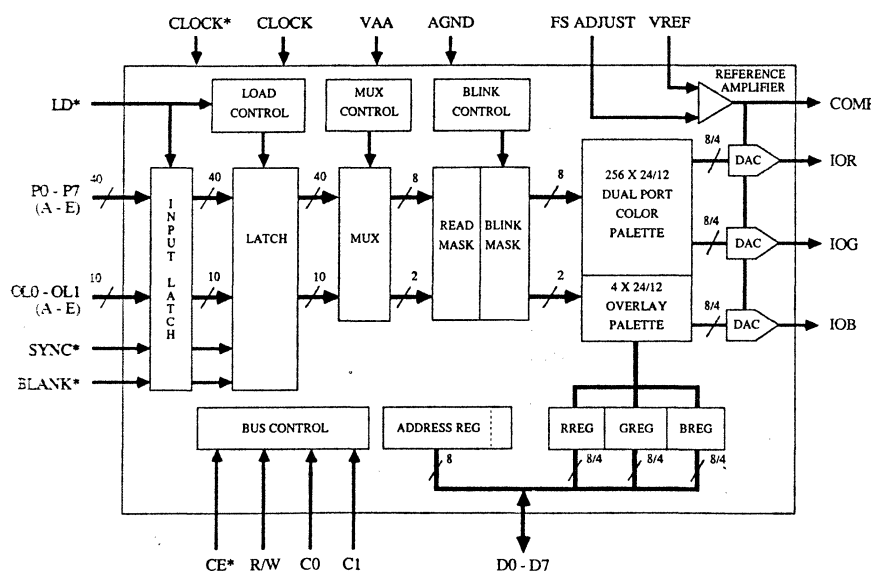
The Bt458 and Bt451 are pin-compatible and software-compatible RAMDACs designed specifically for high performance, high resolution color graphics. The architecture enables the display of 1280 x 1024 bit mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL compatible interfacing (up to 32 MHz) to the frame buffer, while maintaining the 125 MHz video data rates required for sophisticated color graphics.

The Bt458 has a 256 x 24 color lookup table with triple 8-bit video D/A converters, while the pin-compatible Bt451 contains a 256 x 12 color lookup table with triple 4-bit video D/A converters. On chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt458 supports up to 259 simultaneous colors from a 16.8 million color palette, while the Bt451 supports up to 259 simultaneous colors from a 4096 color palette. Both generate RS-343A compatible red, green, and blue video signals, and are capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering.

Implemented in CMOS for low power dissipation, the Bt458 and the Bt451 operate at frequencies up to 125 MHz, and are available in an 84-pin ceramic pin grid array package.

Functional Block Diagram

Brooktree®

Bt458/451

MPU Interface

As illustrated in the functional block diagram, the Bt458 and the Bt451 support a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 10-bit address register (ADDR) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. When reading or writing to the RAM or overlay registers, the two least significant bits (ADDR0, 1) count modulo 3, enabling the MPU to read or write red, green, and blue data. After each blue read or write cycle, the upper eight bits (ADDR2 - 9) are incremented, addressing the next RAM location or overlay register to be accessed. When addressing the internal RAM and registers, ADDR2 is the LSB. ADDR0 - 1 are used to specify color cycles, and are not accessible to the user.

When writing to the address register, D0 - D7 are latched into ADDR2 - 9 and ADDR0 - 1 are reset. When reading the address register, ADDR2 - 9 are output onto D0 - D7 and ADDR0 - 1 are reset.

As the Bt451 has only 4-bit color values, color information is input from the D4 - D7 data bus pins, with D4 being the LSB. D0 - D3 are ignored.

When writing to the RAM or overlay registers of the Bt458, color information is input from the D0 - D7 data bus pins, with D0 being the LSB. The red (R0 - R7) and green (G0 - G7) values are temporarily stored in registers, and during the blue (B0 - B7) value write cycle, all 24 bits of color information are written. R0, G0, and B0 are the LSBs of the color values.

When reading the color values, the RAM or overlay registers are accessed each time a color value is read. The address register is not incremented when accessing the control registers, facilitating read-modify-write operations. In this instance, the two least significant bits of the address register (ADDR0 - 1), which specify color cycles, are ignored. If an invalid address is loaded into the address register, data written to the device is ignored, and invalid data will be read by the MPU. During color read operations of the Bt451, color information is output onto D4 - D7, and D0 - D3 are a logical zero.

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the blue write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Table 2 is the truth table for reading and writing to the various Bt458 internal registers and palettes, while Table 3 illustrates accessing the Bt451. Figure 1 illustrates the MPU read/write timing when accessing the Bt458/451.

	Value	C1	C0	Addresses
ADDR1, 0 (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR9 - 2 (counts binary, ADDR2 is the LSB)	$00 - $FF	0	1	color palette RAM
	$00	1	1	overlay color 0
	$01	1	1	overlay color 1
	$02	1	1	overlay color 2
	$03	1	1	overlay color 3
	$04	1	0	read mask register
	$05	1	0	blink mask register
	$06	1	0	command register
	$07	1	0	test register

Table 1.   Address Register (ADDR) Operation.

Circuit Description (continued)

| R/W	C1	C0	ADDR1	ADDR0	Function
0	0	0	x	x	write address register; D0 - D7 --> ADDR2 - 9, 0 --> ADDR0 - 1
0	0	1	0	0	write red color; D0 - D7 --> RREG, increment ADDR0 - 9
0	0	1	0	1	write green color; D0 - D7 --> GREG, increment ADDR0 - 9
0	0	1	1	0	write blue color; D0 - D7 --> BREG, write color palette RAM, increment ADDR0 - 9
0	1	0	x	x	write to control register; D0 - D7 --> reg(ADDR), 0 --> ADDR0 - 1
0	1	1	0	0	write red color; D0 - D7 --> RREG, increment ADDR0 - 9
0	1	1	0	1	write green color; D0 - D7 --> GREG, increment ADDR0 - 9
0	1	1	1	0	write blue color; D0 - D7 --> BREG, write overlay register, increment ADDR0 - 9
1	0	0	x	x	read address register; ADDR2 - 9 --> D0 - D7, 0 --> ADDR0 - 1
1	0	1	0	0	read color palette red; R0 - R7 --> D0 - D7, increment ADDR0 - 9
1	0	1	0	1	read color palette green; G0 - G7 --> D0 - D7, increment ADDR0 - 9
1	0	1	1	0	read color palette blue; B0 - B7 --> D0 - D7, increment ADDR0 - 9
1	1	0	x	x	read control register; reg(ADDR) --> D0 - D7, 0 --> ADDR0 - 1
1	1	1	0	0	read overlay palette red; R0 - R7 --> D0 - D7, increment ADDR0 - 9
1	1	1	0	1	read overlay palette green; G0 - G7 --> D0 - D7, increment ADDR0 - 9
1	1	1	1	0	read overlay palette blue; B0 - B7 --> D0 - D7, increment ADDR0 - 9

Table 2. Truth Table for Bt458 Read/Write Operations.
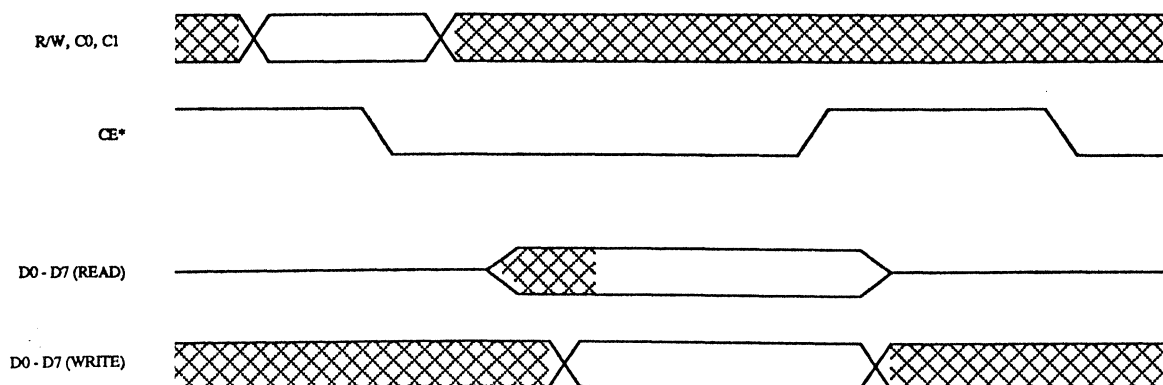
Figure 1. Host MPU Read/Write Timing.

Bt458/451

R/W	C1	C0	ADDR1	ADDR0	Function
0	0	0	x	x	write address register; D0 - D7 --> ADDR2 - 9, 0 --> ADDR0 - 1
0	0	1	0	0	write red color; D4 - D7 --> RREG, increment ADDR0 - 9
0	0	1	0	1	write green color; D4 - D7 --> GREG, increment ADDR0 - 9
0	0	1	1	0	write blue color; D4 - D7 --> BREG, write color palette RAM, increment ADDR0 - 9
0	1	0	x	x	write to control register; D0 - D7 --> reg(ADDR), 0 --> ADDR0 - 1
0	1	1	0	0	write red color; D4 - D7 --> RREG, increment ADDR0 - 9
0	1	1	0	1	write green color; D4 - D7 --> GREG, increment ADDR0 - 9
0	1	1	1	0	write blue color; D4 - D7 --> BREG, write overlay register, increment ADDR0 - 9
1	0	0	x	x	read address register; ADDR2 - 9 --> D0 - D7, 0 --> ADDR0 - 1
1	0	1	0	0	read color palette red; R0 - R3 --> D4 - D7, increment ADDR0 - 9
1	0	1	0	1	read color palette green; G0 - G3 --> D4 - D7, increment ADDR0 - 9
1	0	1	1	0	read color palette blue; B0 - B3 --> D4 - D7, increment ADDR0 - 9
1	1	0	x	x	read control register; reg(ADDR) --> D0 - D7, 0 --> ADDR0 - 1
1	1	1	0	0	read overlay palette red; R0 - R3 --> D4 - D7, increment ADDR0 - 9
1	1	1	0	1	read overlay palette green; G0 - G3 --> D4 - D7, increment ADDR0 - 9
1	1	1	1	0	read overlay palette blue; B0 - B3 --> D4 - D7, increment ADDR0 - 9

Table 3.   Truth Table for Bt451 Read/Write Operations.

Appendix D

Bt458/451

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at reasonable data rates (up to 32 MHz), the Bt458/451 incorporate internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either four or five consecutive pixels, are latched into the device via the 40 pixel select inputs (P0 - P7 {A - E}), the 10 overlay control inputs (OL0 - OL1 {A - E}), and the SYNC* and BLANK* inputs. Note that with this configuration, the sync and blank timing will be recognized only with four or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

On each CLOCK cycle, the Bt458/451 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

Internal Multiplexing

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing the CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of CLOCK phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than four, CLOCK cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the CLOCK rate (up to 125 MHz).

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four CLOCK cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five CLOCK cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.
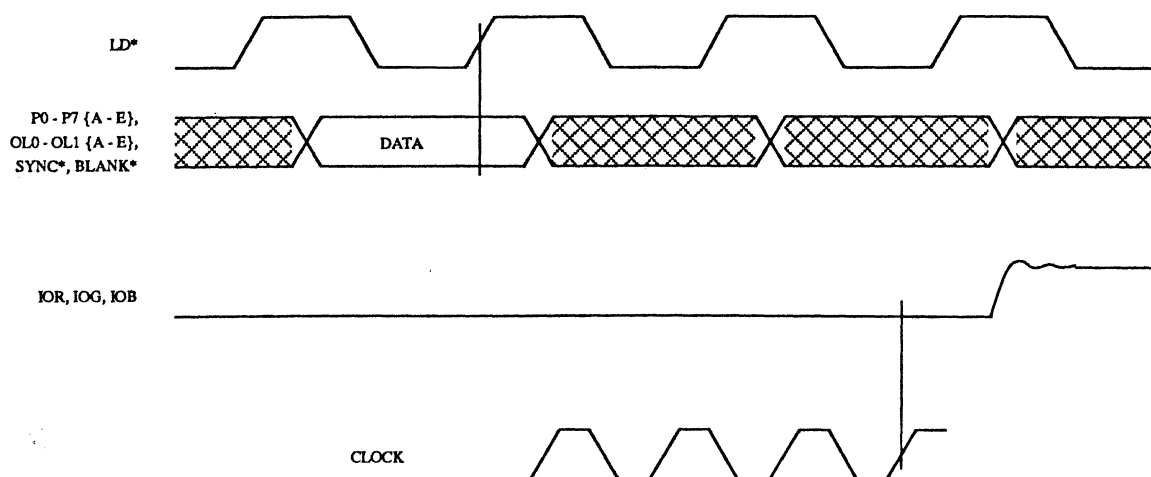

Figure 2. Video Input/Output Timing.

- 5 -

Circuit Description (continued)

Color Selection

On the rising edge of each CLOCK cycle, eight bits of color information (P0 - P7) and two bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e. in the middle of the screen), the Bt458/451 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 4 illustrates the truth table used for color selection.

Video Generation

On every CLOCK cycle, the selected 24 bits (Bt458) or 12 bits (Bt451) of color information (8 or 4 bits each of red, green, and blue) are presented to the three 8-bit or 4-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3 for doubly-terminated 75-ohms loads, and Figure 4 for singly-terminated 75-ohm loads.
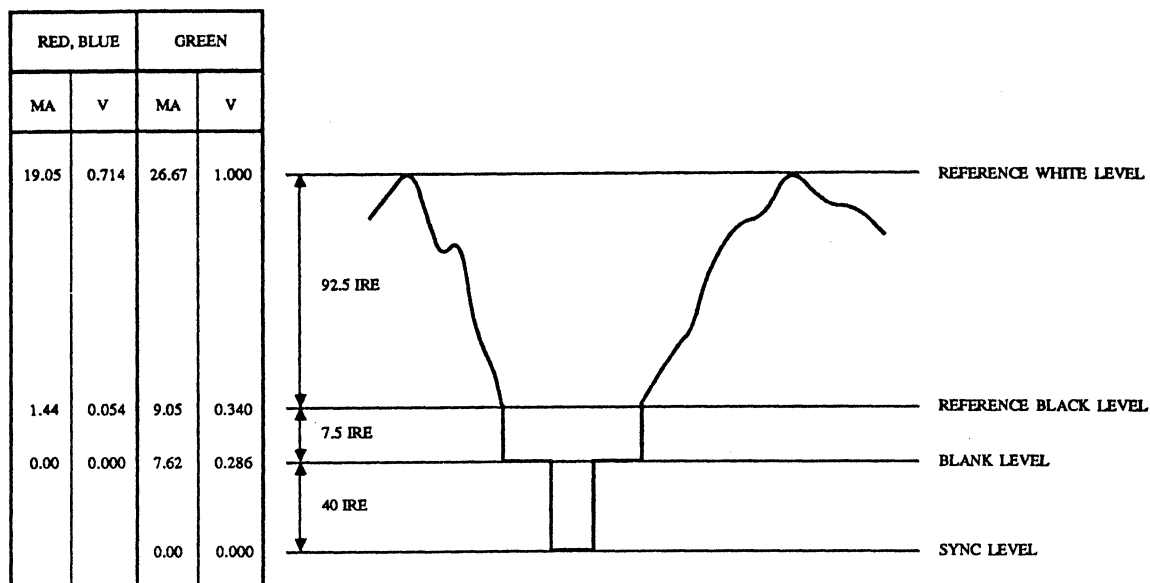
The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) contains sync information. Tables 5 and 6 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt458 and Bt451 use a segmented architecture in which bit currents are routed to either the current output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output against temperature and power supply variations.

CR6	OL1	OL0	P7 - P0	Palette entry addressed
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 4. Palette and Overlay Select Truth Table.

Circuit Description (continued)

RED, BLUE		GREEN			
MA	V	MA	V		
19.05	0.714	26.67	1.000		REFERENCE WHITE LEVEL
				92.5 IRE	
1.44	0.054	9.05	0.340		REFERENCE BLACK LEVEL
				7.5 IRE	
0.00	0.000	7.62	0.286		BLANK LEVEL
				40 IRE	
		0.00	0.000		SYNC LEVEL

Note: 75-ohm doubly-terminated load, RSET = 523 ohms, VREF = 1.235v. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 7.62	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0.00	1	0	$xx
SYNC	0.00		0	0	$xx
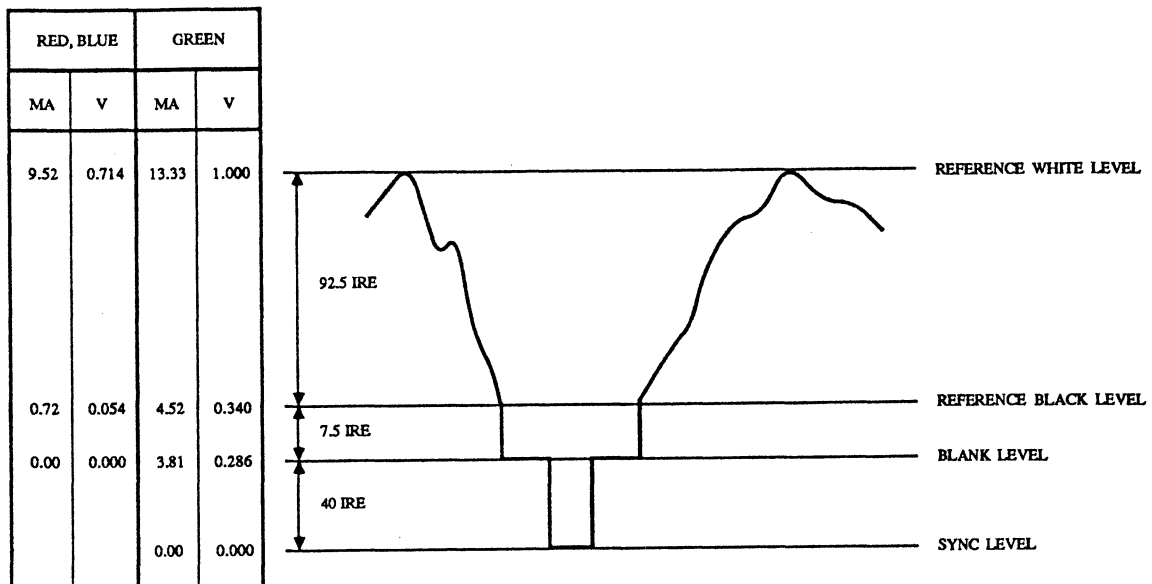
Note: Typical with full scale IOG = 26.67 mA. RSET = 523 ohms, VREF = 1.235v. Note that the Bt451 uses only the upper four DAC input data bits.

Table 5. Video Output Truth Table.

Bt458/451

Circuit Description (continued)

RED, BLUE		GREEN	
MA	V	MA	V
9.52	0.714	13.33	1.000
0.72	0.054	4.52	0.340
0.00	0.000	3.81	0.286
		0.00	0.000

REFERENCE WHITE LEVEL

92.5 IRE

REFERENCE BLACK LEVEL

7.5 IRE

BLANK LEVEL

40 IRE

SYNC LEVEL

Note: 75-ohm singly-terminated load, RSET = 1046 ohms, VREF = 1.235v. RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	13.33	9.52	1	1	$FF
DATA	data + 3.81	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	4.52	0.72	1	1	$00
BLACK - SYNC	0.72	0.72	0	1	$00
BLANK	3.81	0.00	1	0	$xx
SYNC	0.00		0	0	$xx

Note: Typical with full scale IOG = 13.33 mA. RSET = 1046 ohms, VREF = 1.235v. Note that the Bt451 uses only the upper four DAC input data bits.

Table 6. Video Output Truth Table.

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 corresponds to data bus bit D0.

CR7   Multiplex select

         (0)   4:1 multiplexing
         (1)   5:1 multiplexing

This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to the regular PCB ground plane, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate.

CR6   RAM enable

         (0)   use overlay color 0
         (1)   use color palette RAM

When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.

CR5, CR4   Blink rate selection

         (00)   1.024 seconds (75/25)
         (01)   0.512 seconds (50/50)
         (10)   1.024 seconds (50/50)
         (11)   2.048 seconds (50/50)

These two bits specify the blink rate cycle time and duty cycle, assuming a 60 Hz noninterlaced or 30 Hz interlaced refresh rate. For applications having other refresh rates (i.e. 57 Hz noninterlaced), the blink rate is determined by scaling the specified values (i.e. multiplying by 57/60). The numbers in parentheses specify the duty cycle (% on/off).

CR3   OL1 blink enable

         (0)   disable blinking
         (1)   enable blinking

If a logical one, this bit forces the OL1 {A - E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A - E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.

CR2   OL0 blink enable

         (0)   disable blinking
         (1)   enable blinking

If a logical one, this bit forces the OL0 {A - E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A - E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Command Register (continued)

CR1	OL1 display enable	If a logical zero, this bit forces the OL1 {A - E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A - E} inputs.
	(0) disable	
	(1) enable	
CR0	OL0 display enable	If a logical zero, this bit forces the OL0 {A - E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A - E} inputs.
	(0) disable	
	(1) enable	

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A - E}) and D7 corresponds to bit plane 7 (P7 {A - E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A - E}) and D7 corresponds to bit plane 7 (P7 {A - E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper four bits (D4 - D7) are ignored.

The contents of the test register are defined as follows:

D7 - D4	color information (4 bits of red, green, or blue)
D3 D2 D1 D0	low (logical one) or high (logical zero) nibble blue enable green enable red enable

To use the test register, the host MPU writes to it, setting one, and only one, of the (red, green, blue) enable bits. These bits specify which four bits of color information the MPU wishes to read (R0 - R3, G0 - G3, B0 - B3, R4 - R7, G4 - G7, or B4 - B7). When the MPU reads the test register, the four bits of color information from the DAC inputs are contained in the upper four bits, and the lower four bits contain the (red, green, blue, low or high nibble) enable information previously written. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper four bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4 - D7 containing R4 - R7 color bits, and D0 - D3 containing (red, green, blue, low or high nibble) enable information, as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Note that since the Bt451 has 4-bit D/A converters, bit D3 of the test register will always be a logical zero.

When reading the test register, the data valid access time (Pages 24 and 25, Parameter 6) increases to 200 ns. It is recommended that the test register be initialized by the MPU to $00.