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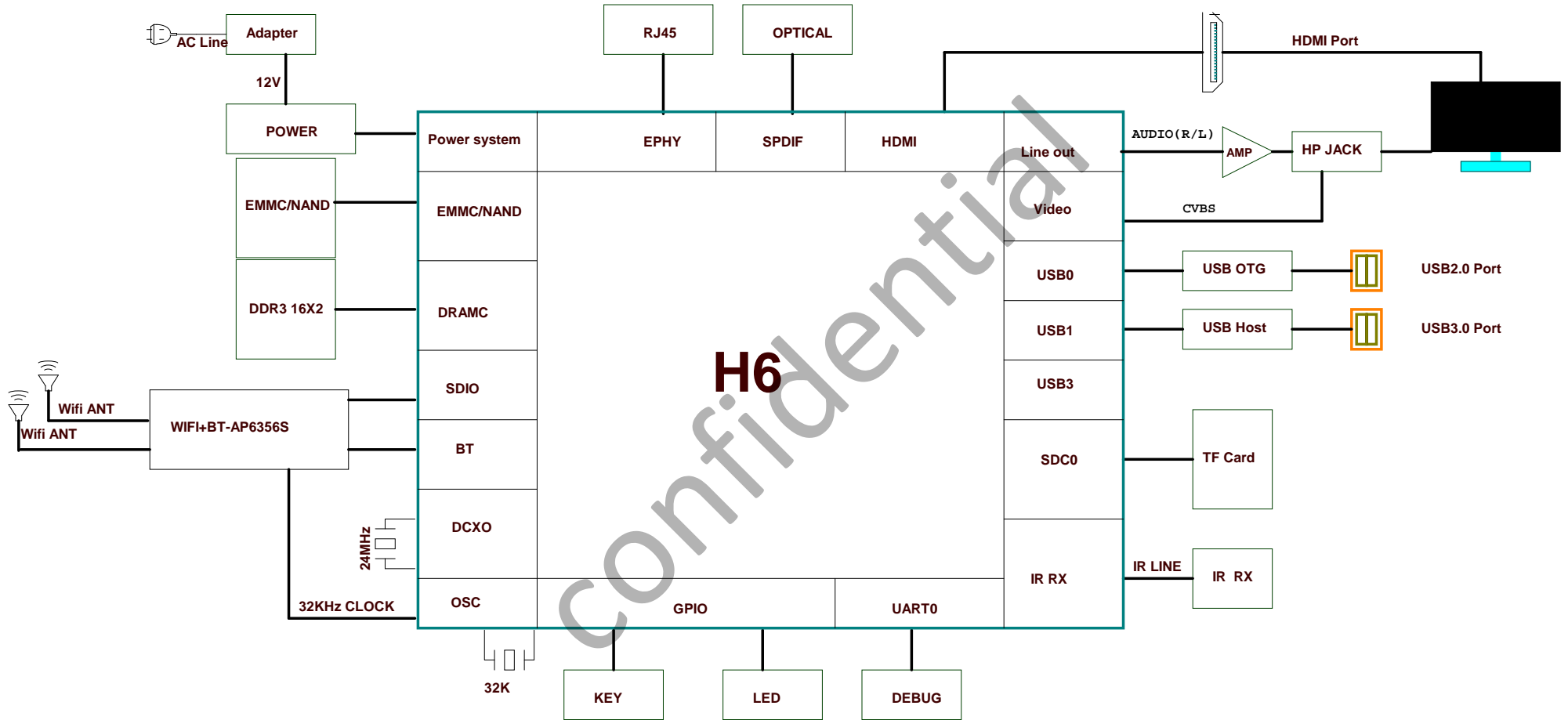
REVISION HISTORY

Revision	Description	Date	Drawn	Checked
Ver 0.5	Initial Version	2016-12-26	HJ	
Ver 0.9		2017-04-10	HJ	
Ver 1.0		2017-06-14	HJ	

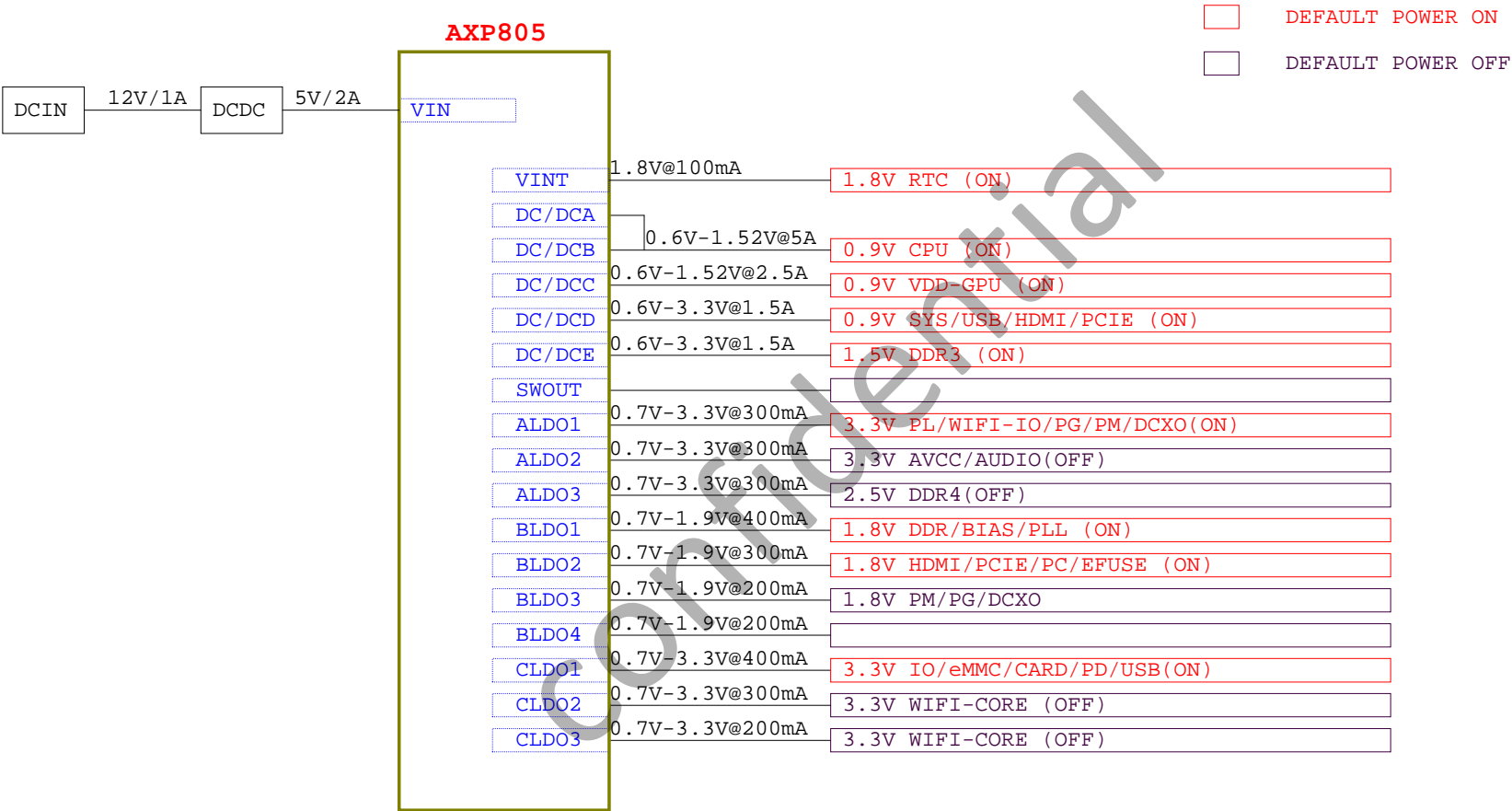
Schematics Index:

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P10: CARD-USB-IR-SPDIF
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Confidential



POWER TREE



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE	2	NAND/eMMC
PC1	NAND_ALE/SDC2_DS	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE0	2	
PC4	NAND_RE/SDC2_CLK	2/3	
PC5	NAND_RB0/SDC2_CMD	2/3	
PC6	NAND_DQ0/SDC2_D0	2/3	
PC7	NAND_DQ1/SDC2_D1	2/3	
PC8	NAND_DQ2/SDC2_D2	2/3	
PC9	NAND_DQ3/SDC2_D3	2/3	
PC10	NAND_DQ4/SDC2_D4	2/3	
PC11	NAND_DQ5/SDC2_D5	2/3	
PC12	NAND_DQ6/SDC2_D6	2/3	
PC13	NAND_DQ7/SDC2_D7	2/3	
PC14	NAND_DQS/SDC2_RST	2/3	
PC15	NAND_CE1	2	
PC16	NAND_RB1	2	

PIN	Define	CFG	Function
PD0			
PD1			
PD2			
PD3			
PD4			
PD5			
PD6			
PD7			
PD8			
PD9			
PD10			
PD11			
PD12			
PD13			
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19			
PD20			
PD21			
PD22			
PD23			
PD24			
PD25			
PD26			

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	WIFI+BT
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	
PG7	UART1_RX	2	
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14			

PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD0
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0_DET	2	

PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2	DDC_CEC_EN	6	
PH3			
PH4			
PH5			
PH6			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	
PH9	HSDA	2	
PH10	HCEC	2	HDMI

PIN	Define	CFG	Function
PL0	PMU-SCK	3	WIFI+BT
PL1	PMU-SDA	3	
PL2	RECOVERY	6	
PL3	LINK-LED	1	
PL4	PWR-LED	1	
PL5	USB0-DRVVBUS	1	
PL6	MUTE	1	
PL7	STATUS-LED	1	
PL8	BT-WIFI-ON	1	
PL9	IR-RX	2	
PL10			
PM0	WL-WAKE-AP	6	
PM1	BT-WAKE-AP	6	
PM2	AP-WAKE-BT	1	
PM3	WL-REG-ON	1	
PM4	BT-REG-ON	1	

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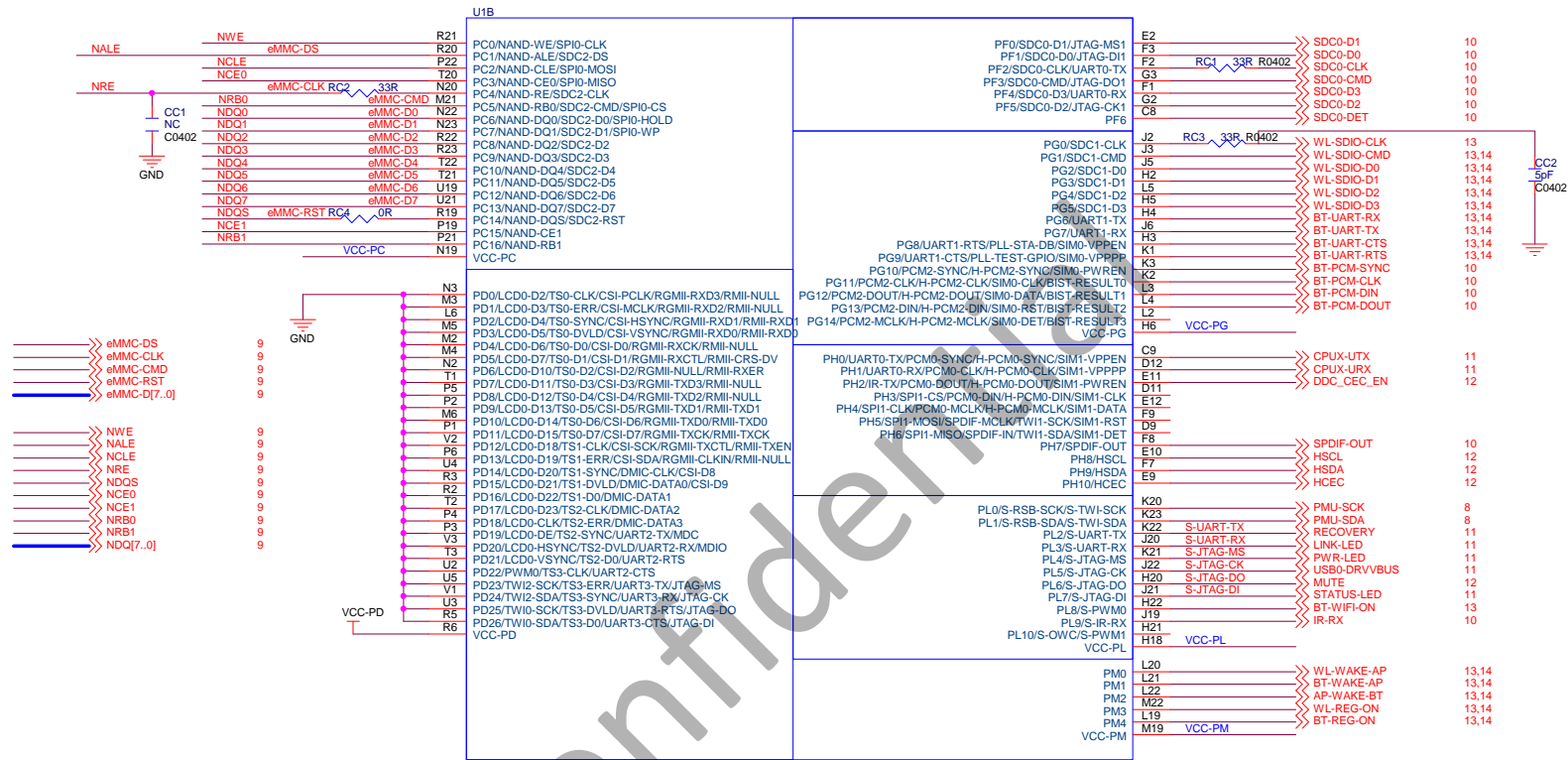
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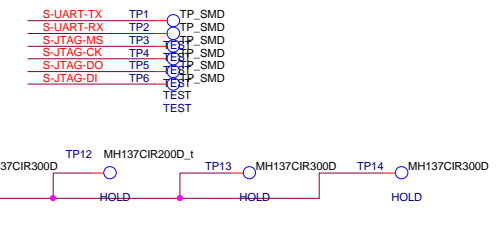
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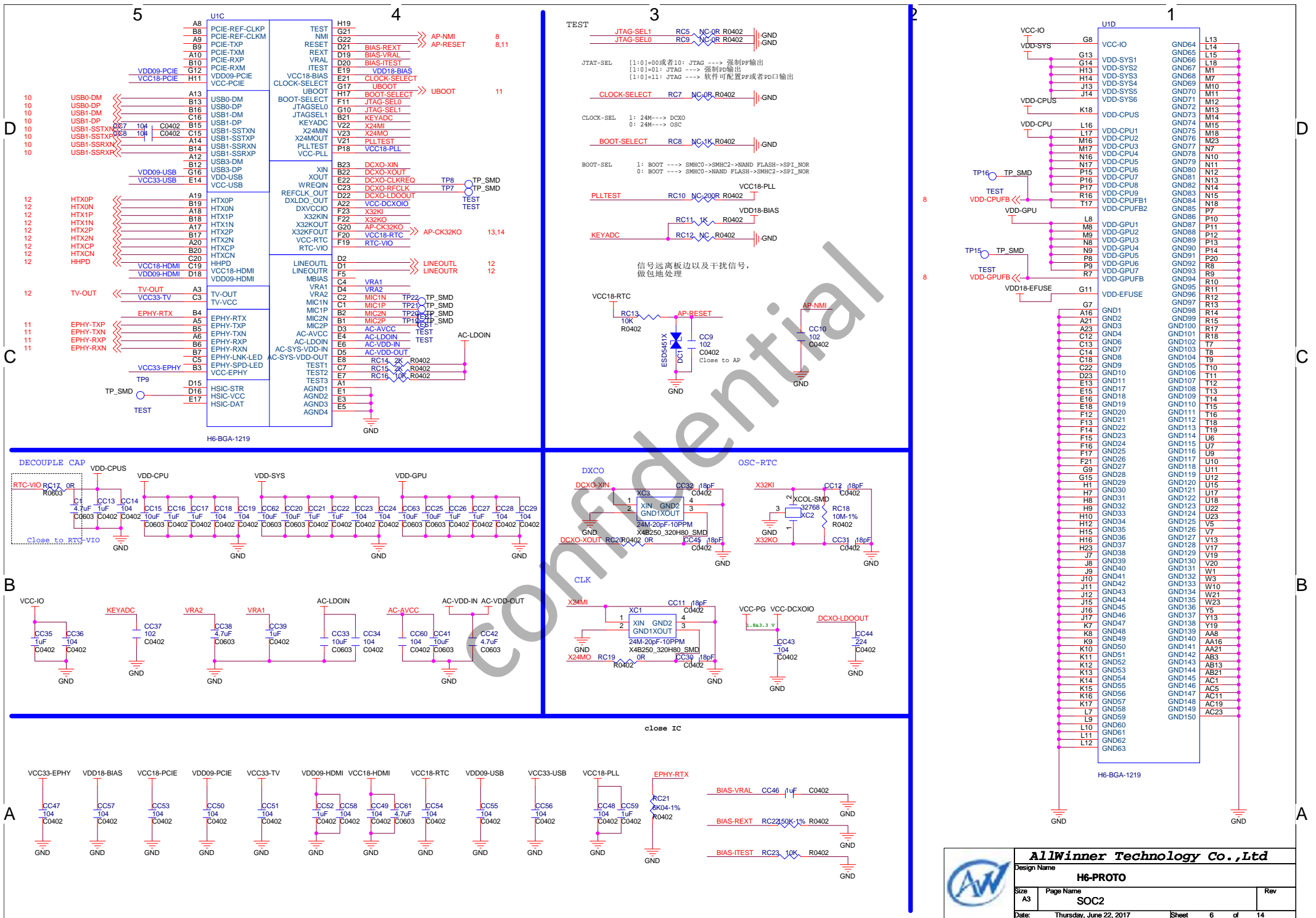
PC, PD, 部分IO口不具备中断功能
PF, PG, PH, PL, PM, 部分IO口有中断功能



H6-BGA-1219

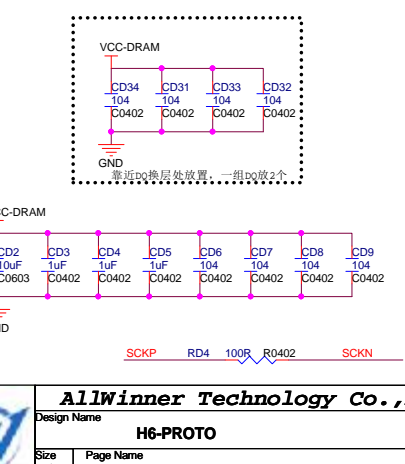
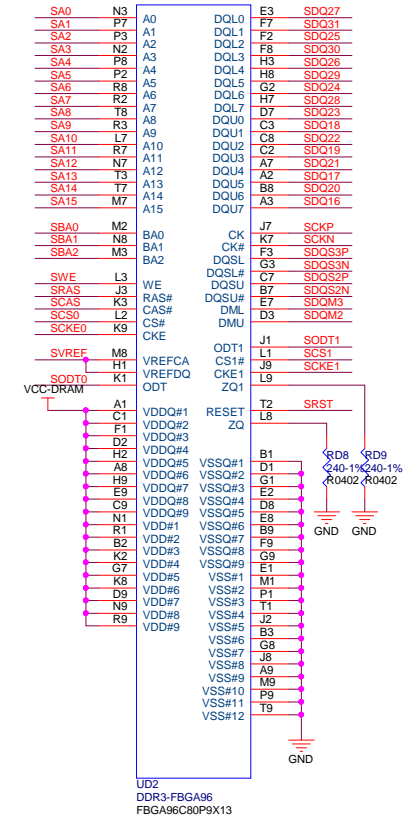
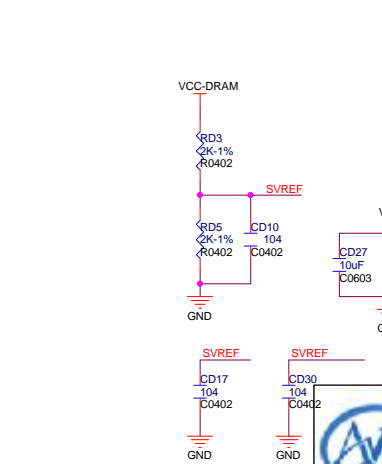
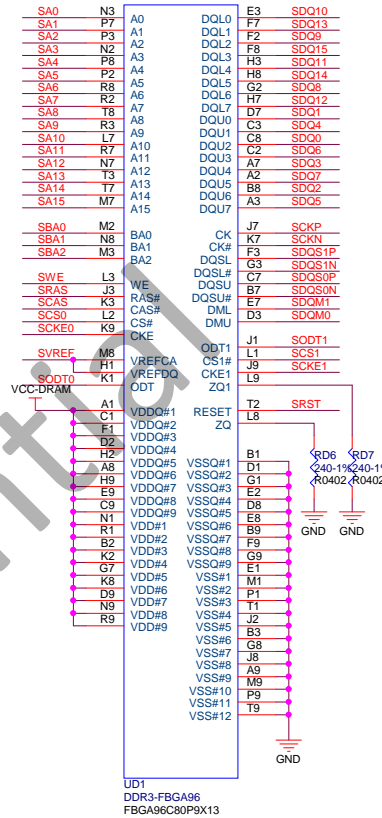
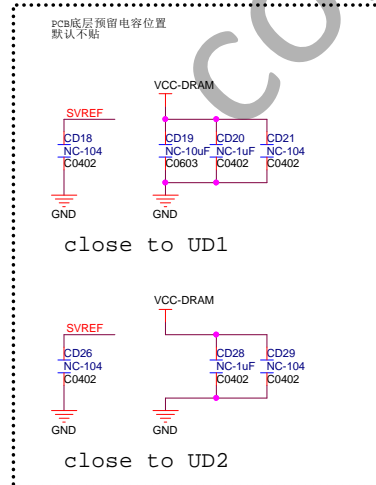
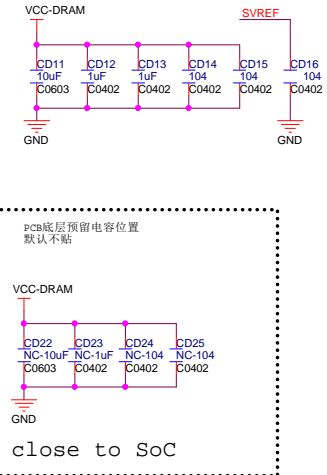
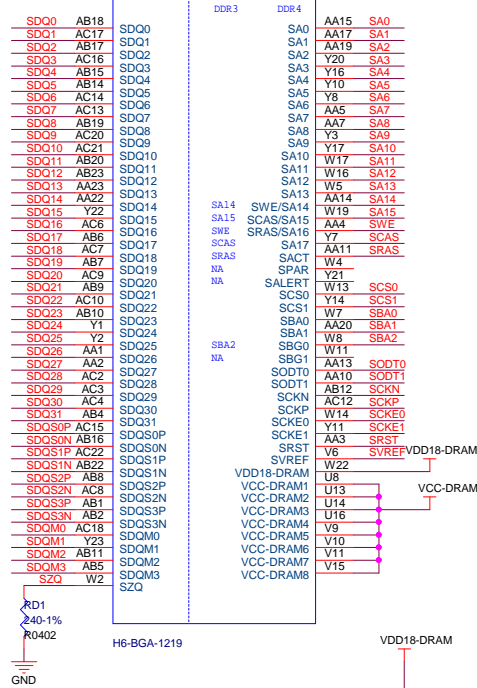


Allwinner Technology Co., Ltd			
Design Name		H6-PROTO	
Size	Page Name	Rev	
A3	SOC1		
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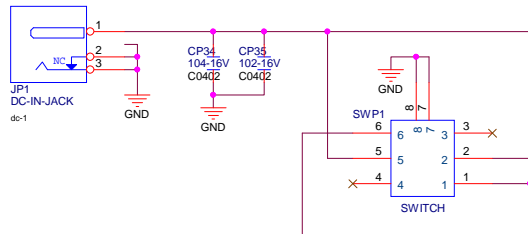


DDR3 16X2

U1A

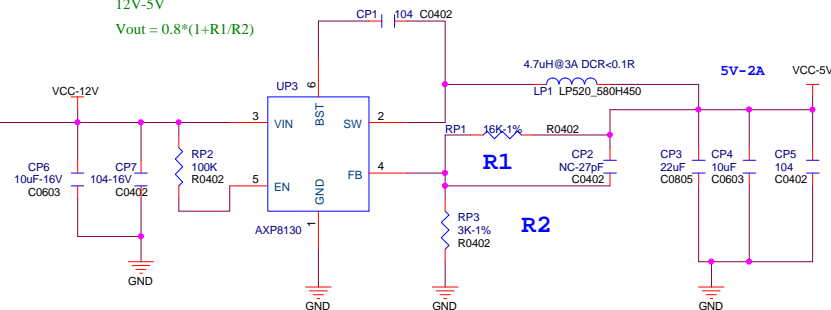


DCIN



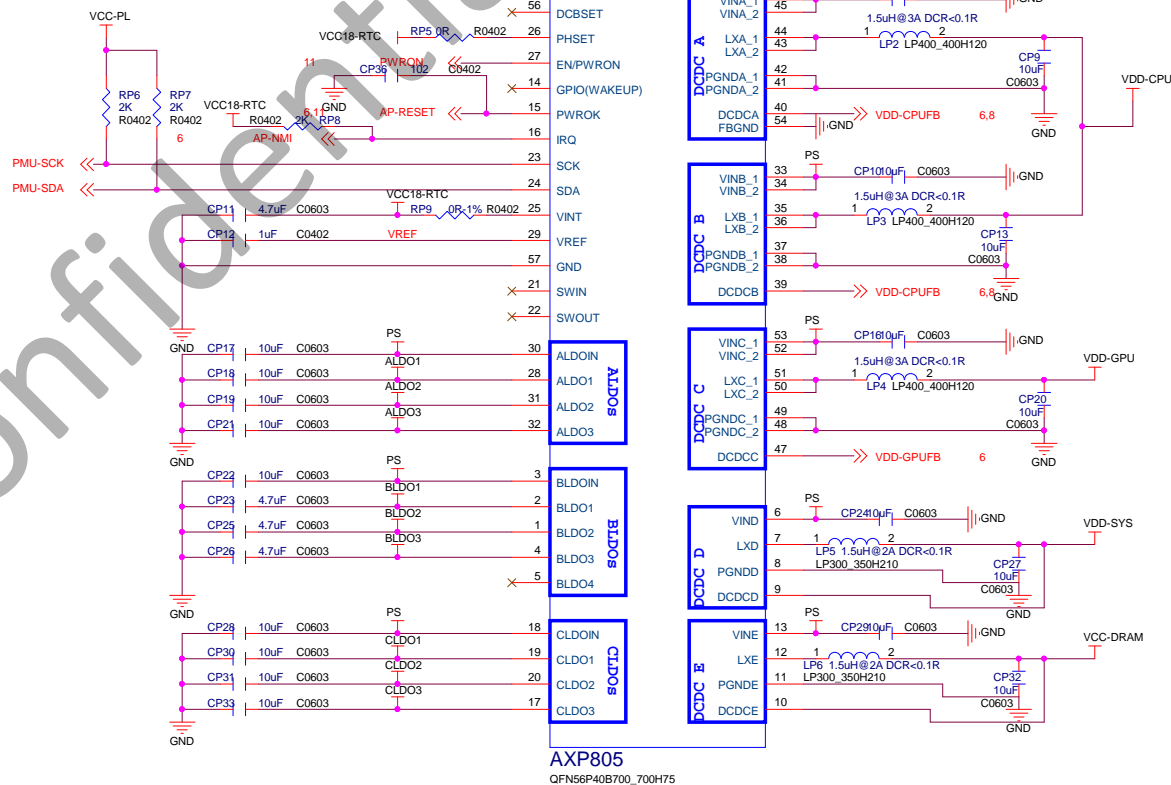
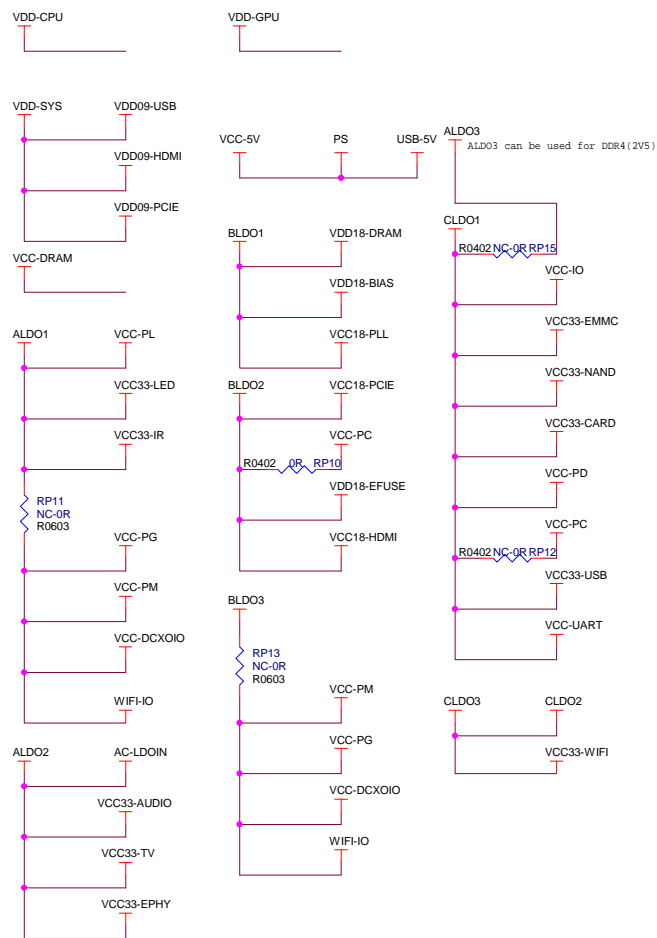
12V->5V

12V-5V
Vout = 0.8*(1+R1/R2)



PMIC

AXP805



AXP805
QFN56P40B700_700H75



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Design Name		H6-PROTO	
Size	Page Name	POWER	
A3		Rev	
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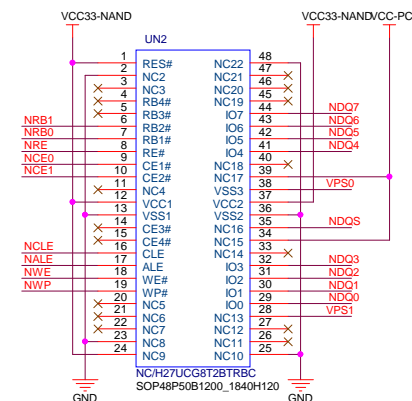
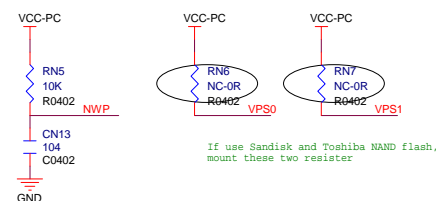


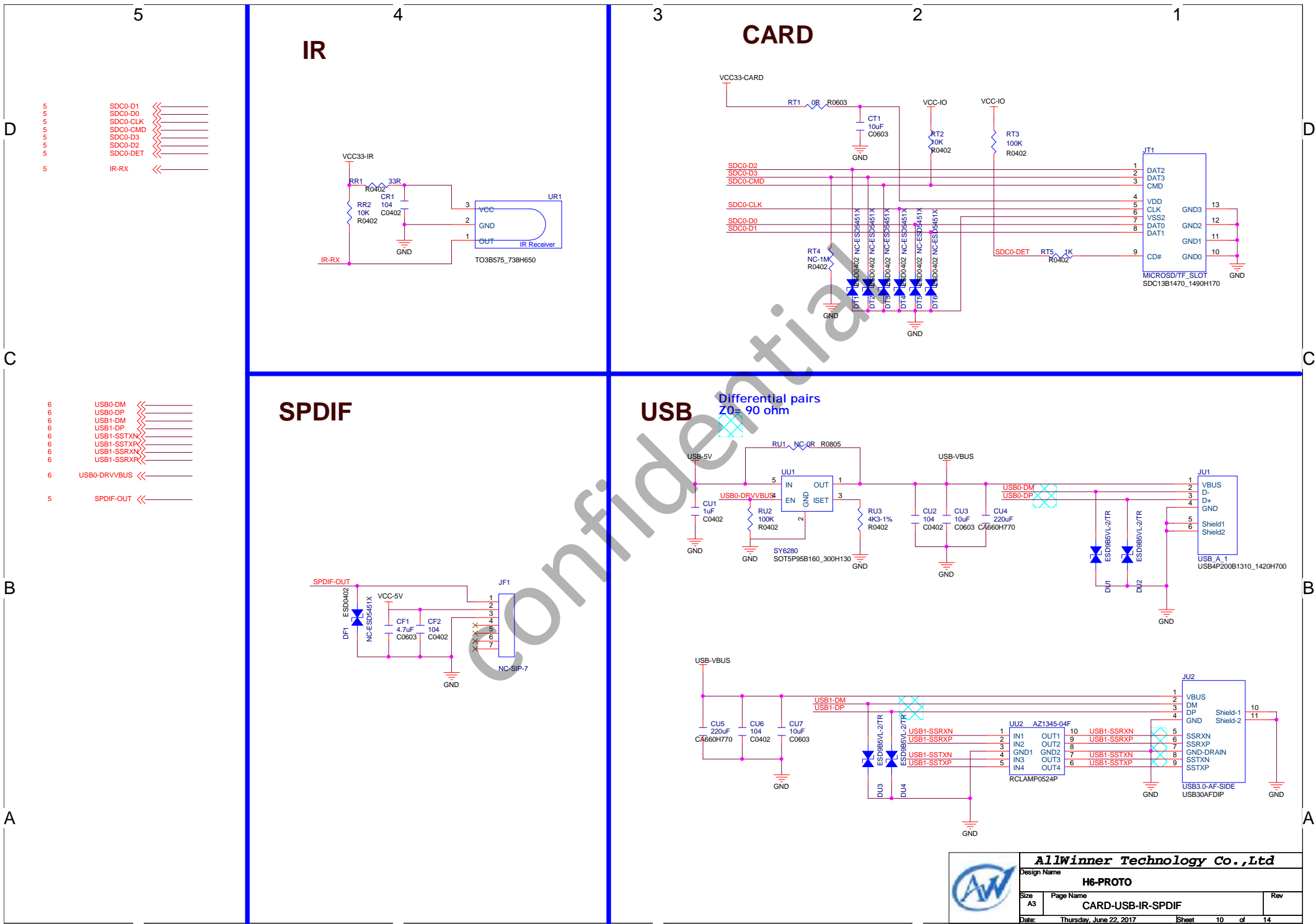
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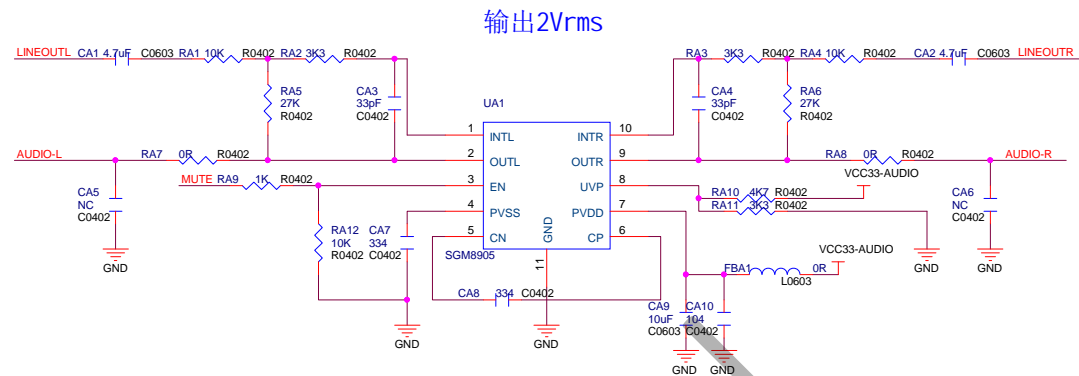


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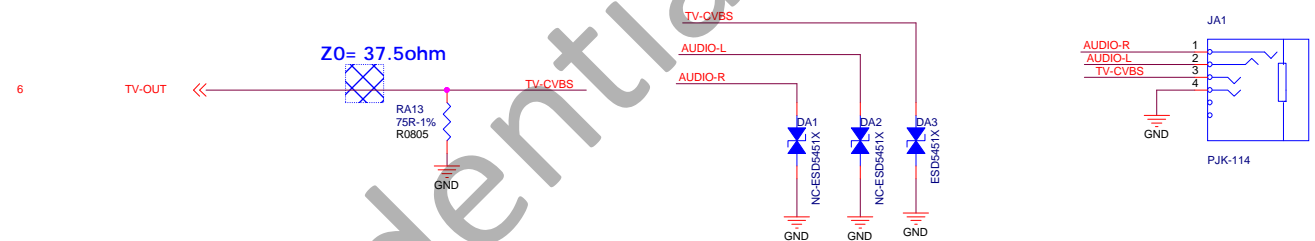




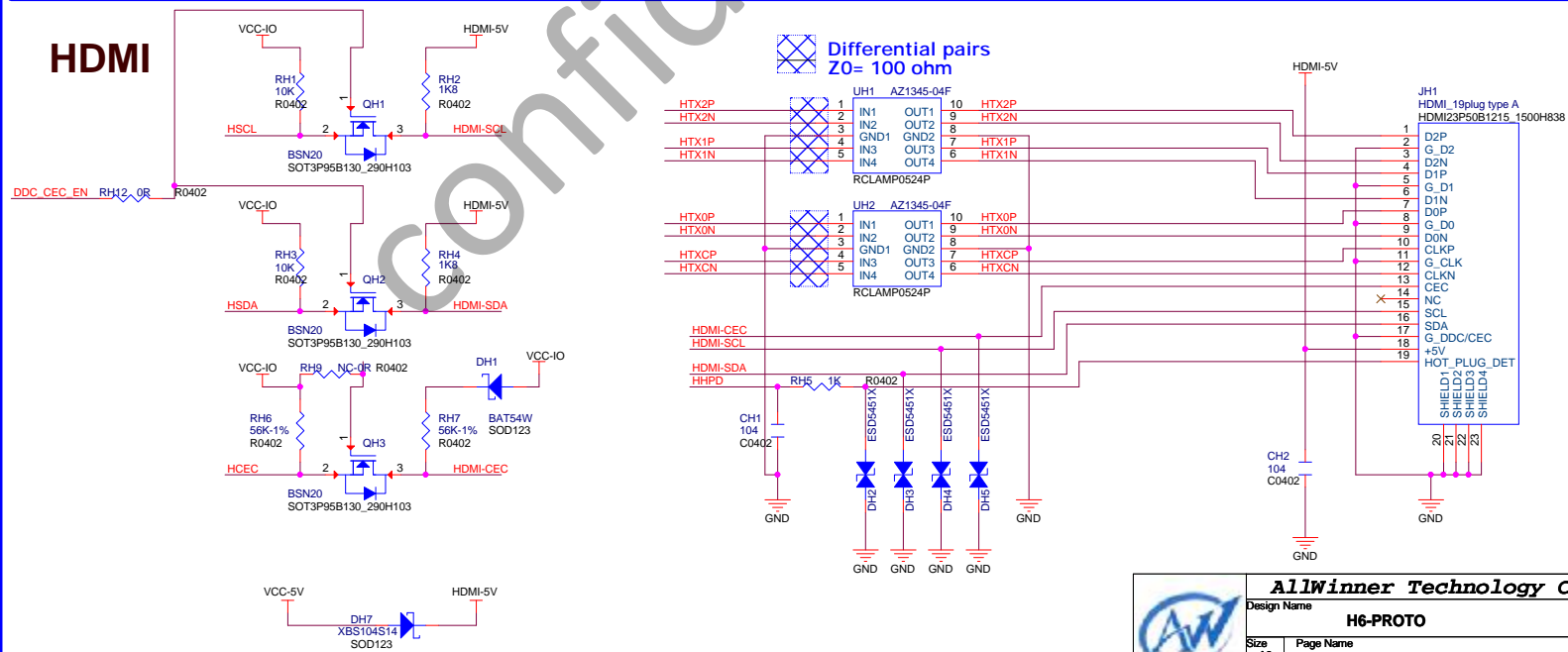
D	6	LINEOUTL	≡≡≡	≡
	6	LINEOUTR	≡≡≡	≡
	5	MUTE	≡≡	≡



6	HTX0P	
6	HTX0N	
6	HTX1P	
6	HTX1N	
6	HTX2P	
6	HTX2N	
6	HTXCP	
6	HTXCN	
5	HSCL	
5	HSDA	
6	HHPD	
5	HCEC	



5 DDC_CEC_EN <<—



Design Name **H6-PROTO**

Size	Page Name	Re
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A3	AV-HDMI	
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WIFI+BT 2T2R

5,14 WL-SDIO-CMD
5,14 WL-SDIO-D0
5,14 WL-SDIO-D1
5,14 WL-SDIO-D2
5,14 WL-SDIO-D3
5 WL-SDIO-CLK

5,14 BT-UART-TX
5,14 BT-UART-RX
5,14 BT-UART-RTS
5,14 BT-UART-CTS
5 BT-PCM-SYNC
5 BT-PCM-CLK
5 BT-PCM-DIN
5 BT-PCM-DOUT

5 BT-REG-ON
5,14 WL-WAKE-AP
5,14 BT-WAKE-AP
5,14 AP-WAKE-BT
5,14 WL-REG-ON
5,14 AP-CK32KO

5 BT-WIFI-ON

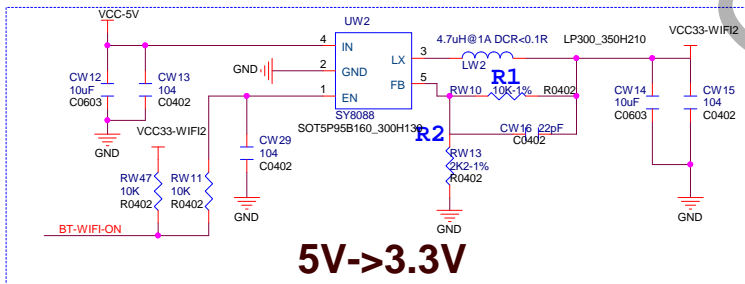
NOTE FOR crystal:

AP6356s	37.4M
WCT6RA2001S	48M

NOTE FOR:

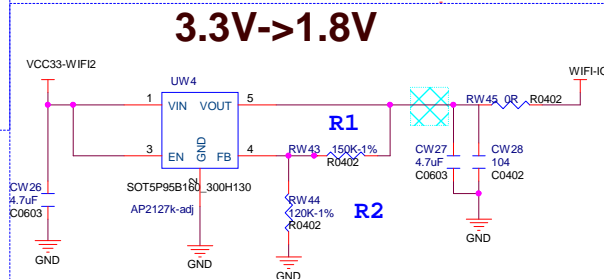
AP6356s	4.7uH	4.7uF
WCT6RA2001S	1.5uH	22uF

NOTE:
L1, rated current 1A
expectation specification.



5V->3.3V

5V->3.3V (WIFI) and 3.3V->1.8V (WIFI-I/O) circuit is only for products that need BT regulator. If there are no products that need BT regulator, you can use CLD02+CLD03 to supply WIFI1, ALD01 or BLD03 to supply WIFI-I/O.



3.3V->1.8V

NOTE SDIO-CLK: R

AP6356s	NC
WCT6RA2001S	10K

50 Ohm RF trace

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