Debounced 8×8 Key-Scan Controller

Description

The SN7326 is a 64 key, key-scan controller. It offloads the burden of keyboard scanning from the host processor. The SN7326 supports keypad matrix of up to 8×8. Key press and release events are encoded into a byte format and loaded into a key event register for retrieval by the host processor.

The SN7326 integrates a debounce function which rejects false or transient key switch activities. The interrupt output ($\overline{INT}$) is used to signify if there are any keypad activities.

To minimize power, the SN7326 automatically enters a low power standby mode when there is no keypad, I/O, or host activity.

The SN7326 is available in a Pb-free 4mm × 4mm QFN-24 package.

Features

- 2.4V to 5.5V operation
- 400kHz I^2C serial interface
- Available for multi-key press detect
- Low 0.3μA (typ.) standby current
- Operate in −40°C to +125°C
- Pb-free 4mm × 4mm QFN-24 package

Applications

- Keypad of QWERTY type phones
- PDAs, games, and other handheld applications

Typical Application Circuit

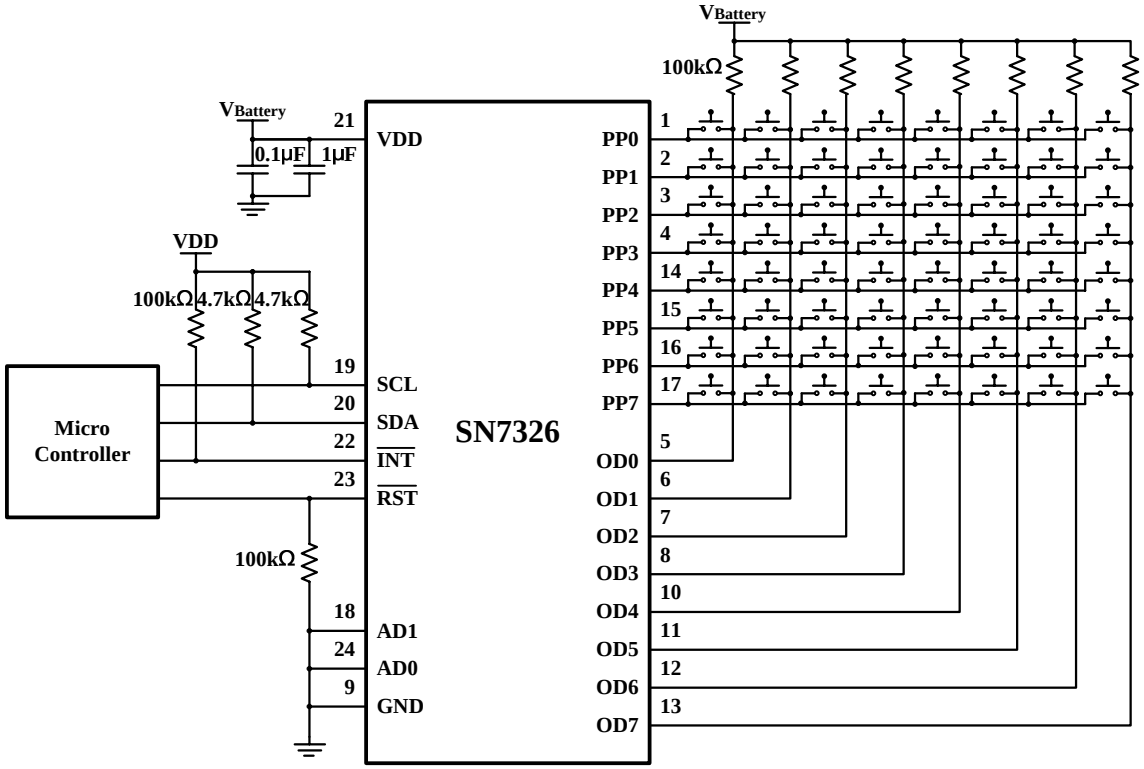
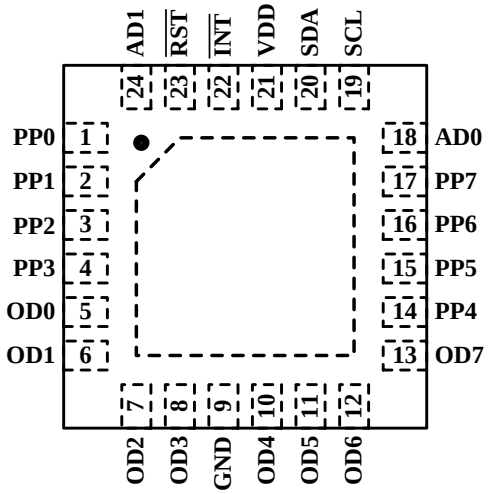


Figure 1 Typical application circuit

Pin Configuration

Package	Pin Configuration (Top View)
WQFN-24	

Pin Description

No.	Pin	I/O	Description
1~4, 14~17	PP0~PP7	O	Output ports
5~8, 10~13	OD0~OD7	I	Input ports
9	GND	I	Ground
18	AD0	I	Address setting
19	SCL	I	I2C serial clock
20	SDA	I/O	I2C serial data
21	VDD	I	Power supply voltage
22	$\overline{\text{INT}}$	O	Interrupt output, active low
23	$\overline{\text{RST}}$	I	Reset input, active low
24	AD1	I	Address setting
Thermal Pad	Thermal Pad		Connect to GND

Ordering Information

Order Number	Package Type	QTY/Reel	Operating Temperature Range
SN7326A424E	WQFN-24	2500	−40°C to +125°C

SN7326 □ □ □ □

Environmental Code
E: Lead Free

Pin Code
24: 24pins

Package Type
4: WQFN, 4mm × 4mm

Temperature Code
A: Automotive, −40°C to +125°C

Absolute Maximum Ratings

Supply voltage, V_{DD} ---------- −0.3V to 6.0V
Voltage at any input pin(Except PP0-PP7) ---------- −0.3V to 6.0V
Voltage at PP0-PP7 ---------- −0.3V to (V_{DD} +0.3V)
SDA sink current ---------- 10mA
$\overline{INT}$ sink current ---------- 10mA
Continuous power dissipation (T_A = 70°C) WQFN-24 (derate 33.2mW/°C over 70°C) ---------- 2.65W
Lead temperature (soldering, 10s) ---------- 300°C
Storage temperature Range ---------- −65°C to +150°C
Operating temperature range ---------- −40°C to +125°C
Junction temperature, T_{JMAX} ---------- 150°C
ESD HBM ---------- 4KV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

T_A= −40°C to +125°C, V_{DD} = 2.4V to 5.5V, unless otherwise noted. Typical values are at T_A = 25°C, V_{DD} = 3.3V. (*Note 1*)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage		2.4		5.5	V
V_{POR}	Power-on-reset voltage	V_{DD} falling			2.35	V
I_{STB}	Standby current (Interface idle)	SCL,SDA and other digital inputs at V_{DD}		0.3	1.9	μA
I+	Supply current (Interface running)	f_{SCL} = 400kHz other digital inputs at V_{DD}		6.5	25	μA
V_{IH}	Logic "1" input voltage		1.4			V
V_{IL}	Logic "0" input voltage				0.4	V
I_{IH}, I_{IL}	Input leakage current	SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7 at V_{DD} or GND	−0.2		+0.2	μA
C_{IN}	Input capacitance SDA, SCL, AD0, AD1, $\overline{RST}$, OD0~OD7, PP0~PP7	*(Note 2)*		10		pF
V_{OL}	Logic "0" output voltage PP0~PP7	V_{DD} = 2.5V, I_{SINK} = 10mA			200	mV
		V_{DD} = 3.3V, I_{SINK} = 15mA			240	
		V_{DD} = 5.0V, I_{SINK} = 20mA			250	
V_{OH}	Logic "1" output voltage PP0~PP7	V_{DD} = 2.5V, I_{SOURCE} = 5mA	V_{CC} -316			mV
		V_{DD} = 3.3V, I_{SOURCE} = 5mA	V_{CC} -213			
		V_{DD} = 5.0V, I_{SOURCE} = 10mA	V_{CC} -289			
V_{OLSDA}	Output low-voltage SDA	I_{SINK} = 6mA			180	mV
$V_{OL\overline{INT}}$	Output low-voltage $\overline{INT}$	I_{SINK} = 5mA			180	mV
t_{SCAN}	Time to scan key matrix completely	Configuration Register bit SD = 0		16		ms
		Configuration Register bit SD = 1		9		

Timing Characteristics

T_A = −40°C to +125°C, V_{DD} = 2.4V to 5.5V, unless otherwise noted. Typical values are at T_A = 25°C, V_{DD} = 3.3V. *(Note 3)*

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SCL}	Serial-clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time	*(Note 3)*			0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	*(Note 4)*		20 + 0.1Cb	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	*(Note 4)*		20 + 0.1Cb	300	ns
$t_{F, TX}$	Fall time of SDA transmitting	*(Note 4)*		20 + 0.1Cb	250	ns
t_{SP}	Pulse width of spike suppressed	*(Note 5)*		50		ns
C_b	Capacitive load for each bus line				400	pF
t_W	$\overline{RST}$ pulse width		500			ns
$t_{\overline{RST}}$	$\overline{RST}$ rising to START condition setup time		1			μs

Port and Interrupt Timing Characteristics

T = −40°C to +125°C, V_{DD} = 2.4V to 5.5V, unless otherwise noted. Typical values are at T_A = 25°C, V_{DD} = 3.3V *(Note 3)*

Symbol	Parameter	Condition	Min.	Typ.	Max.	Untis
t_{PV}	Port output data valid	$C_L \leq$ 100pF			4	μs
t_{PSU}	Port input setup time	$C_L \leq$ 100pF	0			μs
t_{PH}	Port input hold time	$C_L \leq$ 100pF	4			μs
t_{IV}	$\overline{INT}$ input data valid time	$C_L \leq$ 100pF			4	μs
t_{IR}	$\overline{INT}$ reset delay time from acknowledge	$C_L \leq$ 100pF			4	μs

Note 1: All parameters are tested at T_A = 25°C. Specifications over temperature are guaranteed by design.

Note 2: Guaranteed by design.

Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

Note 4: Cb = total capacitance of one bus line in pF. $I_{SINK} \leq$ 6mA. t_R and t_F measured between 0.3 × V_{DD} and 0.7× V_{DD}.

Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Detailed Description

I2C Interface

The SN7326 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The SN7326 has a 7-bit slave address (A7:A1), followed by the R/$\overline{W}$ bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The bit A2:A1 are selected by the connection of AD1/AD0 pin.

The complete slave address is:

Table 1 Slave Address:

Bit	A7:A3	A2	A1	A0
Default	10110	AD1	AD0	0/1

AD1/AD0 connects to VDD, AD1/AD0=1;

AD1/AD0 connects to GND, AD1/AD0=0;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the SN7326.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high (Figure 4). The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the SN7326's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the SN7326 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of SN7326, the register address byte is sent, most significant bit first. SN7326 must generate another acknowledge indicating that the register address has been received.

An 8-bit data byte is sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the SN7326 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high (Figure 4).

Writing to the registers

Transmit data to the SN7326 by sending the device slave address and setting the LSB to "0". The command byte is sent after the address and determines which registers receive the data following the command byte (Figure 2).

Reading port registers

To read the device data, the bus master must first send the SN7326 address with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the SN7326 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the SN7326 to the master (Figure 6).

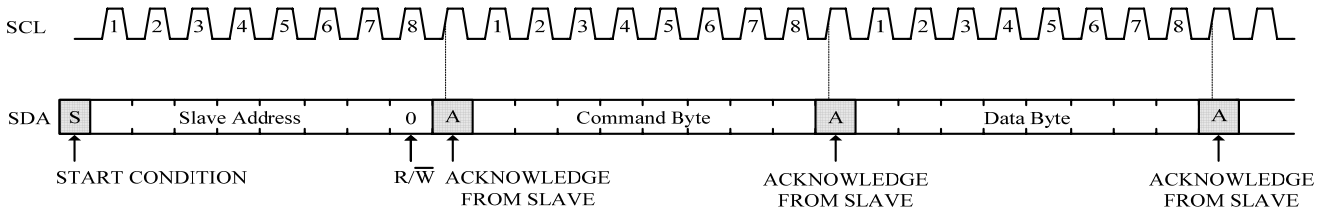


Figure 2 Writing to SN7326

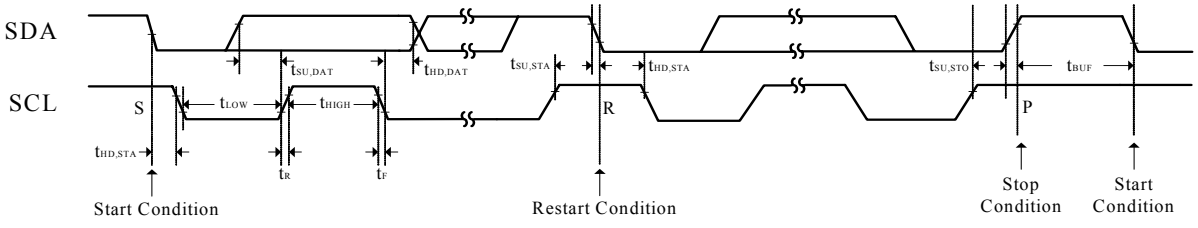


Figure 3 Interface timing

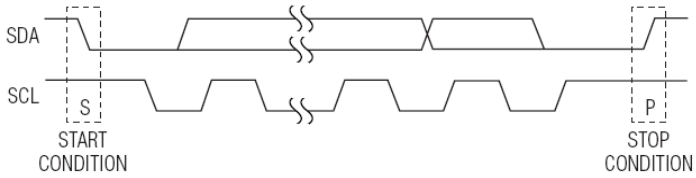


Figure 4 START and STOP conditions

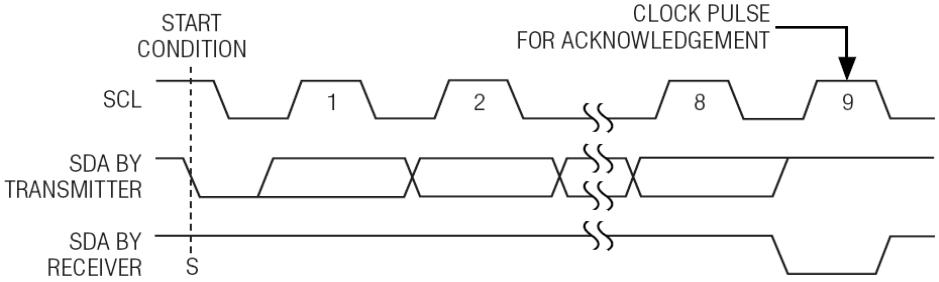


Figure 5 Acknowledge signal

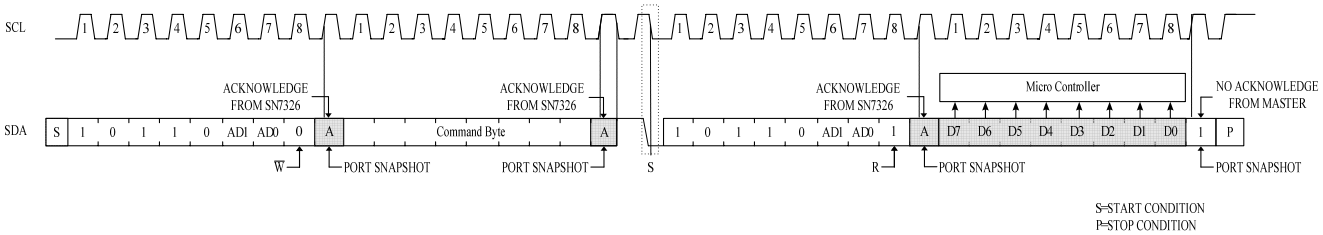


Figure 6 Reading I/O ports of SN7326

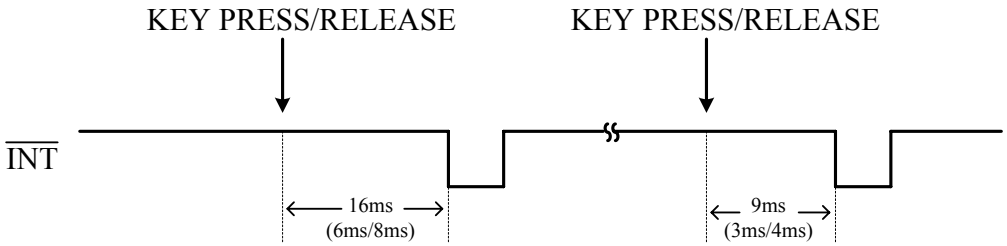


Figure 7 $\overline{INT}$ timing

Register Definition

Table 2 Register Function

Address	Name	Function	Default	Table
08h	Configuration Register	Configure the keypad scan function	0001 0000	3
10h	Key Status Register	Contains the information of the key events	0000 0000	4

Table 3 08h Configuration Register

Bit	D7	D6:D5	D4	D3	D2	D1:D0
Name	Reserved	ACI	DE	SD	LE	LT
Default	0	00	1	0	0	00

The Configuration Register is used to configure the keypad scan function.

ACI Auto Clear $\overline{INT}$

00 Auto clear $\overline{INT}$ disabled

01 Auto clear $\overline{INT}$ in 5ms

10 Auto clear $\overline{INT}$ in 10ms

DE Input Port Filter Enable

0 Input port filter disable

1 Input port filter enable

SD Key Scan Debounce Time

0 Double debounce time (6ms, 8ms)

1 Normal debounce time (3ms, 4ms)

LE Long-pressed Key Detect Enable

0 Disable

1 Enable

LT Long-pressed Key Detect Delay Time

00 20ms

01 40ms

10 1s

11 2s

Table 4 10h Key Status Register

Bit	D7	D6	D5:D0
Name	DN	KS	KM
Default	0	0	000000

The Key Status Register contains the information of the key events that have been debounced (see the Table5 of the key mapping).

DN Indicate Data Number

0 One key event to report

1 More than one key to report

KS Key State

0 Key released

1 Key pressed

KM Key Mapping

KM denotes which of the 64 keys have been debounced and the keys are numbered as shown in the Table5.

When the Key Status Register is read over (DN=0), the register is set to "0000 0000", and the $\overline{INT}$ is cleared.

Table 5 Key Mapping (D5:D0)

	PP0	PP1	PP2	PP3	PP4	PP5	PP6	PP7
OD0	000000	000001	000010	000011	000100	000101	000110	000111
OD1	001000	001001	001010	001011	001100	001101	001110	001111
OD2	010000	010001	010010	010011	010100	010101	010110	010111
OD3	011000	011001	011010	011011	011100	011101	011110	011111
OD4	100000	100001	100010	100011	100100	100101	100110	100111
OD5	101000	101001	101010	101011	101100	101101	101110	101111
OD6	110000	110001	110010	110011	110100	110101	110110	110111
OD7	111000	111001	111010	111011	111100	111101	111110	111111

Examples

1. If the key PP1-OD3 pressed only, and other keys keep released state, the $\overline{INT}$ asserts, the data in Key Status Register would be "0101 1001";
2. If the key PP4-OD6 released only, and other keys keep released state, the $\overline{INT}$ asserts, the data in Key Status Register would be "0011 0100";
3. If the key PP2-OD4 and PP3-OD7 are pressing, then PP2-OD4 released, the $\overline{INT}$ asserts, the first data in Key Status Register would be "1010 0010", the second data would be "0111 1011". Then judge the MSB (bit DN) in the second data is "0". Data has read over, and $\overline{INT}$ goes to high.

We must read over the data in Key Status Register when the $\overline{INT}$ asserts. When judge the MSB (bit DN) in the data is "0", stop reading the Key Status Register. If there are some keys connected to the same OD port pressing at the same time, SN7326 only can detect the first pressed key and others will ignore.

Application Information

Input and Output Port Structure

A 100kΩ pull-up resistor will force input port high at V_{DD}.

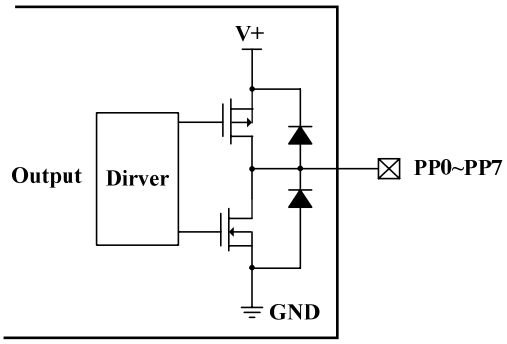


Figure 8 Output Port Structure

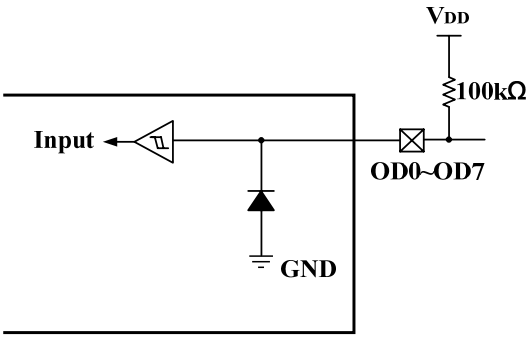


Figure 9 Input Port Structure

Power-On Reset

The SN7326 contains an integral power-on-reset circuit that ensures all registers are reset to a known state on power-up. When V_{DD} rises above 2.4V, the circuit releases the registers and the I2C interface for normal operation. When V_{DD} drops to less than V_{POR}, the SN7326 resets all register contents to the default value.

RST I2C reset control

The active-low $\overline{RST}$ input voids any I2C transaction involving the SN7326, forcing the SN7326 into the I2C STOP condition. A reset does not affect the interrupt output.

Standby Mode

When the serial interface is idle, the SN7326 automatically enters standby mode, drawing minimal supply current.

Keypad Auto Scan

The SN7326 can support an 8×8 matrix keypad scan. The 8 input ports (OD ports) need a 100kΩ pull-up resistor for each column, the 8 output ports (PP ports) for the rows pull low in standby mode.

If a change of the state of the keypad is detected, the keypad would be scanned thrice between the debounce delay. When the state changes have been reliably captured, the key event(s) are encoded and written to temporary key status registers. The $\overline{INT}$ asserts when the key event(s) is (are) stored. Reading the Key Status Register reports the key events in the order of lowest encoding value to the highest (see Table 5). The $\overline{INT}$ will remain low until all of the key events are read, with one exception: When the Auto-Clear $\overline{INT}$ is enabled, if all of the key event data is not read before the programmed time, the $\overline{INT}$ will return high after the programmed time. However the temporary key status registers will remain unchanged and the key event data may continue to be read until another key event is detected.

Debounce

When the bit SD of the Configuration Register (08h) is set to "0" and there is a change of the state of the keypad, the keypad scans first and stores the data in temporary registers, then waits for about 6ms (3ms) and scans again, then waits for another 8ms (4ms) and scans a final time. If the results are the same, the data is latched into the temporary key status registers and the $\overline{INT}$ asserted. Otherwise, the scan is halted and the device returns to standby mode. No data is latched into the temporary key status registers and the $\overline{INT}$is not asserted.

Long-pressed Key Detect

When the bit LE of the Configuration Register (08h) is set to "0", this function is disabled. When LE is set to "1", this function is enabled. When a key is pressed for a long period of time, the chip automatically scans again after the $\overline{INT}$ is deasserted. When the key is still pressed, the $\overline{INT}$ asserts again and the key event is latched into the temporary key status registers. The scanning continues until all of the keys are released. The delay time between the $\overline{INT}$ deasserting to the next scan beginning is set by the Configuration Register (08h) bits LT.

Key Event Interrupt (INT)

Once there is key event code latched in the temporary key status registers, the device produces an interrupt signal to the MCU on the $\overline{INT}$ pin. When the $\overline{INT}$ is asserted, any keypad state changes are ignored. The $\overline{INT}$ will remain low until all of the key events are read, with one exception: When the Auto-Clear $\overline{INT}$ is enabled, if all of the key event data is not read before the programmed

time, the $\overline{INT}$ will return high after the programmed time. However the temporary key status registers will remain unchanged and the key event data may continue to be read until another key event is detected. After all of the key events have been read, the device returns to standby mode waiting for the next scan.

Auto-Clear INT Function

When the ACI bits of the Configuration Register (08h) are set to "01" or "10", this function is enabled. Setting the ACI bits to "00" disables the function. When enabled, the $\overline{INT}$ would be cleared in 5ms or 10ms after it asserts if there is no read of the Key Status Register. The data in the temporary key status registers does not change when the $\overline{INT}$ goes low. The Key Status Register can be read regardless of whether the $\overline{INT}$ is high or not. However, when the $\overline{INT}$ is cleared and there is new key event activity before the old key event data is read, the temporary key status registers are rewritten and the $\overline{INT}$ asserts again. In this case, the previous key event data is lost and only the new key event(s) can be read.

The Input Port Filter

The bit DE of the Configuration Register (08h) is used to enable the input port filter. When DE is set to "0", the input port filter is disabled, and the chip responds to any changes at the input port. When DE is set to "1", the input port filter is enabled and any glitch shorter than 100ns is filtered. If the input pulse width is greater than 100ns, the chip responds (Figure 10).

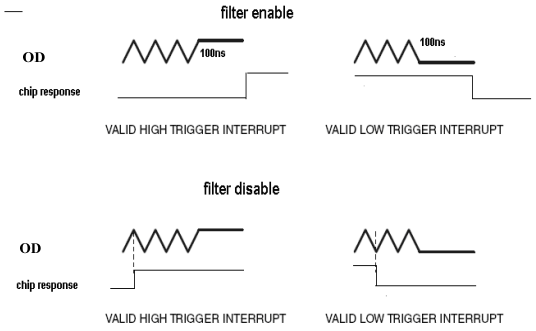


Figure 10 Input port debounce function

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

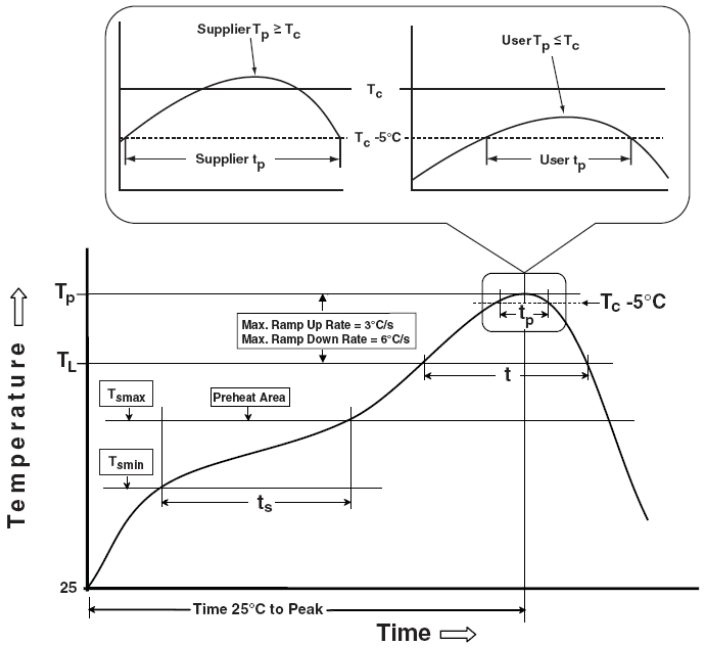
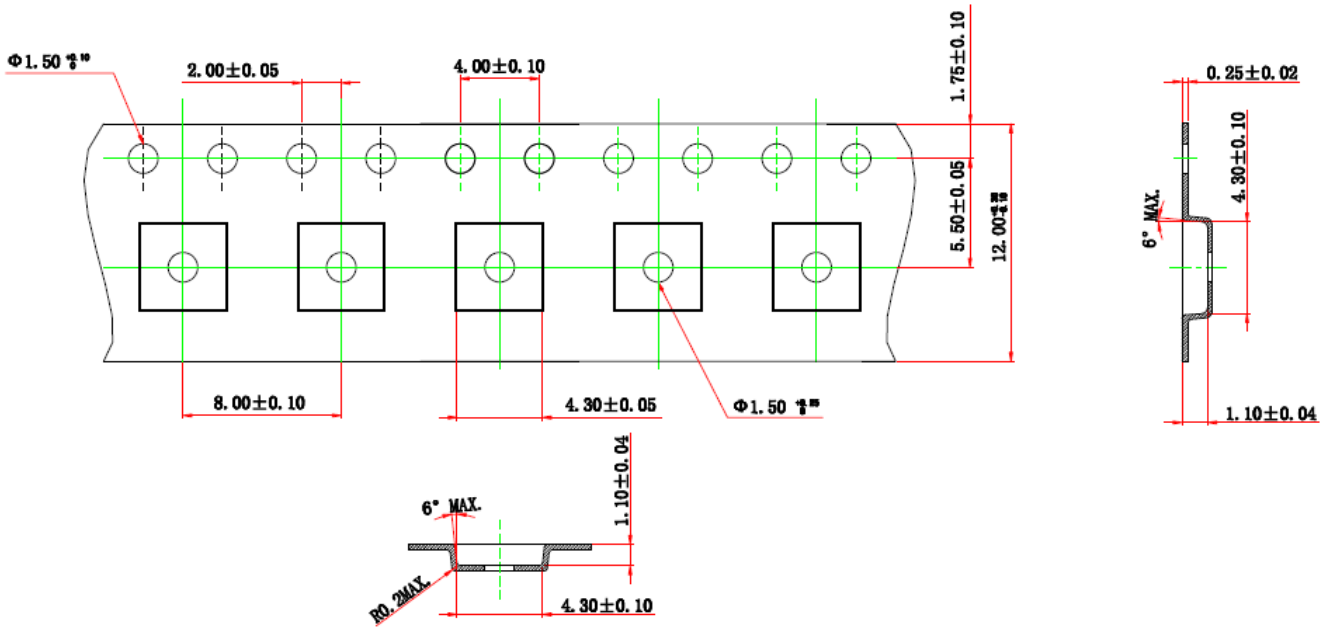


Figure 11 Classification profile

Tape and Reel Information



NOTES:[技术要求]:

1.CARRIER TAPE COLOR:BLACK[载带颜色为黑色]

2.COVER TAPE WIDTH:9.50±0.10 [配套9.5±0.10宽盖带]

3.COVER TAPE COLOR:TRANSPARENT[盖带颜色无色透明]

4. ANTISTATIC COATED 10^{8}~ 10^{11} OHMS/SQ.[单位面积表面阻抗为$10^{8}\Omega$/□~$10^{11}\Omega$/□]

5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.

[10个传送定位孔间距累积公差0.20MAX.]

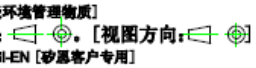
6.SUPPLIER:3M[供应商3M]

7.MOLD# WSFBP(4×4×0.75/0.85)[载带规格WSFBP(4×4×0.75/0.85)]

8.ALL DIMS IN mm.[所有单位为mm]

9.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.

[禁止使用长电科技规定的一级环境管理物质]

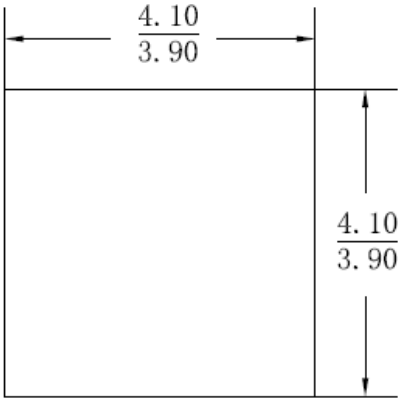
10.THE DERECTION OF VIEW:  。[视图方向:]

11.SPECIAL FOR CUSTOMER SI-EN [矽恩客户专用]

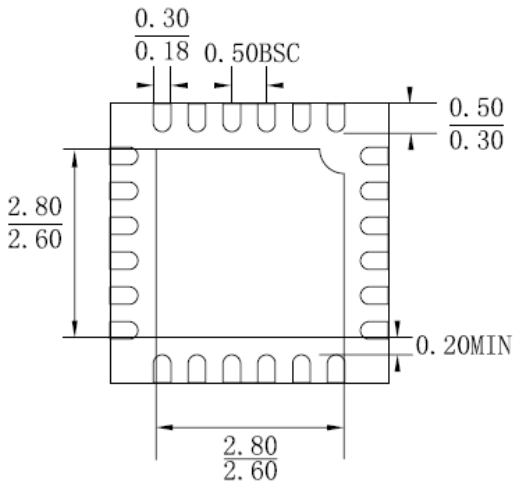
Package Information

WQFN-24

Bottom View



Top View



Side View