



**EDM1-CF-IMX6**

**REV. A2 – VER. 1.01**

**August 14, 2014**

## REVISION HISTORY

| Revision | Date             | Originator | Notes  |
|----------|------------------|------------|--|
| 0.90-rc3 | April 11, 2013   | TechNexion | Initial Public release candidate   |
| 0.90-rc4 | November 8, 2013 | TechNexion | Clarified Pin 76 and Pin 82  |
| 0.99     | December 6, 2013 | TechNexion | Clarified CAN Bus,<br>Added note SATA only<br>on i.MX6 Dual/Quad<br>configurations |
| 1.00     | January 22, 2014 | TechNexion | added table for<br>WiFi/Bluetooth signals  |
| 1.01     | August 14, 2014  | TechNexion | Add additional<br>alternatives for eMMC,<br>DDR3                                   |

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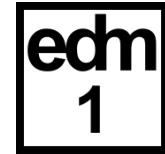
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## 1. Introduction

### 1.1. General Introduction

The EDM1-CF-IMX6 is a high performance highly integrated EDM type 1 System-on-Module designed around the Freescale i.MX6 Multicore ARM Cortex-A9. The EDM1-CF-IMX6 provides an ideal building block that easily integrates with a wide range of target markets requiring rich multimedia functionality, powerful graphics and video capabilities, as well as high-processing power, compact, cost effective and with low power consumption.



The EDM1-CF-IMX6 System-on-Module is typically being used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, Gigabit Ethernet and display interfaces are concentrated on the module. The modules are used with application specific carrier boards that implement other features such as audio CODECs, touch controllers, sensors and etcetera.

The modular approach offered by the EDM standard gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

## 1.2. General Care and Maintenance

Your device is a product of superior design and craftsmanship and should be treated with care.

The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

Regulatory information



Disposal of Waste Equipment by Users in Private Household in the European Union  
This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.



We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

## TechNexion Ltd.

17F-1 No. 16 Jian Ba Road  
Chung Ho City, 23511, Taipei, Taiwan R.O.C.  
Phone : +886-2-8227 3585  
Fax : +886-2-8227 3590

### The Compliance of RoHS /REACH

We warrant that all the materials, products and components which provided by TechNexion to customer comply according directive EU RoHS (2002/95/EC), RoHS II amendment, REACH (1907/2006/ED) SVHC and Annex 17, JIG-101, as follows:

|                           |                 |
|---------------------------|-----------------|
| Cadmium (Cd)              | : Under 100ppm  |
| Lead (Pb)                 | : Under 1000ppm |
| Mercury (Hg)              | : Under 1000ppm |
| Hexavalent Chromium (Cr6) | : Under 1000ppm |
| PBB                       | : Under 1000ppm |
| PBDE (include DecaBDE)    | : Under 1000ppm |

### RoHS Compliance Statement

We are aware of above directive and our product can meet the specification requirements above.



Company Stamp



Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15  
This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

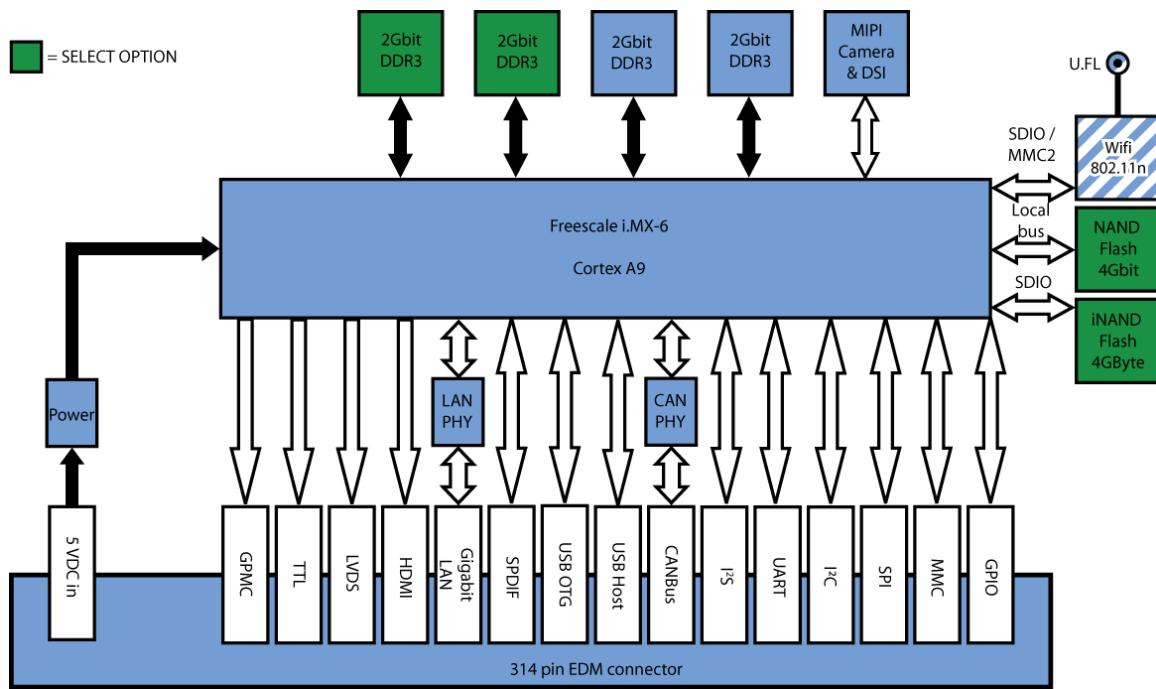
- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a different circuit from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help.



**WARNING!** To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

### 1.3. Block Diagram

Figure 1 - EDM1-CF-IMX6 Block Diagram

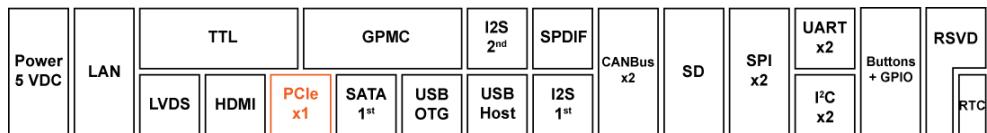


## 1.4. EDM Compatibility

The EDM1-CF-IMX6 is fully compatible with the EDM Type 1 Standard specifications.

For additional details, please refer to the “EDM Standard Specifications”.

**Figure 2 – EDM Type 1 Compatibility Chart**



**Table 1 - EDM Compatibility Overview**

| Interface        | Description  |
|------------------|--|
| LAN              | 1 Gigabit Ethernet   |
| LVDS             | 1 single channel 18/24 bit   |
| HDMI             | 1 HDMI ver.1.4 compatible  |
| TTL Display      | 1 TTL 18/24 bit Display  |
| PCIe             | 1 Lane PCIe 2.0  |
| SATA             | 1 SATA II  |
| USB Host         | 1 USB 2.0 Host port  |
| USB OTG          | 1 USB 2.0 OTG port (possible to use in Host mode)  |
| GPMC             | 8 bit localbus interface with 4 chip selects   |
| I2S              | 2 Independent I <sup>2</sup> S interfaces  |
| SPDIF            | 1 S/P DIF interface  |
| CAN Bus          | 2 FlexCAN CAN 2.0B protocol compliant interfaces   |
| UART             | 2 UART 4 wire  |
| SDIO             | 1 SDIO interface 4 bit   |
| SPI              | 2 SPI interfaces with 2 chip selects   |
| I <sup>2</sup> C | 2 independent general purpose interfaces<br>1 dedicated towards display/system functions |
| GPIO             | 10 dedicated GPIO's available  |
| RTC              | On carrierboard  |

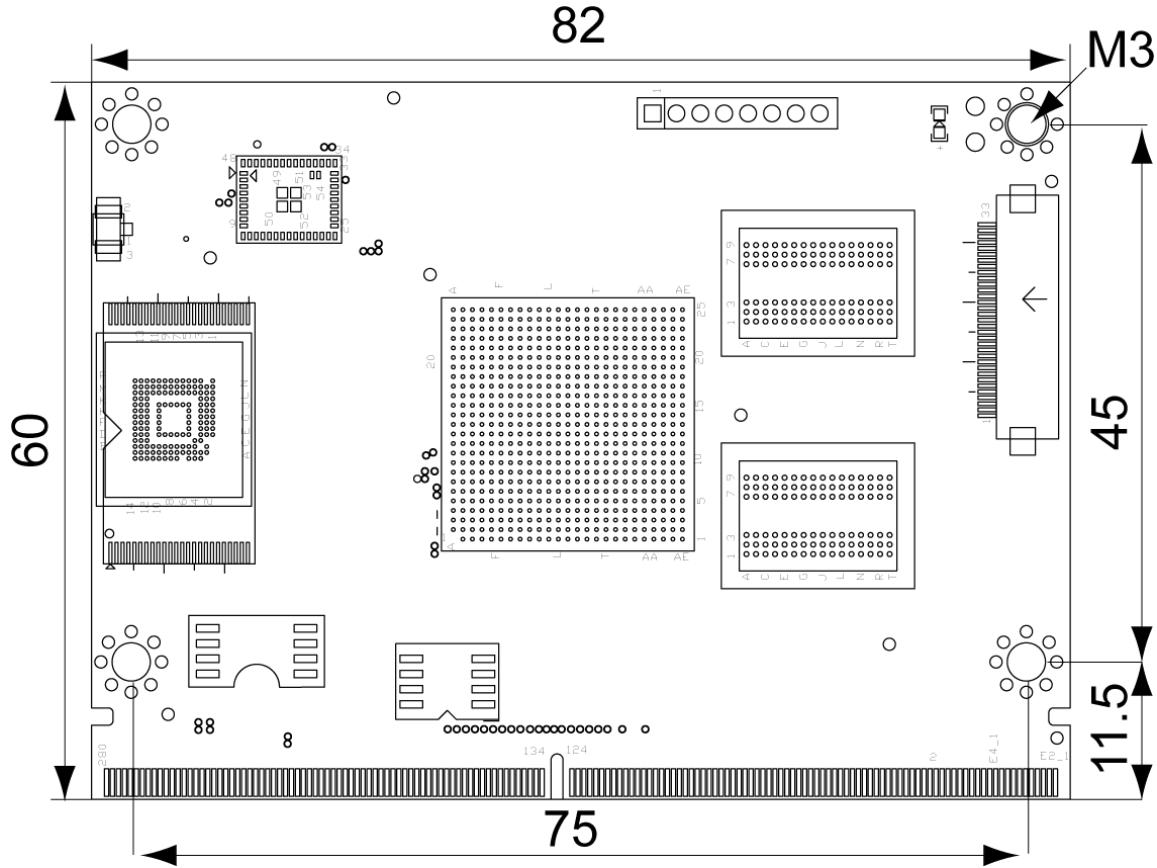
## 1.5. Dimensional Drawing

The EDM1-CF-IMX6 is an EDM Type 1 Compact Form Factor System-on-Module and follows the EDM Standard Specifications in regards of dimensions and mounting options.

2D and 3D files can be obtained from the [www.technexion.com](http://www.technexion.com) homepage.

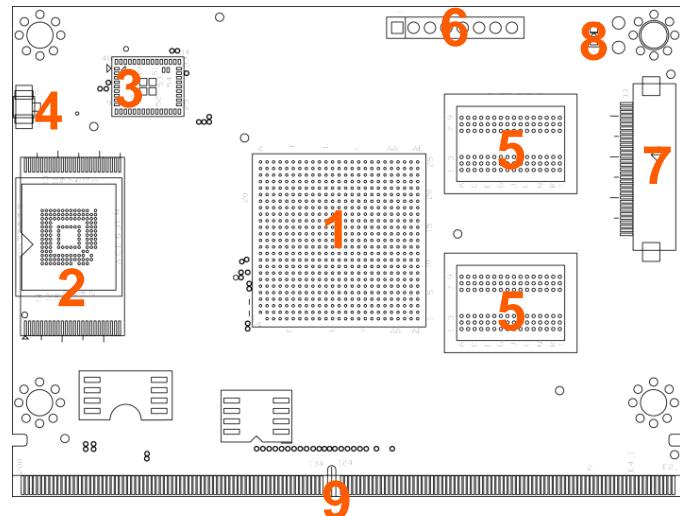
For additional details, please refer to the “EDM Standard Specifications”.

**Figure 3 - EDM1-CF-IMX6 Dimensional Drawing**



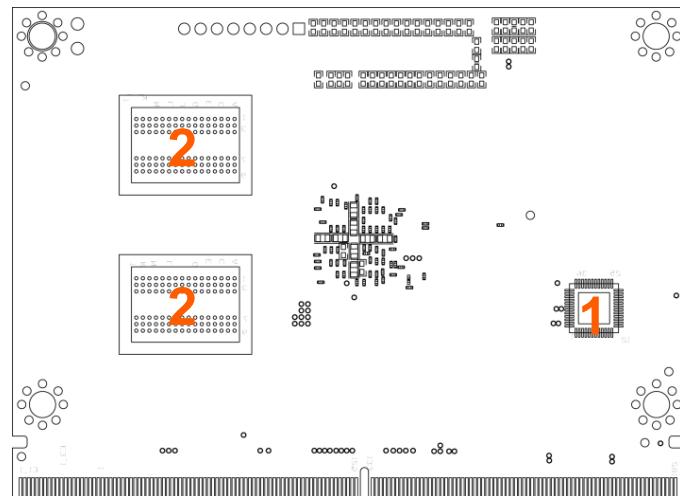
## 1.6. Component Location

**Figure 4 - EDM1-CF-IMX6 Top view**



| Item | Description                   | Item | Description                     |
|------|-------------------------------|------|---------------------------------|
| 1    | Freescale i.MX6 Processor     | 6    | JTAG Interface                  |
| 2    | NAND Flash / eMMC (co-layout) | 7    | MIPI Camera / Display Connector |
| 3    | BCM4330 WiFi/Bluetooth IC     | 8    | Power LED                       |
| 4    | Antenna connector             | 9    | EDM Type 1 Connector            |
| 5    | Memory IC (2)                 |      |                                 |

**Figure 5 - EDM1-CF-IMX6 Bottom view**



| Item | Description                         | Item | Description   |
|------|-------------------------------------|------|---------------|
| 1    | Atheros AR8031 Gigabit Ethernet PHY | 2    | Memory IC (2) |

## 1.7. Product Ordering Part Numbers

The EDM1-CF-IMX6 is available in a number of standard configurations. Custom tailored versions with other memory configuration, de-population of interfaces or extended and industrial temperature options are available upon request.

### 1.7.1 Standard Part Numbers

Standard EDM1-CF-IMX6 System-on-Modules part numbers can be ordered in multiples of 10 units in the following configurations.

#### Standard Part numbers featuring Freescale i.MX6 Solo

| Part Number                | Description  |
|----------------------------|--|
| EDM1CFIMX6S10R512NI4GL2C   | EDM Compact Type 1 Freescale i.MX6 Solo 1Ghz + 512MB RAM + 4GB eMMC + Gigabit LAN + 2 CAN                                    |
| EDM1CFIMX6S10R512NI4GBWL2C | EDM Compact Type 1 Freescale i.MX6 Solo 1Ghz + 512MB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + <b>802.11bgn + Bluetooth 4.0</b> |

#### Standard Part numbers featuring Freescale i.MX6 Duallite

| Part Number                | Description  |
|----------------------------|--|
| EDM1CFIMX6U10R1GBNI4GL2C   | EDM Compact Type 1 Freescale i.MX6 Duallite 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN                                    |
| EDM1CFIMX6U10R1GBNI4GBWL2C | EDM Compact Type 1 Freescale i.MX6 Duallite 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + <b>802.11bgn + Bluetooth 4.0</b> |

#### Standard Part numbers featuring Freescale i.MX6 Dual

| Part Number                 | Description   |
|-----------------------------|---|
| EDM1CFIMX6D10R1GBNI4GLS2C   | EDM Compact Type 1 Freescale i.MX6 Dual 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA                                    |
| EDM1CFIMX6D10R1GBNI4GBWSL2C | EDM Compact Type 1 Freescale i.MX6 Dual 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA + <b>802.11bgn + Bluetooth 4.0</b> |

#### Standard Part numbers featuring Freescale i.MX6 Quad

| Part Number                 | Description   |
|-----------------------------|---|
| EDM1CFIMX6Q10R2GBNI4GLS2C   | EDM Compact Type 1 Freescale i.MX6 Quad 1Ghz + 2GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA                                    |
| EDM1CFIMX6Q10R2GBNI4GBWLS2C | EDM Compact Type 1 Freescale i.MX6 Quad 1Ghz + 2GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA + <b>802.11bgn + Bluetooth 4.0</b> |

NOTE: For a complete overview of available evaluation kits. Please refer to chapter 5. Development Kits, Proto-type Components and Accessories of this hardware manual.

### 1.7.2. Custom Part Number Creation Rules

The EDM1-CF-IMX6 can be ordered in custom tailored to meet special application requirements and conditions according to the following custom part number creation rules.

Custom part numbers carry minimum order quantities. Please connect with your TechNexion distributor or account manager for conditions and availability.

Part number format:

**EDM1-CF-IMX6Q10-R2GB-NI4G-BW-L-S-2C-xx-xxxx**

| Interface           | Code | Description   |
|---------------------|------|---|
| Processor           | S    | i.MX6 Solo  |
|                     | U    | i.MX6 Duallite  |
|                     | D    | i.MX6 Dual  |
|                     | Q    | i.MX6 Quad  |
| Processor speed     | 08   | 800 Mhz   |
|                     | 10   | 1 Ghz (Default)   |
|                     | 12   | 1.2 Ghz   |
| Memory              | R512 | 512 MB DDR3   |
|                     | R1GB | 1GB DDR3  |
|                     | R2GB | 2GB DDR3  |
| Storage             | NI4G | eMMC 4GB (Default)  |
|                     | NIxG | Other capacities of eMMC are possible (8GB, 16GB, 32GB, 64GB)                   |
|                     | N512 | 512 MB NAND Flash IC  |
|                     | Nxxx | NAND Flash IC other capacity (1GB, 2GB)   |
| Network             | -    | No  |
|                     | L    | Gigabit Ethernet interface (Default)  |
| Wireless Networking | -    | No  |
|                     | BW   | 802.11bgn + Bluetooth 4.0 (optional)  |
| SATA                | -    | No  |
|                     | S    | Only available on i.MX6 Dual/Quad configurations (Default)                      |
| CAN Bus             | -    | No  |
|                     | 2C   | 2 CAN Bus interfaces (Default)  |
| Temperature Range   | -    | Commercial Temperature range (0~60°C) (Default)                                 |
|                     | TE   | Extended Temperature range (-20~70°C)   |
|                     | TI   | Industrial Temperature range (-40~85°C)   |
|                     | TEC  | Certified Extended Temperature range (-20~70°C)                                 |
|                     | TIC  | Certified Industrial Temperature range (-40~85°C)                               |
| Custom ID           | XXXX | Custom Partnumber ID for customized software loader and special component (BOM) |

NOTE: Wireless Networking option is not available in “TI” Industrial Temperature Range.

NOTE: eMMC storage is not available in “TI” Industrial Temperature Range. If onboard storage is required a NAND Flash IC should be selected.

## 2. Core Components

### 2.1. Freescale i.MX6 Cortex-A9 Multi-core Processor

The Freescale i.MX6 processor is an implementation of the Single/Dual/Quad ARM Cortex™-A9 core, which operates at frequencies up to 1.2 GHz. The i.MX6 provides a variety of interfaces and supports the following main features:

- Single / Dual / Quad Core ARM Cortex™-A9. Core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor
- Level 2 Cache—Unified instruction and data (up to 1 MByte)
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- NEON MPE coprocessor:
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
- Integrated Power Management unit:
  - Temperature Sensor for monitoring the die temperature
  - DVFS techniques for low power modes
  - Flexible clock gating control scheme
- Multimedia Hardware Accelerators

**Figure 6 – Freescale i.MX6 Processor Blocks**

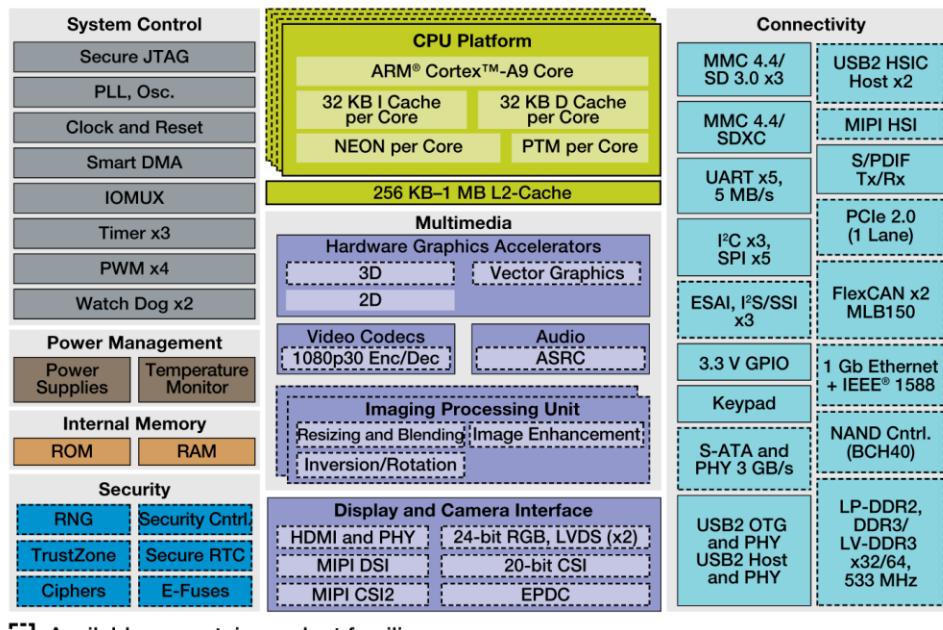


Figure 7 – Freescale i.MX6 Processor Scalability Overview (Solo/DualLite/Dual/Quad)

Red indicates change from column to the left

| i.MX6Solo  | i.MX6DualLite  | i.MX6Dual   | i.MX6Quad   |
|--|--|---|---|
| <ul style="list-style-type: none"> <li>Single ARM Cortex-A9 up to 1.0 GHz</li> <li><b>512 KB L2 cache, Neon, VFPv16 Trustzone</b></li> <li><b>3D graphics with one shader</b></li> <li>2D graphics</li> <li>32-bit DDR3 and LPDDR2 at 400 MHz</li> <li>Integrated EPD controller</li> <li><b>HDMIv1.4 controller plus PHY</b></li> <li><b>LVDS controller plus PHY</b></li> <li><b>PCIe controller plus PHY</b></li> <li><b>MLB and FlexCan controllers</b></li> </ul>  | <ul style="list-style-type: none"> <li>Dual ARM Cortex-A9 up to 1.0 GHz</li> <li>512 KB L2 cache, Neon, VFPv16 Trustzone</li> <li>3D graphics with one shader</li> <li>2D graphics</li> <li><b>64-bit DDR3 and 2-channel 32-bit LPDDR2 at 400 MHz</b></li> <li>Integrated EPD controller</li> <li><b>HDMIv1.4 controller plus PHY</b></li> <li><b>LVDS controller plus PHY</b></li> <li><b>PCIe controller plus PHY</b></li> <li><b>MLB and FlexCan controllers</b></li> </ul>  | <ul style="list-style-type: none"> <li>Dual ARM Cortex-A9 up to <b>1.2 GHz</b></li> <li><b>1 MB L2 cache, Neon, VFPv16 Trustzone</b></li> <li>3D graphics with <b>four shaders</b></li> <li><b>Two 2D graphics engines</b></li> <li>64-bit DDR3 and 2-channel 32-bit LPDDR2 at <b>533 MHz</b></li> <li>Integrated <b>SATA-II</b></li> <li><b>HDMIv1.4 controller plus PHY</b></li> <li><b>LVDS controller plus PHY</b></li> <li><b>PCIe controller plus PHY</b></li> <li><b>MLB and FlexCan controllers</b></li> </ul>  | <ul style="list-style-type: none"> <li><b>Quad ARM Cortex-A9 up to 1.2 GHz</b></li> <li>1 MB L2 cache, Neon, VFPv16 Trustzone</li> <li>3D graphics with four shaders</li> <li>Two 2D graphics engines</li> <li>64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz</li> <li>Integrated SATA-II</li> <li>HDMIv1.4 controller plus PHY</li> <li>LVDS controller plus PHY</li> <li>PCIe controller plus PHY</li> <li>MLB and FlexCan controllers</li> </ul>  |
|     |     |     |      |

### 2.1.1. i.MX6 Memory Interfaces

- The memory system consists of the following components:
  - Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
  - Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
  - Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 16-bit, 32-bit, and 64-bit DDR3-1066 and LV-DDR3-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size,
  - BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 32 bit.

### 2.1.2. i.MX6 DMA Engine

The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:

- Powered by a 16-bit Instruction-Set micro-RISC engine
- Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels
- 48 events with total flexibility to trigger any combination of channels
- Memory accesses including linear, FIFO, and 2D addressing
- Shared peripherals between ARM and SDMA
- Very fast Context-Switching with 2-level priority based preemptive multi-tasking
- DMA units with auto-flush and prefetch capability
- Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)
- DMA ports can handle unit-directional and bi-directional flows (copy mode)
- Up to 8-word buffer for configurable burst transfers
- Support of byte-swapping and CRC calculations
- Library of Scripts and API is available

### 2.1.3. i.MX6 Video and Graphics Subsystems

The EDM1-CF-IMX6 video graphics subsystem consists of the following i.MX6 sub-blocks.

- VPU: A multi-standard high performance video codec engine supporting encode/decode operations of the following:
  - Decoding: H.264 BP/CBP/MP/HP, VC-1 SP/MP/AP, MPEG-4 SP/ASP, H.263 P0/P3, MPEG-1/2 MP, Divx (Xvid) HP/PP/HTP/HDP, VP8 (1280x720), AVS, H.264-MVC (1280x720), MJPEG BP (max. 8192x8192) up to full-HD 1920x1088 @30fps plus D1 @30fps.
  - Encoding: H.264 BP/CBP, MPEG-4 SP, H.263 P0/P3, MJPEG BP (max. 192x8192) up to full-HD 1920x1088@30fps.
- GPU2Dv2: Hardware acceleration of 2D graphics (Bit BLT and Stretch BLT). Based on the Vivante GC320 IP core.
- GPUVG: An OpenVG 1.1 Graphics Processing Unit providing hardware acceleration of vector graphics. Based on the Vivante GC355 IP core

Additionally the EDM1-CF-IMX6 incorporates the following 3D GPU engine

The EDM1-CF-IMX6 featuring an i.MX6 Dual or Quad processor:

- GPU3Dv4: A 3D GPU (Vivante GC2000), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

The EDM1-CF-IMX6 featuring an i.MX6 Duallite or Solo processor:

- GPU3Dv5: A 3D GPU (Vivante GC880), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.

## 2.2. Memory

The EDM1-CF-IMX6 integrates Double Data Rate III (DDR3) Synchronous DRAM in either a single (32 bit) or a dual (64 bit) channel configuration.

The following memory chips have been validated and tested on the EDM1-CF-IMX6 System-on-Module:

### 2.2.1 SKHynix

SKHynix CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SKHynix DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

SK Hynix memory features:

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10 and 11, 13 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase of 0o C ~ 95 o C)
  - 7.8 µs at 0 o C ~ 85 o C
  - 3.9 µs at 85 o C ~ 95 o C
- Auto Self Refresh supported
- JEDEC standard 78ball FBGA(x4/x8), 96ball FBGA (x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

More information can be retrieved from SKHynix:

Part number:

H5TQ2G63FFR-PBC preferred part 2Gbit  
H5TQ2G63DFR-H9C backup part 2Gbit

H5TQ4G63FFR-PBC preferred part 4Gbit  
H5TQ4G63DFR-H9C backup part 4Gbit

## 2.2.2. Micron

Micron 1.35V DDR3L SDRAM device is a low-voltage version of the 1.5V DDR3 SDRAM device. Unless stated otherwise, the DDR3L SDRAM device meets the functional and timing specifications listed in the equivalent density standard or automotive DDR3 SDRAM data sheet located on [www.micron.com](http://www.micron.com).

Micron memory features:

- VDD = VDDQ = 1.35V (1.283–1.45V)
- Backward-compatible to VDD = VDDQ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- TC of 0°C to +95°C
  - 64ms, 8192-cycle refresh at 0°C to +85°C
  - 32ms at +85°C to +95°C
- Self refresh temperature (SRT)

More information can be retrieved from Micron:

Part number:

MT41K128M16JT-125 IT:K for general configurations 2Gbit

MT41K256M16HA-125 IT:E for general configurations 4Gbit

## 2.3. eMMC Storage

The EDM1-CF-IMX6 can be ordered with onboard eMMC storage in different configurations and capacity.

The onboard eMMC device is connected on the SD3 pins of the i.MX6 processor in a 8 bit width configuration.

The following eMMC chips have been validated and tested on the EDM1-CF-IMX6 System-on-Module:

### 2.3.1. Sandisk iNAND SDIN7DP2

iNAND Ultra is an Embedded Flash Drive (EFD) designed for mobile handsets and consumer electronic devices. iNAND Ultra is a hybrid device combining an embedded thin flash controller and standard MLC NAND flash memory, with an industry standard e.MMC 4.511 interface. Empowered with a new e.MMC4.51 feature set such as Power Off Notifications and Packed commands, as well as legacy e.MMC4.41 features such as Boot and RPMB partitions, HPI, and HW Reset the iNAND Ultra e.MMC is the optimal device for reliable code and data storage.

iNAND provides mass storage of up to 128GB in JEDEC compatible form factors, with low power consumption and high performance.

In addition to the high reliability and high system performance, it offers plug-and-play integration and support for multiple NAND technology transitions, as well as features such as advanced power management scheme.

iNAND Ultra uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by embedded flash management software running as firmware on the flash controller.

The architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-levelling, and automatic block management to ensure high data reliability and maximize flash life expectancy.

SanDisk iNAND Extreme, with MMC interface, features include the following:

- Memory controller and NAND flash
- Complies with e.MMC Specification Ver. 4.512
- Mechanical design complies with JEDED MO-276C Specification
- Offered in two TFBGA packages of e.MMC 4.513
- Operating temperature range: -25C° to +85C°
- Dual power system
- Core voltage (VCC) 2.7-3.6v
- I/O (VCCQ) voltage 2.7-3.6v
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed)
- Up to 104 MB/sec bus transfer rate, using 8 parallel data lines at 52 MHz, DDR Mode
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage

More information can be retrieved from Kingston:

Part number:  
SDIN7DP2 for general configurations

### 2.3.2. Kingston KE4CN2H5A

Kingston e•MMC™ products follow the JEDEC e•MMC™ 4.5 standard. It is an ideal universal storage solutions for many electronic devices, including smartphones, tablet PCs, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. E•MMC™ encloses the MLC NAND and e•MMC™ controller inside as one JEDEC standard package, providing a standard interface to the host. The e•MMC™ controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

The Kingston NAND Device is fully compatible with the JEDEC Standard Specification No.JESD84-B45. This datasheet describes the key and specific features of the Kingston e•MMC™ Device. Any additional information required interfacing the Device to a host system and all the practical methods for device detection and access can be found in the proper sections of the JEDEC Standard Specification.

Kingston e•MMC™, with MMC interface, features include the following:

- Packaged NAND flash memory with e•MMC™ 4.5 interface
- Compliant with e•MMC™ Specification Ver.4.4, 4.41 & 4.5
- Bus mode
  - High-speed e•MMC™ protocol
  - Provide variable clock frequencies of 0-200MHz.
  - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset.
- Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate : up to 200Mbyte/s @ HS200(Host clock @ 200MHz)
  - Dual data rate : up to 104Mbyte/s @ 52MHz
- Supports (Alternate) Boot Operation Mode to provide a simple boot sequence method
- Supports SLEEP/AWAKE (CMD5).
- Host initiated explicit sleep mode for power saving
- Enhanced Write Protection with Permanent and Partial protection options
- Supports Multiple User Data Partition with Enhanced User Data Area options
- Supports Background Operations & High Priority Interrupt (HPI)
- Supports enhanced storage media feature for better reliability
- Operating voltage range :
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Support secure bad block erase commands
  - Enhanced write Protection with permanent and partial protection options

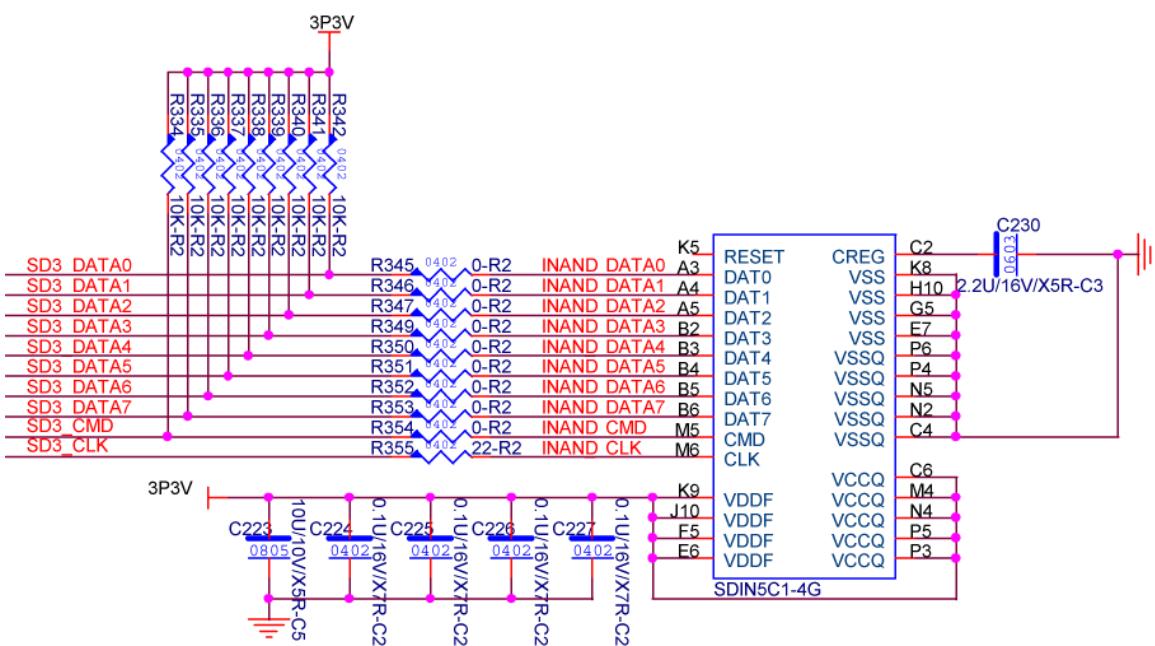
More information can be retrieved from Kingston:

Part number:

KE4CN2H5A for general configurations

**Table 2 - eMMC Signal Description**

| i.MX6 BALL | PAD NAME | Signal     | V         | I/O | Description         |
|------------|----------|------------|-----------|-----|---------------------|
| E14        | SD3_DAT0 | eMMC_DATA0 | CMOS 3.3V | I/O | MMC/SDIO Data bit 0 |
| F14        | SD3_DAT1 | eMMC_DATA1 | CMOS 3.3V | I/O | MMC/SDIO Data bit 1 |
| A15        | SD3_DAT2 | eMMC_DATA2 | CMOS 3.3V | I/O | MMC/SDIO Data bit 2 |
| B15        | SD3_DAT3 | eMMC_DATA3 | CMOS 3.3V | I/O | MMC/SDIO Data bit 3 |
| D13        | SD3_DAT4 | eMMC_DATA4 | CMOS 3.3V | I/O | MMC/SDIO Data bit 4 |
| C13        | SD3_DAT5 | eMMC_DATA5 | CMOS 3.3V | I/O | MMC/SDIO Data bit 5 |
| E13        | SD3_DAT6 | eMMC_DATA6 | CMOS 3.3V | I/O | MMC/SDIO Data bit 6 |
| F13        | SD3_DAT7 | eMMC_DATA7 | CMOS 3.3V | I/O | MMC/SDIO Data bit 7 |
| B13        | SD3_CMD  | eMMC_CMD   | CMOS 3.3V | I/O | MMC/SDIO Command    |
| D14        | SD3_CLK  | eMMC_CLK   | CMOS 3.3V | O   | MMC/SDIO Clock      |

**Figure 8 - eMMC Schematics**

## 2.4. NAND Flash Storage

The EDM1-CF-IMX6 can be ordered with onboard NAND Flash storage in different configurations and capacity.

The following NAND Flash chips have been validated and tested on the EDM1-CF-IMX6 System-on-Module:

### 2.4.1. Samsung K9F2G08U0B

Offered in 256Mx8bit, the K9F2G08X0B is a 2G-bit NAND Flash Memory with spare 64M-bit. Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 200 $\mu$ s on the (2K+64)Byte page and an erase operation can be performed in typical 1.5ms on a (128K+4K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F2G08X0B's extended reliability of 100K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm. The K9F2G08X0B is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

Features:

- Voltage Supply 3.3V device(K9F2G08U0B): 2.70V ~ 3.60V
- Organization
  - Memory Cell Array : (256M + 8M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read : 25 $\mu$ s(Max.)
  - Serial Access : 25ns(Min.)
- Fast Write Cycle Time
  - Page Program time : 200 $\mu$ s(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles(with 1bit/528Byte ECC)
  - Data Retention : 10 Years
- Command Driven Operation
- Unique ID for Copyright Protection

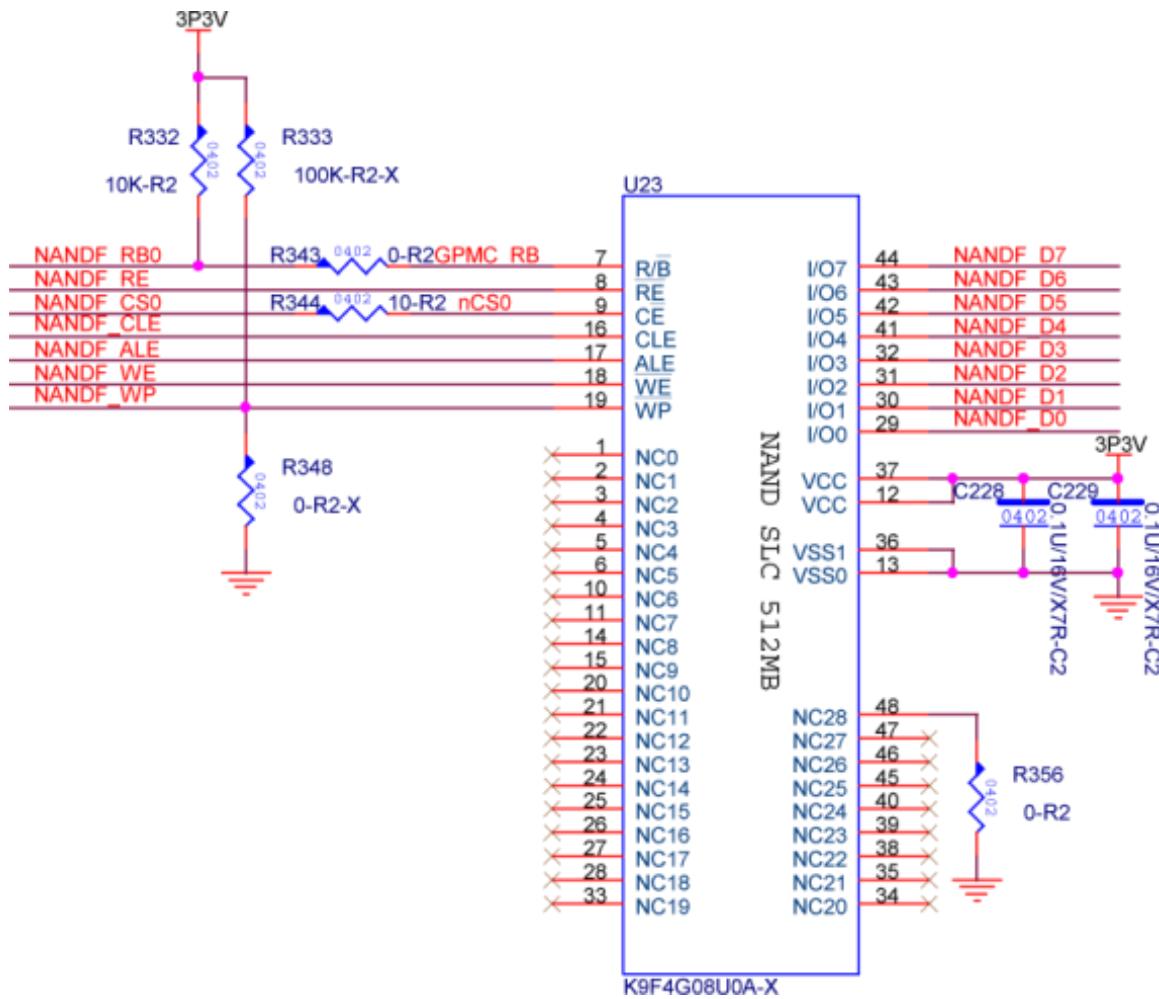
More information can be retrieved from Samsung:

Part number:  
K9F2G08U0B for general configurations

**Table 3 - NAND Signal Description**

| i.MX6 BALL | PAD NAME   | Signal | V         | I/O | Description  |
|------------|------------|--------|-----------|-----|--|
| A18        | NANDF_D0   | I/O0   | CMOS 3.3V | I/O | GPMC data bit 0  |
| C17        | NANDF_D1   | I/O1   | CMOS 3.3V | I/O | GPMC data bit 1  |
| F16        | NANDF_D2   | I/O2   | CMOS 3.3V | I/O | GPMC data bit 2  |
| D17        | NANDF_D3   | I/O3   | CMOS 3.3V | I/O | GPMC data bit 3  |
| A19        | NANDF_D4   | I/O4   | CMOS 3.3V | I/O | GPMC data bit 4  |
| B18        | NANDF_D5   | I/O5   | CMOS 3.3V | I/O | GPMC data bit 5  |
| E17        | NANDF_D6   | I/O6   | CMOS 3.3V | I/O | GPMC data bit 6  |
| C18        | NANDF_D7   | I/O7   | CMOS 3.3V | I/O | GPMC data bit 7  |
| B16        | NANDF_RB0  | RB     | CMOS 3.3V | I   | External indication of wait                                |
| B17        | SD4_CMD    | RE     | CMOS 3.3V | O   | GPMC Read Enable   |
| F15        | NANDF_CS0  | CS     | CMOS 3.3V | I/O | GPMC Chip Select 0   |
| C15        | NANDF_CLE  | CLE    | CMOS 3.3V | O   | GPMC Lower Byte Enable. Also used for Command Latch Enable |
| A16        | NANDF_ALE  | ALE    | CMOS 3.3V | O   | GPMC Address Valid or Address Latch Enable                 |
| E16        | SD4_CLK    | WE     | CMOS 3.3V | I   | GPMC Write Enable  |
| E15        | NANDF_WP_B | WP     | CMOS 3.3V | O   | GPMC Write Protect / Enable                                |

NOTE: On configurations where NAND Flash is mounted instead of eMMC, EDM PIN# 86 is not connected.

**Figure 9 - NAND IC Schematics**

## 2.5. Broadcom BCM4330 WiFi/Bluetooth SIP Module

The EDM1-CF-IMX6 can be ordered with an optional onboard WiFi/Bluetooth SIP module. The 802.11b/g/n + BT SIP module is a small sized BGA mounted module that provides full function of 802.11b/g/n (draft n) and Bluetooth class 4.0 +HS

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded 802.11b/g/n Wi-Fi + Bluetooth features.

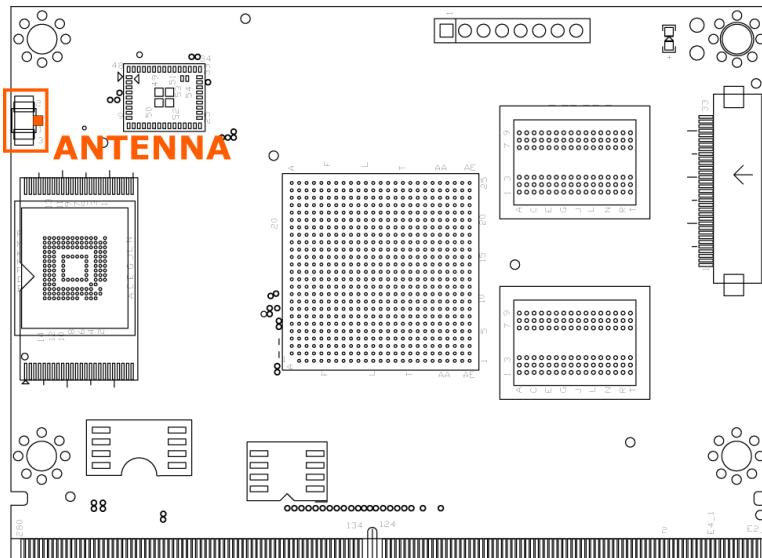
The SIP module is based on Broadcom 4330 chipset which is a WiFi + BT SOC. The Radio architecture & high integration MAC/BB chip provide excellent sensitivity with rich system performance.

In addition to WEP 64/128, WPA and TKIP, AES, CCX is supported to provide the latest security requirement on your network.

The SIP module is designed to operate with a single antenna for WiFi and Bluetooth to be connected to the U.FL connector available on the EDM1-CF-IMX6.

For the software and driver development, TechNexion provides extensive technical document and reference software code for the system integration under the agreement of Broadcom International Ltd.

**Figure 10 - EDM1-CF-IMX6 Antenna U.FL Connector Location**



**Table 4 - BCM4330 WiFi Signal Description**

| i.MX6 BALL | PAD NAME   | Signal         | I/O | Description   |
|------------|------------|----------------|-----|---|
| A22        | SD2_DAT0   | SDIO_D0        | I/O | MMC/SDIO Data bit 0   |
| E20        | SD2_DAT1   | SDIO_D1        | I/O | MMC/SDIO Data bit 1   |
| A23        | SD2_DAT2   | SDIO_D2        | I/O | MMC/SDIO Data bit 2   |
| B22        | SD2_DAT3   | SDIO_D3        | I/O | MMC/SDIO Data bit 3   |
| F19        | SD2_CMD    | SDIO_CMD       | I/O | MMC/SDIO Command  |
| C21        | SD2_CLK    | SDIO_CLK       | I/O | MMC/SDIO Clock  |
| W20        | ENET_TXD1  | SDIO_HOST_WAKE | I/O | General purpose interface pin. This pin is high-impedance on power up and reset. Subsequently, it becomes an input or output through software control. This pin has a programmable weak pull-up/down.               |
| W22        | ENET_RXD1  | WL_REG_ON      | I   | Used by PMU (OR-gated with BT_REG_ON) to power up or power down internal BCM4330 regulators used by the WLAN section. This pin is also a low-asserting reset for WLAN only (Bluetooth is not affected by this pin). |
| M4         | CSI0_DAT14 | WL_TRST_N      | I   | For normal operation, connect as described in the JTAG specification. Otherwise, if JTAG is not used, this pin can be left unconnected (NC) as it has an internal weak pull-up resistor.                            |

The BCM4330 can be completely powered down in software by using the following pin:

**Table 5 - BCM4330 General Power Control Signal**

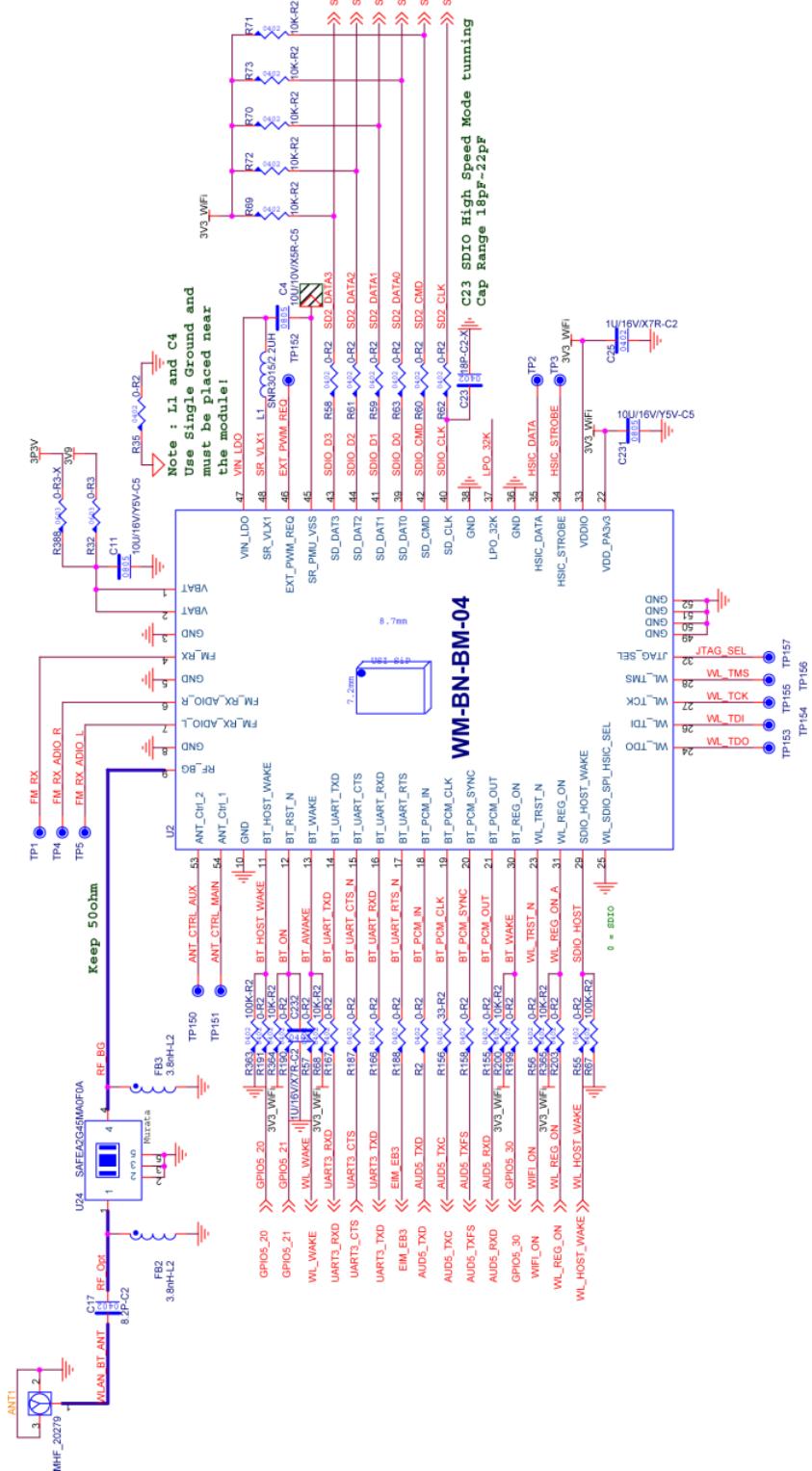
| i.MX6 BALL | PAD NAME   | Signal   | V         | Description                   |
|------------|------------|----------|-----------|-------------------------------|
| L1         | CSI0_DAT13 | GPIO5_31 | CMOS 3.3V | ON/OFF signal pin for BCM4330 |

**Table 6 - BCM4330 Bluetooth Signal Description**

| i.MX6 BALL | PAD NAME     | Signal       | I/O | Description  |
|------------|--------------|--------------|-----|--|
| A22        | UART3_TXD    | BT_UART_RXD  | I   | Bluetooth UART Serial Input. Serial data input for the HCI UART Interface  |
| E20        | UART3_RXD    | BT_UART_TXD  | O   | Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.   |
| A23        | UART3_CTS    | BT_UART_CTS  | I/O | Bluetooth UART Clear to Send. Active-low clear-to-send signal for the HCI UART interface.  |
| B22        | EIM_EB3      | BT_UART_RTS  | I/O | Bluetooth UART Request to Send. Active-low request-to-send signal for the HCI UART interface.  |
| V6         | KEY_ROW0     | BT_PCM_IN    | I   | PCM data input   |
| U6         | KEY_ROW1     | BT_PCM_OUT   | O   | PCM data output  |
| W5         | KEY_COL0     | BT_PCM_CLK   | I/O | PCM clock  |
| U7         | KEY_COL1     | BT_PCB_SYNC  | I/O | PCM sync signal  |
| U20        | ENET_TXD0    | BT_WAKE      | I   | Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention.<br>• Asserted: Bluetooth device must wake-up or remain awake.<br>• Desereted: Bluetooth device may sleep when sleep criteria are met.<br>The polarity of this signal is software configurable and can be asserted high or low. |
| N2         | CSI0_VSYNC   | BT_RST_N     | I   | Low asserting reset for BT core  |
| P3         | CSI0_DATA_EN | BT_HOST_WAKE | O   | Host UART wake up. Signal from the module to the host indicating that the module requires Attention.<br>• Asserted: Host device must wake-up or remain awake.<br>• Desereted: Host device may sleep when sleep criteria are met.<br>The polarity of this signal is software configurable and can be asserted high or low.                |
| M2         | CSI0_DAT12   | BT_REG_ON    | I   | Used by PMU (OR-gated with WL_REG_ON) to power up or power down internal BCM4330 regulators used by the BT section   |

NOTE: The BT\_PCM signals are shared with EDM I<sup>2</sup>S secondary signals (EDM PIN# 186, 188, 190, 192).

## **Figure 11 - WiFi / BT Schematics**



## 2.6. Atheros AR8031 Gigabit LAN

The EDM1-CF-IMX6 connects the i.MX6 processor RGMII interface to the Atheros AR8031 gigabit Ethernet chip.

The AR8031 is Atheros' 4th generation, single port, 10/100/1000 Mbps, Tri-speed Ethernet PHY. It supports both RGMII and SGMII interfaces to the MAC.

The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length.

The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

Features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Supports 1000 BASE-T PCS and auto-negotiation with next page support
- Supports RGMII and/or SGMII interfaces to MAC devices
- Supports Fibre and Copper combo mode when MAC interface works in RGMII mode
- Supports additional IEEE 1000 BASE-X and 100 BASE-FX with Integrated SerDes
- RGMII timing modes support internal delay and external delay on Rx path
- Supports Atheros Green ETHOS® power saving modes with internal automatic DSP power saving scheme
- Supports IEEE 802.3az (Energy Efficient Ethernet) n Supports SmartEEE which allows MAC/ SoC devices without 802.3az support to function as the complete 802.3az system
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Supports Synchronous Ethernet with selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of  $\pm 6$  kV
- Error-free operation over up to 140 meters of CAT5 cable
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Jumbo Frame support up to 10KB (full duplex)
- Multiple loopback modes for diagnostics
- Robust Surge Protection with  $\pm 750$  V/ differential mode and  $\pm 4$  kV/common mode
- Cable Diagnostic Test (CDT)

More information can be retrieved from Atheros:

Part number:

AR8031-AL1A for general configurations

AR8031-AL1B for industrial temperature configurations

**Table 7 - Gigabit Ethernet interconnect between i.MX6 and AR8031**

| i.MX6 BALL | PAD NAME     | Signal        | AR8031 PIN | Description                          |
|------------|--------------|---------------|------------|--------------------------------------|
| D21        | RGMII_TXC    | ETH_TXCLK     | 35         | RGMII transmit clock                 |
| C22        | RGMII_TD0    | ETH_RXD0      | 36         | RGMII transmit data 0                |
| F20        | RGMII_TD1    | ETH_RXD1      | 37         | RGMII transmit data 1                |
| E21        | RGMII_TD2    | ETH_RXD2      | 38         | RGMII transmit data 2                |
| A24        | RGMII_TD3    | ETH_RXD3      | 39         | RGMII transmit data 3                |
| C23        | RGMII_RX_CTL | ETH_RXEN      | 34         | RGMII transmit enable                |
| B25        | RGMII_RXC    | ETH_RXCLK     | 33         | RGMII receive clock                  |
| C24        | RGMII_RD0    | ETH_RXD0      | 31         | RGMII receive data 0                 |
| B23        | RGMII_RD1    | ETH_RXD1      | 30         | RGMII receive data 1                 |
| B24        | RGMII_RD2    | ETH_RXD2      | 28         | RGMII receive data 2                 |
| D23        | RGMII_RD3    | ETH_RXD3      | 27         | RGMII receive data 3                 |
| D22        | RGMII_RX_CTL | ETH_RXDV      | 32         | RGMII receive data valid             |
| V22        | ENET_REF_CLK | CLK_25M       | 25         | Synchronous Ethernet recovered clock |
| V21        | ENET_TX_EN   | ETH_INTn      | 5          | Ethernet interrupt output            |
| J19        | EIM_D29      | RST           | 2          | System reset                         |
| V20        | ENET_MDC     | ETH_MDIO_CLK  | 1          | Management data clock reference      |
| V23        | ENET_MDIO    | ETH_MDIO_DATA | 48         | Management data                      |

**Table 8 – EDM Gigabit Ethernet Signal Description**

| EDM Pin | Signal         | V         | I/O | Description  |
|---------|----------------|-----------|-----|--|
| E3_2    | GBE_MDI2+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal |
| E4_2    | GBE_MDI0+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal |
| E3_3    | GBE_MDI2-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal |
| E4_3    | GBE_MDI0-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal |
| E3_5    | GBE_MDI3+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal |
| E4_5    | GBE_MDI1+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal |
| E3_6    | GBE_MDI3-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal |
| E4_6    | GBE_MDI1-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal |
| E3_7    | LED1_ACT       | CMOS 3.3V | O   | Gigabit Ethernet LED Activity indicator  |
| E4_8    | LED1_nLink100  | CMOS 3.3V | O   | Gigabit Ethernet 100Mbit/sec LED link indicator                                      |
| E4_9    | LED1_nLink1000 | CMOS 3.3V | O   | Gigabit Ethernet 1000Mbit/sec LED link indicator                                     |

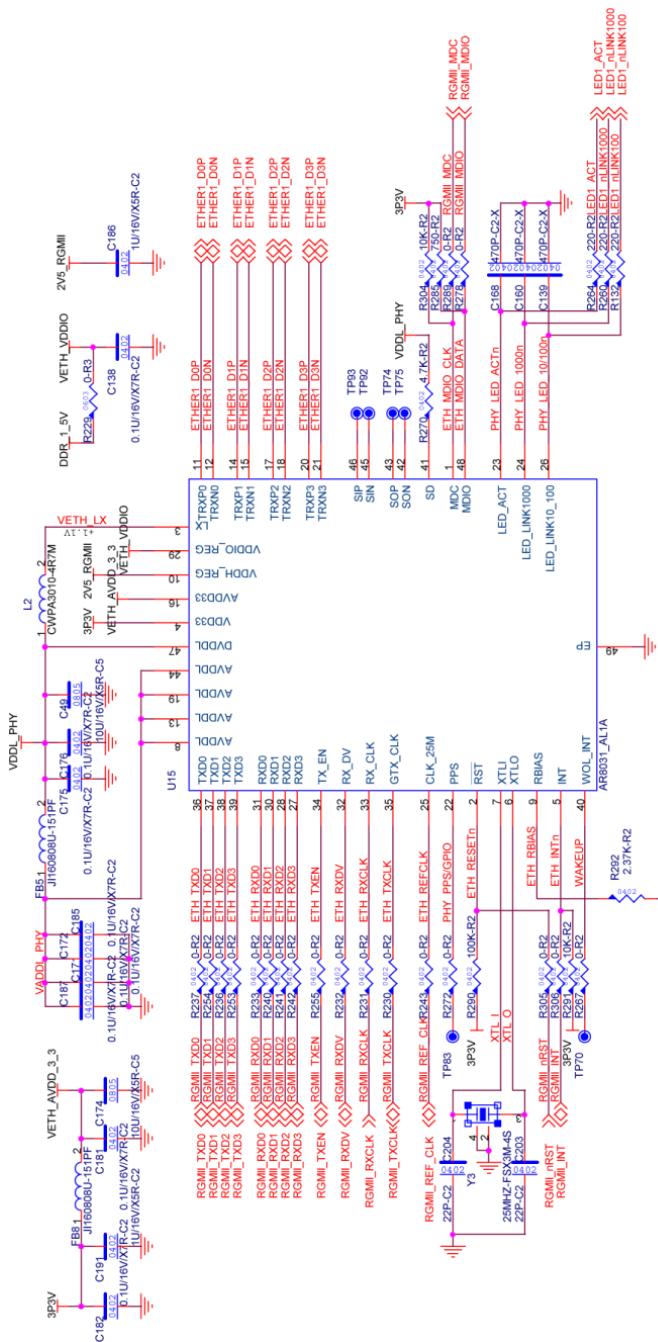
## 2.6.1. Gigabit Ethernet Magnetics

A Gigabit Ethernet coupling transformer either discrete or integrated inside a RJ45 jack should be integrated on the EDM carrier board.

The following table is a selection of compatible Ethernet PHY's available in the market that has been validated with the EDM1-CF-IMX6.

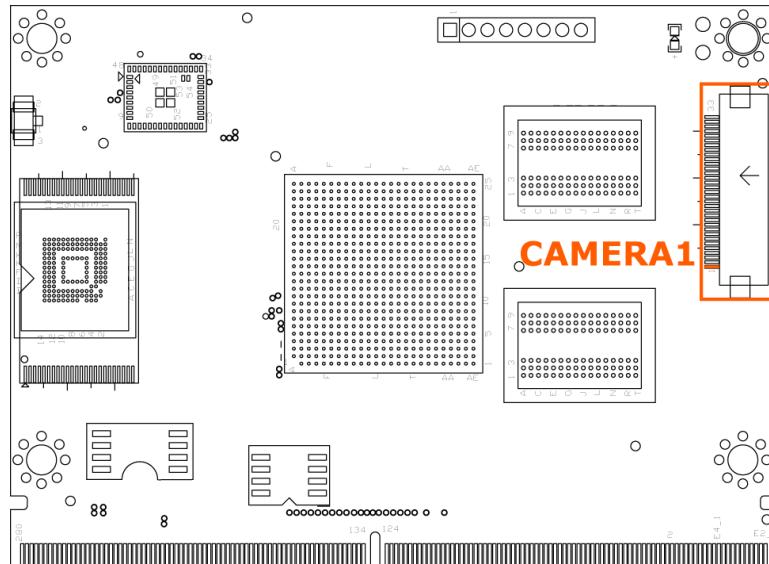
| Manufacturer      | Partnumber   | Technology       | Description   |
|-------------------|--------------|------------------|---|
| Pulse Engineering | H5007        | 10/100/1000BaseT | Discrete magnetics module                             |
| Pulse Engineering | JK0-0036     | 10/100/1000BaseT | RJ45 jack with integrated magnetics and activity LEDs |
| Bel Fuse          | S558-5999-P3 | 10/100/1000BaseT | Discrete magnetics module                             |
| Pulse             | JW0A1P01R-E  | 10/100/1000BaseT | RJ45 jack with integrated magnetics and USB jacks     |
| Foxconn           | UB11123-J51  | 10/100/1000BaseT | RJ45 jack with integrated magnetics and USB jacks     |

## **Figure 12 - Gigabit Ethernet Schematics**



## 2.7 MIPI Camera and Display Connector

The EDM1-CF-IMX6 expansion FPC connector carries the MIPI Serial Interface camera and display signals.



### 2.7.1 MIPI Camera

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 – 29 November 2005
- Supports up to 4 Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Supports all primary and secondary data formats:
- RGB, YUV and RAW color space definitions
- From 24-bit down to 6-bit per pixel
- Generic or user-defined byte-based data types

For additional details on MIPI-CSI and other relevant system blocks, please refer to chapters 18, 39 and 36.4.3.1 of the “i.MX6 Reference Manual”.

## 2.7.2 MIPI Display

The MIPI DSI Host Controller supports the following features:

IPU SIDE (input):

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008
- Fully Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29 November 2005.

Supported DBI types are:

- Type B
- 16bit, 9bit and 8bit Data bus width
- DBI and DPI interface can coexist (only one is operational at a time)
- Support all commands defined in MIPI Alliance Specification for Display Command Set (DCS), Version 1.02.00 - 23 July 2009

D-PHY side (output):

- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 2 D-PHY Data Lanes:
- Bidirectional Communication and Escape Mode Support through Data Lane 0.
- Programmable display resolutions, from 160x120(QVGA) to 1024x768(XVGA).
- Multiple Peripheral Support capability, configurable Virtual Channels.
- Video Mode Pixel Formats, 16bpp(RGB565), 18bpp(RGB666) packed, 18bpp(RGB666) loosely, 24bpp(RGB888).

For additional details, please refer to the “MIPI DSI Host Controller” chapter of the “i.MX6 Reference Manual”.

**Table 9 - MIPI Display and Camera Expansion Connector Signal Description**

| Pin # | i.MX6 PIN | PAD NAME  | Signal    | V         | I/O | Description  |
|-------|-----------|-----------|-----------|-----------|-----|--|
| 1     | F3        | CSI_CLK0P | CSI_CLK0P | CMOS 2.5V | I   | MIPI Camera Serial Interface clock pair positive signal  |
| 2     | F4        | CSI_CLK0M | CSI_CLK0M | CMOS 2.5V | I   | MIPI Camera Serial Interface clock pair negative signal  |
| 3     |           |           | GND       | GND       | P   | Ground   |
| 4     | E3        | CSI_D0P   | CSI_D0P   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 0 positive signal |
| 5     | E4        | CSI_D0M   | CSI_D0M   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 0 negative signal |
| 6     |           |           | GND       | GND       | P   | Ground   |
| 7     | D2        | CSI_D1P   | CSI_D1P   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 1 positive signal |
| 8     | D1        | CSI_D1M   | CSI_D1M   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 1 negative signal |
| 9     |           |           | GND       | GND       | P   | Ground   |
| 10    | E2        | CSI_D2P   | CSI_D2P   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 2 positive signal |

| Pin # | i.MX6 BALL | PAD NAME  | Signal    | V         | I/O | Description   |
|-------|------------|-----------|-----------|-----------|-----|---|
| 11    | E1         | CSI_D2M   | CSI_D2M   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 2 negative signal  |
| 12    |            |           | GND       | GND       | P   | Ground  |
| 13    | F1         | CSI_D3P   | CSI_D3P   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 3 positive signal  |
| 14    | F2         | CSI_D3M   | CSI_D3M   | CMOS 2.5V | I   | MIPI Camera Serial Interface data pair 3 negative signal  |
| 15    |            |           | GND       | GND       | P   | Ground  |
| 16    | H1         | DSI_D1P   | DSI_D1P   |           | O   | MIPI Display Serial Interface data pair 1 positive signal |
| 17    | H2         | DSI_D1M   | DSI_D1M   |           | O   | MIPI Camera Serial Interface data pair 1 negative signal  |
| 18    |            |           | GND       | GND       | P   | Ground  |
| 19    | G1         | DSI_D0P   | DSI_D0P   | CMOS 2.5V | O   | MIPI Display Serial Interface data pair 0 positive signal |
| 20    | G2         | DSI_D0M   | DSI_D0M   | CMOS 2.5V | O   | MIPI Camera Serial Interface data pair 0 negative signal  |
| 21    |            |           | GND       | GND       | P   | Ground  |
| 22    | H4         | DSI_CLK0P | DSI_CLK0P | CMOS 2.5V | O   | MIPI Display Serial Interface clock pair positive signal  |
| 23    | H3         | DSI_CLK0M | DSI_CLK0M | CMOS 2.5V | O   | MIPI Camera Serial Interface clock pair negative signal   |
| 24    |            |           | GND       | GND       | P   | Ground  |
| 25    | U5         | KEY_COL3  | I2C2_SCL  | CMOS 3.3V | I/O | I <sup>2</sup> C bus clock line                           |
| 26    | T7         | KEY_ROW3  | I2C2_SDA  | CMOS 3.3V | I/O | I <sup>2</sup> C bus data line                            |
| 27    |            |           |           | 3.3V      | P   | Power Supply 3.3VDC                                       |
| 28    |            |           |           | 3.3V      | P   | Power Supply 3.3VDC                                       |
| 29    | R7         | GPIO_3    | GPIO      | CMOS 3.3V | I/O | General Purpose Input Output                              |
| 30    | T3         | GPIO_6    | GPIO      | CMOS 3.3V | I/O | General Purpose Input Output                              |
| 31    | R5         | GPIO_8    | GPIO      | CMOS 3.3V | I/O | General Purpose Input Output                              |
| 32    |            |           | VCC       | 5V        | P   | Power Supply 5VDC ± 5%                                    |
| 33    |            |           | VCC       | 5V        | P   | Power Supply 5VDC ± 5%                                    |

NOTE: MIPI Camera Serial Interface data pair 2 and data pair 3 are only available on the i.MX6 Dual and i.MX6 Quad processor.

## 2.8 JTAG Connector

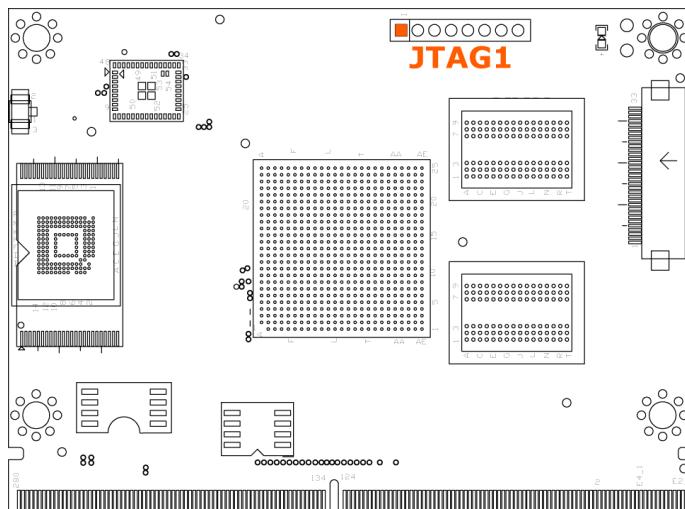
The EDM1-CF-IMX6 JTAG interface is derived from the i.MX6 processor integrated SJC module.

The SJC module implements and manages the daisy-chained topology consisting of its' own TAP and those of the SDMA, and the ARM Debug Access Port (DAP).

The SJC supports the following main features:

- IEEE P1149.1, 1149.6 (standard JTAG) interface to off-chip test and development equipment
- Debug-related control and status

For additional details, please refer to the SJC chapter of the “I.MX6 Reference Manual”.



**Table 10 - JTAG Expansion Header Signal Description**

| Pin # | i.MX6 BALL | Signal     | V    | I/O | Description  |
|-------|------------|------------|------|-----|--|
| 1     |            | 3.3V       | 3.3V | P   | Power Supply 3.3VDC  |
| 2     | C2         | JTAG_nTRST |      | I   | Test Reset (TRST). This is used to asynchronously initialize the test controller. The TRST pin has an internal pull-up resistor  |
| 3     | C3         | JTAG_TMS   |      | I   | Test Mode Select (TMS). This is used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and includes an internal pull-up resistor                                     |
| 4     | G5         | JTAG_TDI   |      | I   | Test Data Input (TDI). Serial test instruction and data are received through the test data input (TDI) pin. TDI is sampled on the rising edge of TCK and includes an internal pull-up resistor               |
| 5     | G6         | JTAG_TDO   |      | O   | Test Data Output (TDO). The serial output for test instructions and data. TDO is tri-stat able and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK |
| 6     | C11        | JTAG_nSRST |      | I   | System Reset (SRST). This is used to asynchronously initialize the test controller. The SRST pin has an internal pull-up resistor  |
| 7     | H5         | JTAG_TCK   |      | I   | Test Clock (TCK). This is used to synchronize the test logic and includes an internal pull-up resistor   |
| 8     |            | GND        | GND  | P   | Ground   |

### 3. EDM Type 1 Connector Interfaces

#### 3.1 Gigabit Ethernet

The EDM1-CF-IMX6 gigabit Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks.

More information can be found in chapter 2.6. Atheros AR8031 Gigabit LAN of this hardware manual

**Table 11 - EDM Gigabit Ethernet Signal Description**

| EDM Pin | Signal         | V         | I/O | Description  |
|---------|----------------|-----------|-----|--|
| E3_2    | GBE_MDI2+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal |
| E4_2    | GBE_MDI0+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal |
| E3_3    | GBE_MDI2-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal |
| E4_3    | GBE_MDI0-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal |
| E3_5    | GBE_MDI3+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal |
| E4_5    | GBE_MDI1+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal |
| E3_6    | GBE_MDI3-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal |
| E4_6    | GBE_MDI1-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal |
| E3_7    | LED1_ACT       | CMOS 3.3V | O   | Gigabit Ethernet LED Activity indicator  |
| E4_8    | LED1_nLink100  | CMOS 3.3V | O   | Gigabit Ethernet 100Mbit/sec LED link indicator                                      |
| E4_9    | LED1_nLink1000 | CMOS 3.3V | O   | Gigabit Ethernet 1000Mbit/sec LED link indicator                                     |

### 3.2. LVDS Interface

The EDM1-CF-IMX6 is equipped with single LVDS Display interfaces. The LVDS Display Bridge (LDB) connects the IPU (Image Processing Unit) to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data from the IPU to external display devices through LVDS interface.

The LDB output complies with the EIA-644-A standard and supports the following features:

- Connectivity to relevant devices - Displays with LVDS receivers.
- Arranging the data as required by the external display receiver and by LVDS display standards.
- Synchronization and control capabilities.
- Data input interface (inside the i.MX6 processor)
  - RGB Data of 18 or 24 bits
  - Pixel clock
  - Control signals: HSYNC, VSYNC, DE, and 1 additional optional general purpose control ( $I^2C$ )
- Single channel output data output interface
  - Total of up to 28 bits per data interface are transferred per pixel clock cycle.
- Data Rates
  - Overall: LDB supports rates needed by WUXGA 16:10 aspect ratio (1920 x 1200 @ 60 frames per second, data rate supported up to 170 MHz)
  - For single input data interface case: Up to 170 MHz pixel clock (WUXGA 1920x1200)
  - For dual input data interface case: Up to 85 MHz per interface. (WXGA 1366x768 @ 60 frames per second, 35% blanking).

For additional details, please refer to chapter 39 of the “i.MX6 Reference Manual”.

**Table 12 - LVDS Signal Description**

| <b>EDM PIN</b> | <b>i.MX6 BALL</b> | <b>PAD NAME</b> | <b>Signal</b> | <b>V</b>  | <b>I/O</b> | <b>Description</b>                                       |
|----------------|-------------------|-----------------|---------------|-----------|------------|--|
| E3_9           | U2                | LVDS0_TX0_N     | LVDS_A0-      | LVDS      | O          | LVDS primary channel differential pair 0 negative signal |
| E3_10          | U1                | LVDS0_TX0_P     | LVDS_A0+      | LVDS      | O          | LVDS primary channel differential pair 0 positive signal |
| 3              | U4                | LVDS0_TX1_N     | LVDS_A1-      | LVDS      | O          | LVDS primary channel differential pair 1 negative signal |
| 5              | U3                | LVDS0_TX1_P     | LVDS_A1+      | LVDS      | O          | LVDS primary channel differential pair 1 positive signal |
| 9              | V2                | LVDS0_TX2_N     | LVDS_A2-      | LVDS      | O          | LVDS primary channel differential pair 2 negative signal |
| 11             | V1                | LVDS0_TX2_P     | LVDS_A2+      | LVDS      | O          | LVDS primary channel differential pair 2 positive signal |
| 15             | W2                | LVDS0_TX3_N     | LVDS_A3-      | LVDS      | O          | LVDS primary channel differential pair 3 negative signal |
| 17             | W1                | LVDS0_TX3_P     | LVDS_A3+      | LVDS      | O          | LVDS primary channel differential pair 3 positive signal |
| 21             | V4                | LVDS0_CLK_N     | LVDS_ACLK-    | LVDS      | O          | LVDS primary channel clock negative signal               |
| 23             | V3                | LVDS0_CLK_P     | LVDS_ACLK+    | LVDS      | O          | LVDS primary channel clock positive signal               |
| 27             | B19               | SD4_DAT1        | LVDS_ABL_CTRL | CMOS 3.3V | O          | LVDS primary channel panel backlight control             |
| 29             | D18               | SD4_DAT0        | LVDS_AEN      | CMOS 3.3V | O          | LVDS primary channel panel backlight enable              |
| 31             | NC                |                 | LVDS_AVDD_EN  | CMOS 3.3V | O          | LVDS primary channel panel power enable                  |

The following pins can be used for LVDS panel detection.

**Table 13 - LVDS Panel Detection Pins**

| <b>EDM PIN</b> | <b>i.MX6 BALL</b> | <b>PAD NAME</b> | <b>Signal</b> | <b>V</b>  | <b>I/O</b> | <b>Description</b>  |
|----------------|-------------------|-----------------|---------------|-----------|------------|---|
| 37             | G23               | EIM_D28         | I2C_SDA       | CMOS 3.3V | I/O        | Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus data line   |
| 39             | H20               | EIM_D21         | I2C_SCL       | CMOS 3.3V | I/O        | Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus clock line |

NOTE: The I<sup>2</sup>C signals for LVDS panel control are fully documented in chapter 3.14. I<sup>2</sup>C Bus of this hardware manual.

### 3.3. HDMI (High Definition Multi-Media Interface)

The HDMI interface available with EDM-CF-IMX6 is based on the “HDMI transmitter” & “HDMI 3D Tx PHY” integrated into the i.MX6 processor. The “HDMI transmitter” combines video/display data from the IPU, Audio data from i.MX6 memory & control/status data from the ARM complex, into TMDS data & clock channels. The “HDMI 3D TX PHY” transmits the combined data by means of 3 TMDS data pairs and a TMDS clock pair together with the DDC/I<sup>2</sup>C configuration signals to the EDM connector.

The HDMI 3D TX PHY integrated into the i.MX6 processor supports the following standards & features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Digital Visual Interface, Revision 1.0
- HDMI Compliance Test Specification, Version 1.4a
- Support for up to 720p at 100Hz and 720i at 200Hz or 1080p at 60Hz and 1080i/720i at 120Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

For additional details, please refer to chapters 32 and 33 of the “i.MX6 Reference Manual”.

**Table 14 - HDMI Signal Description**

| EDM PIN | I.MX6 BALL | PAD NAME  | Signal     | V         | I/O   | Description   |
|---------|------------|-----------|------------|-----------|-------|---|
| 43      | J6         | HDMI_CLKP | HDMI1_CLK+ | HDMI      | O     | HDMI differential pair clock positive signal  |
| 45      | J5         | HDMI_CLKM | HDMI1_CLK- | HDMI      | O     | HDMI differential pair clock negative signal  |
| 49      | K6         | HDMI_D0P  | HDMI1_D0+  | HDMI      | O     | HDMI differential pair 0 positive signal  |
| 51      | K5         | HDMI_D0M  | HDMI1_D0-  | HDMI      | O     | HDMI differential pair 0 negative signal  |
| 55      | J4         | HDMI_D1P  | HDMI1_D1+  | HDMI      | O     | HDMI differential pair 1 positive signal  |
| 57      | J3         | HDMI_D1M  | HDMI1_D1-  | HDMI      | O     | HDMI differential pair 1 negative signal  |
| 61      | K4         | HDMI_D2P  | HDMI1_D2+  | HDMI      | O     | HDMI differential pair 2 positive signal  |
| 63      | K3         | HDMI_D2M  | HDMI1_D2-  | HDMI      | O     | HDMI differential pair 2 negative signal  |
| 67      | K1         | HDMI_HPD  | HDMI1_HPD  | CMOS 3.3V | I     | HDMI/DP Hot plug detection signal that serves as an interrupt request   |
| 69      | NC         |           | HDMI1_CAD  | HDMI      | I / O | Cable Adaptor Detect  |
| 71      | H19        | EIM_A25   | HDMI1_CEC  | HDMI      | I / O | HDMI Consumer Electronics Control   |
| 73      | H20        | EIM_D21   | I2C_SCL    | CMOS 5V   | I/O   | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus clock line |
| 75      | G23        | EIM_D28   | I2C_SDA    | CMOS 5V   | I/O   | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus data line  |

### 3.4. Digital Display Sub-System (DSS) or TTL Interface

The Parallel Display interface of EDM1-CF-IMX6 is derived directly from the DI0 port of the IPU, effectively bypassing all the i.MX6 integrated display bridges.

Each DI port supports the following:

- Compatible with MIPI-DPI standard.
- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols.
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)
- Scan Order: progressive or interlaced
- Synchronization:
  - Programmable horizontal and vertical synchronization output signals
  - Data enabling output signal
  - The combined data rate for the two DI ports is up to 240 MP/sec
- Supported pixel data formats:
  - RGB - color depth fully configurable; up to 8 bits/value (color component)
  - YUV 4:2:2, 8 bits/value
  - All mandatory formats in MIPI DBI, DPI and DSI

For examples of valid mappings, please refer to the “IPU Display Interface Signal Mapping” chapter of the i.MX6 datasheet.

For detailed information please refer to the “Bus Mapping Unit” chapter of the “i.MX6 Reference Manual” and “EDM Standard Specifications”.

**Table 15 - TTL Display Signal Description**

| <b>EDM PIN</b> | <b>i.MX6 BALL</b> | <b>PAD NAME</b> | <b>Signal</b> | <b>V</b> | <b>I/O</b> | <b>Description</b>               |
|----------------|-------------------|-----------------|---------------|----------|------------|----------------------------------|
| 2              | P24               | DISP0_DAT0      | LCD_D0        | TTL      | O          | LCD Pixel Data bit 0             |
| 4              | P22               | DISP0_DAT1      | LCD_D1        | TTL      | O          | LCD Pixel Data bit 1             |
| 8              | P23               | DISP0_DAT2      | LCD_D2        | TTL      | O          | LCD Pixel Data bit 2             |
| 10             | P21               | DISP0_DAT3      | LCD_D3        | TTL      | O          | LCD Pixel Data bit 3             |
| 14             | P20               | DISP0_DAT4      | LCD_D4        | TTL      | O          | LCD Pixel Data bit 4             |
| 16             | R25               | DISP0_DAT5      | LCD_D5        | TTL      | O          | LCD Pixel Data bit 5             |
| 20             | R23               | DISP0_DAT6      | LCD_D6        | TTL      | O          | LCD Pixel Data bit 6             |
| 22             | R24               | DISP0_DAT7      | LCD_D7        | TTL      | O          | LCD Pixel Data bit 7             |
| 26             | R22               | DISP0_DAT8      | LCD_D8        | TTL      | O          | LCD Pixel Data bit 8             |
| 28             | T25               | DISP0_DAT9      | LCD_D9        | TTL      | O          | LCD Pixel Data bit 9             |
| 32             | R21               | DISP0_DAT10     | LCD_D10       | TTL      | O          | LCD Pixel Data bit 10            |
| 34             | T23               | DISP0_DAT11     | LCD_D11       | TTL      | O          | LCD Pixel Data bit 11            |
| 36             | T24               | DISP0_DAT12     | LCD_D12       | TTL      | O          | LCD Pixel Data bit 12            |
| 38             | R20               | DISP0_DAT13     | LCD_D13       | TTL      | O          | LCD Pixel Data bit 13            |
| 40             | U25               | DISP0_DAT14     | LCD_D14       | TTL      | O          | LCD Pixel Data bit 14            |
| 44             | T22               | DISP0_DAT15     | LCD_D15       | TTL      | O          | LCD Pixel Data bit 15            |
| 46             | T21               | DISP0_DAT16     | LCD_D16       | TTL      | O          | LCD Pixel Data bit 16            |
| 50             | U24               | DISP0_DAT17     | LCD_D17       | TTL      | O          | LCD Pixel Data bit 17            |
| 52             | V25               | DISP0_DAT18     | LCD_D18       | TTL      | O          | LCD Pixel Data bit 18            |
| 56             | U23               | DISP0_DAT19     | LCD_D19       | TTL      | O          | LCD Pixel Data bit 19            |
| 58             | U22               | DISP0_DAT20     | LCD_D20       | TTL      | O          | LCD Pixel Data bit 20            |
| 62             | T20               | DISP0_DAT21     | LCD_D21       | TTL      | O          | LCD Pixel Data bit 21            |
| 64             | V24               | DISP0_DAT22     | LCD_D22       | TTL      | O          | LCD Pixel Data bit 22            |
| 68             | W24               | DISP0_DAT23     | LCD_D23       | TTL      | O          | LCD Pixel Data bit 23            |
| 70             | N19               | DIO_DISP_CLK    | LCD_CLK       | TTL      | O          | LCD Pixel Clock                  |
| 72             | N25               | DIO_PIN2        | LCD_HSYNC     | TTL      | O          | LCD Horizontal Synchronization   |
| 74             | N20               | DIO_PIN3        | LCD_VSYNC     | TTL      | O          | LCD Vertical Synchronization     |
| 76             | P25               | DIO_PIN4        | LCD_BKLEN     | TTL      | O          | LCD backlight enable/disable     |
| 78             | N21               | DIO_PIN15       | LCD_DRD_Y     | TTL      | O          | LCD dot enable pin signal        |
| 80             | A20               | SD4_DAT3        | LCD_VDDE      | TTL      | O          | LCD Voltage On                   |
| 82             | F17               | SD4_DAT2        | LCD_CNTRST    | TTL      | O          | LCD Backlight brightness Control |

### 3.5. Audio Interface

The EDM1-CF-IMX6 incorporates two I<sup>2</sup>S / AUDMUX signals, one S/P DIF interface and can as well provide surround audio over the HDMI data signals.

The AUDMUX provides flexible, programmable routing of the serial interfaces (SSI1 or SSI2) to and from off-chip devices. The AUDMUX routes audio data (and even splices together multiple time-multiplexed audio streams) but does not decode or process audio data itself. The AUDMUX is controlled by the ARM but can route data even when the ARM is in a low-power mode.

The ESAI (Enhanced Serial Audio Interface) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI is connected to the IOMUX and to the ESAI\_BIFIFO module.

The ESAI\_BIFIFO (ESAI Bus Interface and FIFO) is the interface between the ESAI module and the shared peripheral bus. It contains the FIFOs used to buffer data to and from the ESAI, as well as providing the data word alignment and padding necessary to match the 24-bit data bus of the ESAI to the 32-bit data bus of the shared peripheral bus.

The SPDIF (Sony/Philips Digital Interface) audio module is a stereo transceiver that allows the processor to receive and transmit digital audio over it. The SPDIF receiver section includes a frequency measurement block that allows the precise measurement of incoming sampling frequency. A recovered clock is provided by the SPDIF receiver section and may be used to drive both internal and external components in the system. The SPDIF is connected to the shared peripheral bus.

The ASRC (Asynchronous Sample Rate Converter) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversions of up to 10 channels of over 120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs. The ASRC is connected to the shared peripheral bus.

Key features of the audio signal block include:

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx frame sync and clock direction selection for host or peripheral
- Each host interface's capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)
- Transmit and receive data switching to support external network mode

**Table 16 - Primary I<sup>2</sup>S Audio Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME  | Signal    | V         | I/O | Description  |
|---------|------------|-----------|-----------|-----------|-----|--|
| 187     | N3         | CSI0_DAT7 | I2S1_RXD  | CMOS 3.3V | I   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel receive data line            |
| 189     | N4         | CSI0_DAT6 | I2S1_TXFS | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel frame synchronization signal |
| 191     | P2         | CSI0_DAT5 | I2S1_TXD  | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel transmit data line           |
| 193     | N1         | CSI0_DAT4 | I2S1_TXC  | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel word clock signal            |
| 195     | T5         | GPIO_0    | I2S1_CLK  | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel master clock signal          |

**Table 17 - Secondary I<sup>2</sup>S Audio Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal    | V         | I/O | Description  |
|---------|------------|----------|-----------|-----------|-----|--|
| 186     | U6         | KEY_ROW1 | I2S2_RXD  | CMOS 3.3V | I   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel receive data line            |
| 188     | U7         | KEY_COL1 | I2S2_TXFS | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel frame synchronization signal |
| 190     | V6         | KEY_ROW0 | I2S2_TXD  | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel transmit data line           |
| 192     | W5         | KEY_COL0 | I2S2_TXC  | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel word clock signal            |
| 194     | T5         | GPIO_0   | I2S2_CLK  | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel master clock signal          |

NOTE: On EDM1-CF-IMX6 System-on-Modules that feature WiFi / Bluetooth functionality. The Secondary I<sup>2</sup>S is routed to the onboard Broadcom BCM4330 chip.

### 3.5.1. S/P DIF Audio

S/P DIF (Sony/Philips Digital Interconnect Format) is a type of digital audio interconnects cable used in consumer audio equipment to output audio over reasonably short distances. The signal is transmitted over either a coaxial cable with RCA connectors or a fibre optic cable with TOSLINK connectors. S/P DIF is based on the professional AES3 interconnect standard. S/P DIF can carry two channels of PCM audio or a multi-channel compressed surround sound format such as Dolby Digital or DTS.

The EDM1-CF-IMX6 features an S/P DIF interface allowing EDM module to transmit digital audio data. The S/PDIF interface is implemented by means of the i.MX6 integrated S/P DIF transceiver.

For additional details, please refer to chapter 59 of the “i.MX6 Reference Manual”.

**Table 18 - S/P DIF Audio Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME  | Signal    | V     | I/O | Description   |
|---------|------------|-----------|-----------|-------|-----|---|
| 196     | W21        | ENET_RXD0 | SPDIF_OUT | SPDIF | O   | Sony / Philips Digital Interconnect Format Audio output |

### 3.6. PCI Express

The EDM1-CF-IMX6 is equipped with a single lane PCI Express interface, implemented in the i.MX6 processor.

The PCI Express interface complies with PCIe specification Gen 2.0 and supports the PCI Express 1.1/2.0 standards. The PCI Express module is a dual mode complex, supporting root complex operations and endpoint operations.

#### PCI Express PHY Features

- 5 Gbps data transmission rate
- Integrated PHY includes transmitter, receiver, PLL, digital core, and ESD.
- Programmable RX equalization
- Designed for excellent performance margin and receiver sensitivity
- Robust PHY architecture tolerates wide process, voltage and temperature variations
- Low-jitter PLL technology with excellent supply isolation
- IEEE 1149.6 (JTAG) boundary scan
- Built-in Self-Test (BIST) features for production, at-speed, testing on any digital tester
- 5Gb/s PCIe Gen 2 and 2.5Gb/s PCIe Gen 1.1 test modes supported
- Advanced built-in diagnostics including on-chip sampling scope for easy debug
- Visibility & controllability of hard macro functionality thru programmable registers in the design
- Over-rides on all ASIC side inputs for easy debug
- Access register space thru simple 16 bit parallel interface
- Access register space thru JTAG

For additional details, please refer to chapter 49 of the “i.MX6 Reference Manual”.

**Table 19 - PCI Express Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal     | V         | I/O | Description   |
|---------|------------|----------|------------|-----------|-----|---|
| 85      | D7         | CLK1_P   | PCIEA_CLK+ | PCIE      | O   | PCI Express channel A clock differential pair positive signal           |
| 87      | C7         | CLK1_N   | PCIEA_CLK- | PCIE      | O   | PCI Express channel A clock differential pair negative signal           |
| 91      | B3         | PCIE_TXP | PCIEA_TX+  | PCIE      | O   | PCI Express channel A Transmit output differential pair positive signal |
| 93      | A3         | PCIE_TXM | PCIEA_TX-  | PCIE      | O   | PCI Express channel A Transmit output differential pair negative signal |
| 97      | B2         | PCIE_RXP | PCIEA_RX+  | PCIE      | I   | PCI Express channel A Receive input differential pair positive signal   |
| 99      | B1         | PCIE_RXM | PCIEA_RX-  | PCIE      | I   | PCI Express channel A Receive input differential pair negative signal   |
| 119     | H21        | EIM_D31  | PCIE_RST#  | CMOS 3.3V | O   | PCI Express Reset signal for external devices                           |

NOTE: The PCIE\_RX pair has decoupling capacitors on the EDM module valued 10nF

### 3.7. Serial ATA Interface

The EDM-CF-IMX6 incorporates a single SATA-II port implemented with the Freescale i.MX6 integrated SATA controller and PHY.

The interface supports the following main features:

- The SATA block fully complies with AHCI specification version 1.10 and partially complies with AHCI specification version 1.3 (FIS-based switching is currently not supported).
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- Power management features including automatic partial-to-slumber transition.
- eSATA (external analog logic also needs to support eSATA).
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries.

For additional details, please refer to chapter 53 of the “i.MX6 Reference Manual”.

**Table 20 - Serial ATA Signal Description**

| Pin # | i.MX6<br>BALL | PAD NAME   | Signal     | V    | I/O | Description   |
|-------|---------------|------------|------------|------|-----|---|
| 123   | B14           | SATA_RXP   | SATA1_RXP  | SATA | I   | Serial ATA channel 1 Receive differential pair positive signal                |
| 125   | A14           | SATA_RXM   | SATA1_RXN  | SATA | I   | Serial ATA channel 1 Receive differential pair negative signal                |
| 133   | M5            | CSI0_DAT15 | SATA1_nACT | SATA | I/O | Serial ATA LED. Open collector output pin driven during SATA command activity |
| 135   | A12           | SATA_TXP   | SATA1_TXP  | SATA | O   | Serial ATA channel 1 Transmit differential pair positive signal               |
| 137   | B12           | SATA_TXM   | SATA1_TXN  | SATA | O   | Serial ATA channel 1 Transmit differential pair negative signal               |

NOTE: SATA is only available on EDM1-CF-IMX6 modules that feature the i.MX6 Dual or i.MX6 Quad processor and is not available on the i.MX6 Solo and i.MX6 Duallite processor.

### 3.8. Universal Serial Bus (USB) Interface

The EDM-CF-IMX6 incorporates a single USB Host controller and an additional USB Host/OTG controller.

Each of the USB controllers provides the following main features:

#### USB 2.0 Host/OTG Controller

- High-Speed/Full-Speed/Low-Speed OTG core
- HS/FS/LS UTMI compliant interface
- High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
- High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints
- Support charger detection

#### USB 2.0 Host Controller

- High-Speed/Full-Speed/Low-Speed Host-Only core
- HS/FS/LS UTMI compliant interface

For additional details, please refer to chapter 65 of the “i.MX6 Reference Manual”.

**Table 21 - USB Host Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME    | Signal       | V         | I/O | Description   |
|---------|------------|-------------|--------------|-----------|-----|---|
| 139     | R1         | GPIO_17     | USB1_HUB_RST | USB       | O   | Universal Serial Bus carrier board hub reset pin                |
| 165     | J20        | EIM_D30     | USB1_OC      | CMOS 3.3V | I   | Over current detect input pin to monitor USB power over current |
| 179     | F10        | USB_H1_DN   | USB1_D-      | USB       | I/O | Universal Serial Bus port 1 differential pair negative signal   |
| 181     | E10        | USB_H1_DP   | USB1_D+      | USB       | I/O | Universal Serial Bus port 1 differential pair positive signal   |
| 183     | D10        | USB_H1_VBUS | USB1_VBUS    | 5V        | I/O | Universal Serial Bus port 1 power                               |

**Table 22 - USB OTG Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME     | Signal      | V         | I/O | Description   |
|---------|------------|--------------|-------------|-----------|-----|---|
| 141     | T2         | GPIO_9       | USB2_OC     | CMOS 3.3V | I   | Over current detect input pin to monitor USB power over current |
| 155     | T4         | GPIO_1       | USB2_OTG_ID | USB       | I   | Universal Serial Bus On-The-Go detection signal                 |
| 157     | A6         | USB_OTG_DP   | USB2_D+     | USB       | I/O | Universal Serial Bus port 2 differential pair positive signal   |
| 159     | B6         | USB_OTG_DN   | USB2_D-     | USB       | I/O | Universal Serial Bus port 2 differential pair negative signal   |
| 161     | E9         | USB_OTG_VBUS | USB2_VBUS   | 5V        | I/O | Universal Serial Bus port 2 power                               |
| 163     | E23        | EIM_D22      | USB2_PWR_EN | USB       | O   | Universal Serial Bus power enable                               |

NOTE: While using USB OTG in USB HOST mode. The USB2\_OTG\_ID pin (EDM pin 155) should have a pull-down resistor to GND.

### 3.9. SDIO/MMC Interface

The EDM1-CF-IMX6 features a MMC / SD / SDIO host interfaces connected to the Freescale i.MX6 integrated “Ultra Secured Digital Host Controller” (uSDHC).

The following main features are supported by uSDHC:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.5.
- Conforms to the SD Host Controller Standard Specification version 3.0.
- Compatible with the SD Memory Card Specification version 3.0 and supports the “Extended Capacity SD Memory Card” .
- Compatible with the SDIO Card Specification version 3.0.
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit

The MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

For additional details, please refer to chapter 65 of the “i.MX6 Reference Manual”.

**Table 23 - SDIO/MMC Interface Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME    | Signal    | V         | I/O | Description            |
|---------|------------|-------------|-----------|-----------|-----|------------------------|
| 203     | T1         | GPIO_2      | SDIO_CD   | CMOS 3.3V | I/O | MMC/SDIO Card Detect   |
| 205     | B21        | SD1_CMD     | SDIO_CMD  | CMOS 3.3V | I/O | MMC/SDIO Command       |
| 206     | D20        | SD1_CLK     | SDIO_CLK  | CMOS 3.3V | O   | MMC/SDIO Clock         |
| 207     | N6         | CSI0_DAT8   | SDIO_WP   | CMOS 3.3V | I/O | MMC/SDIO Write Protect |
| 208     | P4         | CSI0_MCLK   | SDIO_LED  | CMOS 3.3V | O   | MMC/SDIO LED           |
| 209     | C20        | SD1_DAT1    | SDIO_DAT1 | CMOS 3.3V | I/O | MMC/SDIO Data bit 1    |
| 210     | P1         | CSI0_PIXCLK | SDIO_PWR  | CMOS 3.3V | O   | MMC/SDIO Power Enable  |
| 211     | F18        | SD1_DAT3    | SDIO_DAT3 | CMOS 3.3V | I/O | MMC/SDIO Data bit 3    |
| 212     | A21        | SD1_DAT0    | SDIO_DAT0 | CMOS 3.3V | I/O | MMC/SDIO Data bit 0    |
| 214     | E19        | SD1_DAT2    | SDIO_DAT2 | CMOS 3.3V | I/O | MMC/SDIO Data bit 2    |

### 3.10. General Purpose Memory Controller Bus (Local Bus)

The EDM1-CF-IMX6 features a general-purpose media interface which is connected to the Freescale i.MX6 GPMI controller.

The general-purpose media interface has several features to efficiently support NAND:

- Individual chip select pins and ganged ready/busy pin for up to four NANDs.
- Individual state machine and DMA channel for each chip select.
- Special command modes work with DMA controller to perform all normal NAND functions without CPU intervention.
- Configurable timing based on a dedicated clock allows optimal balance of high NAND performance and low system power.

GPMI and DMA have been designed to handle complex multi-page operations without CPU intervention. The DMA uses a linked descriptor function with branching capability to automatically handle all of the operations needed to read/write multiple pages:

- Data/Register Read/Write-The GPMI can be programmed to read or write multiple cycles to the NAND address, command or data registers.
- Wait for NAND Ready-The GPMI's Wait-for-Ready mode can monitor the ready/ busy signal of a single NAND flash and signal the DMA when the device has become ready. It also has a time-out counter and can indicate to the DMA that a time-out error has occurred. The DMAs can conditionally branch to a different descriptor in the case of an error.
- Check Status-The Read-and-Compare mode allows the GPMI to check NAND status against a reference. If an error is found, the GPMI can instruct the DMA to branch to an alternate descriptor, which attempts to fix the problem or asserts a CPU IRQ.

For additional details, please refer to chapter 29 of the “I.MX6 Reference Manual”.

**Table 24 - GPMC / Local Bus Signal Description**

| <b>EDM PIN</b> | <b>i.MX6 BALL</b> | <b>PAD NAME</b> | <b>Signal</b> | <b>V</b>  | <b>I/O</b> | <b>Description</b>   |
|----------------|-------------------|-----------------|---------------|-----------|------------|--|
| 86             | F15               | NANDF_CS0       | GPMC_nCSA     | CMOS 3.3V | O          | GPMC Chip Select bit A                                     |
| 90             | C16               | NANDF_CS1       | GPMC_nCSB     | CMOS 3.3V | O          | GPMC Chip Select bit B                                     |
| 92             | A17               | NANDF_CS2       | GPMC_nCSC     | CMOS 3.3V | O          | GPMC Chip Select bit C                                     |
| 96             | D16               | NANDF_CS3       | GPMC_nCSD     | CMOS 3.3V | O          | GPMC Chip Select bit D                                     |
| 102            | B16               | NANDF_RB0       | GPMC_WAIT     | CMOS 3.3V | I          | External indication of wait                                |
| 104            | E15               | NANDF_WP_B      | GPMC_WP       | CMOS 3.3V | O          | GPMC Write Protect / Enable                                |
| 106            | C15               | NANDF_CLE       | GPMC_CLE      | CMOS 3.3V | O          | GPMC Lower Byte Enable. Also used for Command Latch Enable |
| 108            | A16               | NANDF_ALE       | GPMC_ALE      | CMOS 3.3V | O          | GPMC Address Valid or Address Latch Enable                 |
| 110            | E16               | SD4_CLK         | GPMC_WE       | CMOS 3.3V | I          | GPMC Write Enable  |
| 112            | B17               | SD4_CMD         | GPMC_RE       | CMOS 3.3V | O          | GPMC Read Enable   |
| 168            | C18               | NANDF_D7        | GPMC_D7       | CMOS 3.3V | I/O        | GPMC data bit 7  |
| 170            | E17               | NANDF_D6        | GPMC_D6       | CMOS 3.3V | I/O        | GPMC data bit 6  |
| 172            | B18               | NANDF_D5        | GPMC_D5       | CMOS 3.3V | I/O        | GPMC data bit 5  |
| 174            | A19               | NANDF_D4        | GPMC_D4       | CMOS 3.3V | I/O        | GPMC data bit 4  |
| 176            | D17               | NANDF_D3        | GPMC_D3       | CMOS 3.3V | I/O        | GPMC data bit 3  |
| 178            | F16               | NANDF_D2        | GPMC_D2       | CMOS 3.3V | I/O        | GPMC data bit 2  |
| 180            | C17               | NANDF_D1        | GPMC_D1       | CMOS 3.3V | I/O        | GPMC data bit 1  |
| 182            | A18               | NANDF_D0        | GPMC_D0       | CMOS 3.3V | I/O        | GPMC data bit 0  |

NOTE: On configurations where the NAND Flash IC is mounted instead of eMMC, EDM PIN# 86 is left un-connected.

### 3.11. CAN BUS Interface signals

The EDM1-CF-IMX6 features two CAN bus interfaces. The CAN bus interfaces are implemented with the i.MX6 on chip “Flexible Controller Area Network” (FlexCAN) communication modules.

FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

Integration of a CAN Bus transceiver and optional galvanic isolation should be incorporated on the EDM carrier board.

For additional details, please refer to chapter 25 of the “i.MX6 Reference Manual”.

**Table 25 - Primary CAN Bus Signal Description**

| Pin # | i.MX6 BALL | PAD NAME | Signal  | V   | I/O | Description   |
|-------|------------|----------|---------|-----|-----|---|
| 200   | W6         | KEY_COL2 | CAN1_TX | CAN | I/O | Primary CAN (controller Area Network) transmit signal |
| 202   | W4         | KEY_ROW2 | CAN1_RX | CAN | I/O | Primary CAN (controller Area Network) receive signal  |

NOTE: The CAN1\_TX signal (EDM PIN# 200) is shared with the SPI1\_CS1 (EDM PIN# 230) and only one function can be used simultaneously.

**Table 26 - Secondary CAN Bus Signal Description**

| Pin # | i.MX6 BALL | PAD NAME | Signal  | V   | I/O | Description   |
|-------|------------|----------|---------|-----|-----|---|
| 197   | T6         | KEY_COL4 | CAN2_TX | CAN | I/O | Secondary CAN (controller Area Network) transmit signal |
| 199   | V5         | KEY_ROW4 | CAN2_RX | CAN | I/O | Secondary CAN (controller Area Network) receive signal  |

### 3.12. Universal Asynchronous Receiver/Transmitter (UART) Interface

The EDM1-CF-IMX6 makes 2 UART ports available on the EDM connector and utilizes an additional UART on the module to connect to the WiFi/Bluetooth module.

The i.MX6 processor integrated UARTs support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive

For additional details, please refer to chapter 62 of the “i.MX6 Reference Manual”.

**Table 27 - Primary UART Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME   | Signal    | V    | I/O | Description  |
|---------|------------|------------|-----------|------|-----|--|
| 241     | G21        | EIM_D19    | UART1_CTS | UART | O   | Universal Asynchronous Receive Transmit secondary channel clear to send signal   |
| 243     | M1         | CSI0_DAT10 | UART1_TXD | UART | O   | Universal Asynchronous Receive Transmit secondary channel transmit data signal   |
| 245     | M3         | CSI0_DAT11 | UART1_RXD | UART | I   | Universal Asynchronous Receive Transmit secondary channel receive data signal    |
| 247     | G20        | EIM_D20    | UART1_RTS | UART | O   | Universal Asynchronous Receive Transmit secondary channel request to send signal |

NOTE: it is recommended to use the UART1 interface as system debug where possible and use the UART2 signals in applications where one serial port is required.

**Table 28 - Secondary UART Signal Description**

| <b>EDM PIN</b> | <b>i.MX6 BALL</b> | <b>PAD NAME</b> | <b>Signal</b> | <b>V</b> | <b>I/O</b> | <b>Description</b>   |
|----------------|-------------------|-----------------|---------------|----------|------------|--|
| 234            | B20               | SD4_DAT6        | UART2_CTS     | UART     | O          | Universal Asynchronous Receive Transmit secondary channel clear to send signal   |
| 236            | D19               | SD4_DAT7        | UART2_TXD     | UART     | O          | Universal Asynchronous Receive Transmit secondary channel transmit data signal   |
| 238            | E18               | SD4_DAT4        | UART2_RXD     | UART     | I          | Universal Asynchronous Receive Transmit secondary channel receive data signal    |
| 240            | C19               | SD4_DAT5        | UART2_RTS     | UART     | O          | Universal Asynchronous Receive Transmit secondary channel request to send signal |

NOTE: UART3 is not listed in this section. This interface is connected from the i.MX6 processor towards the WiFi/Bluetooth interface present on EDM1-CF-IMX6 and can be found in the WiFi/Bluetooth section of this manual.

### 3.13. Serial Peripheral Interface (SPI)

The EDM1-CF-IMX6 features two Enhanced Configurable SPI ports, which are derived from the i.MX6 processor, integrated ECSPI IPs.

The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable Direct Memory Access (DMA) support

For additional details, please refer to chapter 20 of the “i.MX6 Reference Manual”.

**Table 29 - Primary SPI Channel Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal    | V         | I/O | Description   |
|---------|------------|----------|-----------|-----------|-----|---|
| 219     | J23        | EIM_CS1  | SPI2_MOSI | CMOS 3.3V | O   | Serial Peripheral Interface primary channel master output slave input signal                              |
| 221     | J24        | EIM_OE   | SPI2_MISO | CMOS 3.3V | I   | Serial Peripheral Interface primary channel master input slave output signal                              |
| 223     | H24        | EIM_CS0  | SPI2_CLK  | CMOS 3.3V | O   | Serial Peripheral Interface primary channel clock signal  |
| 225     | K20        | EIM_RW   | SPI2_CS0  | CMOS 3.3V | O   | Serial Peripheral Interface primary channel Chip Select 0 signal  |
| 227     | K22        | EIM_LBA  | SPI2_CS1  | CMOS 3.3V | O   | Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used |

NOTE: The CAN1\_TX signal (EDM PIN# 200) is shared with the SPI1\_CS1 (EDM PIN# 230) and only one function can be used.

**Table 30 - Secondary SPI Channel Signal Description**

| <b>EDM PIN</b> | <b>i.MX6 BALL</b> | <b>PAD NAME</b> | <b>Signal</b> | <b>V</b>  | <b>I/O</b> | <b>Description</b>  |
|----------------|-------------------|-----------------|---------------|-----------|------------|---|
| 222            | D24               | EIM_D18         | SPI1_MOSI     | CMOS 3.3V | O          | Serial Peripheral Interface secondary channel master output slave input signal                              |
| 224            | F21               | EIM_D17         | SPI1_MISO     | CMOS 3.3V | I          | Serial Peripheral Interface secondary channel master input slave output signal                              |
| 226            | C25               | EIM_D16         | SPI1_CLK      | CMOS 3.3V | O          | Serial Peripheral Interface secondary channel clock signal  |
| 228            | E22               | EIM_EB2         | SPI1_CS0      | CMOS 3.3V | O          | Serial Peripheral Interface secondary channel Chip Select 0 signal  |
| 230            | W6 (*)            | KEY_COL2        | SPI1_CS1      | CMOS 3.3V | O          | Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used |

### 3.14. I<sup>2</sup>C Bus

The EDM1-CF-IMX6 I<sup>2</sup>C interfaces are implemented with the i.MX6 integrated I<sup>2</sup>C controller. There are two general purpose I<sup>2</sup>C interfaces and one I<sup>2</sup>C interface dedicated towards display and system management functions.

The following features are supported:

- Compliance with Philips I<sup>2</sup>C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

For additional details, please refer to chapter 34 of the “i.MX6 Reference Manual”.

#### 3.14.1. Display and System Management Purpose I<sup>2</sup>C Bus

The I<sup>2</sup>C interface that manages display and system management functions is available at two instances.

**Table 31 - Display and System Management Purpose I<sup>2</sup>C Bus Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal   | V       | I/O | Description   |
|---------|------------|----------|----------|---------|-----|---|
| 73      | H20        | EIM_D21  | I2C1_SCL | CMOS 5V | I/O | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus clock line |
| 75      | G23        | EIM_D28  | I2C1_SDA | CMOS 5V | I/O | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus data line  |

NOTE: The 5.0V I<sup>2</sup>C signals are normally connected towards the external HDMI display interface and should not be connected to other parts of the system on an EDM carrier board if possible.

NOTE: The 5.0V I<sup>2</sup>C signals have an TX0102DCUR voltage level shift incorporated.

| EDM PIN | i.MX6 BALL | PAD NAME | Signal   | V         | I/O | Description   |
|---------|------------|----------|----------|-----------|-----|---|
| 37      | G23        | EIM_D28  | I2C1_SDA | CMOS 3.3V | I/O | Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus data line   |
| 39      | H20        | EIM_D21  | I2C1_SCL | CMOS 3.3V | I/O | Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus clock line |

NOTE: The 3.3V I<sup>2</sup>C signals are normally connected towards the LVDS display interface and smart battery solutions and should not be connected to other parts of the system on an EDM carrier board if possible.

### 3.14.2. General Purpose I<sup>2</sup>C Bus

The general purpose I<sup>2</sup>C interfaces are both independent and have no reserved addresses or devices on the EDM1-CF-IMX6.

**Table 32 – Primary General Purpose I<sup>2</sup>C Bus Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal   | V         | I/O | Description                     |
|---------|------------|----------|----------|-----------|-----|---------------------------------|
| 231     | U5         | KEY_COL3 | I2C2_SCL | CMOS 3.3V | I/O | I <sup>2</sup> C bus clock line |
| 233     | T7         | KEY_ROW3 | I2C2_SDA | CMOS 3.3V | I/O | I <sup>2</sup> C bus data line  |

**Table 33 - Secondary General Purpose I<sup>2</sup>C Bus Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal   | V         | I/O | Description                     |
|---------|------------|----------|----------|-----------|-----|---------------------------------|
| 235     | R4         | GPIO_5   | I2C3_SCL | CMOS 3.3V | I/O | I <sup>2</sup> C bus clock line |
| 237     | R2         | GPIO_16  | I2C3_SDA | CMOS 3.3V | I/O | I <sup>2</sup> C bus data line  |

NOTE: All I<sup>2</sup>C bus data and clock lines for all I<sup>2</sup>C interfaces have 2.2K Ω pull-up to 3.3V resistors present on the EDM1-CF-IMX6 module.

### 3.15. General Purpose Input/Output (GPIO)

The EDM Standard stipulates 10 dedicated GPIO pins. Many of the EDM1-CF-IMX6 can be put in GPIO mode. Using the additional pins in GPIO mode however might break upgradability to other EDM modules.

The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to chapter 27 of the “I.MX6 Reference Manual”.

**Table 34 - GPIO Signal Description**

| EDM PIN | i.MX6 BALL | PAD NAME   | Signal | V         | I/O | Description                  |
|---------|------------|------------|--------|-----------|-----|------------------------------|
| 255     | L6         | CSI0_DAT19 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 256     | L4         | CSI0_DAT16 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 257     | M6         | CSI0_DAT18 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 258     | E25        | EIM_D27    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 259     | E24        | EIM_D26    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 260     | N22        | EIM_BCLK   | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 261     | L3         | CSI0_DAT17 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 262     | W23        | ENET_RX_ER | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 263     | P5         | GPIO_19    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |
| 264     | D15        | SD3_RST    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output |

NOTE: It is suggested to use the GPIO's connected to pin 263 and 264 for touch controller related functions.

### 3.16. Manufacturing and Boot Control

The EDM Standard reserves a number of pins for manufacturing purposes and boot behavior to override the default boot media present on the EDM1-CF-IMX6 System-on-Module (eMMC or NAND Flash).

For additional details, please refer to “EDM Standard Specifications”

**Table 35 - EDM MNF Pin Description**

| EDM PIN | i.MX6 BALL | PAD NAME | Signal | V | I/O | Description                                    |
|---------|------------|----------|--------|---|-----|--|
| 267     | M23        | EIM_DA13 | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 269     | N23        | EIM_DA14 | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 271     | L22        | EIM_DA4  | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 273     | L23        | EIM_DA5  | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 275     | K25        | EIM_DA6  | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 277     | L25        | EIM_DA7  | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 278     | M20        | EIM_DA11 | MNF    |   | I   | Pins for manufacturing and validation purposes |
| 280     | M24        | EIM_DA12 | MNF    |   | I   | Pins for manufacturing and validation purposes |

The EDM1-CF-IMX6 can boot from the following devices that are present on the carrier board.

**Table 36 - EDM MNF Boot Configuration Option Overview**

| EDM PIN | SATA | SD Cardslot | eMMC on Carrier board |
|---------|------|-------------|-----------------------|
| 267     | N.C. | HIGH        | HIGH                  |
| 269     | N.C. | LOW         | N.C.                  |
| 271     | LOW  | HIGH        | N.C.                  |
| 273     | HIGH | LOW         | HIGH                  |
| 275     | LOW  | HIGH        | HIGH                  |
| 277     | LOW  | LOW         | LOW                   |
| 278     | N.C  | LOW         | LOW                   |
| 280     | N.C  | LOW         | LOW                   |

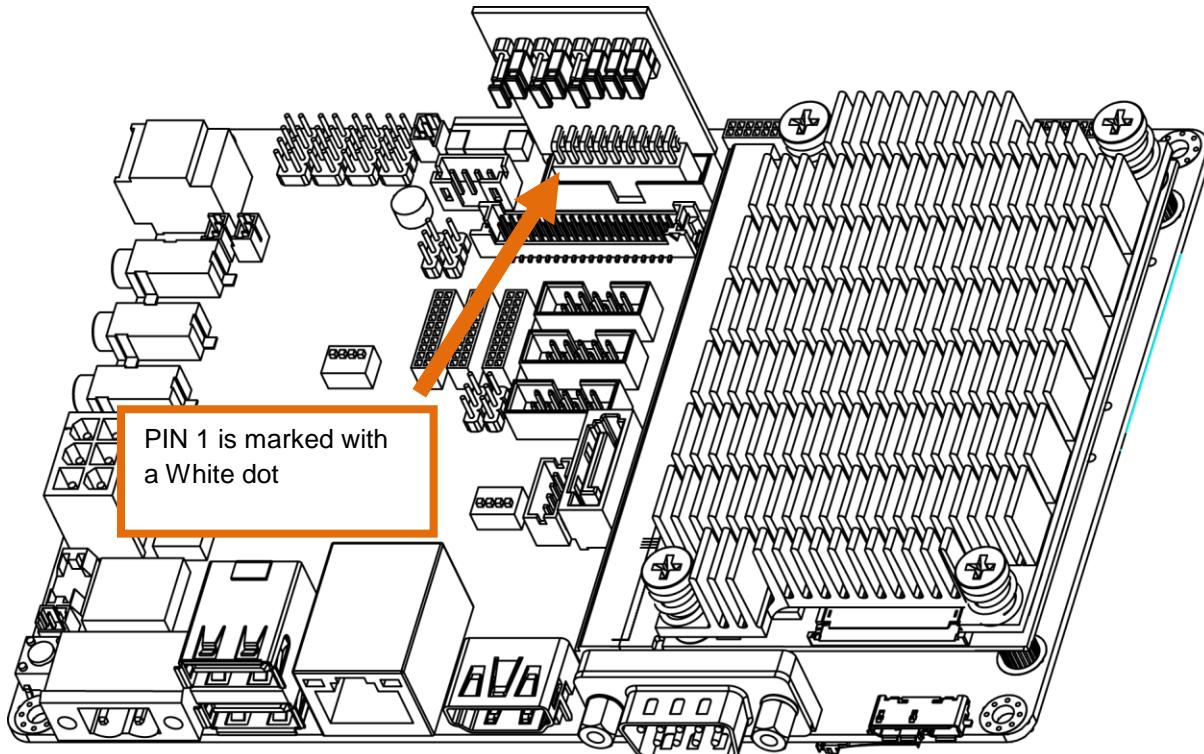
NOTE: The signals that should be “HIGH” should have 10K Ω pull-up to 3.3V resistors.

When using EDM1-CF-IMX6 on the TechNexion EDM1-FAIRY evaluation carrier board. You can simply configure the EDM-MNF-BOOT PCB that comes with the EDM1-FAIRY-START evaluation kit as follow:

**Table 37 - EDM-MNF-BOOT Configuration for EDM1-FAIRY**

| SATA | SD Cardslot | eMMC on Carrier board |
|------|-------------|-----------------------|
|      |             |                       |

**Figure 13 - EDM1-FAIRY with EDM-MNF-BOOT**



### 3.17. Input Power Requirements

The EDM1-CF-IMX6 is designed to be driven with a single +5V input power rail.

The power domain pins have to be connected as follow:

- All GND pins have to be connected to the carrier board ground pane.
- All VCC pins should be connected to the +5V main power source.

If ATX functionality is desired the following power domains pin should also be connected (ATX mode only):

- All 5VSB pins should be connected to the +5VSB main power source.
- EDM PIN#251 should be connected to the ATX power circuit PWGIN circuit

**Table 38 - Input Power Signals**

| Power Rail   | Nominal Input | Input Range     | Maximum Input Ripple |
|--------------|---------------|-----------------|----------------------|
| VCC (18 pin) | 5V            | +4.75V - +5.25V | ±50 mV               |
| 5VSB (2 pin) | 5VSB          | +4.75V - +5.25V | ±50 mV               |

#### 3.17.1. Power Management Signals

The EDM1-CF-IMX6 has the following set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states. The minimum hardware requirements for an ACPI compliant system are an EDM module supporting ACPI, ATX conforming power supply and a power button.

| EDM PIN | i.MX6 BALL     | PAD NAME | Signal | V         | I/O | Description   |
|---------|----------------|----------|--------|-----------|-----|---|
| 251     | 5VSB with 10KΩ |          | S3     | CMOS 3.3V | O   | S3 signal shuts off power to all runtime system components that are not maintained during S3 state (suspend to RAM) |
| 252     | D12            | ONOFF    | ON/OFF | CMOS 3.3V | I   | Power ON button input signal  |
| 254     | C11            | POR_B    | RESET  | CMOS 3.3V | I   | Reset button input signal   |

### 3.17.2. Power Sequencing for AT based configurations

EDM1-CF-IMX6 input power sequencing requirements for AT based configurations are as follow:

If a backup RealTime Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the EDM carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I<sup>2</sup>C can be used.

**Start Sequence:**

VCC\_RTC must come up at the same time or before VCC comes up.

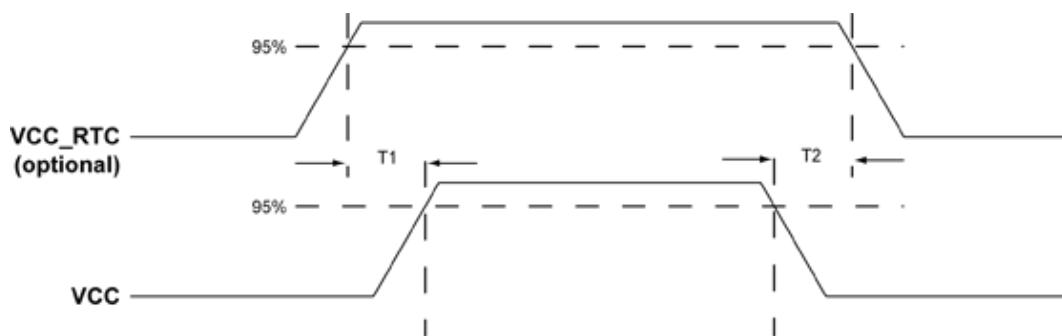
**Stop Sequence:**

VCC must go down at the same time or before VCC\_RTC goes down

**Table 39 - Input Power Sequencing for AT based configurations**

| Item | Description              | Value  |
|------|--------------------------|--------|
| T1   | VCC_RTC rise to VCC rise | ≥ 0 ms |
| T2   | VCC fall to VCC_RTC fall | ≥ 0 ms |

**Figure 14 - Input Power sequence for AT based configurations**



### 3.17.3. Power Sequencing for ATX based configurations

EDM1-CF-IMX6 input power sequencing requirements for ATX based configurations are as follow:

If a backup RealTime Clock (RTC) is required in the host system. We recommend to design an RTC circuit on the EDM carrier board. For example the Maxim Integrated DS1337+ connected over the general purpose I<sup>2</sup>C can be used.

#### **Start Sequence:**

Optional VCC\_RTC must come up at the same time or before 5VSB comes up.

5VSB must come up at the same time or before VCC comes up.

A 5V return signal is generated on EDM PIN# 251

PWGIN must be active at the same time or after VCC comes up.

#### **Stop Sequence:**

PWGIN must be inactive at the same time or before VCC goes down

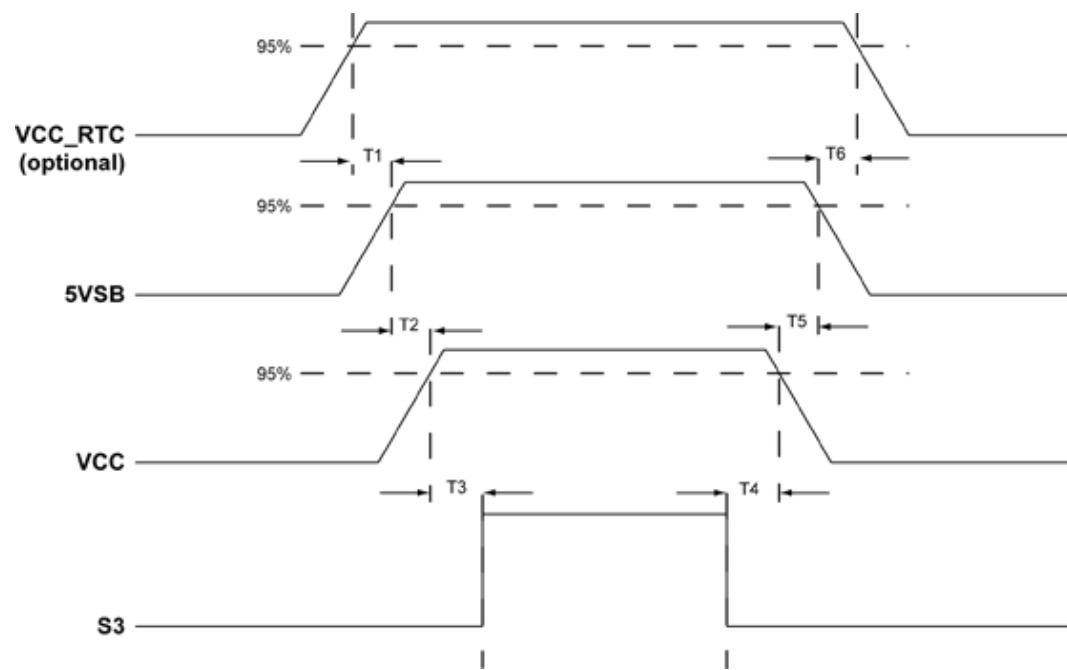
VCC must go down at the same time or before 5VSB goes down

5VSB must go down at the same time or before VCC\_RTC goes down

**Table 40 - Input Power Sequencing for ATX based configurations**

| Item | Description                 | Value       |
|------|-----------------------------|-------------|
| T1   | VCC_RTC rise to 5VSD rise   | $\geq 0$ ms |
| T2   | 5VSB rise to VCC rise       | $\geq 0$ ms |
| T3   | VCC rise to PWGIN (S3) rise | $\geq 0$ ms |
| T4   | PWGIN (S3) fall to VCC fall | $\geq 0$ ms |
| T5   | VCC fall to 5VSB fall       | $\geq 0$ ms |
| T6   | 5VSB fall to VCC_RTC fall   | $\geq 0$ ms |

**Figure 15 - Input Power sequence for ATX based configurations**

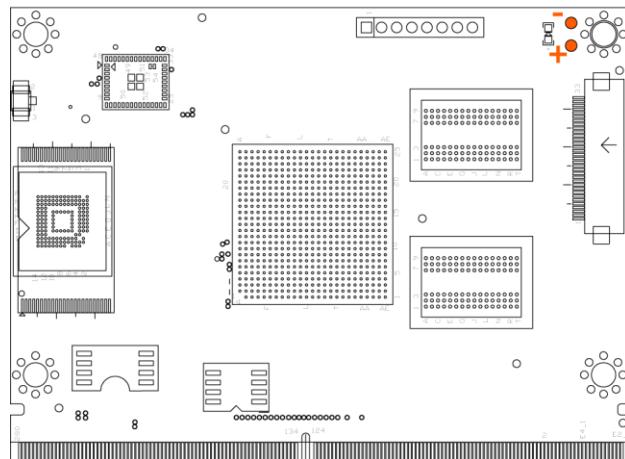


### 3.17.4. EDM1-CF-IMX6 Power Option without Carrier Board

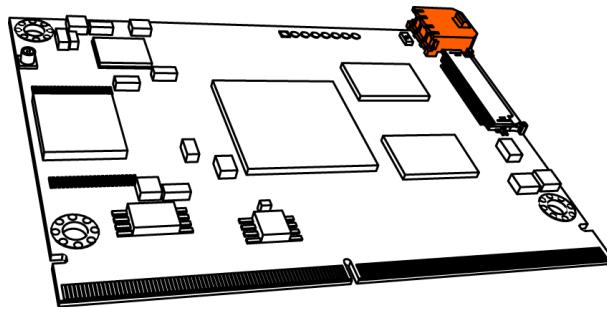
The EDM1-CF-IMX6 provides support to be powered without a carrier board by mounting a power connector that provides +5V to the System-on-Module directly.

A Molex 43650-0200 connector should be mounted at the following location.

**Figure 16 - EDM1-CF-IMX6 Optional Power Connector Location**

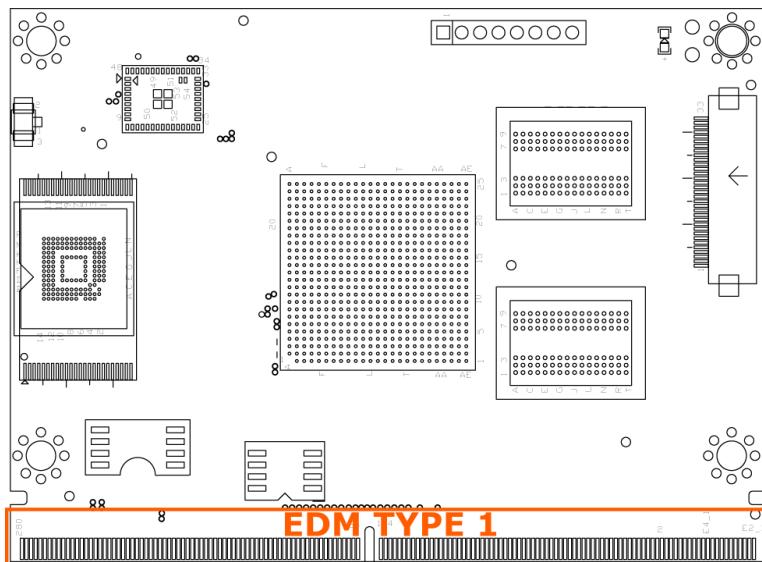


**Figure 17 - EDM1-CF-IMX6 with mounted Molex 43650-0200 Connector**



## 4. EDM Connector Pin Assignment

The EDM1-CF-IMX6 EDM connector 314 pin assignment is listed in the table below.



| EDM PIN | i.MX6 BALL       | PAD NAME | Signal    | V    | I/O | Description  |
|---------|------------------|----------|-----------|------|-----|--|
| E1_1    |                  |          | 5VSB      | 5VSB | P   | Standby Power Supply 5VDC ± 5%   |
| E2_1    |                  |          | 5VSB      | 5VSB | P   | Standby Power Supply 5VDC ± 5%   |
| E1_2    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_2    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_3    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_3    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_4    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_4    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_5    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_5    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_6    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_6    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_7    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_7    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_8    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_8    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_9    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_9    |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E1_10   |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E2_10   |                  |          | VCC       | 5V   | P   | Power Supply 5VDC ± 5%   |
| E3_1    |                  |          | GND       | GND  | P   | Ground   |
| E4_1    |                  |          | GND       | GND  | P   | Ground   |
| E3_2    | AR8031<br>pin 17 |          | GBE_MDI2+ | LAN  | I/O | Gigabit Ethernet Media<br>Dependent Interface (MDI)<br>differential pair 2 positive signal |

| EDM PIN | i.MX6 BALL    | PAD NAME    | Signal         | V         | I/O | Description  |
|---------|---------------|-------------|----------------|-----------|-----|--|
| E4_2    | AR8031 pin 11 |             | GBE_MDI0+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal |
| E3_3    | AR8031 pin 18 |             | GBE_MDI2-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal |
| E4_3    | AR8031 pin 12 |             | GBE_MDI0-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal |
| E3_4    |               |             | GND            | GND       | P   | Ground   |
| E4_4    |               |             | GND            | GND       | P   | Ground   |
| E3_5    | AR8031 pin 20 |             | GBE_MDI3+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal |
| E4_5    | AR8031 pin 14 |             | GBE_MDI1+      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal |
| E3_6    | AR8031 pin 21 |             | GBE_MDI3-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal |
| E4_6    | AR8031 pin 15 |             | GBE_MDI1-      | LAN       | I/O | Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal |
| E3_7    | AR8031 pin 23 |             | LED1_ACT       | CMOS 3.3V | O   | Gigabit Ethernet LED Activity indicator  |
| E4_7    |               |             | GND            | GND       | P   | Ground   |
| E3_8    |               |             | GND            | GND       | P   | Ground   |
| E4_8    | AR8031 pin 26 |             | LED1_nLink100  | CMOS 3.3V | O   | Gigabit Ethernet 100Mbit/sec LED link indicator                                      |
| E3_9    | U2            | LVDS0_TX0_N | LVDS_A0-       | LVDS      | O   | LVDS primary channel differential pair 0 negative signal                             |
| E4_9    | AR8031 pin 24 |             | LED1_nLink1000 | CMOS 3.3V | O   | Gigabit Ethernet 1000Mbit/sec LED link indicator                                     |
| E3_10   | U1            | LVDS0_TX0_P | LVDS_A0+       | LVDS      | O   | LVDS primary channel differential pair 0 positive signal                             |
| E4_10   |               |             | GND            | GND       | P   | Ground   |
| 1       |               |             | GND            | GND       | P   | Ground   |
| 2       | P24           | DISP0_DAT0  | LCD_D0         | TTL       | O   | LCD Pixel Data bit 0   |
| 3       | U4            | LVDS0_TX1_N | LVDS_A1-       | LVDS      | O   | LVDS primary channel differential pair 1 negative signal                             |
| 4       | P22           | DISP0_DAT1  | LCD_D1         | TTL       | O   | LCD Pixel Data bit 1   |
| 5       | U3            | LVDS0_TX1_P | LVDS_A1+       | LVDS      | O   | LVDS primary channel differential pair 1 positive signal                             |
| 6       |               |             | GND            | GND       | P   | Ground   |
| 7       |               |             | GND            | GND       | P   | Ground   |
| 8       | P23           | DISP0_DAT2  | LCD_D2         | TTL       | O   | LCD Pixel Data bit 2   |
| 9       | V2            | LVDS0_TX2_N | LVDS_A2-       | LVDS      | O   | LVDS primary channel differential pair 2 negative signal                             |
| 10      | P21           | DISP0_DAT3  | LCD_D3         | TTL       | O   | LCD Pixel Data bit 3   |
| 11      | V1            | LVDS0_TX2_P | LVDS_A2+       | LVDS      | O   | LVDS primary channel differential pair 2 positive signal                             |

| EDM PIN | i.MX6 BALL   | PAD NAME    | Signal        | V         | I/O | Description   |
|---------|--------------|-------------|---------------|-----------|-----|---|
| 12      |              |             | GND           | GND       | P   | Ground  |
| 13      |              |             | GND           | GND       | P   | Ground  |
| 14      | P20          | DISP0_DAT4  | LCD_D4        | TTL       | O   | LCD Pixel Data bit 4  |
| 15      | W2           | LVDS0_TX3_N | LVDS_A3-      | LVDS      | O   | LVDS primary channel differential pair 3 negative signal  |
| 16      | R25          | DISP0_DAT5  | LCD_D5        | TTL       | O   | LCD Pixel Data bit 5  |
| 17      | W1           | LVDS0_TX3_P | LVDS_A3+      | LVDS      | O   | LVDS primary channel differential pair 3 positive signal  |
| 18      |              |             | GND           | GND       | P   | Ground  |
| 19      |              |             | GND           | GND       | P   | Ground  |
| 20      | R23          | DISP0_DAT6  | LCD_D6        | TTL       | O   | LCD Pixel Data bit 6  |
| 21      | V4           | LVDS0_CLK_N | LVDS_ACLK-    | LVDS      | O   | LVDS primary channel clock negative signal  |
| 22      | R24          | DISP0_DAT7  | LCD_D7        | TTL       | O   | LCD Pixel Data bit 7  |
| 23      | V3           | LVDS0_CLK_P | LVDS_ACLK+    | LVDS      | O   | LVDS primary channel clock positive signal  |
| 24      |              |             | GND           | GND       | P   | Ground  |
| 25      |              |             | GND           | GND       | P   | Ground  |
| 26      | R22          | DISP0_DAT8  | LCD_D8        | TTL       | O   | LCD Pixel Data bit 8  |
| 27      | B19          | SD4_DAT1    | LVDS_ABL_CTRL | CMOS 3.3V | O   | LVDS primary channel panel backlight control  |
| 28      | T25          | DISP0_DAT9  | LCD_D9        | TTL       | O   | LCD Pixel Data bit 9  |
| 29      | D18          | SD4_DAT0    | LVDS_AEN      | CMOS 3.3V | O   | LVDS primary channel panel backlight enable   |
| 30      |              |             | GND           | GND       | P   | Ground  |
| 31      | NC           |             | LVDS_AVDD_EN  | CMOS 3.3V | O   | LVDS primary channel panel power enable   |
| 32      | R21          | DISP0_DAT10 | LCD_D10       | TTL       | O   | LCD Pixel Data bit 10   |
| 33      | NC           |             | eDP0_SELFTEST | CMOS 3.3V | I   | Embedded Display Port Detection pin   |
| 34      | i.MX6 pinT23 | DISP0_DAT11 | LCD_D11       | TTL       | O   | LCD Pixel Data bit 11   |
| 35      | NC           |             | eDP0_HPD      | CMOS 3.3V | I   | Embedded Display Port Hot Plug Detection pin  |
| 36      | T24          | DISP0_DAT12 | LCD_D12       | TTL       | O   | LCD Pixel Data bit 12   |
| 37      | G23          | EIM_D28     | I2C_SDA       | CMOS 3.3V | I/O | Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus data line   |
| 38      | R20          | DISP0_DAT13 | LCD_D13       | TTL       | O   | LCD Pixel Data bit 13   |
| 39      | H20          | EIM_D21     | I2C_SCL       | CMOS 3.3V | I/O | Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus clock line |
| 40      | U25          | DISP0_DAT14 | LCD_D14       | TTL       | O   | LCD Pixel Data bit 14   |
| 41      |              |             | GND           | GND       | P   | Ground  |
| 42      |              |             | GND           | GND       | P   | Ground  |
| 43      | J6           | HDMI_CLKP   | HDMI1_CLK+    | HDMI      | O   | HDMI differential pair clock positive signal  |

| EDM PIN | i.MX6 BALL | PAD NAME     | Signal     | V         | I/O | Description   |
|---------|------------|--------------|------------|-----------|-----|---|
| 44      | T22        | DISP0_DAT15  | LCD_D15    | TTL       | O   | LCD Pixel Data bit 15   |
| 45      | J5         | HDMI_CLKM    | HDMI1_CLK- | HDMI      | O   | HDMI differential pair clock negative signal  |
| 46      | T21        | DISP0_DAT16  | LCD_D16    | TTL       | O   | LCD Pixel Data bit 16   |
| 47      |            |              | GND        | GND       | P   | Ground  |
| 48      |            |              | GND        | GND       | P   | Ground  |
| 49      | K6         | HDMI_D0P     | HDMI1_D0+  | HDMI      | O   | HDMI differential pair 0 positive signal  |
| 50      | U24        | DISP0_DAT17  | LCD_D17    | TTL       | O   | LCD Pixel Data bit 17   |
| 51      | K5         | HDMI_D0M     | HDMI1_D0-  | HDMI      | O   | HDMI differential pair 0 negative signal  |
| 52      | V25        | DISP0_DAT18  | LCD_D18    | TTL       | O   | LCD Pixel Data bit 18   |
| 53      |            |              | GND        | GND       | P   | Ground  |
| 54      |            |              | GND        | GND       | P   | Ground  |
| 55      | J4         | HDMI_D1P     | HDMI1_D1+  | HDMI      | O   | HDMI differential pair 1 positive signal  |
| 56      | U23        | DISP0_DAT19  | LCD_D19    | TTL       | O   | LCD Pixel Data bit 19   |
| 57      | J3         | HDMI_D1M     | HDMI1_D1-  | HDMI      | O   | HDMI differential pair 1 negative signal  |
| 58      | U22        | DISP0_DAT20  | LCD_D20    | TTL       | O   | LCD Pixel Data bit 20   |
| 59      |            |              | GND        | GND       | P   | Ground  |
| 60      |            |              | GND        | GND       | P   | Ground  |
| 61      | K4         | HDMI_D2P     | HDMI1_D2+  | HDMI      | O   | HDMI differential pair 2 positive signal  |
| 62      | T20        | DISP0_DAT21  | LCD_D21    | TTL       | O   | LCD Pixel Data bit 21   |
| 63      | K3         | HDMI_D2M     | HDMI1_D2-  | HDMI      | O   | HDMI differential pair 2 negative signal  |
| 64      | V24        | DISP0_DAT22  | LCD_D22    | TTL       | O   | LCD Pixel Data bit 22   |
| 65      |            |              | GND        | GND       | P   | Ground  |
| 66      |            |              | GND        | GND       | P   | Ground  |
| 67      | K1         | HDMI_HPD     | HDMI1_HPD  | CMOS 3.3V | I   | HDMI/DP Hot plug detection signal that serves as an interrupt request   |
| 68      | W24        | DISP0_DAT23  | LCD_D23    | TTL       | O   | LCD Pixel Data bit 23   |
| 69      | NC         |              | HDMI1_CAD  | HDMI      | I/O | Cable Adaptor Detect  |
| 70      | N19        | DI0_DISP_CLK | LCD_CLK    | TTL       | O   | LCD Pixel Clock   |
| 71      | H19        | EIM_A25      | HDMI1_CEC  | HDMI      | I/O | HDMI Consumer Electronics Control   |
| 72      | N25        | DI0_PIN2     | LCD_HSYNC  | TTL       | O   | LCD Horizontal Synchronization  |
| 73      | H20        | EIM_D21      | I2C_SCL    | CMOS 5V   | I/O | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus clock line |
| 74      | N20        | DI0_PIN3     | LCD_VSYNC  | TTL       | O   | LCD Vertical Synchronization  |
| 75      | G23        | EIM_D28      | I2C_SDA    | CMOS 5V   | I/O | Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I <sup>2</sup> C bus data line  |
| 76      | P25        | DI0_PIN4     | LCD_BKLEN  | TTL       | O   | LCD backlight enable/disable  |

| EDM PIN | i.MX6 BALL | PAD NAME   | Signal     | V         | I/O | Description   |
|---------|------------|------------|------------|-----------|-----|---|
| 77      |            |            | GND        | GND       | P   | Ground  |
| 78      | N21        | DI0_PIN15  | LCD_DRD_Y  | TTL       | O   | LCD dot enable pin signal   |
| 79      | NC         |            | PCIEB_CLK+ | PCIE      | O   | PCI Express channel B clock differential pair positive signal           |
| 80      | A20        | SD4_DAT3   | LCD_VDDEN  | TTL       | O   | LCD Voltage On  |
| 81      | NC         |            | PCIEB_CLK- | PCIE      | O   | PCI Express channel B clock differential pair negative signal           |
| 82      | F17        | SD4_DAT2   | LCD_CNTRST | TTL       | O   | LCD Backlight brightness Control  |
| 83      |            |            | GND        | GND       | P   | Ground  |
| 84      |            |            | RSVD       |           |     | Reserved  |
| 85      | D7         | CLK1_P     | PCIEA_CLK+ | PCIE      | O   | PCI Express channel A clock differential pair positive signal           |
| 86      | F15        | NANDF_CS0  | GPMC_nCSA  | CMOS 3.3V | O   | GPMC Chip Select bit A  |
| 87      | C7         | CLK1_N     | PCIEA_CLK- | PCIE      | O   | PCI Express channel A clock differential pair negative signal           |
| 88      |            |            | GND        | GND       | P   | Ground  |
| 89      |            |            | GND        | GND       | P   | Ground  |
| 90      | C16        | NANDF_CS1  | GPMC_nCSB  | CMOS 3.3V | O   | GPMC Chip Select bit B  |
| 91      | B3         | PCIE_TXP   | PCIEA_TX+  | PCIE      | O   | PCI Express channel A Transmit output differential pair positive signal |
| 92      | A17        | NANDF_CS2  | GPMC_nCSC  | CMOS 3.3V | O   | GPMC Chip Select bit C  |
| 93      | A3         | PCIE_TXM   | PCIEA_TX-  | PCIE      | O   | PCI Express channel A Transmit output differential pair negative signal |
| 94      |            |            | GND        | GND       | P   | Ground  |
| 95      |            |            | GND        | GND       | P   | Ground  |
| 96      | D16        | NANDF_CS3  | GPMC_nCSD  | CMOS 3.3V | O   | GPMC Chip Select bit D  |
| 97      | B2         | PCIE_RXP   | PCIEA_RX+  | PCIE      | I   | PCI Express channel A Receive input differential pair positive signal   |
| 98      | NC         |            | GPMC_nCSE  | CMOS 3.3V | O   | GPMC Chip Select bit E  |
| 99      | B1         | PCIE_RXM   | PCIEA_RX-  | PCIE      | I   | PCI Express channel A Receive input differential pair negative signal   |
| 100     |            |            | GND        | GND       | P   | Ground  |
| 101     |            |            | GND        | GND       | P   | Ground  |
| 102     | B16        | NANDF_RB0  | GPMC_WAIT  | CMOS 3.3V | I   | External indication of wait   |
| 103     | NC         |            | PCIEB_TX+  | PCIE      | O   | PCI Express channel B Transmit output differential pair positive signal |
| 104     | E15        | NANDF_WP_B | GPMC_WP    | CMOS 3.3V | O   | GPMC Write Protect / Enable   |
| 105     | NC         |            | PCIEB_TX-  | PCIE      | O   | PCI Express channel B Transmit output differential pair negative signal |

| EDM PIN | i.MX6 BALL | PAD NAME   | Signal      | V         | I/O | Description  |
|---------|------------|------------|-------------|-----------|-----|--|
| 106     | C15        | NANDF_CLE  | GPMC_CLE    | CMOS 3.3V | O   | GPMC Lower Byte Enable. Also used for Command Latch Enable                             |
| 107     | NC         |            | PCIE_PRST#  | PCIE      | I   | PCI Express interface presence detection pin   |
| 108     | A16        | NANDF_ALE  | GPMC_ALE    | CMOS 3.3V | O   | GPMC Address Valid or Address Latch Enable   |
| 109     | NC         |            | PCIEB_RX+   | PCIE      | I   | PCI Express channel B Receive input differential pair positive signal                  |
| 110     | E16        | SD4_CLK    | GPMC_WE     | CMOS 3.3V | I   | GPMC Write Enable  |
| 111     | NC         |            | PCIEB_RX-   | PCIE      | I   | PCI Express channel B Receive input differential pair negative signal                  |
| 112     | B17        | SD4_CMD    | GPMC_RE     | CMOS 3.3V | O   | GPMC Read Enable   |
| 113     | NC         |            | PCIECLK_OEA | PCIE      | O   | PCI Express channel A hot plug detection signal  |
| 114     |            |            | RSVD        |           |     | Reserved   |
| 115     | NC         |            | PCIECLK_OEB | PCIE      | O   | PCI Express channel B hot plug detection signal  |
| 116     | NC         |            | GPMC_A10    | CMOS 3.3V | O   | GPMC output address bit 10   |
| 117     | NC         |            | PCIE_WAKE#  | CMOS 3.3V | I   | PCI Express Wake Event: Sideband wake signal asserted by components requesting wake up |
| 118     | NC         |            | GPMC_A9     | CMOS 3.3V | O   | GPMC output address bit 9  |
| 119     | H21        | EIM_D31    | PCIE_RST#   | CMOS 3.3V | O   | PCI Express Reset signal for external devices  |
| 120     | NC         |            | GPMC_A8     | CMOS 3.3V | O   | GPMC output address bit 8  |
| 121     |            |            | GND         | GND       | P   | Ground   |
| 122     | NC         |            | GPMC_A7     | CMOS 3.3V | O   | GPMC output address bit 7  |
| 123     | B14        | SATA_RXP   | SATA1_RXP   | SATA      | I   | Serial ATA channel 1 Receive differential pair positive signal                         |
| 124     |            |            | GND         | GND       | P   | Ground   |
| 125     | A14        | SATA_RXM   | SATA1_RXN   | SATA      | I   | Serial ATA channel 1 Receive differential pair negative signal                         |
| 126     |            |            | KEY         |           |     |  |
| 127     |            |            | KEY         |           |     |  |
| 128     |            |            | KEY         |           |     |  |
| 129     |            |            | KEY         |           |     |  |
| 130     |            |            | KEY         |           |     |  |
| 131     |            |            | KEY         |           |     |  |
| 132     |            |            | KEY         |           |     |  |
| 133     | M5         | CSI0_DAT15 | SATA1_nACT  | SATA      | I/O | Serial ATA LED. Open collector output pin driven during SATA command activity          |
| 134     | NC         |            | GPMC_A6     | CMOS 3.3V | O   | GPMC output address bit 6  |

| EDM PIN | I.MX6 BALL | PAD NAME   | Signal       | V         | I/O | Description   |
|---------|------------|------------|--------------|-----------|-----|---|
| 135     | A12        | SATA_TXP   | SATA1_TXP    | SATA      | O   | Serial ATA channel 1 Transmit differential pair positive signal               |
| 136     | NC         |            | GPMC_A5      | CMOS 3.3V | O   | GPMC output address bit 5   |
| 137     | B12        | SATA_TXM   | SATA1_TXN    | SATA      | O   | Serial ATA channel 1 Transmit differential pair negative signal               |
| 138     | NC         |            | GPMC_A4      | CMOS 3.3V | O   | GPMC output address bit 4   |
| 139     | R1         | GPIO_17    | USB1_HUB_RST | USB       | O   | Universal Serial Bus carrier board hub reset pin                              |
| 140     | NC         |            | GPMC_A3      | CMOS 3.3V | O   | GPMC output address bit 3   |
| 141     | T2         | GPIO_9     | USB2_OC      | CMOS 3.3V | I   | Over current detect input pin to monitor USB power over current               |
| 142     | NC         |            | GPMC_A2      | CMOS 3.3V | O   | GPMC output address bit 2   |
| 143     | NC         |            | StdB2_SSRX+  | USB       | I   | Universal Serial Bus Superspeed receiver differential pair positive signal    |
| 144     | NC         |            | GPMC_A1      | CMOS 3.3V | O   | GPMC output address bit 1   |
| 145     | NC         |            | StdB2_SSRX-  | USB       | I   | Universal Serial Bus Superspeed receiver differential pair negative signal    |
| 146     | NC         |            | GPMC_D15     | CMOS 3.3V | I/O | GPMC data bit 15  |
| 147     | NC         |            | GND2_DRAIN   | USB       | P   | Universal Serial Bus ground for signal return                                 |
| 148     |            |            | GND          | GND       | P   | Ground  |
| 149     | NC         |            | StdB2_SSTX+  | USB       | O   | Universal Serial Bus Superspeed transmitter differential pair positive signal |
| 150     | NC         |            | GPMC_D14     | CMOS 3.3V | I/O | GPMC data bit 14  |
| 151     | NC         |            | StdB2_SSTX-  | USB       | O   | Universal Serial Bus Superspeed transmitter differential pair negative signal |
| 152     | NC         |            | GPMC_D13     | CMOS 3.3V | I/O | GPMC data bit 13  |
| 153     |            |            | GND          | GND       | P   | Ground  |
| 154     |            |            | GND          | GND       | P   | Ground  |
| 155     | T4         | GPIO_1     | USB2_OTG_ID  | USB       | I   | Universal Serial Bus On-The-Go detection signal                               |
| 156     | NC         |            | GPMC_D12     | CMOS 3.3V | I/O | GPMC data bit 12  |
| 157     | A6         | USB_OTG_DP | USB2_D+      | USB       | I/O | Universal Serial Bus port 2 differential pair positive signal                 |
| 158     | NC         |            | GPMC_D11     | CMOS 3.3V | I/O | GPMC data bit 11  |
| 159     | B6         | USB_OTG_DN | USB2_D-      | USB       | I/O | Universal Serial Bus port 2 differential pair negative signal                 |
| 160     | NC         |            | GPMC_D10     | CMOS 3.3V | I/O | GPMC data bit 10  |

| EDM PIN | I.MX6 BALL | PAD NAME     | Signal      | V         | I/O | Description   |
|---------|------------|--------------|-------------|-----------|-----|---|
| 161     | E9         | USB_OTG_VBUS | USB2_VBUS   | 5V        | I/O | Universal Serial Bus port 2 power   |
| 162     | NC         |              | GPMC_D9     | CMOS 3.3V | I/O | GPMC data bit 9   |
| 163     | E23        | EIM_D22      | USB2_PWR_EN | USB       | O   | Universal Serial Bus power enable   |
| 164     | NC         |              | GPMC_D8     | CMOS 3.3V | I/O | GPMC data bit 8   |
| 165     | J20        | EIM_D30      | USB1_OC     | CMOS 3.3V | I   | Over current detect input pin to monitor USB power over current                   |
| 166     |            |              | GND         | GND       | P   | Ground  |
| 167     | NC         |              | StdB1_SSRX+ | USB       | I   | Universal Serial Bus Superspeed receiver differential pair positive signal        |
| 168     | C18        | NANDF_D7     | GPMC_D7     | CMOS 3.3V | I/O | GPMC data bit 7   |
| 169     | NC         |              | StdB1_SSRX- | USB       | I   | Universal Serial Bus Superspeed receiver differential pair negative signal        |
| 170     | E17        | NANDF_D6     | GPMC_D6     | CMOS 3.3V | I/O | GPMC data bit 6   |
| 171     | NC         |              | GND1_DRAIN  | USB       | P   | Universal Serial Bus ground for signal return                                     |
| 172     | B18        | NANDF_D5     | GPMC_D5     | CMOS 3.3V | I/O | GPMC data bit 5   |
| 173     | NC         |              | StdB1_SSTX+ | USB       | O   | Universal Serial Bus Superspeed transmitter differential pair positive signal     |
| 174     | A19        | NANDF_D4     | GPMC_D4     | CMOS 3.3V | I/O | GPMC data bit 4   |
| 175     | NC         |              | StdB1_SSTX- | USB       | O   | Universal Serial Bus Superspeed transmitter differential pair negative signal     |
| 176     | D17        | NANDF_D3     | GPMC_D3     | CMOS 3.3V | I/O | GPMC data bit 3   |
| 177     |            |              | GND         | GND       | P   | Ground  |
| 178     | F16        | NANDF_D2     | GPMC_D2     | CMOS 3.3V | I/O | GPMC data bit 2   |
| 179     | F10        | USB_H1_DN    | USB1_D-     | USB       | I/O | Universal Serial Bus port 1 differential pair negative signal                     |
| 180     | C17        | NANDF_D1     | GPMC_D1     | CMOS 3.3V | I/O | GPMC data bit 1   |
| 181     | E10        | USB_H1_DP    | USB1_D+     | USB       | I/O | Universal Serial Bus port 1 differential pair positive signal                     |
| 182     | A18        | NANDF_D0     | GPMC_D0     | CMOS 3.3V | I/O | GPMC data bit 0   |
| 183     | D10        | USB_H1_VBUS  | USB1_VBUS   | 5V        | I/O | Universal Serial Bus port 1 power   |
| 184     |            |              | GND         | GND       | P   | Ground  |
| 185     |            |              | GND         | GND       | P   | Ground  |
| 186     | U6         | KEY_ROW1     | I2S2_RXD    | CMOS 3.3V | I   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel receive data line |

| EDM PIN | I.MX6 BALL | PAD NAME  | Signal    | V         | I/O | Description  |
|---------|------------|-----------|-----------|-----------|-----|--|
| 187     | N3         | CSI0_DAT7 | I2S1_RXD  | CMOS 3.3V | I   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel receive data line              |
| 188     | U7         | KEY_COL1  | I2S2_TXFS | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel frame synchronization signal |
| 189     | N4         | CSI0_DAT6 | I2S1_TXFS | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel frame synchronization signal   |
| 190     | V6         | KEY_ROW0  | I2S2_TXD  | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel transmit data line           |
| 191     | P2         | CSI0_DAT5 | I2S1_TXD  | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel transmit data line             |
| 192     | W5         | KEY_COL0  | I2S2_TXC  | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel word clock signal            |
| 193     | N1         | CSI0_DAT4 | I2S1_TXC  | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel word clock signal              |
| 194     | T5         | GPIO_0    | I2S2_CLK  | CMOS 3.3V | O   | Secondary Integrated Interchip Sound (I <sup>2</sup> S) channel master clock signal          |
| 195     | T5         | GPIO_0    | I2S1_CLK  | CMOS 3.3V | O   | Primary Integrated Interchip Sound (I <sup>2</sup> S) channel master clock signal            |
| 196     | W21        | ENET_RXD0 | SPDIF_OUT | SPDIF     | O   | Sony / Philips Digital Interconnect Format Audio output                                      |
| 197     | T6         | KEY_COL4  | CAN2_TX   | CAN       | I/O | Secondary CAN (controller Area Network) transmit signal                                      |
| 198     |            |           | GND       | GND       | P   | Ground   |
| 199     | V5         | KEY_ROW4  | CAN2_RX   | CAN       | I/O | Secondary CAN (controller Area Network) receive signal                                       |
| 200     | W6         | KEY_COL2  | CAN1_TX   | CAN       | I/O | Primary CAN (controller Area Network) transmit signal  |
| 201     |            |           | GND       | GND       | P   | Ground   |
| 202     | W4         | KEY_ROW2  | CAN1_RX   | CAN       | I/O | Primary CAN (controller Area Network) receive signal   |
| 203     | T1         | GPIO_2    | SDIO_CD   | CMOS 3.3V | I/O | MMC/SDIO Card Detect   |
| 204     |            |           | GND       | GND       | P   | Ground   |
| 205     | B21        | SD1_CMD   | SDIO_CMD  | CMOS 3.3V | I/O | MMC/SDIO Command   |
| 206     | D20        | SD1_CLK   | SDIO_CLK  | CMOS 3.3V | O   | MMC/SDIO Clock   |
| 207     | N6         | CSI0_DAT8 | SDIO_WP   | CMOS 3.3V | I/O | MMC/SDIO Write Protect   |
| 208     | P4         | CSI0_MCLK | SDIO_LED  | CMOS 3.3V | O   | MMC/SDIO LED   |
| 209     | C20        | SD1_DAT1  | SDIO_DAT1 | CMOS 3.3V | I/O | MMC/SDIO Data bit 1  |

| EDM PIN | I.MX6 BALL | PAD NAME    | Signal    | V         | I/O | Description   |
|---------|------------|-------------|-----------|-----------|-----|---|
| 210     | P1         | CSI0_PIXCLK | SDIO_PWR  | CMOS 3.3V | O   | MMC/SDIO Power Enable   |
| 211     | F18        | SD1_DAT3    | SDIO_DAT3 | CMOS 3.3V | I/O | MMC/SDIO Data bit 3   |
| 212     | A21        | SD1_DAT0    | SDIO_DAT0 | CMOS 3.3V | I/O | MMC/SDIO Data bit 0   |
| 213     | NC         |             | SDIO_DAT5 | CMOS 3.3V | I/O | MMC/SDIO Data bit 5   |
| 214     | E19        | SD1_DAT2    | SDIO_DAT2 | CMOS 3.3V | I/O | MMC/SDIO Data bit 2   |
| 215     | NC         |             | SDIO_DAT7 | CMOS 3.3V | I/O | MMC/SDIO Data bit 7   |
| 216     | NC         |             | SDIO_DAT4 | CMOS 3.3V | I/O | MMC/SDIO Data bit 4   |
| 217     |            |             | GND       | GND       | P   | Ground  |
| 218     | NC         |             | SDIO_DAT6 | CMOS 3.3V | I/O | MMC/SDIO Data bit 6   |
| 219     | J23        | EIM_CS1     | SPI2_MOSI | CMOS 3.3V | O   | Serial Peripheral Interface primary channel master output slave input signal                                |
| 220     |            |             | GND       | GND       | P   | Ground  |
| 221     | J24        | EIM_OE      | SPI2_MISO | CMOS 3.3V | I   | Serial Peripheral Interface primary channel master input slave output signal                                |
| 222     | D24        | EIM_D18     | SPI1_MOSI | CMOS 3.3V | O   | Serial Peripheral Interface secondary channel master output slave input signal                              |
| 223     | H24        | EIM_CS0     | SPI2_CLK  | CMOS 3.3V | O   | Serial Peripheral Interface primary channel clock signal  |
| 224     | F21        | EIM_D17     | SPI1_MISO | CMOS 3.3V | I   | Serial Peripheral Interface secondary channel master input slave output signal                              |
| 225     | K20        | EIM_RW      | SPI2_CS0  | CMOS 3.3V | O   | Serial Peripheral Interface primary channel Chip Select 0 signal  |
| 226     | C25        | EIM_D16     | SPI1_CLK  | CMOS 3.3V | O   | Serial Peripheral Interface secondary channel clock signal  |
| 227     | K22        | EIM_LBA     | SPI2_CS1  | CMOS 3.3V | O   | Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used   |
| 228     | E22        | EIM_EB2     | SPI1_CS0  | CMOS 3.3V | O   | Serial Peripheral Interface secondary channel Chip Select 0 signal  |
| 229     |            |             | GND       | GND       | P   | Ground  |
| 230     | W6 (*)     | KEY_COL2    | SPI1_CS1  | CMOS 3.3V | O   | Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used |
| 231     | U5         | KEY_COL3    | I2C2_SCL  | CMOS 3.3V | I/O | I <sup>2</sup> C bus clock line   |
| 232     |            |             | GND       | GND       | P   | Ground  |

| EDM PIN | I.MX6 BALL     | PAD NAME   | Signal    | V         | I/O | Description   |
|---------|----------------|------------|-----------|-----------|-----|---|
| 233     | T7             | KEY_ROW3   | I2C2_SDA  | CMOS 3.3V | I/O | I <sup>2</sup> C bus data line  |
| 234     | B20            | SD4_DAT6   | UART2_CTS | UART      | O   | Universal Asynchronous Receive Transmit secondary channel clear to send signal                                      |
| 235     | R4             | GPIO_5     | I2C3_SCL  | CMOS 3.3V | I/O | I <sup>2</sup> C bus clock line   |
| 236     | D19            | SD4_DAT7   | UART2_TXD | UART      | O   | Universal Asynchronous Receive Transmit secondary channel transmit data signal                                      |
| 237     | R2             | GPIO_16    | I2C3_SDA  | CMOS 3.3V | I/O | I <sup>2</sup> C bus data line  |
| 238     | E18            | SD4_DAT4   | UART2_RXD | UART      | I   | Universal Asynchronous Receive Transmit secondary channel receive data signal                                       |
| 239     |                |            | GND       | GND       | P   | Ground  |
| 240     | C19            | SD4_DAT5   | UART2_RTS | UART      | O   | Universal Asynchronous Receive Transmit secondary channel request to send signal                                    |
| 241     | G21            | EIM_D19    | UART1_CTS | UART      | O   | Universal Asynchronous Receive Transmit secondary channel clear to send signal                                      |
| 242     | NC             |            | UART2_DCD | UART      | I   | Universal Asynchronous Receive Transmit secondary channel carrier detect signal                                     |
| 243     | M1             | CSI0_DAT10 | UART1_TXD | UART      | O   | Universal Asynchronous Receive Transmit secondary channel transmit data signal                                      |
| 244     | NC             |            | UART2_DSR | UART      | I   | Universal Asynchronous Receive Transmit secondary channel data set ready signal                                     |
| 245     | M3             | CSI0_DAT11 | UART1_RXD | UART      | I   | Universal Asynchronous Receive Transmit secondary channel receive data signal                                       |
| 246     | NC             |            | UART2_DTR | UART      | O   | Universal Asynchronous Receive Transmit secondary channel data terminal ready signal                                |
| 247     | G20            | EIM_D20    | UART1_RTS | UART      | O   | Universal Asynchronous Receive Transmit secondary channel request to send signal                                    |
| 248     | NC             |            | UART2_RI  | UART      | I   | Universal Asynchronous Receive Transmit secondary channel ring indication signal                                    |
| 249     |                |            | GND       | GND       | P   | Ground  |
| 250     |                |            | GND       | GND       | P   | Ground  |
| 251     | 5VSB with 10KΩ |            | S3        | CMOS 3.3V | O   | S3 signal shuts off power to all runtime system components that are not maintained during S3 state (suspend to RAM) |
| 252     | D12            | ONOFF      | ON/OFF    | CMOS 3.3V | I   | Power ON button input signal  |

| EDM PIN | i.MX6 BALL | PAD NAME   | Signal | V         | I/O | Description  |
|---------|------------|------------|--------|-----------|-----|--|
| 253     | NC         |            | S5     | CMOS 3.3V | O   | S5 signal shuts off power to the system. Restart is only possible with power button or by a system wake up event |
| 254     | C11        | POR_B      | RESET  | CMOS 3.3V | I   | Reset button input signal  |
| 255     | L6         | CSI0_DAT19 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 256     | L4         | CSI0_DAT16 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 257     | M6         | CSI0_DAT18 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 258     | E25        | EIM_D27    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 259     | E24        | EIM_D26    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 260     | N22        | EIM_BCLK   | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 261     | L3         | CSI0_DAT17 | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 262     | W23        | ENET_RX_ER | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 263     | P5         | GPIO_19    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 264     | D15        | SD3_RST    | GPIO   | CMOS 3.3V | I/O | General Purpose Input Output   |
| 265     |            |            | GND    | GND       | P   | Ground   |
| 266     |            |            | GND    | GND       | P   | Ground   |
| 267     | M23        | EIM_DA13   | MNF    |           | I   | Pins for manufacturing and validation purposes   |
| 268     | MNF        |            | MNF    |           |     | Pins for manufacturing and validation purposes   |
| 269     | N23        | EIM_DA14   | MNF    |           | I   | Pins for manufacturing and validation purposes   |
| 270     | MNF        |            | MNF    |           |     | Pins for manufacturing and validation purposes   |
| 271     | L22        | EIM_DA4    | MNF    |           | I   | Pins for manufacturing and validation purposes   |
| 272     | MNF        |            | MNF    |           |     | Pins for manufacturing and validation purposes   |
| 273     | L23        | EIM_DA5    | MNF    |           | I   | Pins for manufacturing and validation purposes   |
| 274     | MNF        |            | MNF    |           |     | Pins for manufacturing and validation purposes   |
| 275     | K25        | EIM_DA6    | MNF    |           | I   | Pins for manufacturing and validation purposes   |
| 276     | MNF        |            | MNF    |           |     | Pins for manufacturing and validation purposes   |
| 277     | L25        | EIM_DA7    | MNF    |           | I   | Pins for manufacturing and validation purposes   |
| 278     | M20        | EIM_DA11   | MNF    |           | I   | Pins for manufacturing and validation purposes   |

| EDM PIN | i.MX6 BALL | PAD NAME | Signal   | V         | I/O | Description                                    |
|---------|------------|----------|----------|-----------|-----|--|
| 279     | NC         |          | Watchdog | CMOS 3.3V | O   | Watchdog event indication signal               |
| 280     | M24        | EIM_DA12 | MNF      |           | I   | Pins for manufacturing and validation purposes |
| 281     | NC         |          | VCC_RTC  | 3.3V      | I   | Input power for RTC clock                      |

## 5. Development Kits, Proto-type Components and Accessories

To evaluate the EDM1-CF-IMX6 TechNexion has made available a large number of evaluation kits and accessories available.

For general evaluation purposes:

- EDM1-CF-IMX6 Evaluation start kits
  - i.MX6 Solo (with and without WiFi/Bluetooth)
  - i.MX6 Duallite
  - i.MX6 Dual
  - i.MX6 Quad
- EDM1-FAIRY-START Evaluation Carrier Board
- Various Display and Touch solutions

For proto-type and mass production:

- EDM Connectorkits
- Heatsinks
- Anteannakits

## 5.1. EDM1-CF-IMX6 Evaluation Kits

### 5.1.1. EDM1CFIMX6S10START Evaluation Start Kit Pack Content



| Item | Partnumber               | Description   |
|------|--------------------------|---|
| 1    | EDM1CFIMX6S10R512NI4GL2C | EDM Compact Type 1 Freescale i.MX6 Solo 1Ghz + 512MB RAM + 4GB eMMC + Gigabit LAN + 2 CAN |

### 5.1.2. EDM1CFIMX6S10BWSTART Evaluation Start Kit Pack Content



| Item | Partnumber                 | Description   |
|------|----------------------------|---|
| 1    | EDM1CFIMX6S10R512NI4GBWL2C | EDM Compact Type 1 Freescale i.MX6 Solo 1Ghz + 512MB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + 802.11bgn + Bluetooth 4.0 |
| 2    | EDMANTP150A138045D2450BK   | 4.5 dB, 2.4/5 GHz, black color antenna<br>U.FL to SMA patch cable   |

### 5.1.3. EDM1CFIMX6U10START Evaluation Start Kit Pack Content



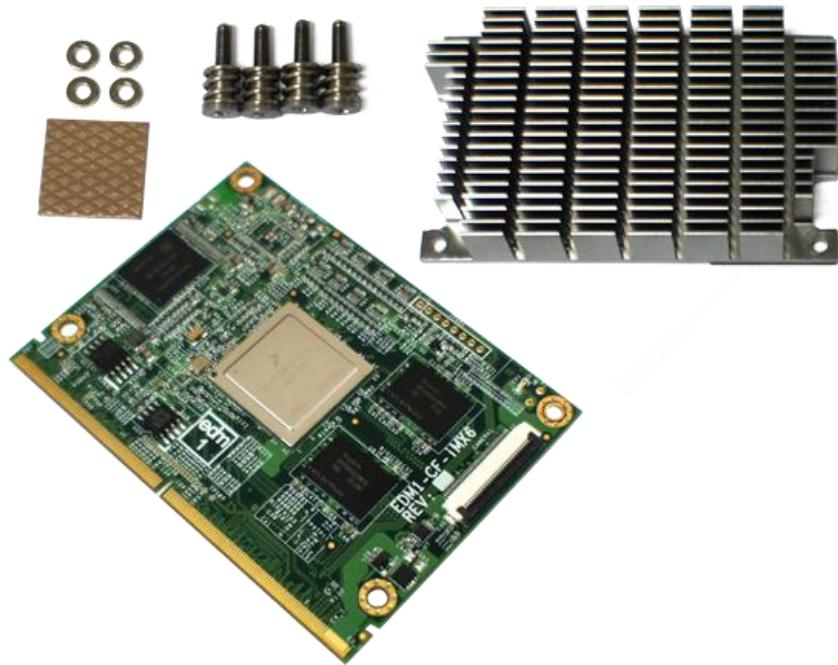
| Item | Partnumber               | Description   |
|------|--------------------------|---|
| 1    | EDM1CFIMX6U10R1GBNI4GL2C | EDM Compact Type 1 Freescale i.MX6 Duallite 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN |

### 5.1.4. EDM1CFIMX6U10BWSTART Evaluation Start Kit Pack Content



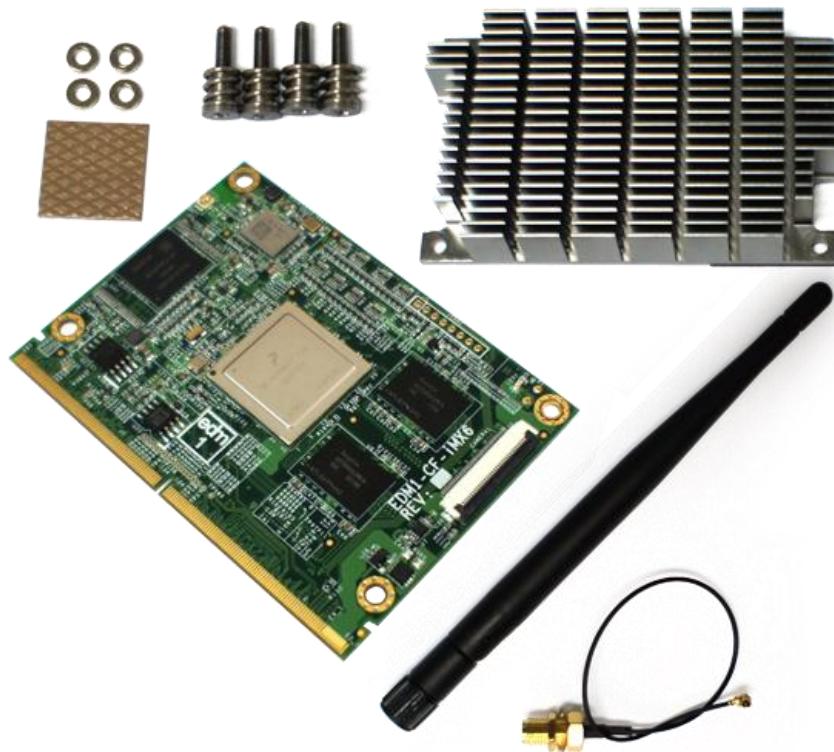
| Item | Partnumber                 | Description   |
|------|----------------------------|---|
| 1    | EDM1CFIMX6U10R1GBNI4GBWL2C | EDM Compact Type 1 Freescale i.MX6 Duallite 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + 802.11bgn + Bluetooth 4.0 |
| 2    | EDMANTP150A138045D2450BK   | 4.5 dB, 2.4/5 GHz, black color antenna<br>U.FL to SMA patch cable   |

### 5.1.5. EDM1CFIMX6D10START Evaluation Start Kit Pack Content



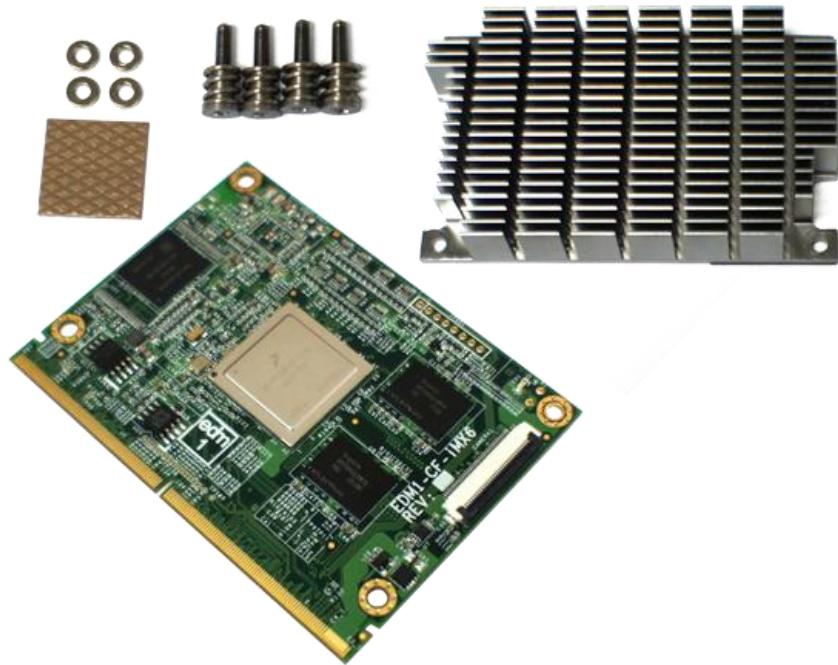
| Item | Partnumber                | Description  |
|------|---------------------------|--|
| 1    | EDM1CFIMX6D10R1GBNI4GLS2C | EDM Compact Type 1 Freescale i.MX6 Dual 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA |
| 2    | EDMHSCP12200501           | EDM Compact 12 mm passive heatsink + mylar   |
|      |                           | 4 screws   |
|      |                           | 4 washers  |
|      |                           | 20*20 mm thermopad with 0.5 mm thickness for Lidded Freescale CPUs                             |

### 5.1.6. EDM1CFIMX6D10BWSTART Evaluation Start Kit Pack Content



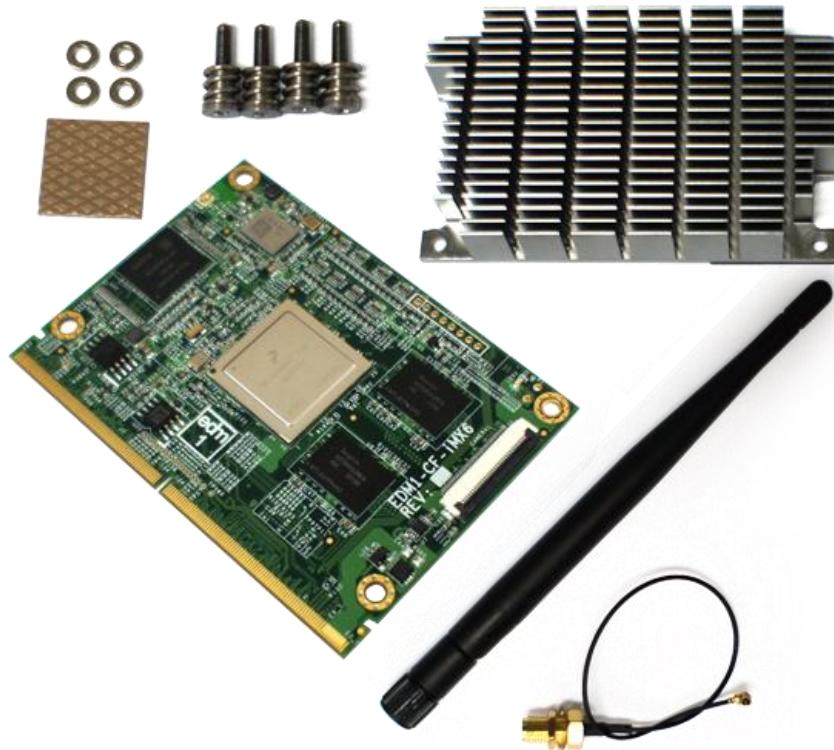
| Item | Partnumber                  | Description   |
|------|-----------------------------|---|
| 1    | EDM1CFIMX6D10R1GBNI4GBWLS2C | EDM Compact Type 1 Freescale i.MX6 Dual 1Ghz + 1GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA + 802.11bgn + Bluetooth 4.0                |
| 2    | EDMHSCP12200501             | EDM Compact 12 mm passive heatsink + mylar<br>4 screws<br>4 washers<br>20*20 mm thermopad with 0.5 mm thickness for Lidded Freescale CPUs |
| 3    | EDMANTP150A138045D2450BK    | 4.5 dB, 2.4/5 GHz, black color antenna<br>U.FL to SMA patch cable   |

### 5.1.7. EDM1CFIMX6Q10START Evaluation Start Kit Pack Content



| Item | Partnumber                | Description  |
|------|---------------------------|--|
| 1    | EDM1CFIMX6Q10R2GBNI4GLS2C | EDM Compact Type 1 Freescale i.MX6 Quad 1Ghz + 2GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA |
| 2    | EDMHSCP12200501           | EDM Compact 12 mm passive heatsink + mylar   |
|      |                           | 4 screws   |
|      |                           | 4 washers  |
|      |                           | 20*20 mm thermopad with 0.5 mm thickness for Lidded Freescale CPUs                             |

### 5.1.8. EDM1CFIMX6Q10BWSTART Evaluation Start Kit Pack Content



| Item | Partnumber                  | Description   |
|------|-----------------------------|---|
| 1    | EDM1CFIMX6Q10R2GBNI4GBWLS2C | EDM Compact Type 1 Freescale i.MX6 Quad 1Ghz + 2GB RAM + 4GB eMMC + Gigabit LAN + 2 CAN + SATA + 802.11bgn + Bluetooth 4.0                |
| 2    | EDMHSCP12200501             | EDM Compact 12 mm passive heatsink + mylar<br>4 screws<br>4 washers<br>20*20 mm thermopad with 0.5 mm thickness for Lidded Freescale CPUs |
| 3    | EDMANTP150A138045D2450BK    | 4.5 dB, 2.4/5 GHz, black color antenna<br>U.FL to SMA patch cable   |

## 5.2. EDM1-FAIRY Carrier Board Evaluation Kits

The EDM1-CF-IMX6 System-on-Module requires a carrier board that contains the interfaces and connectors required for the end equipment application. The EDM1-FAIRY is the ideal evaluation carrier board for the EDM1-CF-IMX6.

### 5.2.1. EDM1FAIRYSTART Evaluation Start Kit Pack Content



| Item | Partnumber     | Description  |
|------|----------------|--|
| 1    | EDM1FAIRYSTART | EDM1-FAIRY Carrier Board for EDM1 modules<br>EDM-MNF-BOOT control/debug PCB Board<br>36 Watt DC Adaptor (12V 3A)<br>DC Jack to Phoenix power convertor<br>AC cables (EU/UK/USA plug)<br>SATA data and power cable (1 set)<br>CAN bus pinheader to DB9 cables (2 pcs)<br>Serial port pinheader to DB9 cable (1 pcs)<br>USB-OTG 3.0 to USB Host cable (1 pcs)<br>Mounting poses and fastening screws (1 set) |

### 5.3. EDM1-FAIRY Compatible Displays

#### 5.3.1. TDHJ070NA4RESKIT Resistive Touch Display Kit Pack Content



| Item | Partnumber       | Description  |
|------|------------------|--|
| 1    | TDHJ070NA4RESKIT | 7 inch LVDS interface LCD display 1024*600 resolution<br>250 nits with 4 wire resistive touchsensor. |
|      |                  | Adaptor interface board to easily connect to EDM<br>Carrier boards                                   |
|      |                  | LVDS signal cable  |
|      |                  | Touch panel link cable   |

NOTE: Many other display and touch solutions are available. Please connect with your TechNexion distributor or account manager for conditions and availability.

### 5.3.2. TDHJ070NAPCAPKIT PCAP Touch Display Kit Pack Content



| Item | Partnumber       | Description   |
|------|------------------|---|
| 1    | TDHJ070NAPCAPKIT | 7 inch LVDS interface LCD display 1024*600 resolution<br>500 nits with PCAP multitouch touchsensor. |
|      |                  | Adaptor interface board to easily connect to EDM<br>Carrier boards                                  |
|      |                  | LVDS signal cable   |
|      |                  | USB Touch panel link cable  |

NOTE: Many other display and touch solutions are available. Please connect with your TechNexion distributor or account manager for conditions and availability.

## 5.4. EDM Prototyping Accessories

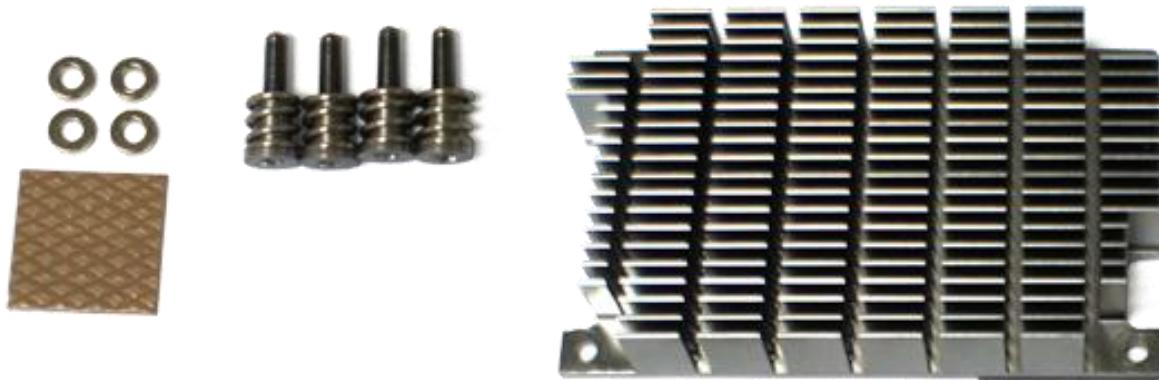
### 5.4.1. EDMCONNECTORKIT Pack Content



| Item | Partnumber      | Description                         |
|------|-----------------|-------------------------------------|
| 1    | EDMCONNECTORKIT | 10 EDM Connectors (AS0B821-S78B-7H) |
|      |                 | 40 M3 6mm mounting screws           |
|      |                 | 40 mounting poses                   |

NOTE: For mass production quantities we can offer tape and reel connectors and mounting poses.  
Please connect with your TechNexion distributor or account manager for conditions and availability.

#### 5.4.2. EDMHSCP12200501 Pack Content



| Item | Partnumber      | Description  |
|------|-----------------|--|
| 1    | EDMHSCP12200501 | EDM Compact 12 mm passive heatsink + mylar                         |
|      |                 | 4 screws   |
|      |                 | 4 washers  |
|      |                 | 20*20 mm thermopad with 0.5 mm thickness for Lidded Freescale CPUs |

### 5.4.3. EDMANTP150A138045D2450BK Pack Content.



| Item | Partnumber               | Description   |
|------|--------------------------|---|
| 1    | EDMANTP150A138045D2450BK | 4.5 dB, 2.4/5 GHz, black color antenna<br>U.FL to SMA patch cable |

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TechNexion Ltd.  
16F-5, No. 736, Zhongzheng Road,  
ZhongHe District, 23511, New Taipei City, Taiwan  
Phone : +886-2-82273585  
Fax : +886-2-82273590  
E-mail : sales@technexion.com  
Web : <http://www.technexion.com/>