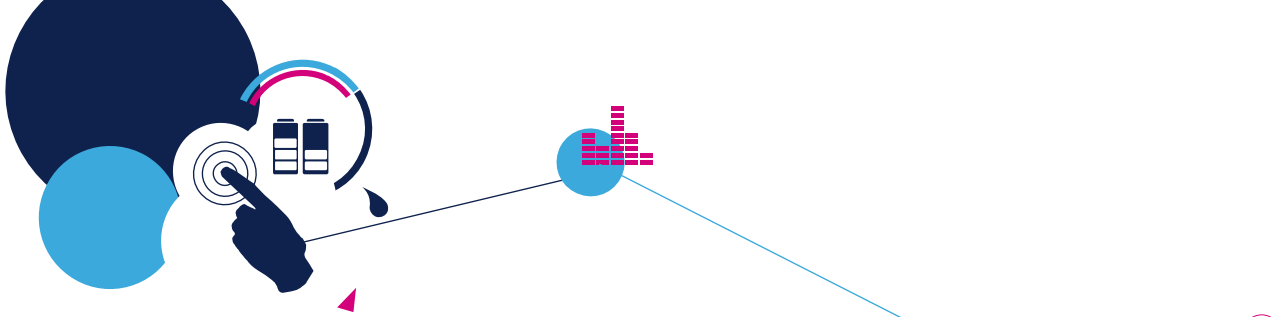

STM32L4 – Architecture

STM32L4 workshop

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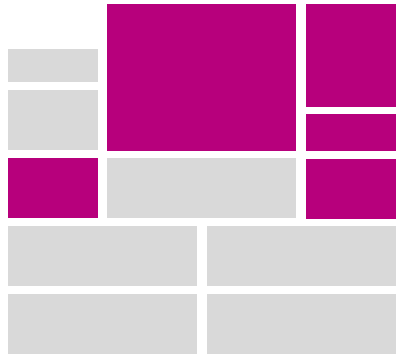
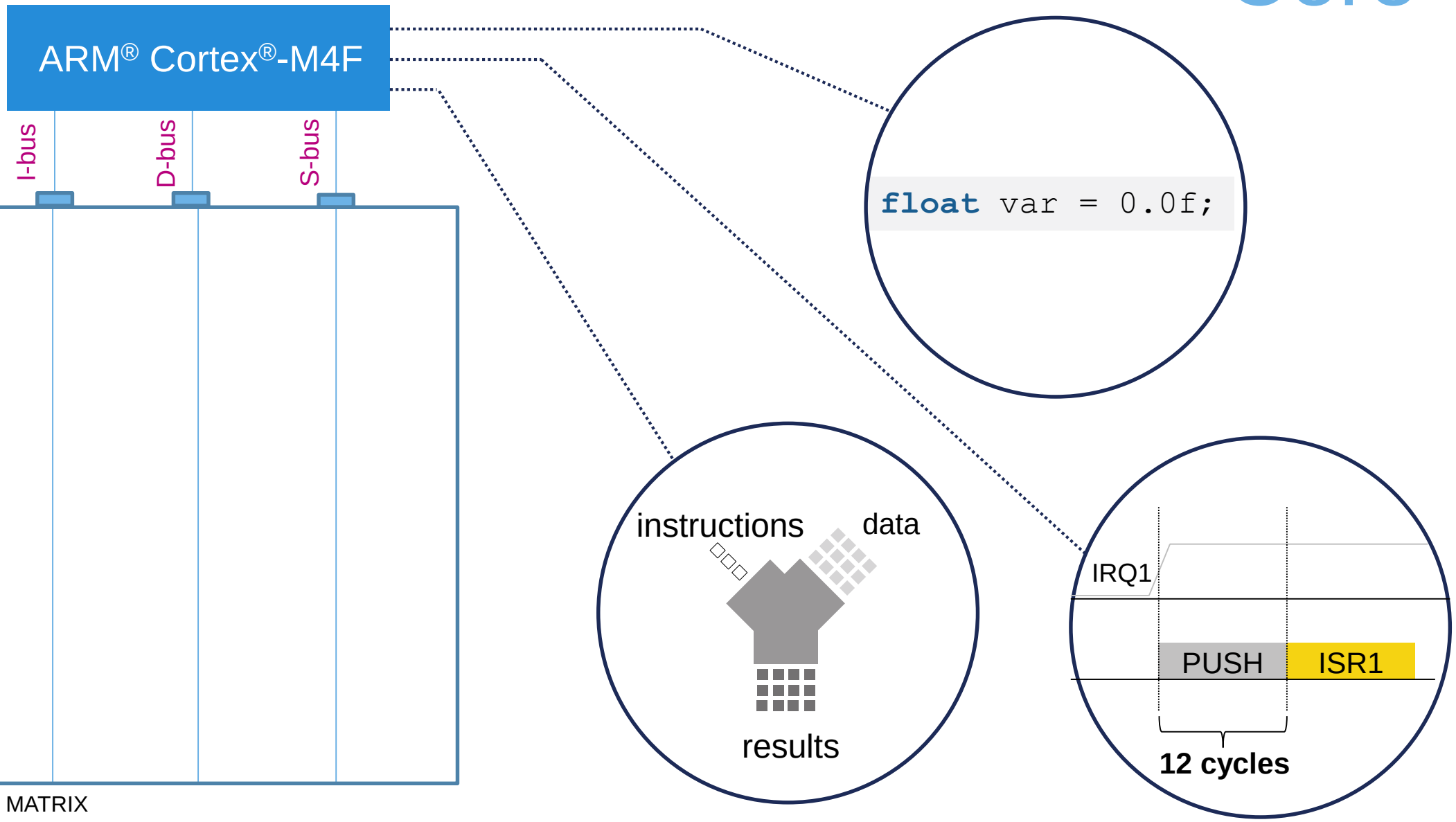
Goal of this part

- Go through the STM32L4 internal structure
- List the key features of main system blocks and peripherals
- Give global overview of the STM32L4 capabilities

1 High-performance




ARM® Cortex®-M4F
I-bus
D-bus
S-bus
BUS MATRIX
float var = 0.0f;
instructions
data
results
IRQ1
PUSH
ISR1
12 cycles

Memory

STM32 L4

ARM® Cortex®-M4F

I-bus D-bus S-bus

BUS MATRIX

~0WS at whatever CPU frequency

Dual-Bank (RWW)

1kB OTP memory

ART

FLASH (1MB)

OTP

System Memory

SRAM1 (96kB)

SRAM2 (32kB)

Bootloaders, calibration values

FMC QUADSPI

NOR FLASH
NAND FLASH
PSRAM
SRAM

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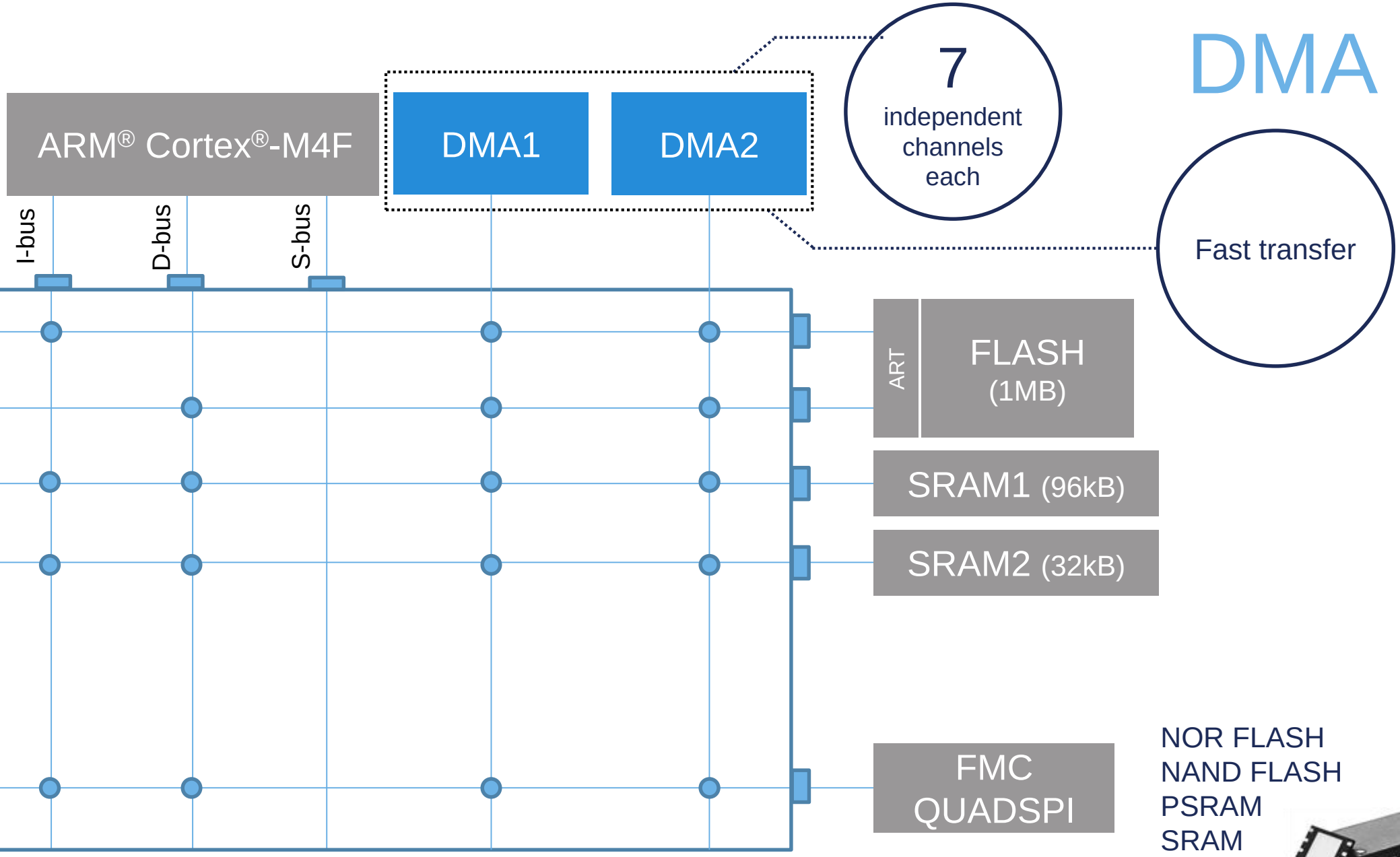
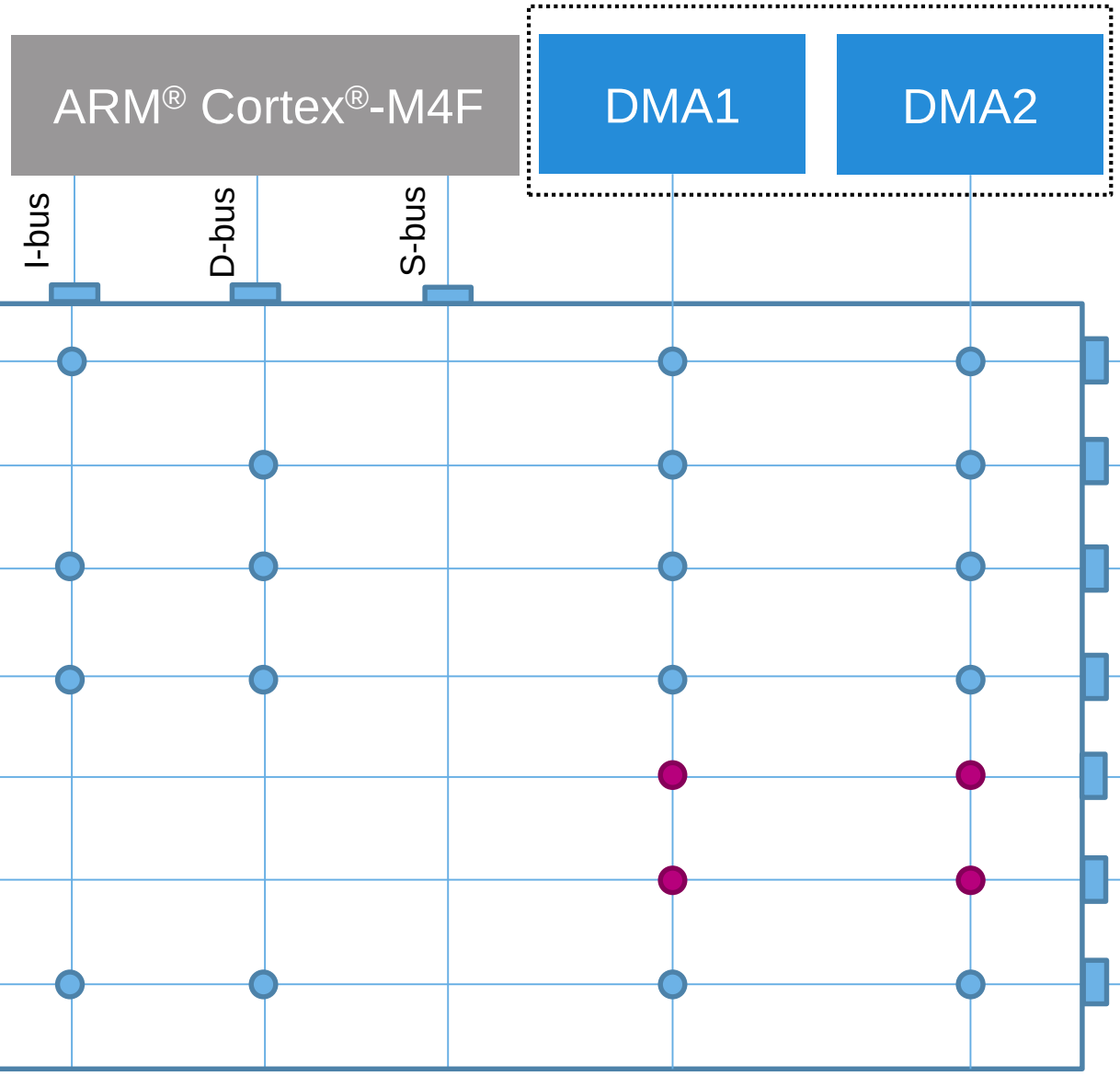
DMA



BUS MATRIX

DMA



Access to Everything

Triggered by whatever peripheral

Fast and Slow peripherals

ART
FLASH (1MB)

SRAM1 (96kB)

SRAM2 (32kB)

AHB1 Periph.

APB1 Periph.

APB2 Periph.

AHB2 Periph.

GPIO
ADC
USB
AES
RNG

FMC
QUADSPI

Clock Sources Parameters

80MHz max

CLK Source	Frequency	Conso	Precision (0-85°C)	Settling time
RESET → MSI (default)	100kHz~48MHz (4MHz default)	**0.6~155µA**	-3.5%~+3%	**10~2.5µs**
MSI (in PLL mode)	100kHz~48MHz		60ps (cycle to cycle jitter)	**252.5µs** (10% of final freq)
HSI	16MHz	155µA	**±1%**	3.8 µs
HSE external crystal	4~48MHz	**~440µA** (8MHz, 10pF)	~ ±0.01% (100ppm)	**2ms**
PLL	2~80MHz	~520µA (@344MHz VCO)	N/A	15µs (2MHz input)
LSI	32kHz	0.11µA	**~10%**	125µs
LSE external crystal	32.768kHz (typ.)	**~0.25µA**	~0.002% (20ppm)	**~2s**

Including stabilization time

+ Clock Source Wake-Up time

LSE usually woken-up only once after power-on

Debug support

- STM32L4 provides on-chip debug support
  - MCU programming
  - Application debugging
  - Code analysis

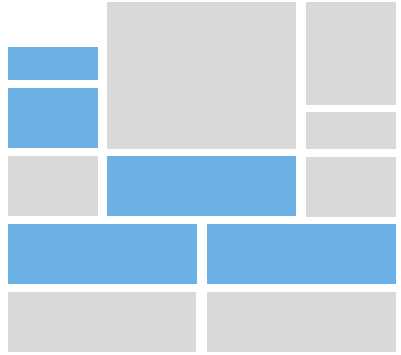
Application benefits

- Basic debugging features
- Advanced features (Embedded Trace Macrocell) to quickly identify malfunctioning code
- Coverage and profiling features

STM32L4 series

1. **High-performance**

2. **Peripherals rich**



Connectivity

STM32 L4

6 UART

- up to 10Mbit/s
- 7, 8, 9 data bits
- Even/odd or no-parity
- Synchronous mode (Master)
- Swappable Tx/Rx pins
- Auto-baudrate detection

IrDA SIR, Smartcard, Modbus, LIN, RS-232/485 flow control

3 I2C

SMBus 2.0
PMBus 1.1

- up to 1Mbit/s (Fast Mode+)
- Master or Slave (Multi)
- 7b and 10b addressing mode
- Multiple 7b addressing mode
- Clock stretching support
- Fully programmable timing

3 SPI

- up to 40MHz ($f_{PCLK/2}$)
- Master or Slave (Multi)
- Full/Half-duplex or Simplex
- Two-wire interface as min.
- Motorola and TI standards
- Tx & Rx FIFOs, CRC

1 USB

- USB2.0 Full Speed (12Mbps)
- OTG2.0 spec support
- Link Power Management
- Battery Charger Detection
- HSE crystal not needed (thanks to MSI in PLL mode)

!

1 CAN

- up to 1Mbit/s
- CAN protocol v2.0A and B
- 2x receive FIFO (3 stages)
- 14 scalable filter banks
- HSE crystal not needed (thanks to 1% HSI)

1 SDMMC

- default speed (<25MHz)
- high-speed support (50MHz)
- 1b, 4b and 8b data mode
- Secure Digital (SD) 2.0
- MultiMediaCard (MMC) 4.2
- SD I/O devices (SDIO) 2.0

Wi-Fi, Bluetooth, Camera, Memory modules

DMA support by all these peripherals

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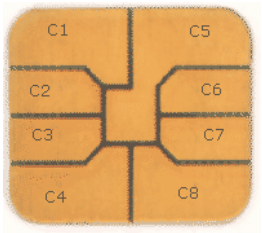
Connectivity addon

1 SWPMI

- 100Kbit/s to 2Mbit/s
- single-wire protocol
- ETSI TS 102 613 standard (Master mode)
- Smartcard interface



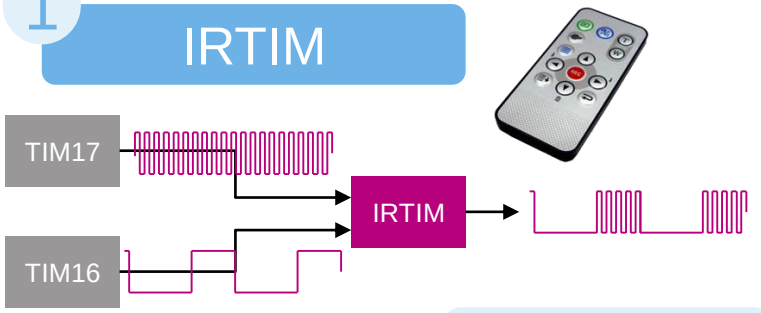
2 SAI

- up to 32-bit/192kHz
- various protocols support (including SPDIF and AC'97)

1 DFSDM

REVEALED LATER

1 IRTIM



Supports RC5, RC6, RCA, SIRC,…

Up to 20mA direct IR LED driving

„Analog chain“

- low consumption (down to 400nA)
- progr. hysteresis (0, 8, 15 or 27mV)
- low propag. delay (down to 0.1µs)

COMP1

COMP2

- up to 4mA output (35µA I_{VDDA})
- low error with load -3/+1(2.048V), ±2 (2.5V)

VREFINT

1.2V

VREFBUF

V_{REF+}

ADC/DAC

2.048V / 2.5V

V_{BAT}

$V_{BAT}/3$

DAC1

DAC2

- 2 channels DAC
- 8b or 12b resolution
- Buffered output
- S&H for low-power app
- Noise & Triangular wave generator

OPAMP1

OPAMP2

PGA

- Rail-to-Rail In/Out
- Normal mode (120µA, 1.6MHz GBW)
- LP mode (45µA, 0.42MHz GBW)

Timers / IRQ

Tsensor

- 4.7µA, 70µs (ON)
- 5µs sampling
- 2.5mV/°C slope
- factory calibration (30°C, 110°C)

V_{TS}

ADC1

ADC2

ADC3

- up to 5.33 Msamples/s (12-bit SAR)
- 16-bit with oversampling
- Sequencer, Differential inputs
- Low consumption (210µA @1MSps)
- 3x analog watchdog per ADC

GPIO

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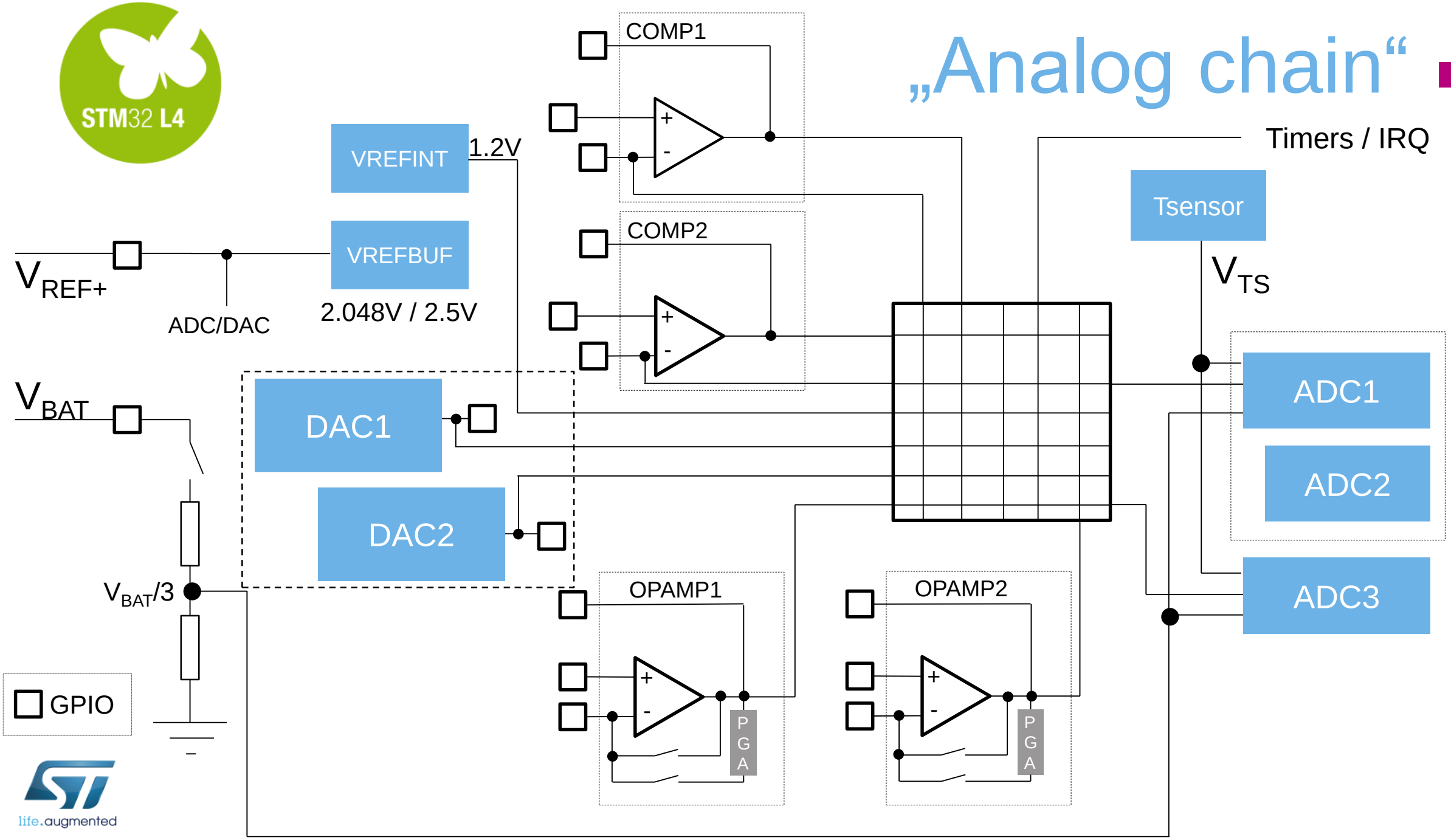
„Analog chain“



Control logic

14

TIM

- 11x 16-bit timers
- 2x 32-bit timers
- 1x 24-bit SysTick (Core)
- 2x Low-Power timer
- 17x CAPCOM in total
- 9x CAPCOM with compl. out

Suitable for motor control

300nA @1.8V

RTC

- full calendar support (BCD)
- 2x Alarm (subsecond res.)
- Periodic Wake-Up Timer
- 3x Tamper pins (opt. filtering)
- Smooth digital calibration
- Inside V_{BAT} domain

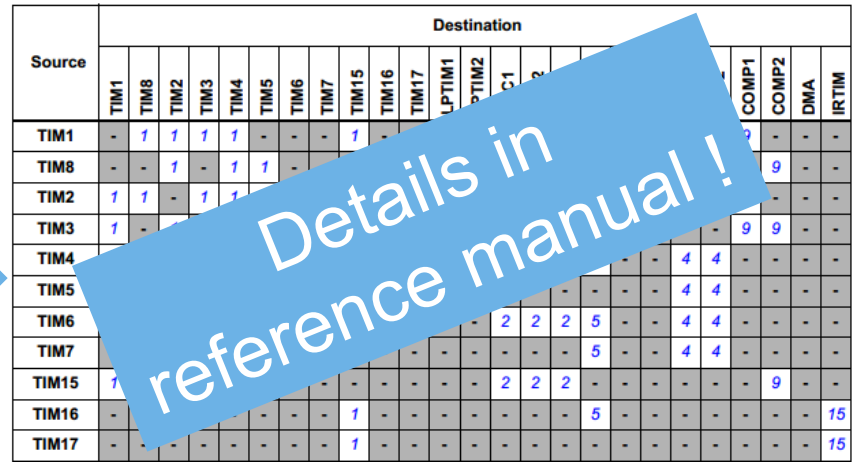
GLASS LCD

- up to 176 (44x4) or 320 (40x8) segments
- 1/2, 1/3, 1/4, 1/8 or static duty
- 1/2, 1/3, 1/4 or static bias
- Dual-buffer LCD_RAM
- Internal STEP-UP

1.5µA @3.0V
1/8 duty, 1/4 bias
64div ratio

TSC

- up to 24 channels / 8 groups
- one capacitor for up to 3ch
- full hardware management
- Spread spectrum to improve EMI robustness



interconnection matrix

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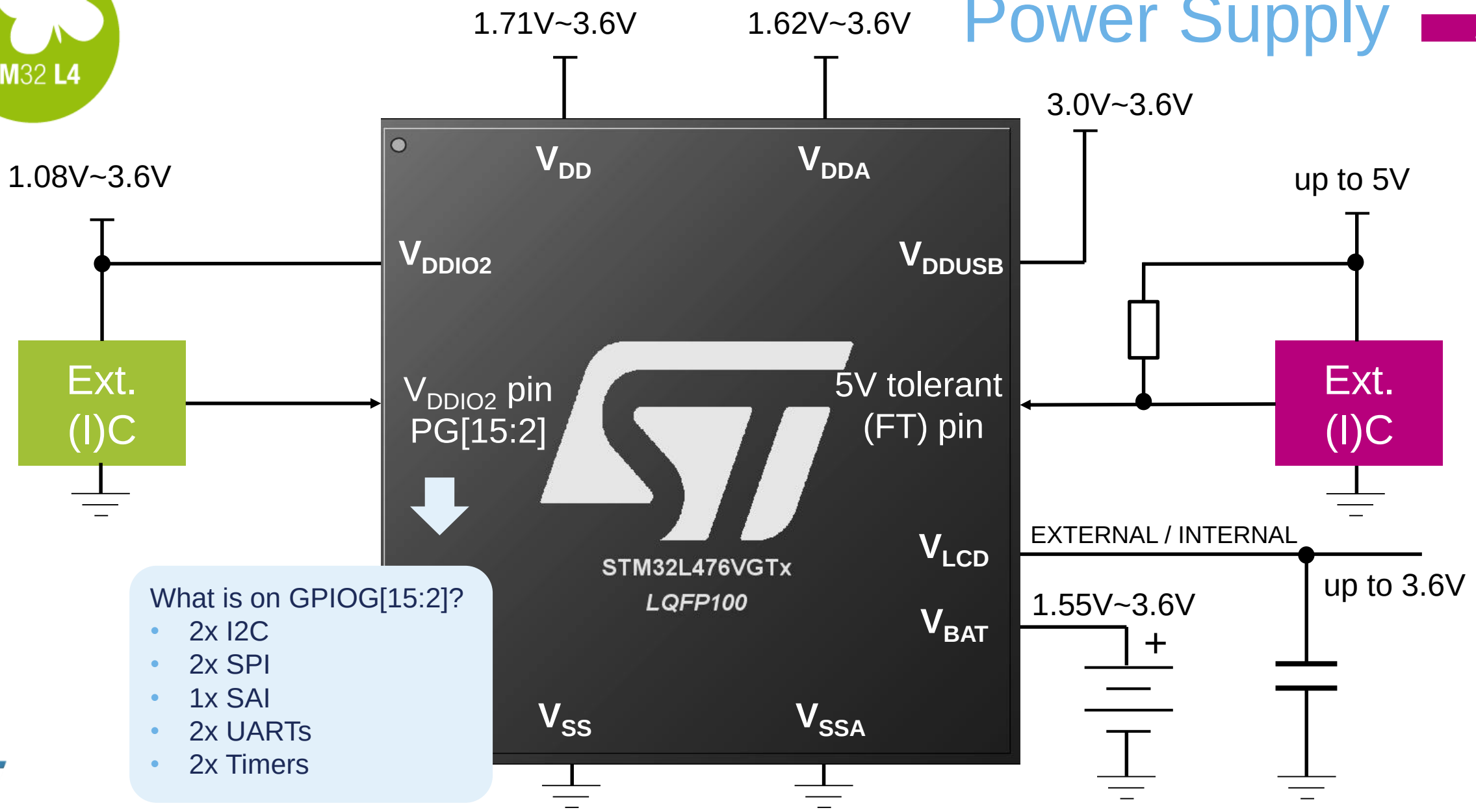
Power Supply



What is on GPIOG[15:2]?

- 2x I2C
- 2x SPI
- 1x SAI
- 2x UARTs
- 2x Timers

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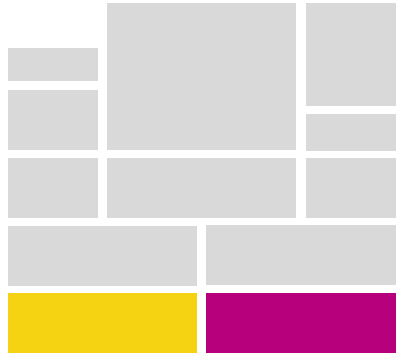
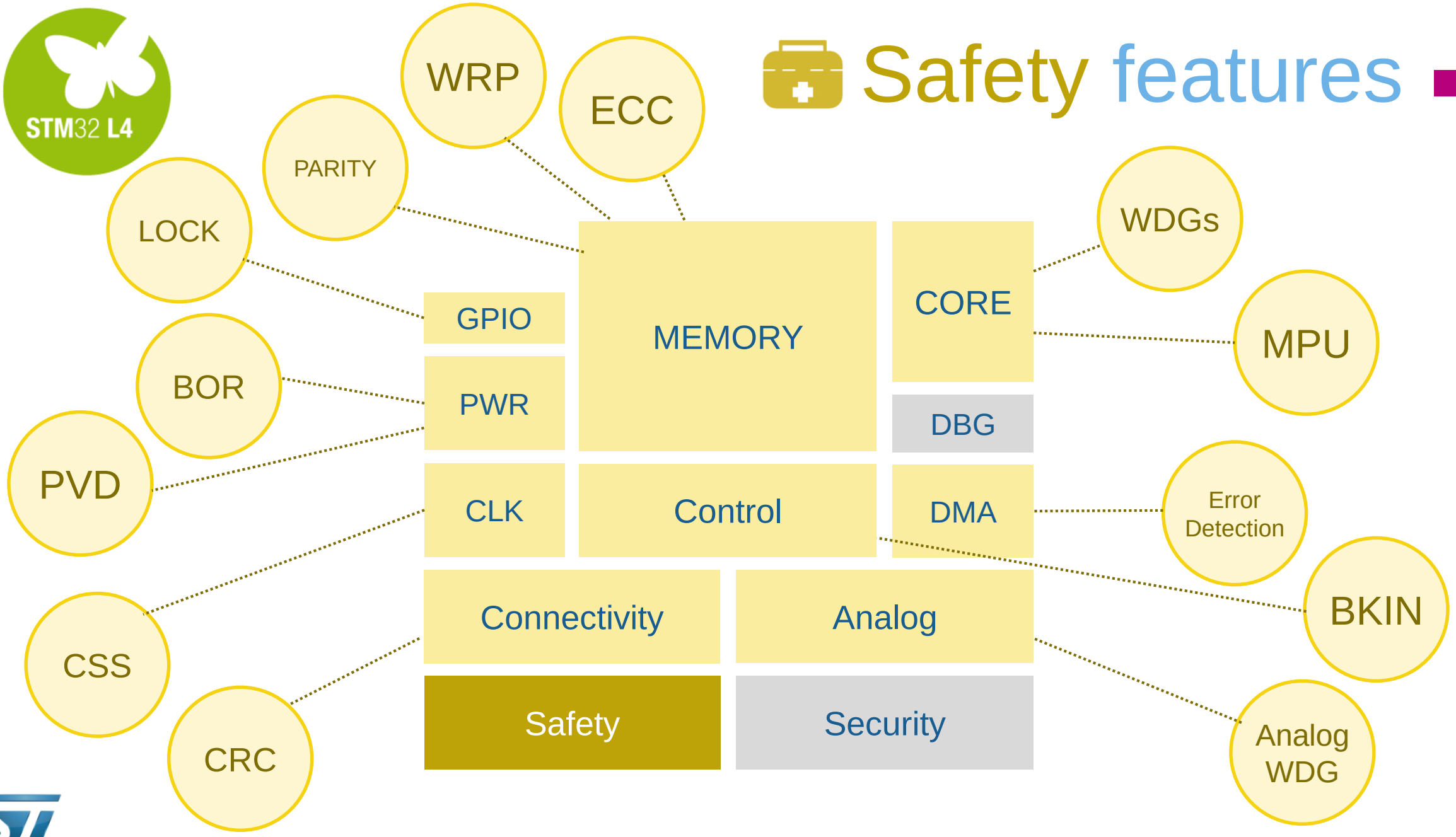
STM32L4 series

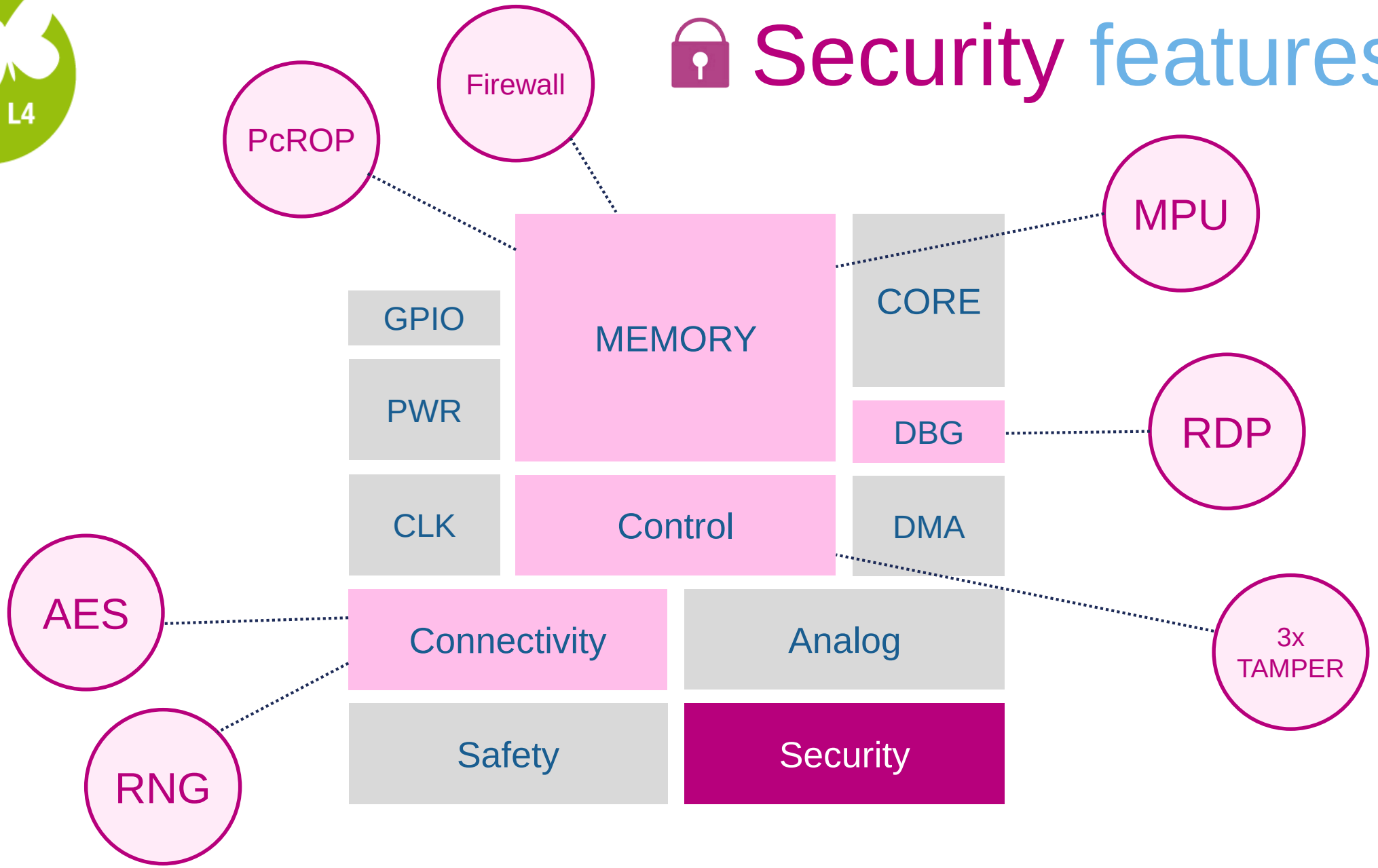
1. **High-performance**
2. **Peripherals rich**
3. **Safety and Security featured**



Safety features



Security features



STM32L4 series

1. High-performance
2. Peripherals rich
3. Safety and Security featured
4. **Ultra-Low-Power consuming**

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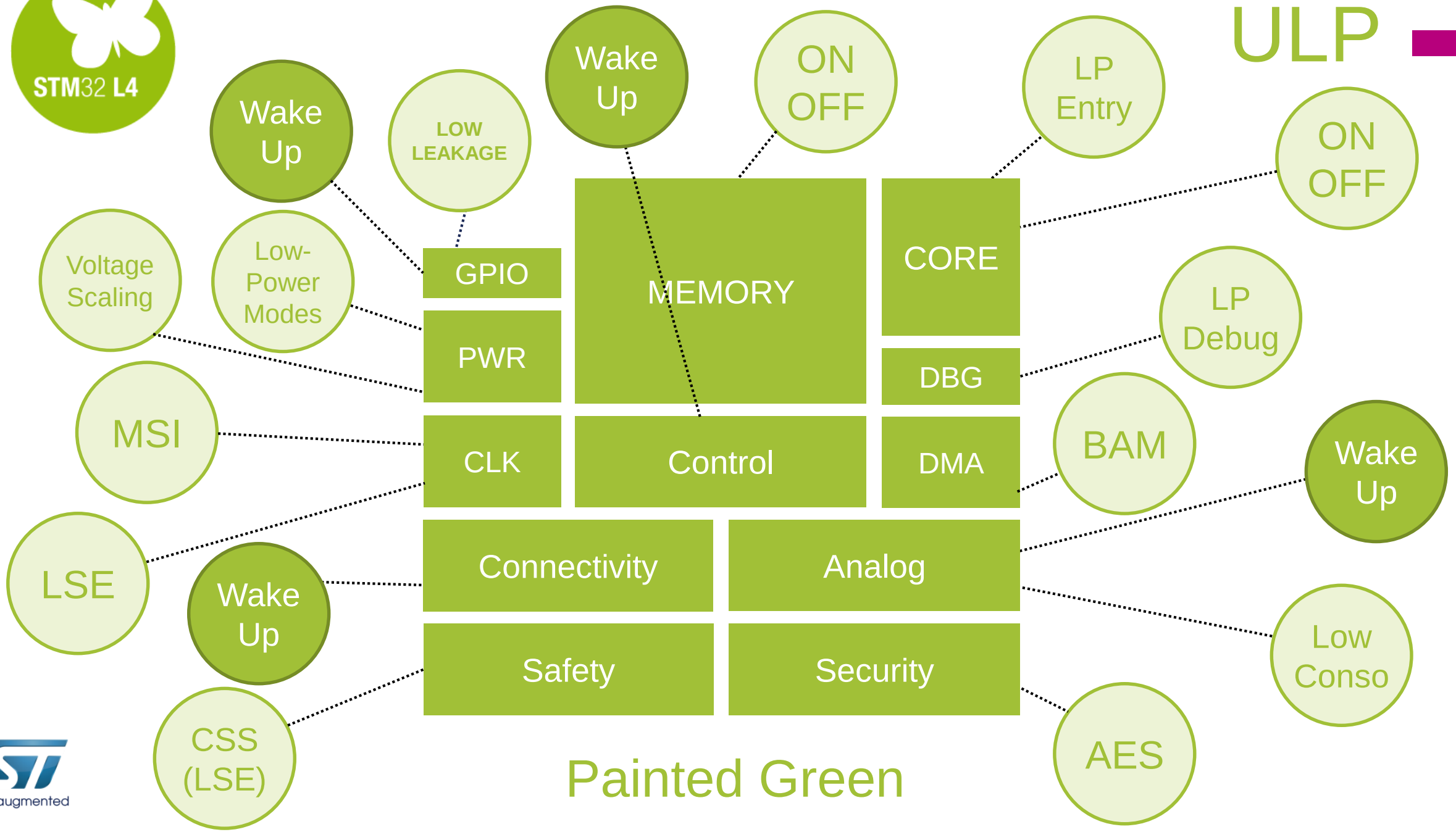
ULP


STM32 L4
Wake Up
LOW LEAKAGE
Wake Up
ON OFF
LP Entry
ON OFF
Voltage Scaling
Low-Power Modes
GPIO
MEMORY
CORE
LP Debug
PWR
DBG
MSI
CLK
Control
DMA
BAM
Wake Up
LSE
Wake Up
Connectivity
Analog
Low Conso
Safety
Security
CSS (LSE)
AES
Painted Green
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STM32L4 series

1. High-performance
2. Peripherals rich
3. Safety and Security featured
4. Ultra-Low-Power consuming

Enjoy!

www.st.com/stm32l4