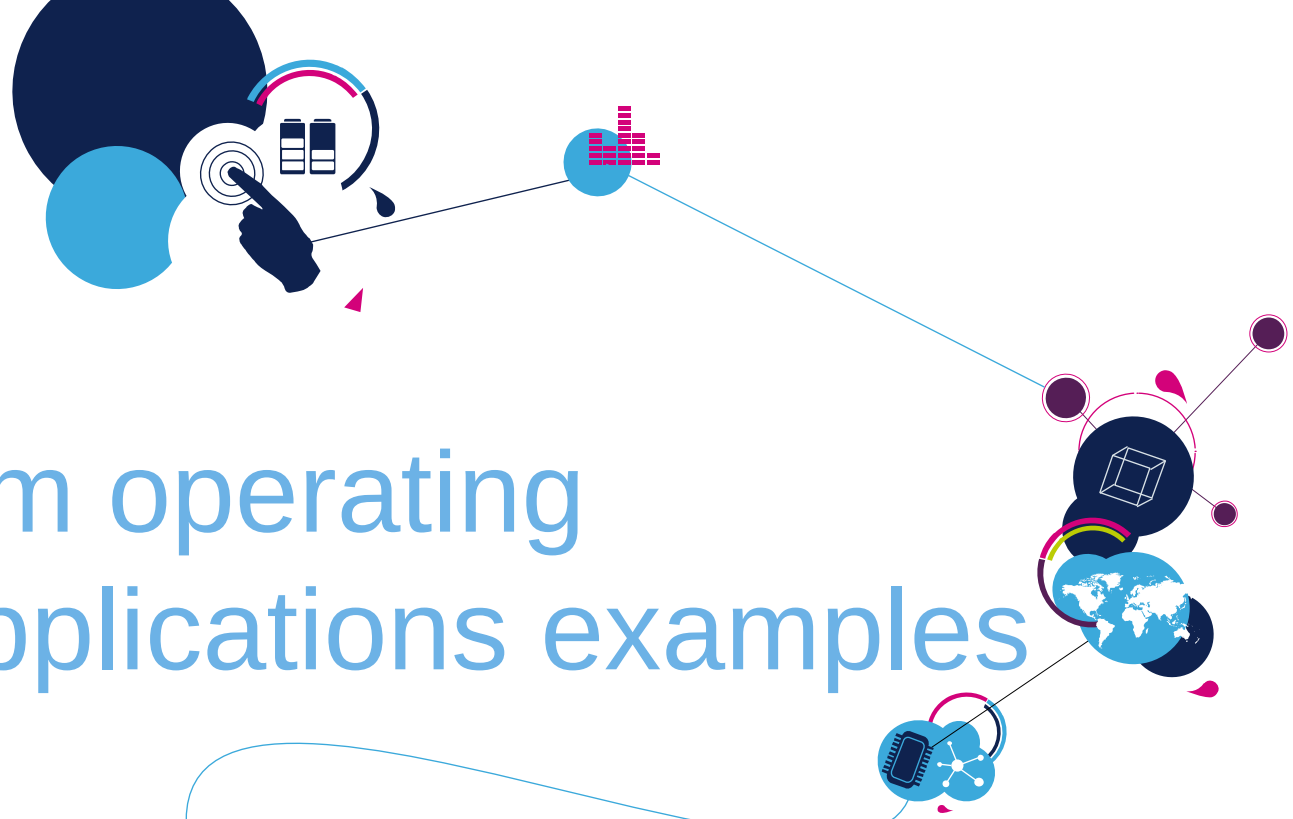
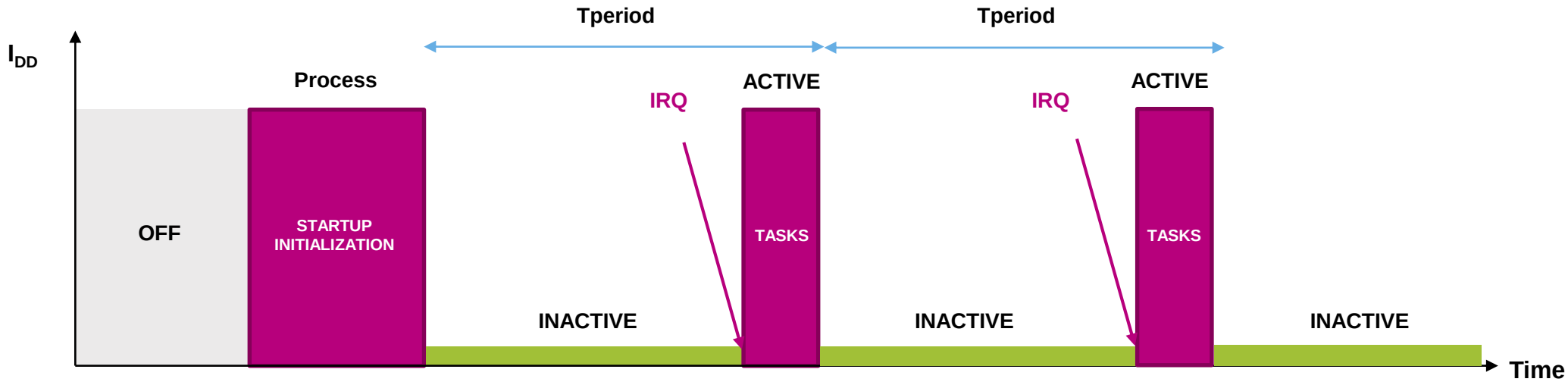


STM32L4 – System operating modes with real applications examples

STM32L4 workshop

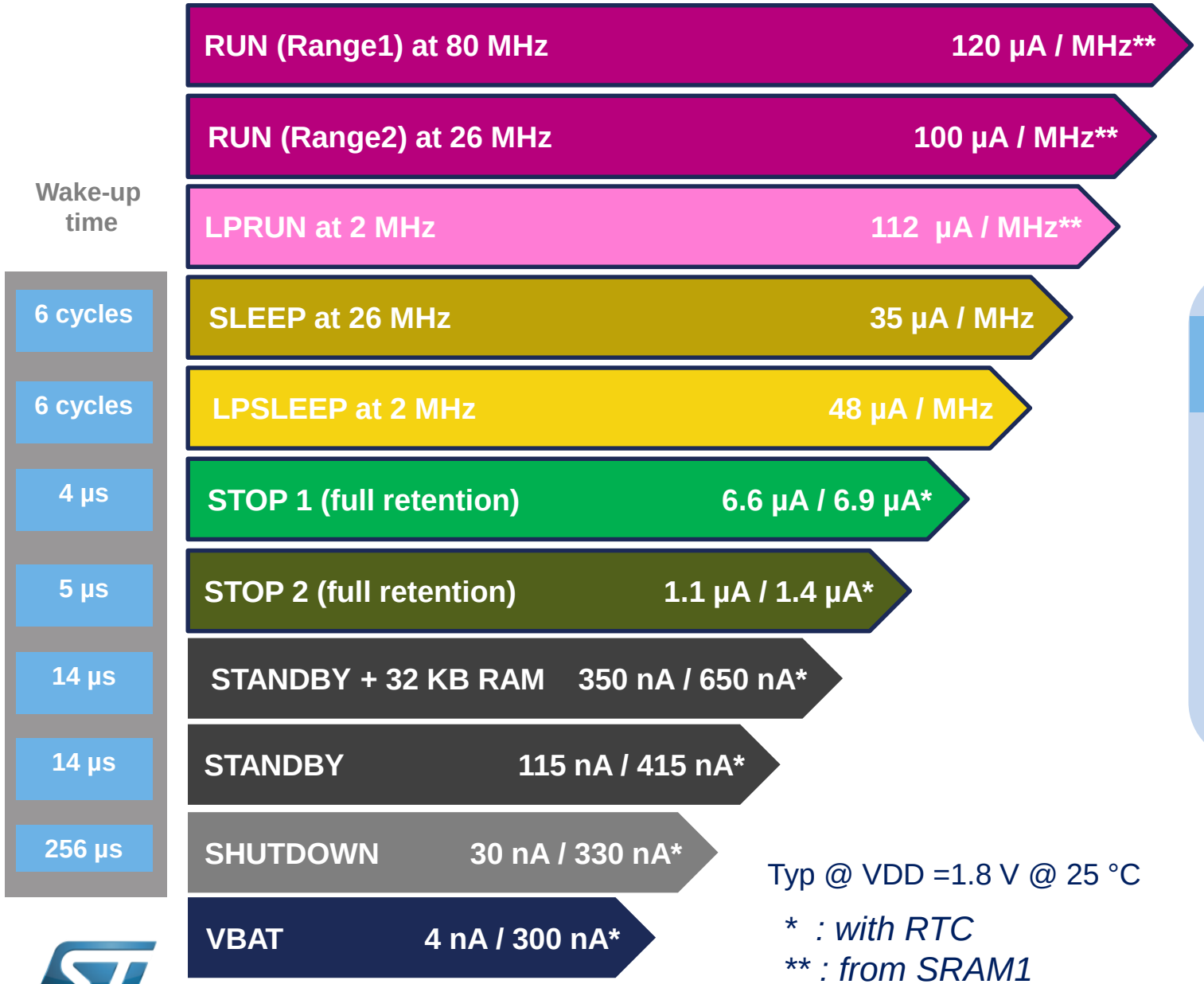
life.augmented

Typical application profile



- Application phases:
  - OFF – power is not applied to MCU
  - STARTUP INITIALIZATION – MCU performs configuration (peripherals, clocks, …)
  - Tperiod
    - INACTIVE – MCU is in low power mode to reduce power consumption
    - ACTIVE – MCU is in normal mode and performs tasks

Overview



Typ @ VDD =1.8 V @ 25 °C

** : with RTC*

*** : from SRAM1*

Application benefits

- High performance
  - ➔ CoreMark score = 273
- Outstanding power efficiency
  - ➔ ULPBbench score = 150

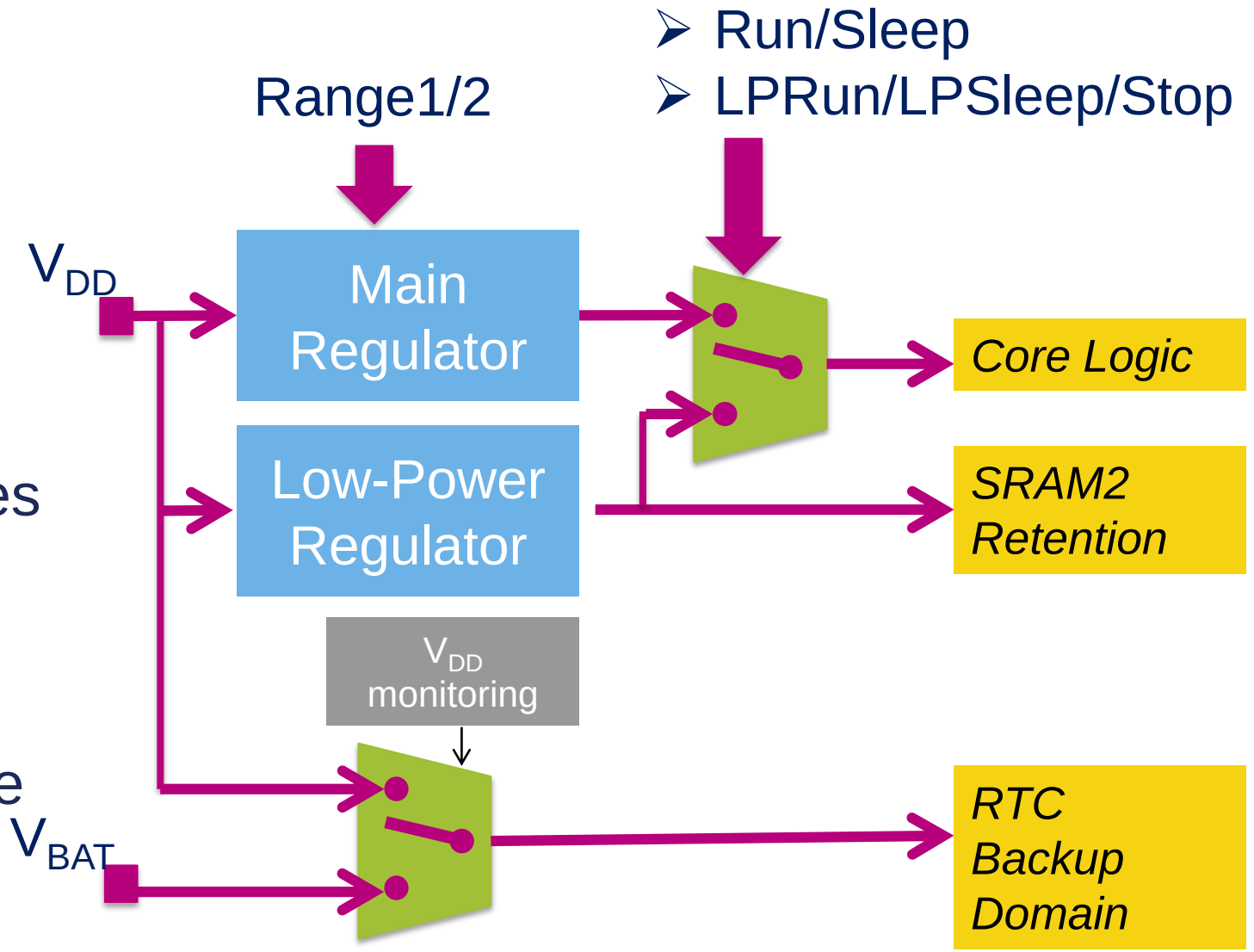
life.augmented

Key features

- Down to 100 µA/MHz in Run mode with code execution from SRAM
- Down to 30 nA with I/O wake-up (Shutdown)
- Down to 350 nA with 32 KB RAM retained (Standby)
- Wake-up from high number of peripherals (RTC in each mode)

Voltage regulators

- Two Voltage Regulators
- One Main regulator with two voltage ranges for Dynamic Voltage Scaling; used in Run and Sleep modes
- One Low-power regulator for Low-power run, Low-power sleep, Stop 1, and Stop 2 modes as well as for RAM retention in Standby
- In Standby and Shutdown mode both regulators are off.



Run mode: Range 1

- All MCU's resources are ON
- System frequency up to maximum value

Available peripherals

GPIO
DMA
FSMC
QUADSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low-power regulator (LPR) up to 2 MHz

Range 1 from Flash
131 µA/MHz at 80 MHz
(10.5 mA)

Available clocks

HSI
HSE
LSI
LSE
MSI

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock

Run mode: Range 2

- Most of MCU's resources are ON
- System frequency is limited

Available peripherals

GPIO
DMA
FSMC
QUADSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHz)

Range 2 (up to 26 MHz)

Low-power regulator (LPR) up to 2 MHz

Range 2 from SRAM1
100 µA/MHz at 26 MHz
(2,6 mA)

Available clocks

HSI
HSE
LSI
LSE
MSI

Active cell

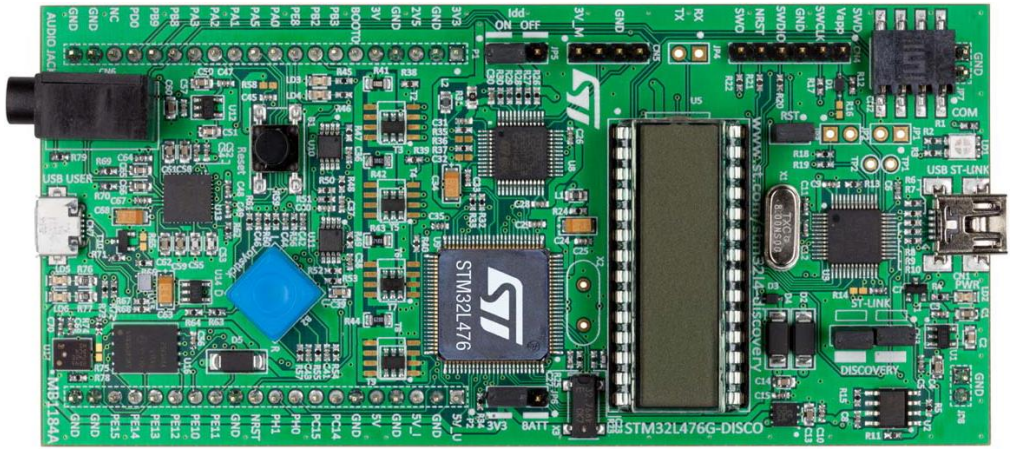
Clocked-off cell

Cell in power-down

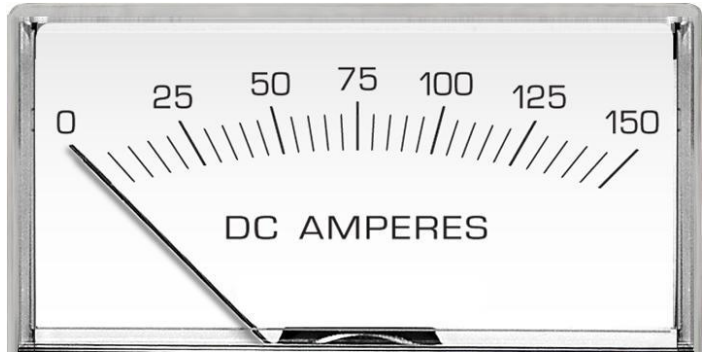
Available Periph and clock

Hands-on: important information

- Examples refer to real applications
- Software for each example was developed using tools:
  - STM32CubeMX initialization code generator
  - IAR EWARM IDE
- Hardware platform for the examples is STM32L476G-DISCO board

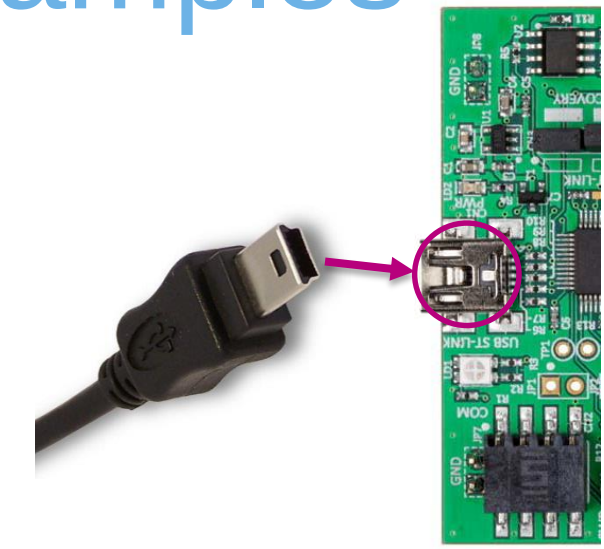


- Each example can be examined by attaching ammeter to the board and measuring current



Running hands-on examples

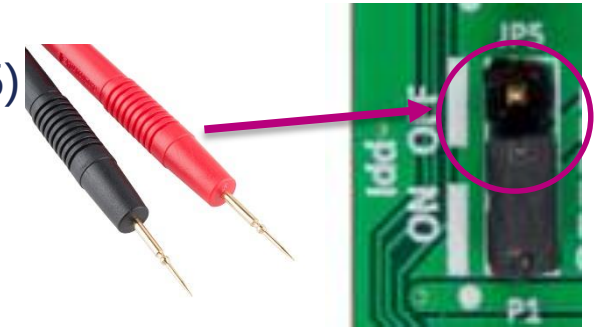
- Make sure that software tools are installed
  - IAR EWARM 7.40
  - CubeMX 4.11.0
  - ST-Link driver



- Attach STM32L476G-DISCO board to laptop (mini USB cable required)

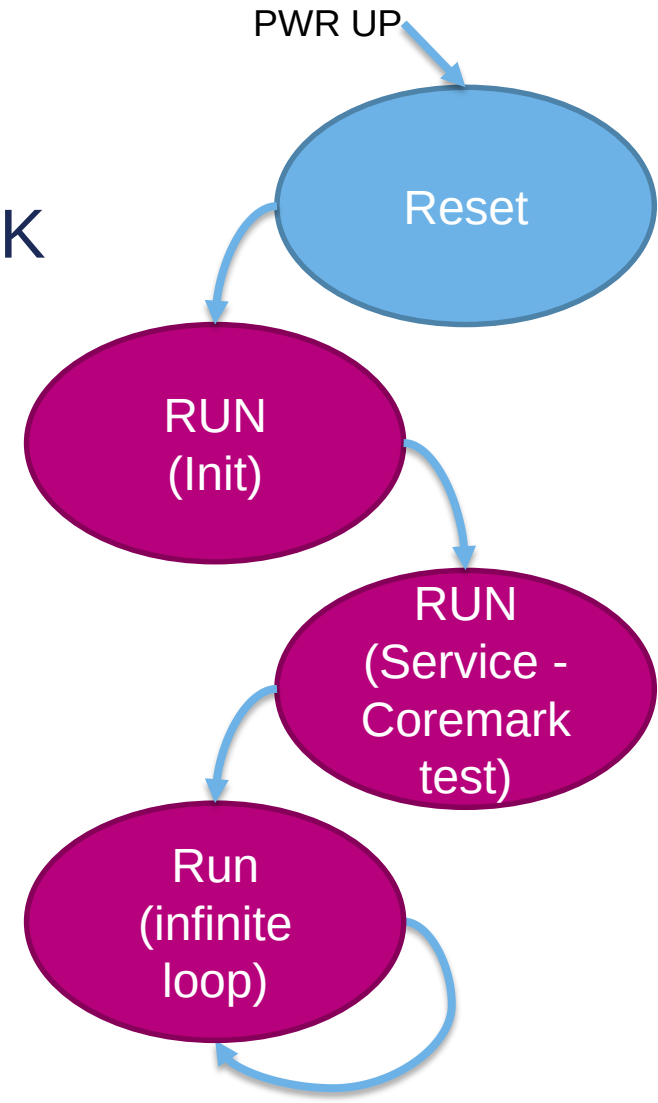
- Find example that you want to examine (they are located in “C:\STM32L4_workshop\HandsOn\1_System_Operating_modes” folder) and open it in IAR EWARM by double-clicking “Project.eww” file
- Run the example by:
  - building it (from Menu: Project->Make or F7)
  - downloading it to MCU (from Menu: Project-> Download->Download Active Application)
  - or debugging it on MCU (from Menu: Project->Download and Debug)

- Measure MCU current consumption by attaching ammeter to Idd connector (JP5) instead of jumper switched to OFF position



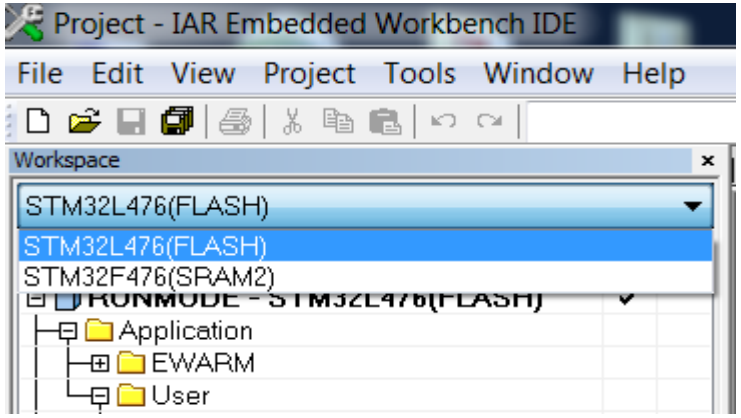
Hands-on example 1: RUN mode

- **Application:** High-performance data processing unit
- **Description of application:** MCU executes COREMARK algorithm
- **Example path:**
  C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\1_RUNMODE
- **Application's parameters:**
  - Clock: 24MHz (MSI@4MHz) / 80 MHz (MSI@4MHz + PLL),
  - Execution space: FLASH/SRAM memory



Hands-on: RUN mode configuration

- **Configuration:**
  - Execution space (FLASH or SRAM2) can be changed by choose linker file



  - Clock frequency can be changed in main.c by uncomment Clock_MSI24MHZ_Enable(), PLL80MHz clock is default

```
94    //ART_Disable();
95    //Clock_MSI24MHZ_Enable();
```

  - Printf instruction is redirected to UART2 / ST-Link Virtual Com Port, jumper SB13, SB16 should be soldered. Uart parameters: 115200b/s,8,N,1
  - Virtual Comport Driver should be installed on the target PC

Hands-on: RUN mode results

- **Result can be obtained in Terminal software:**

```
Running from address:   0x08004495
Data at address: 0x200001A8
WS:  4, ART: ON
System Clock:  80000000
2K performance run parameters for coremark.
CoreMark Size    : 666
Total ticks      : 303264193
Total time (secs): 3.790802
Iterations/Sec   : 263.796392
Iterations       : 1000
Memory location  : STACK
```

- **Results of COREMARK algorithm:**

Conditions	COREMARK result	Average current consumption
FLASH / CLK=80MHz	263.8	14.3 mA (178 uA/MHz)
SRAM1/SRAM2 CLK=80MHz	269.8	14.1 mA (176 uA/ MHz)
FLASH / CLK=24MHz	80.5	4.5 mA (187 uA/MHz)
SRAM1/SRAM2 CLK=24MHz	80.8	3.24 mA (135 uA/MHz)

Low-power run mode

- Main regulator is OFF
- System frequency is limited

Available peripherals

GPIO
DMA
FSMC
QUADSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHZ)

Range 2 (up to 26 MHZ)

Low-power regulator (LPR) up to 2 MHz

from Flash
135 µA/MHz at 2 MHz (269 µA)

From SRAM1
112 µA/MHz at 2 MHz (225 µA)

Available clocks

HSI
HSE
LSI
LSE
MSI

Active cell

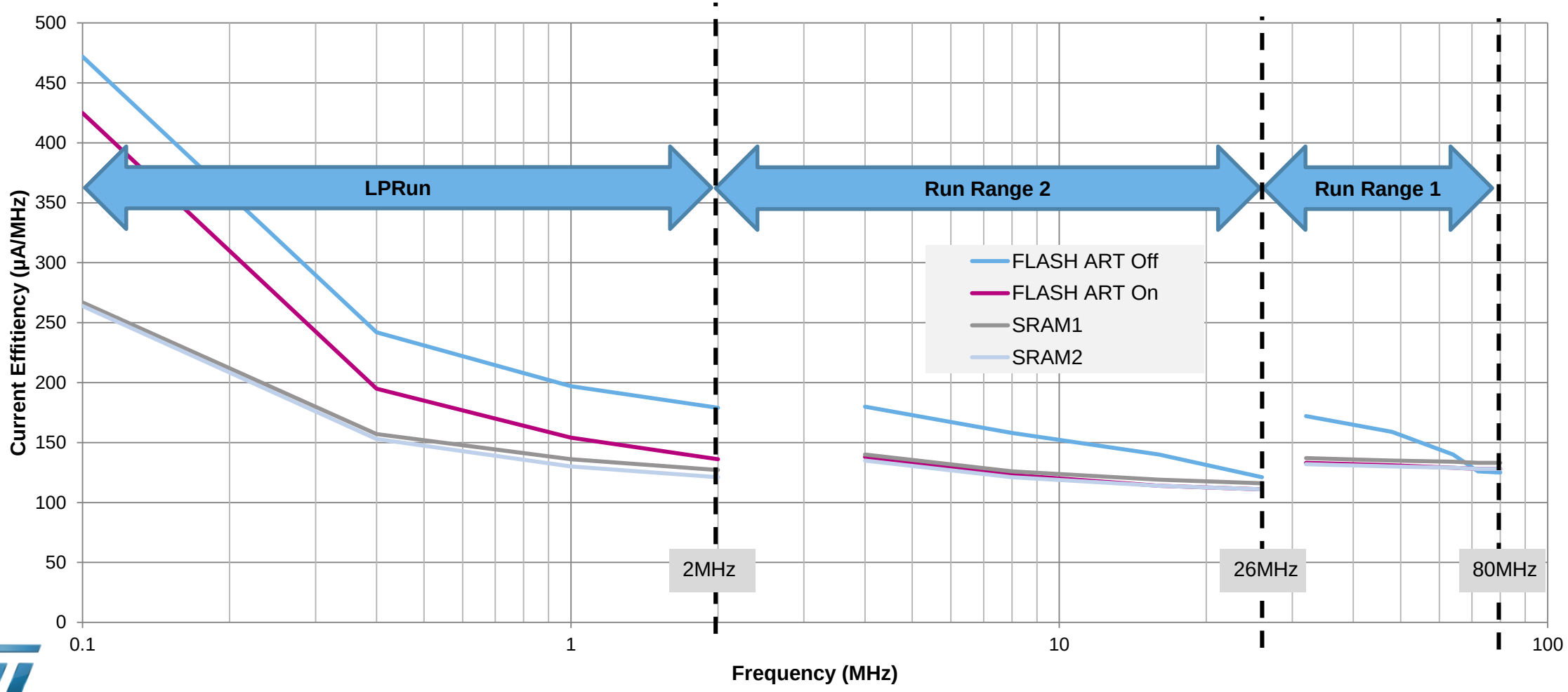
Clocked-off cell

Cell in power-down

Available Periph and clock

Power optimization versus frequency

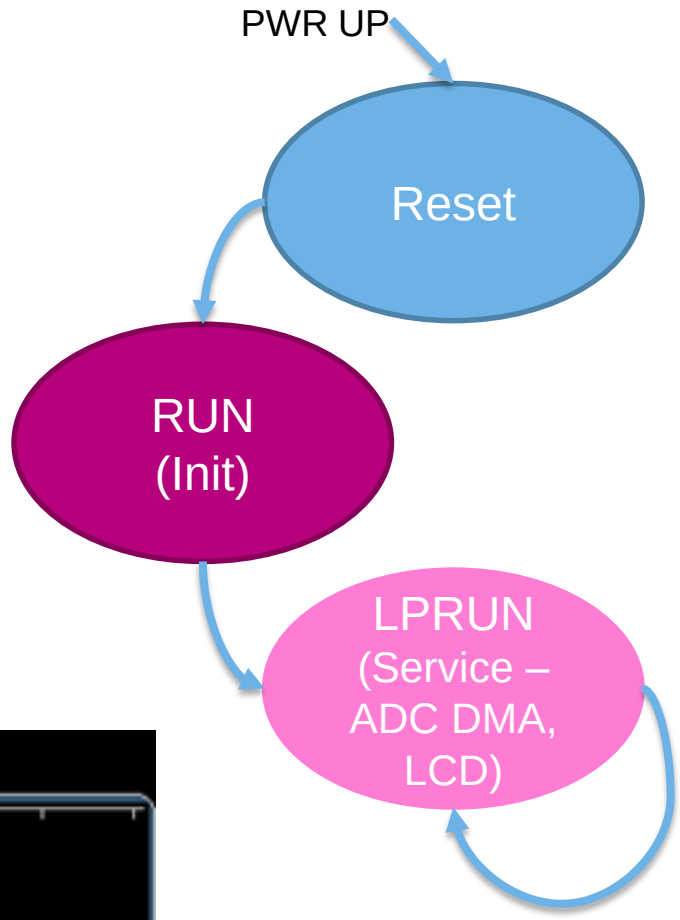
Flexibility between required performance and consumption

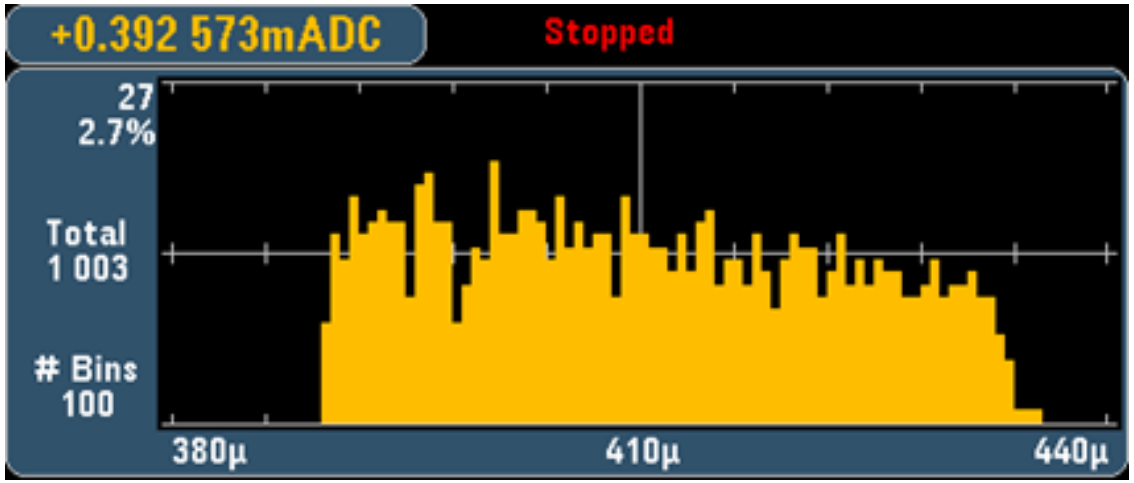


life.augmented

Hands-on example 2: LOW POWER RUN

- **Application name:** Fast data acquisition logger (sensor hub), implementation #1
- **Description of application:** every 1 s ADC reads data from temperature sensor integrated in MCU, then data is sent by DMA to be displayed on LCD
- **Example path:** C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\2_LOWPOWERRUN_RAM
- **Application's parameters:**
  - Clock: 2 MHz (clock source: MSI),
  - Execution space: SRAM1 memory
- **Current consumption:**
  - **Average in LPRUN:** 410 uA
  - **Distribution:** flat current consumption profile





life.augmented

Sleep mode

- Core is stopped
- All peripherals and clocks are available
- Fastest wakeup time

Wakeup time: 6 cycles

Available peripherals

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHZ)

Range 2 (up to 26 MHZ)

Low Power regulator (LPR) up to 2 MHz

Range 1
37 µA/MHz at 80 MHz (2.96 mA)

Range 2
35 µA/MHz at 26 MHz (0.92 mA)

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell

Clocked-off cell

Cell in power-down

Available Periph and clock

Low-power sleep mode

- Core is stopped
- Main regulator is OFF
- Fastest wakeup time

Wakeup time: 6 cycles

Available peripherals

GPIO
DMA
FSMC
QUADSPI
BOR
PVD, PVM
LCD
USB OTG
USART
LP UART
I2C 1 / I2C 2
I2C 3
SPI
CAN
SDMMC
SWPMI
SAI
DFSDM
ADC
DAC
OPAMP
COMP
Temp Sensor
Timers
LPTIM 1
LPTIM 2
IWDG
WWDG
Systick Timer
Touch Sens
RNG
AES
CRC

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Range 1 (up to 80 MHZ)

Range 2 (up to 26 MHZ)

Low Power regulator (LPR) up to 2 MHz

Flash ON, SRAMs OFF
48 µA/MHz at 2 MHz (96 µA)

Available clocks

HSI
HSE
LSI
LSE
MSI

Active cell

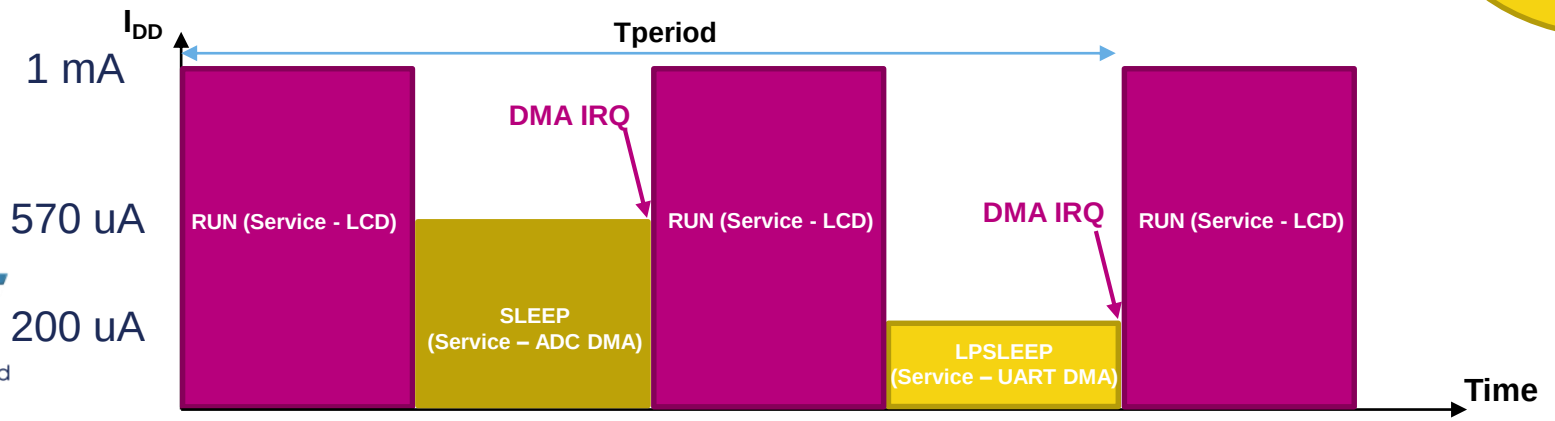
Clocked-off cell

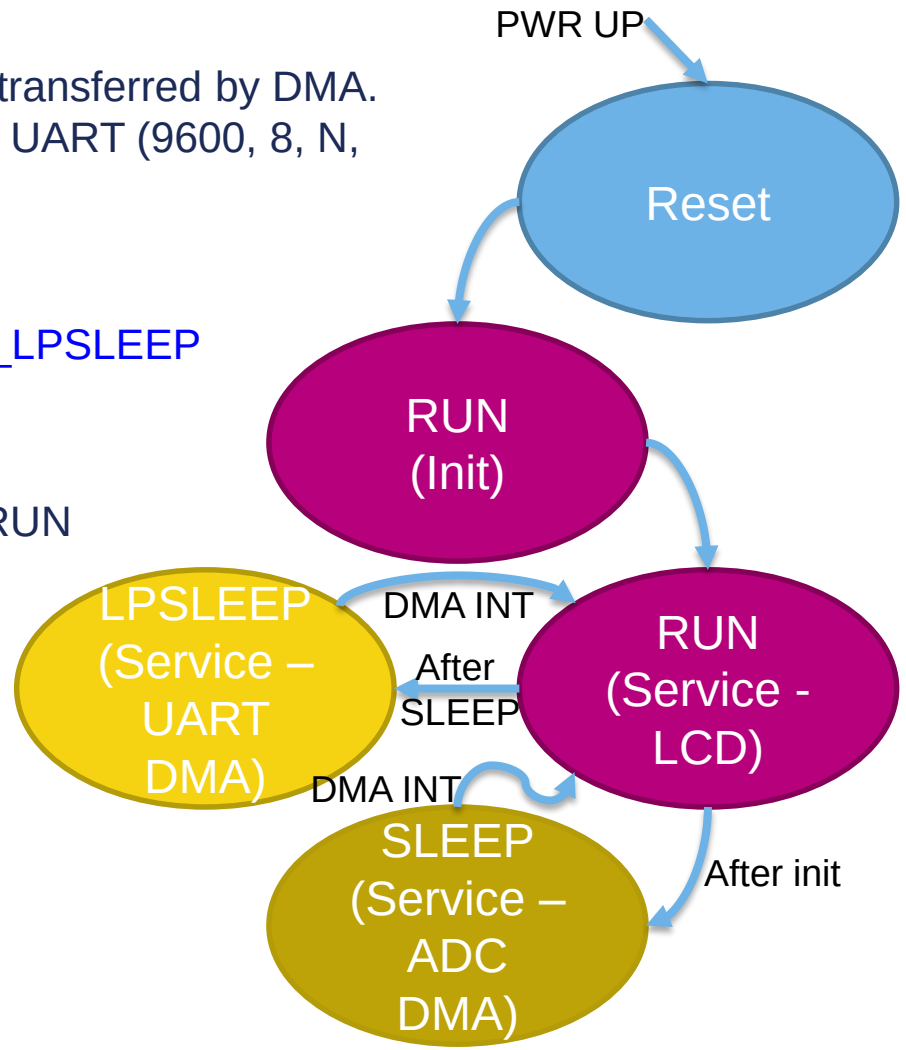
Cell in power-down

Available Periph and clock

Hands-on example 3: SLEEP / LPSLEEP

- **Application name:** Fast data acquisition logger (sensor hub), implementation #2
- **Description of application:** in SLEEP mode data is acquired by ADC and transferred by DMA. In RUN mode data is displayed on LCD. In LPSLEEP data is transferred by UART (9600, 8, N, 1) with DMA.
- **Example path:** C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\3_SLEEP_LPSLEEP
- **Application's parameters:**
  - Clock: 4 MHz MSI in SLEEP, 1 MHz MSI in LPSLEEP, 4 MHz MSI in RUN (clock source: MSI for all),
- **Average current consumption:**



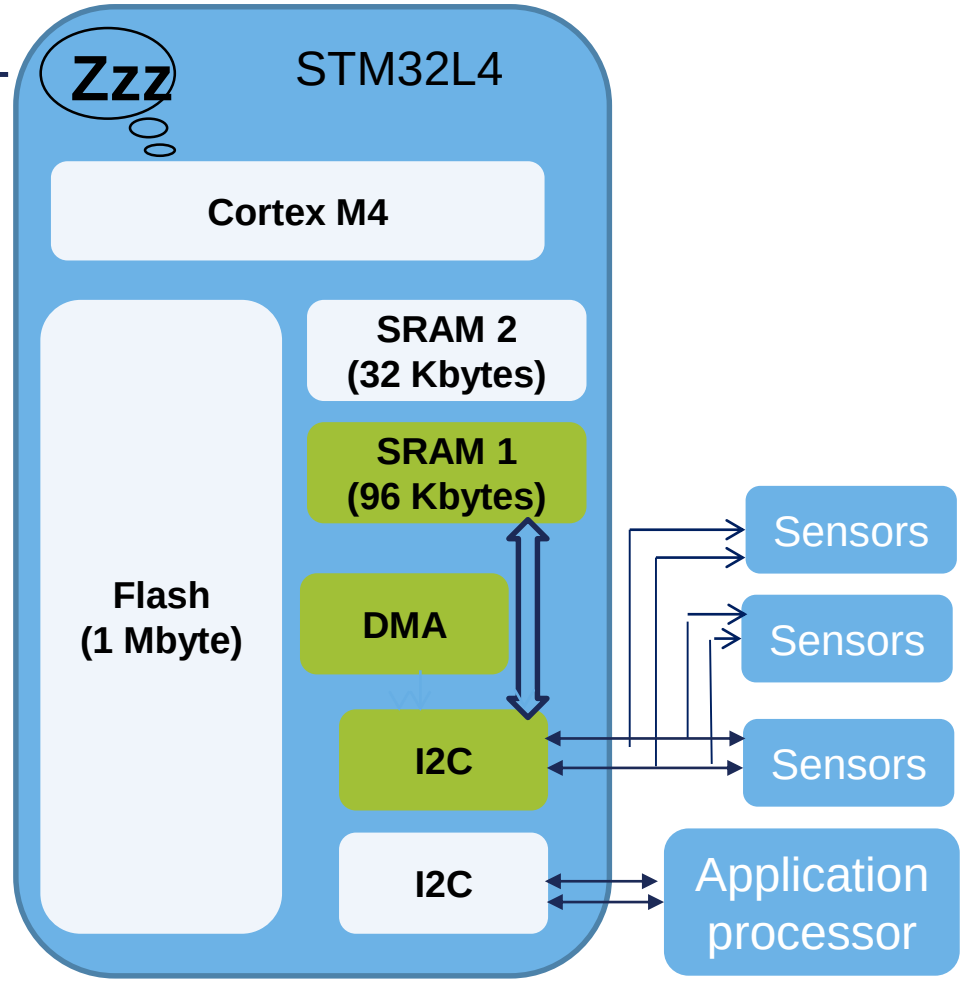


life.augmented

Batch Acquisition mode (BAM)

Optimized mode for transferring data with communication peripherals, while the rest of the device is in low power.

1. Only the needed communication peripheral + 1 DMA + 1 SRAM are configured with clock enabled in Sleep mode
2. Flash memory is put in Power-down mode and Flash clock is gated off during Sleep mode
3. Enter either Sleep or Low-power sleep mode
   - Note that the I2C clock can be at 16 MHz even in Low-power sleep mode, allowing 1 MHz Fast-mode Plus support. U(S)ART/LPUART clock can also be HSI.



Stop modes

Lowest power modes with full retention

- SRAM1, SRAM2 and all peripheral registers retention
- All high-speed clocks are stopped
- LSE (32.768 kHz external oscillator) and LSI (32 kHz internal oscillator) can be enabled
- Several peripherals can be active and wake up from Stop mode
- System clock at wakeup can be **HSI** or **MSI up to 48 MHz**
- In Stop 2 current consumption is lower; in Stop 1 more active peripherals are supported and wake up time is shorter

Stop 1 mode

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os kept, and configurable

w/o RTC: 6.6 µA @ 3.0 V
w/ RTC: 7.1 µA @ 3.0 V

Wakeup time for 48 MHz:
In SRAM: 4 µs
In Flash memory: 6 µs

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Low Power regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

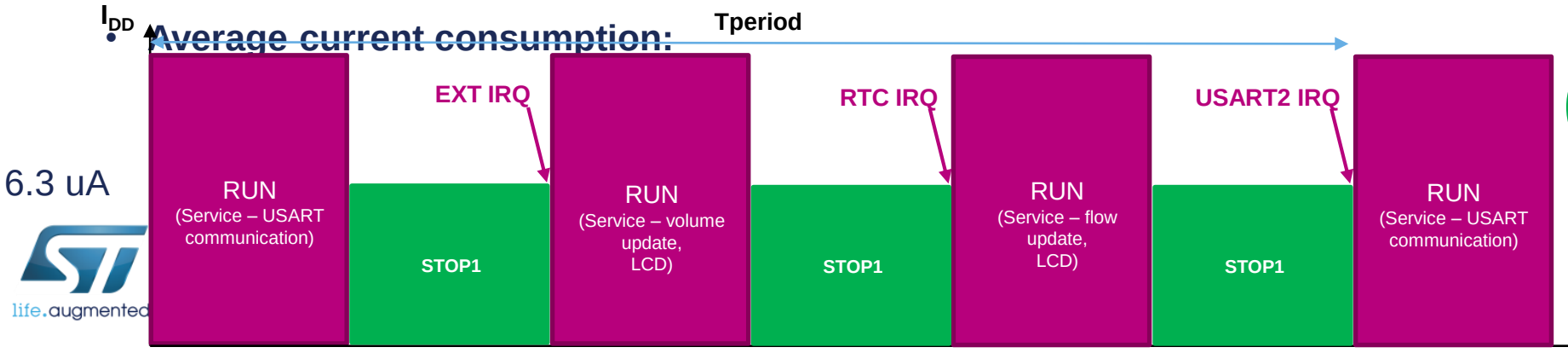
Available clocks

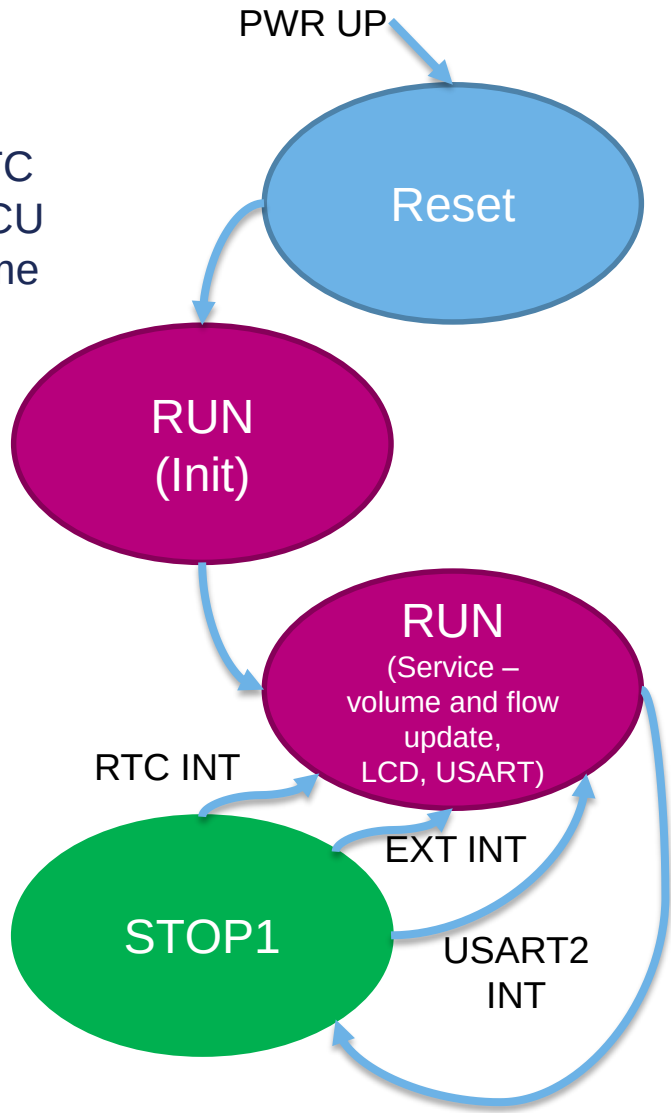
- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Clocked-off cell | Cell in power-down | Available cell

Hands-on example 4: STOP1

- **Application name:** Water meter, implementation #1 (with UART wake-up capability)
- **Description of application:** MCU enters STOP1 mode. Interrupts wakes it up. After RTC interrupt (once every 60 s) MCU updates average flow. After EXTI interrupt (buttons) MCU provides user interface and counts volume. After UART interrupt MCU sends back volume data by UART.
- **Example path:** C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\4_WATER_METER_STOP1
- **Application's parameters:**
  - Clock: 16 MHz (clock source: HSI)
- **Average current consumption:**





Stop 2 mode

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os kept, and configurable

w/o RTC: 1.2 µA @ 3.0 V
w/ RTC: 1.7 µA @ 3.0 V

Wakeup time to 48 MHz:
In SRAM: 5 µs
In Flash memory: 8 µs

Cortex M4

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Main regulator (MR)

Low Power regulator (LPR)

Backup domain

Backup Register (32x32-bits)

RTC

Wake-up event

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

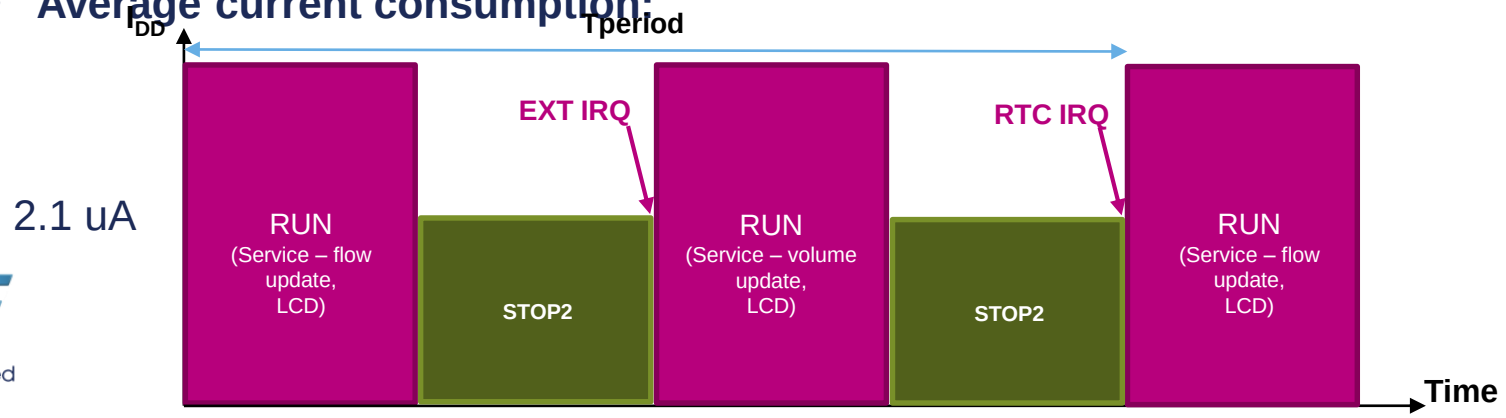
Available clocks

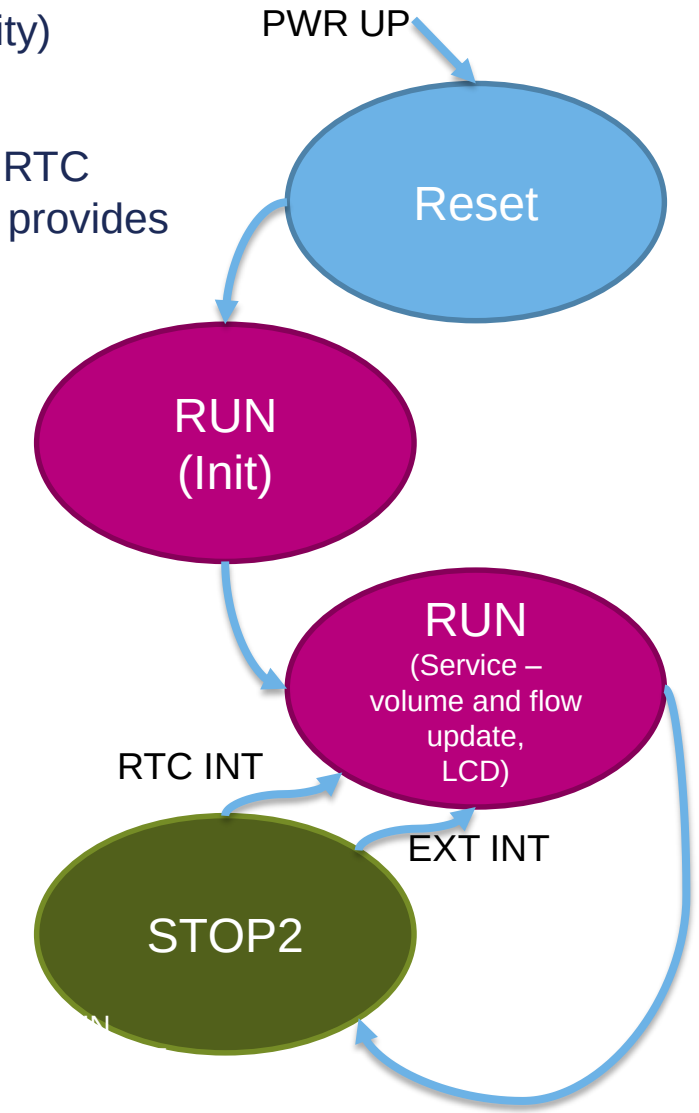
- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Clocked-off cell | Cell in power-down | Available cell

Hands-on example 5: STOP2

- **Application name:** Water meter, implementation #2 (without UART wake-up capability)
- **Description of application:** MCU enters STOP2 mode. Interrupts wakes it up. After RTC interrupt (every 60 s) MCU updates average flow. After EXTI interrupt (buttons) MCU provides user interface and counts volume.
- **Example path:** C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\5_WATER_METER_STOP2
- **Application's parameters:**
  - Clock: 4 MHz (clock source: MSI)
- **Average current consumption:**





life.augmented

Stop 1 & Stop 2 comparison

Voltage range	Stop 1 mode	Stop 2 mode
Consumption	25 °C, 3 V	25 °C, 3 V
	6.6 µA w/o RTC	1.2 µA w/o RTC
Wakeup time to 48 MHz	6 µs in Flash memory 4 µs in RAM	8 µs in Flash memory 5 µs in RAM
Wakeup clock	**MSI** configurable **up to 48 MHz** or **HSI** at **16 MHz**	
Peripherals	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG	
	USB (suspend, ADP) 2 LP TIMERs 1 LP UART (Start, address match or byte reception) 5 UARTx (Start, address match or byte reception) 3 I2C (address match) SWPMI (resume from suspend)	1 LP TIMER (**LPTIM1**) 1 LP UART (Start, address match or byte reception) 1 I2C (**I2C3**) (address match)

Lowest power mode with SRAM2 retention

- Ultra low power consumption, down to 115 nA without SRAM retention
- Possibility to **retain 32 Kbytes of SRAM2**
- **5 wakeup pins**: the polarity of each of the **5** wakeup pins is configurable
- Wakeup clock is **MSI configurable from 1 to 8 MHz**

Standby mode with or without SRAM2

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

w/ SRAM

w/o RTC: 390 nA @ 3.0 V
w/ RTC: 890 nA @ 3.0 V

w/o SRAM

w/o RTC: 150 nA @ 3.0 V
w/ RTC: 650 nA @ 3.0 V

Wakeup time to 8 MHz:
In Flash memory: 14 µs

Cortex M4

Main regulator (MR)

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Low Power regulator (LPR)

Wake-up event

- NRST
- BOR
- RTC + Tamper
- IWDG
- 5 WKUP pins

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Backup domain

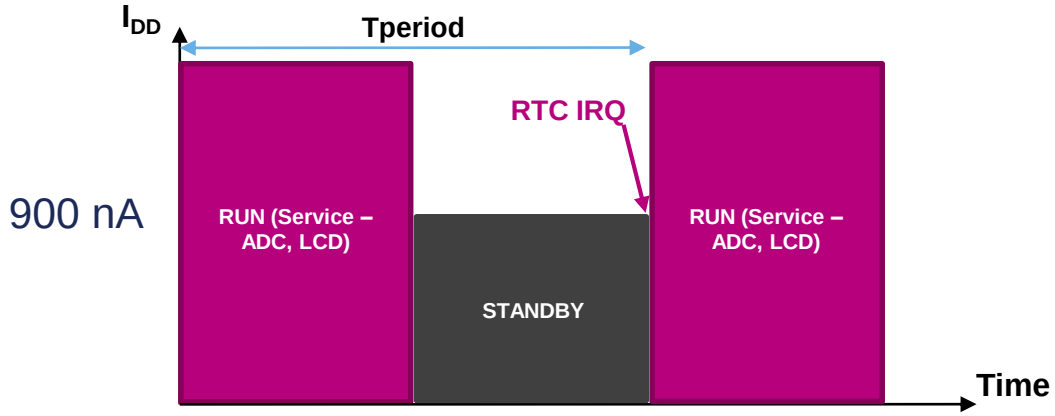
Backup Register (32x32-bits)

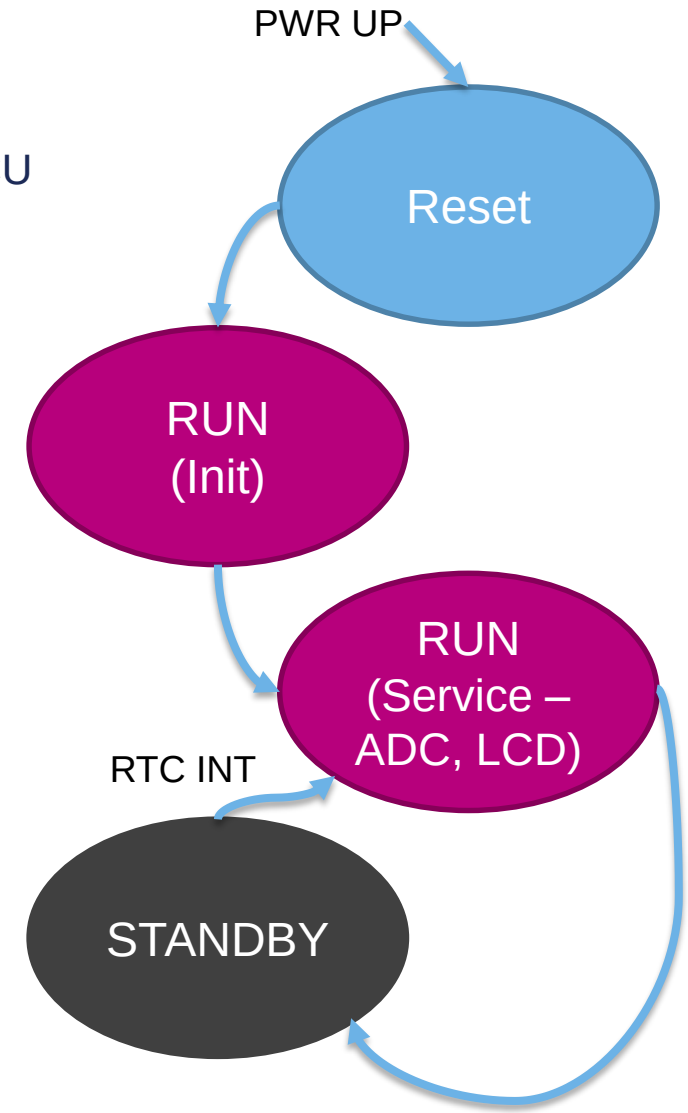
RTC

Active cell | **Clocked-off cell** | **Cell in power-down** | **Available cell**

Hands-on example 6: STANDBY

- **Application name:** Long term temperature logger
- **Description of application:** MCU enters STANDBY mode. After each RTC wake up MCU reads ADC data and displays it on LCD.
- **Example path:** C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\6_LONGTERM_LOGGER_STANDBY_SRAM2
- **Application's parameters:**
  - Clock: 4 MHz (clock source: MSI)
- **Average current consumption:**





life.augmented

Shutdown mode

Lowest power mode

- Similar to Standby but
  - **NO power monitoring:** no BOR, no switch to VBAT
  - **NO LSI**, no IWDG
- 128-byte **backup registers**
- Wakeup sources: **5 wakeup pins**, **RTC**
- Wakeup clock is MSI 4 MHz

Shutdown mode

Available peripherals

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os can be configured
w/ or w/o pull-up
w/ or w/o pull-down
But floating when exit from Shutdown

w/o RTC: 60 nA @ 3.0 V
w/ RTC: 550 nA @ 3.0 V

Wakeup time to 4 MHz:
In Flash memory: 250 µs

Cortex M4

Main regulator (MR)

Flash memory (1 Mbyte)

SRAM 1 (96 Kbytes)

SRAM 2 (32 Kbytes)

Low Power regulator (LPR)

Wake-up event

- NRST
- RTC + Tamper
- 5 WKUP pins

Available clocks

- HSI
- HSE
- LSI
- LSE
- MSI

Backup domain

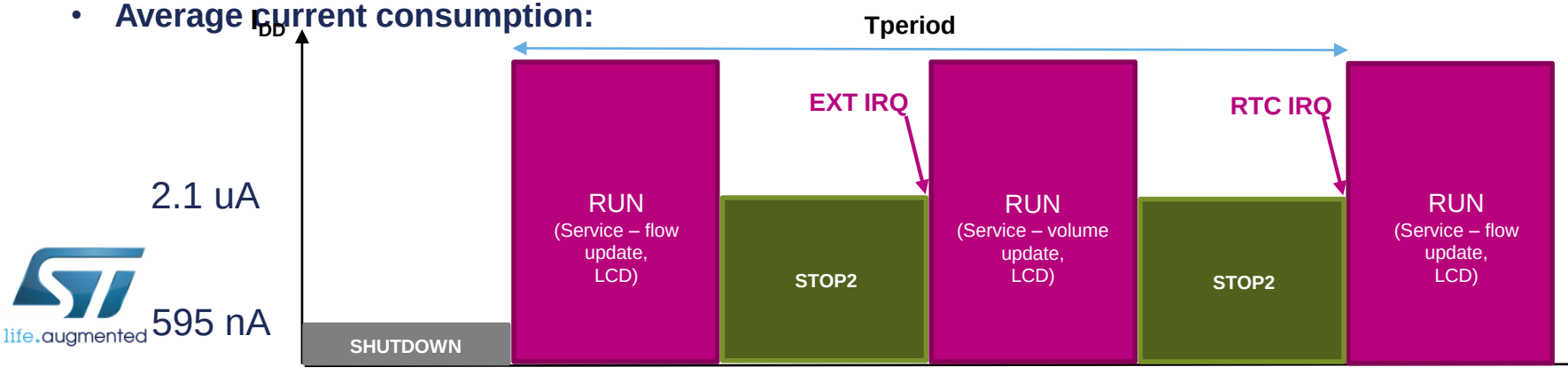
Backup Register (32x32-bits)

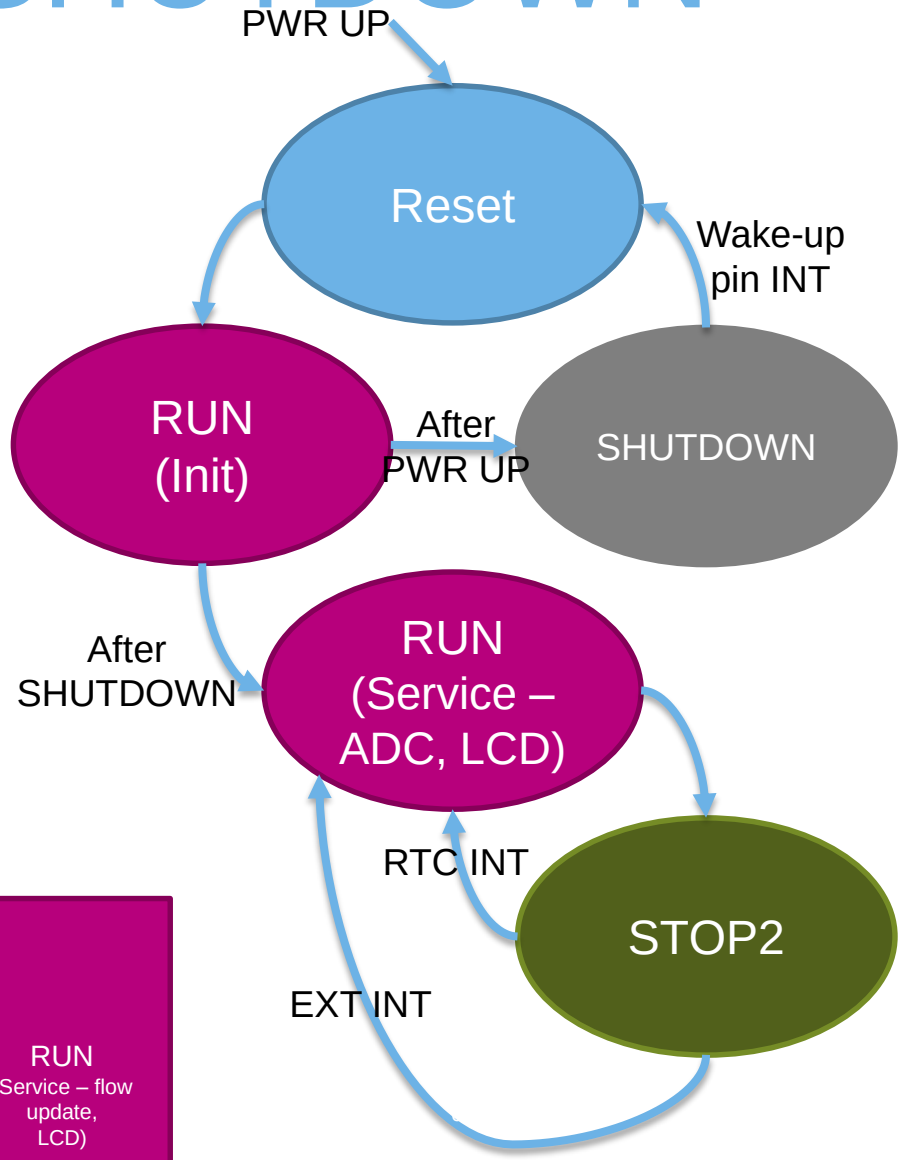
RTC

Active cell | Clocked-off cell | Cell in power-down | Available cell

Hands-on example 7: SHUTDOWN

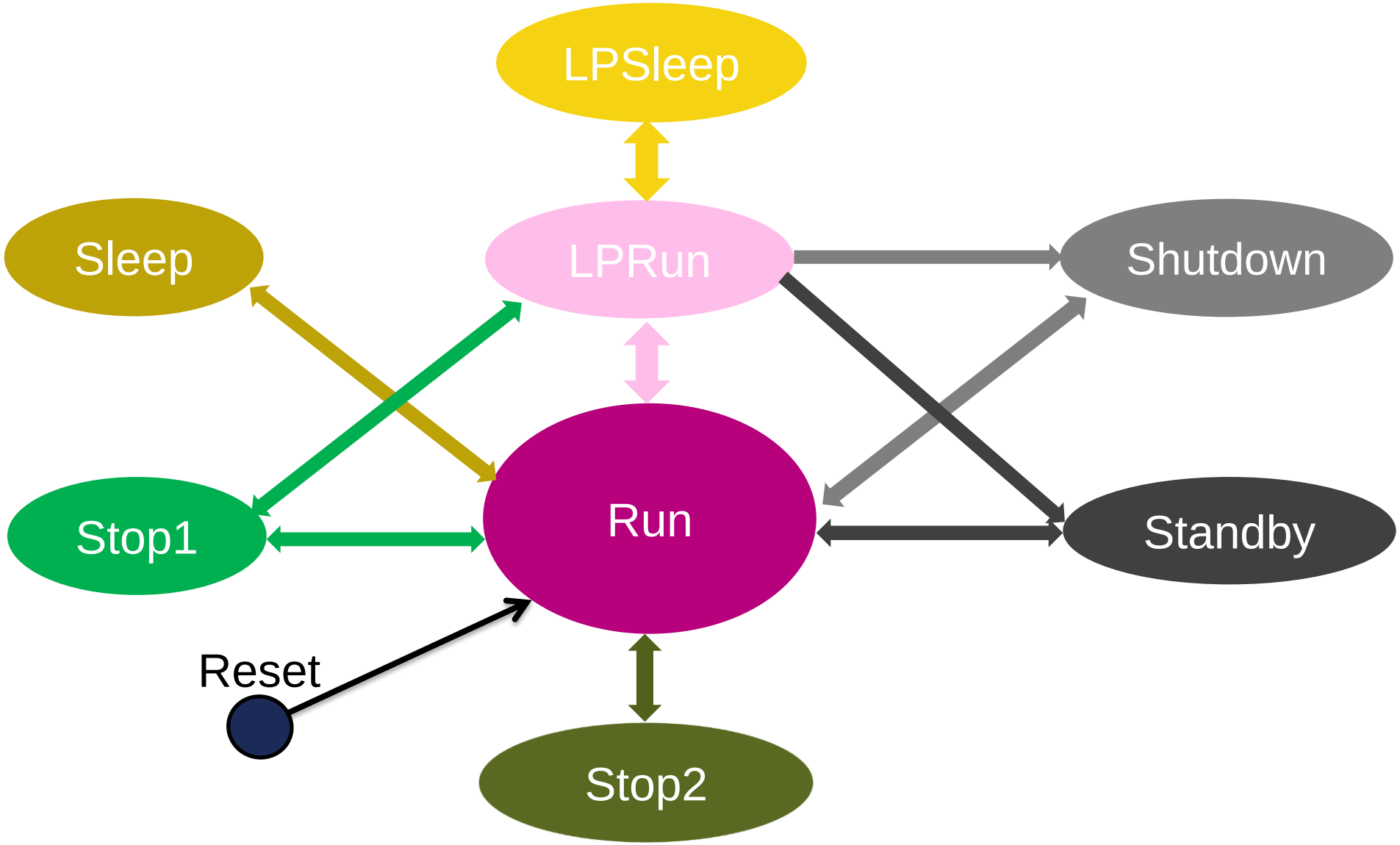
- **Application name:** Water meter, implementation #3 (with SHUTDOWN mode).
- **Description of application:** MCU enters SHUTDOWN mode. This refers to behavior, when already configured battery-operated device is held in warehouse and current consumption should be as low as possible. When the center button is pressed and held, MCU starts to execute water meter application (example 5). This refers to behavior after device is delivered to customer.
- **Example path:** C:\STM32L4_Workshop\HandsOn\1_System_Operating_Modes\7_WATER_METER SHUTDOWN + STOP2 mode
- **Application's parameters:**
  - Clock: 4 MHz (clock source: MSI)
- **Average current consumption:**





life.augmented

Low-power modes transitions



How to associate LP modes

- **RUN:** do you need high computation power, but would like to be green?
- **LOW POWER RUN:** do you have weak power source, but supercapacitors are too costly?
- **SLEEP/LPSLEEP:** do you need peripherals running all the time, but power budget is limited?
- **STOP:** do you need balance between wake up time and low power consumption?
- **STANDBY:** do you need to consume very little power, but still SRAM needs to be retained?
- **SHUTDOWN:** is a low power consumption a top priority in your design?

End

www.st.com/stm32l4