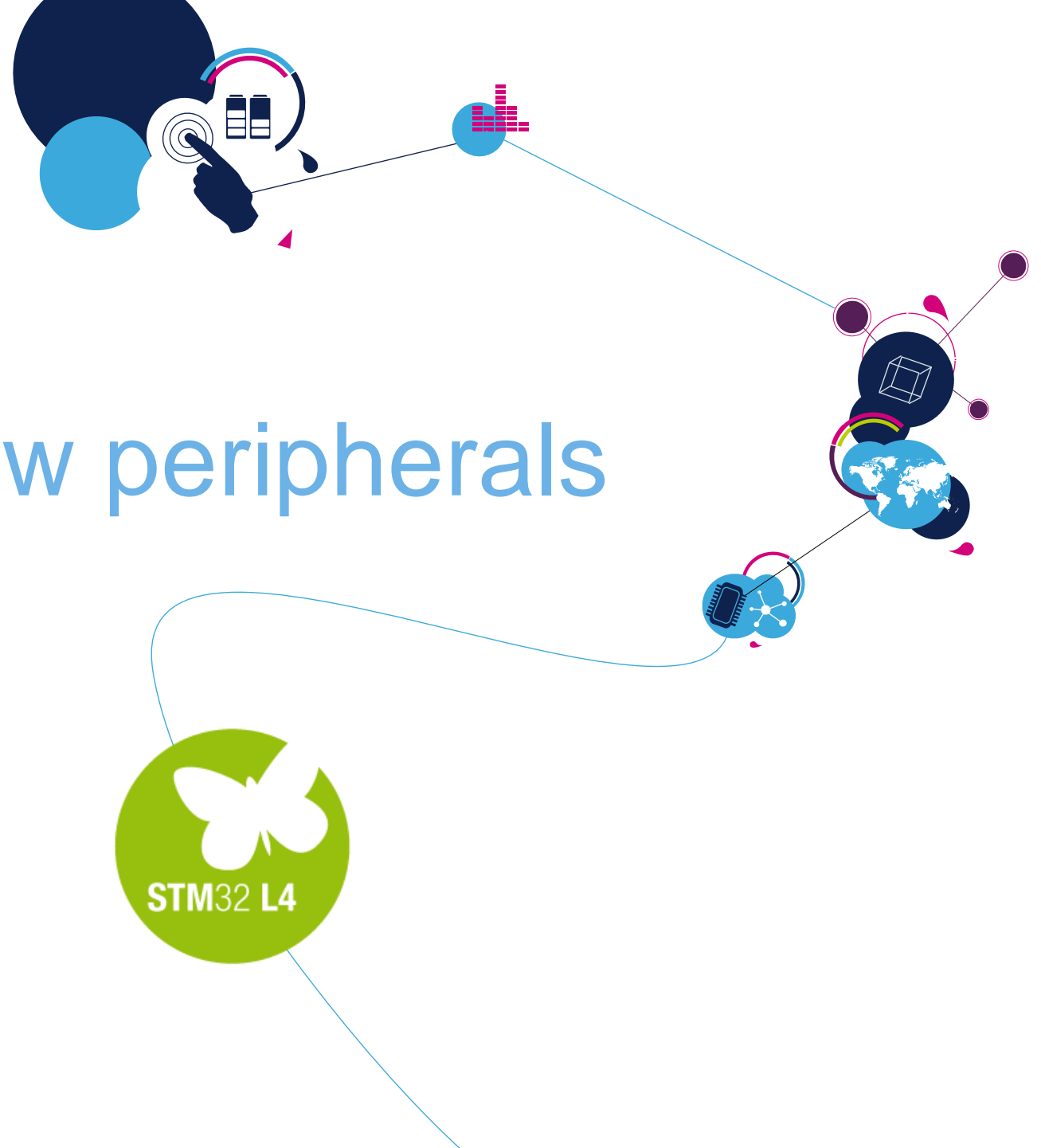


STM32L4 – new peripherals

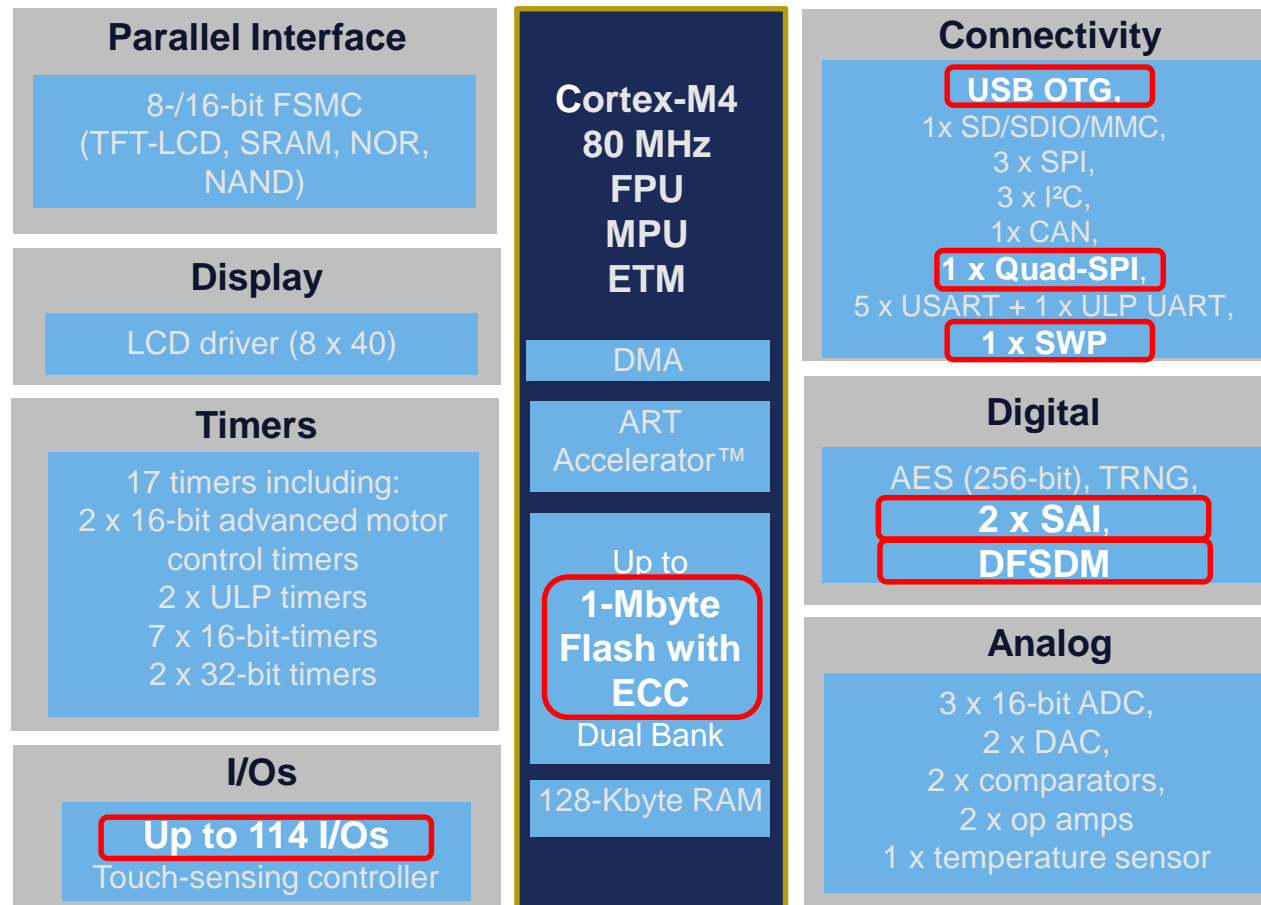
STM32L4 workshop





High integration 2

High integration with high memory size in small packages

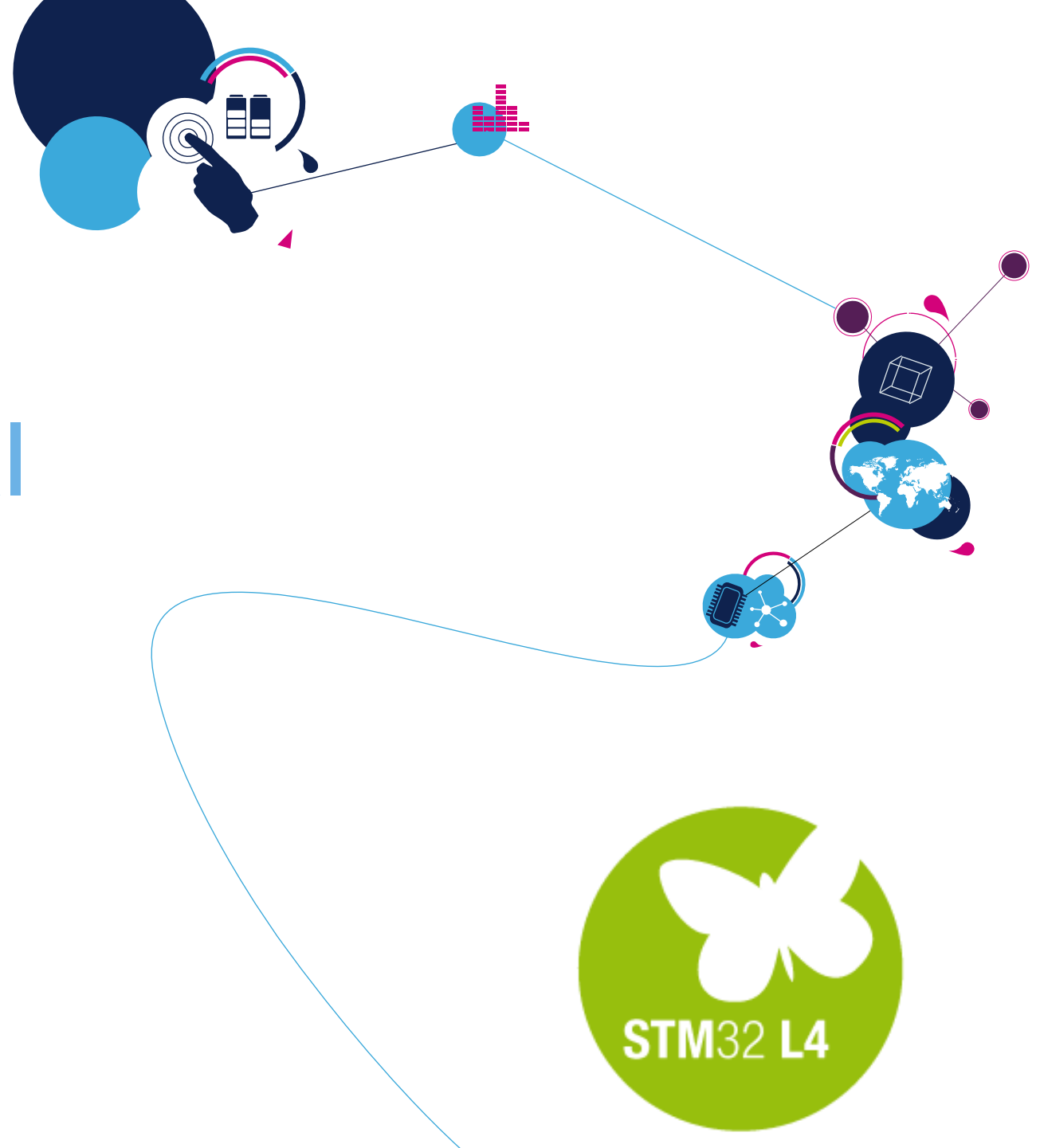


Package size down
to 4.4 x 3.8 mm



STM32L4 - SAI

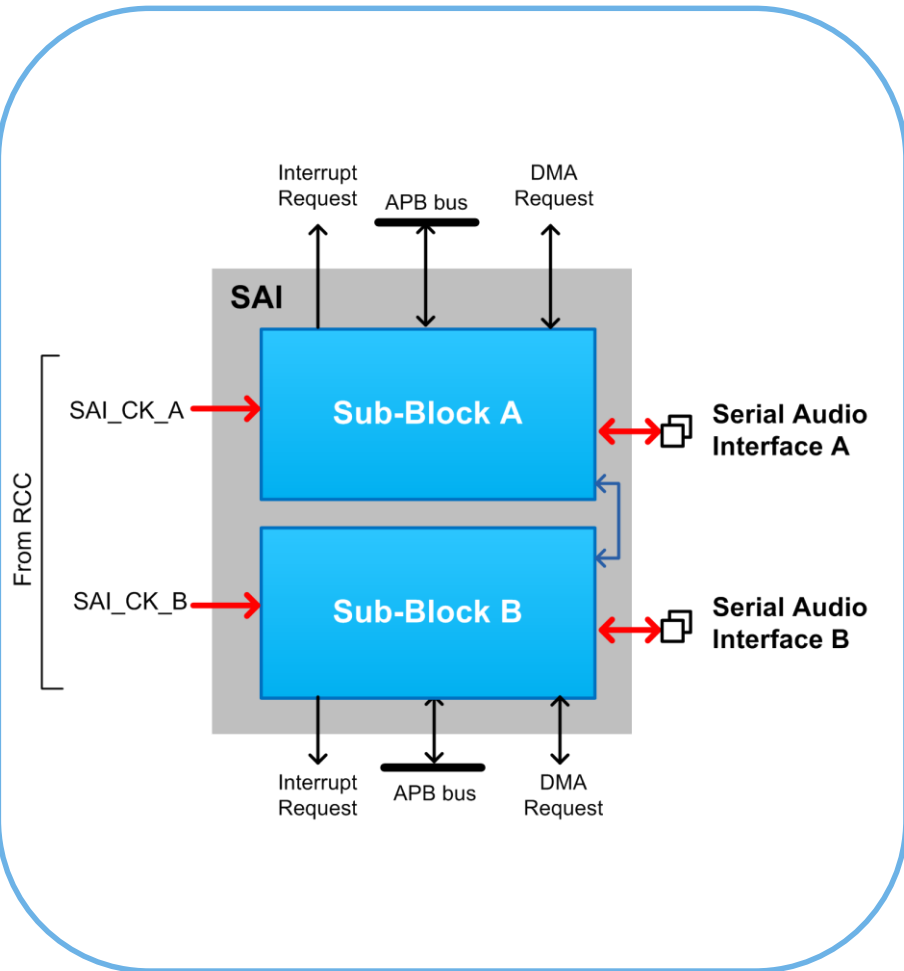
Serial Audio Interface



- Provides communication interface with external audio devices
 - Fully configurable
 - Supports standards: I²S, PCM, TDM, SPDIF, AC97
 - Two Independent Sub-Blocks

Application benefits

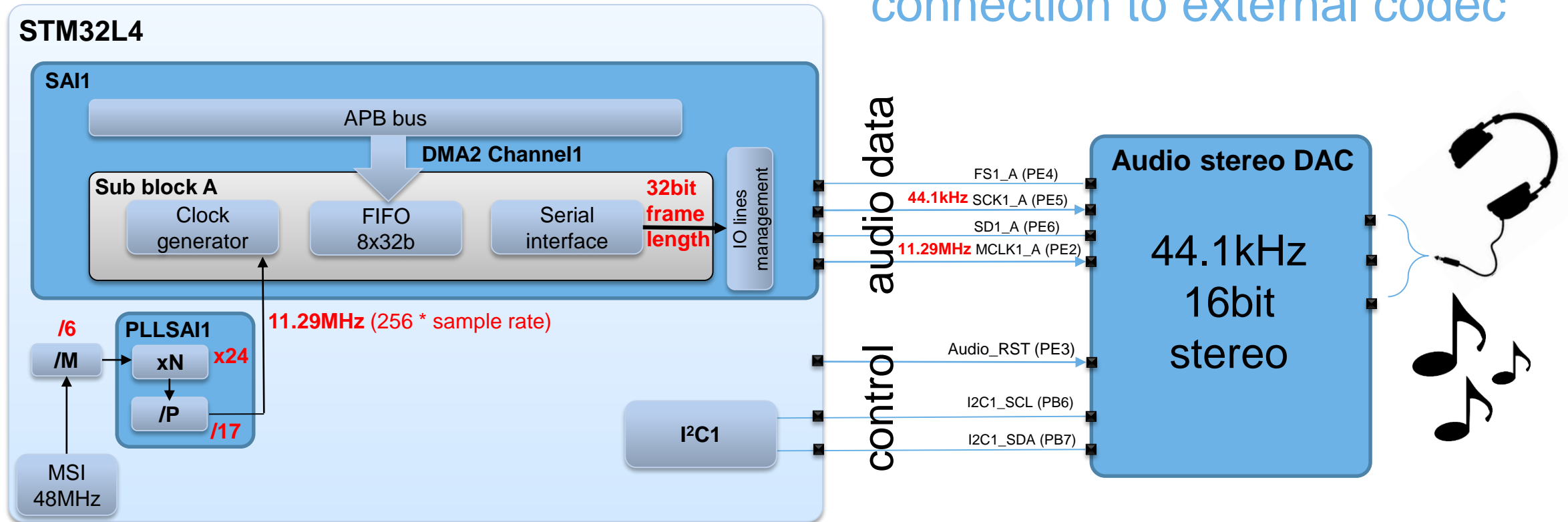
- Supports large variety of audio devices
- Full Duplex operation
- Fully Configurable Digital Audio Formats



SAI use case

connection to external codec

5



- Considering playback the music on external codec with **44.1kHz** sample rate, using **16bit**/channels (Stereo signal) we should connect **11.29MHz** signal clock to SAI module
- Data should be transferred to SAI1 FIFO via DMA2 Channel1 controlled by SAI1_A
- To control external DAC we can use one of I²C interfaces (like I²C1)

STM32L4 - SWPMI

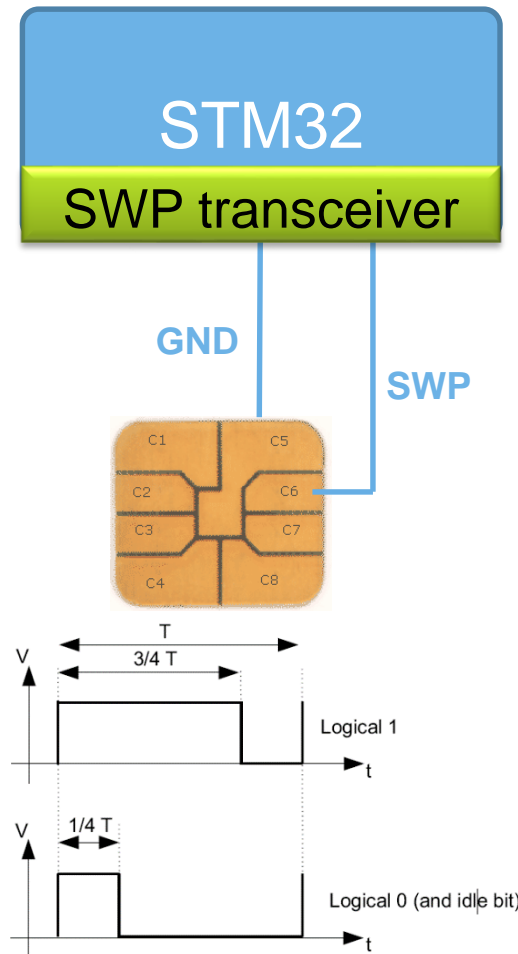
Single Wire Protocol Master Interface



- Implements a full-duplex single-wire communication interface, according to the single-wire protocol defined in the ETSI TS 102 613 standard, in Master mode

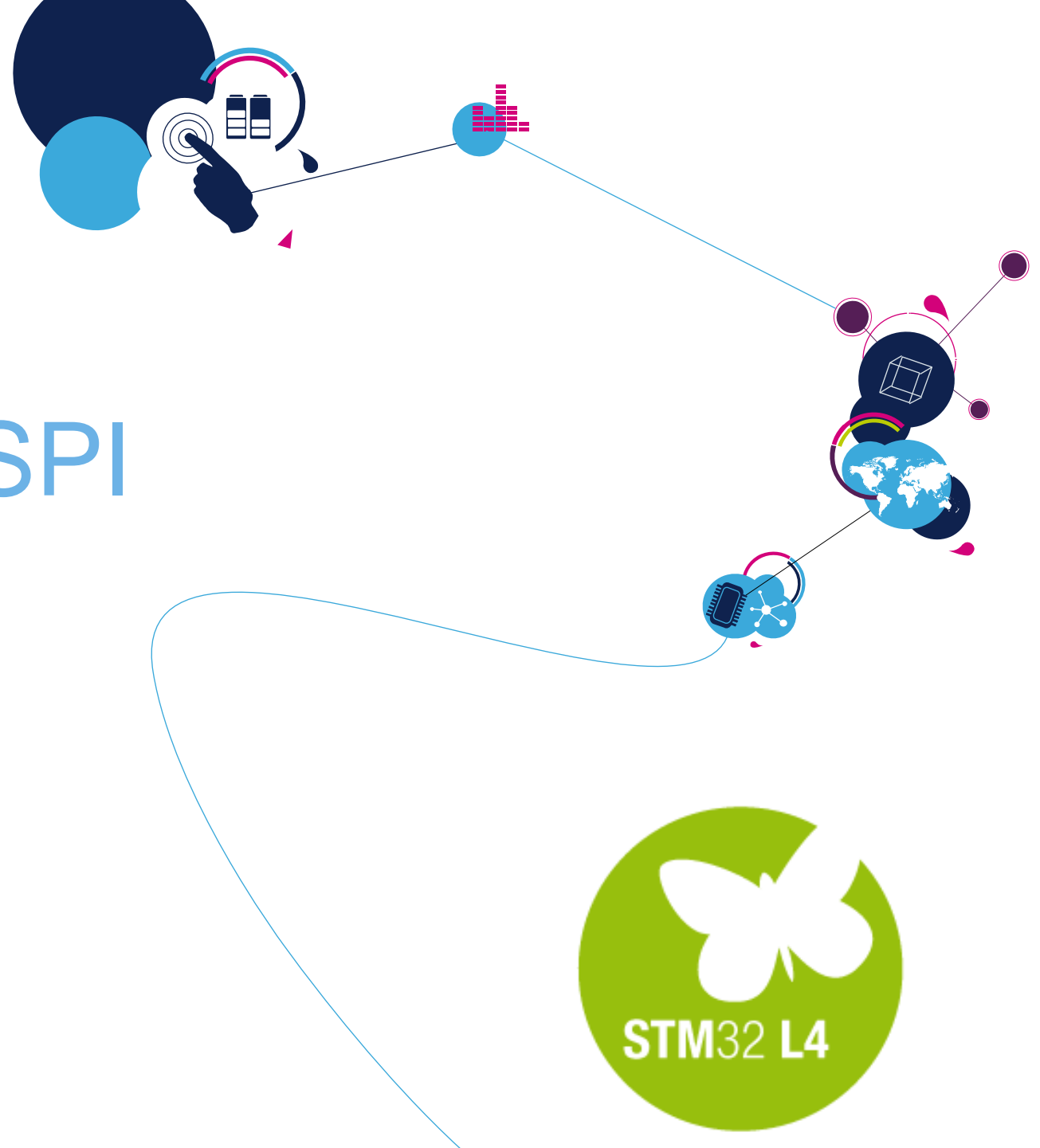
Application benefits

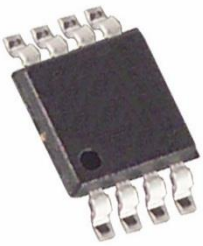
- SWP transceiver embedded inside STM32
- Single-wire full-duplex communications via C6 contact of a smartcard from 100 kbit/s to 2 Mbit/s



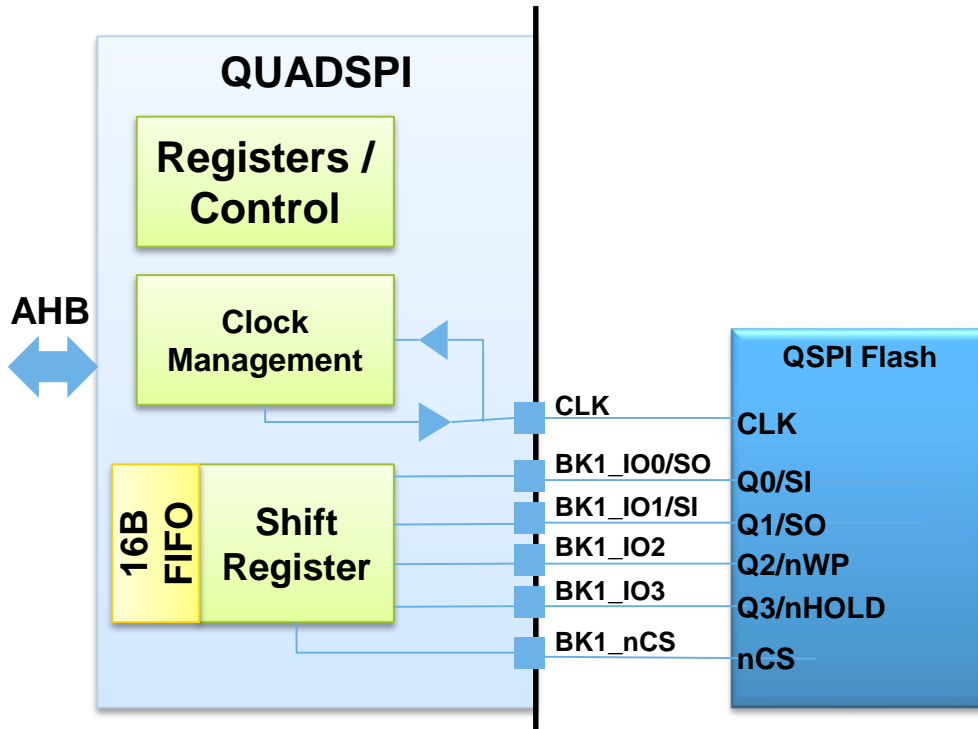
STM32L4 – QSPI

Quad SPI memory interface





Overview 9



- The Quad-SPI memory interface provides a communication interface with **external serial Flash** memories

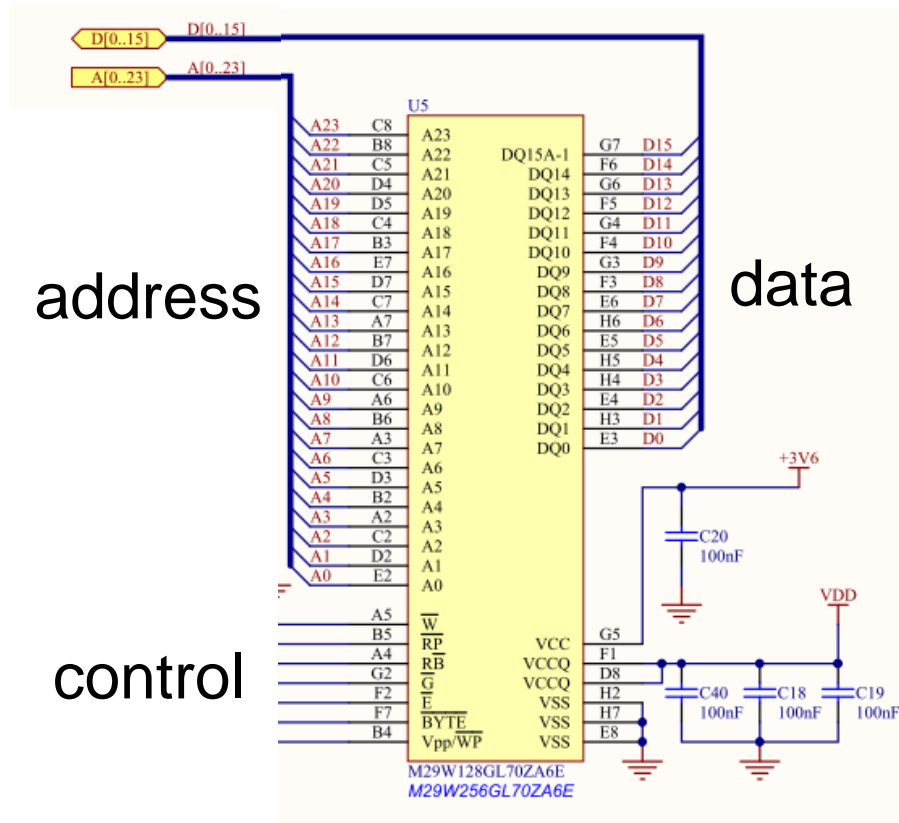
- Fully configurable
- Supports Execute in Place (XiP)
- Memory mapped

Application benefits

- Supports all SPI Flash memories
- Only a few (4+2) pins needed
- Easy memory expansion in existing project

QSPI vs. NOR Flash memories pin hunger

10

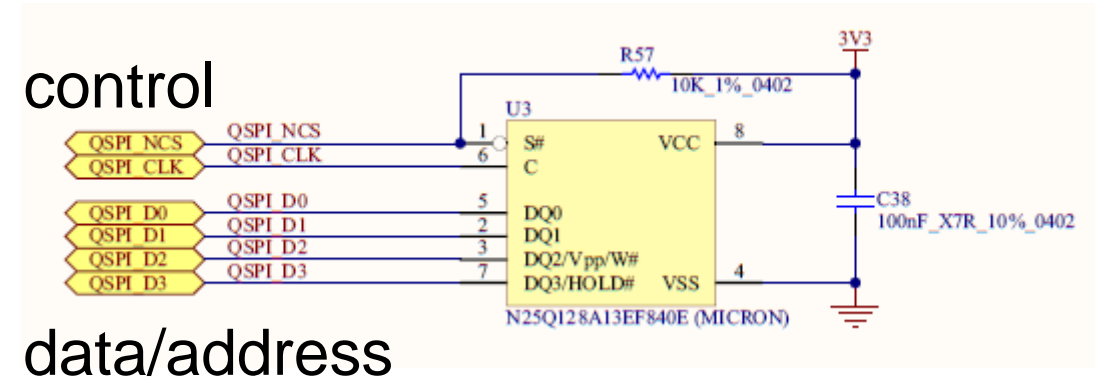


address

data

control

22 lines for address,
16 lines for data,
5 lines for control



control

data/address

4 lines for data,
2 lines for control

Performance & power consumption

11

- Data fetch performance comparison

- Time to read a 10kB table from external Quad-SPI Flash / internal Flash / internal SRAM
- Code execution from internal Flash memory

Conditions	External QSPI	Internal Flash	Internal SRAM
CPU @ 80 MHz – QSPI SDR 4 lanes @ 40 MHz	257 μ s	152 μ s	88 μ s
CPU @ 48 MHz - QSPI DDR 4 lanes @ 48 MHz	214 μs	227 μ s	147 μ s

External Quad-SPI: Micron N25Q256A13EF840E / XiP Mode - Internal Flash: ART enable - Compiler: IAR v7.30.1.7746

- Power consumption of the STM32L4 during this benchmark (External Flash memory excluded)

Conditions	External QSPI	Internal Flash	Internal SRAM
CPU @ 80 MHz – QSPI SDR 4 lanes @ 40 MHz	21 mA	12.74 mA	14.11 mA
CPU @ 48 MHz - QSPI DDR 4 lanes @ 48 MHz	14.6 mA	8.79 mA	8.64 mA

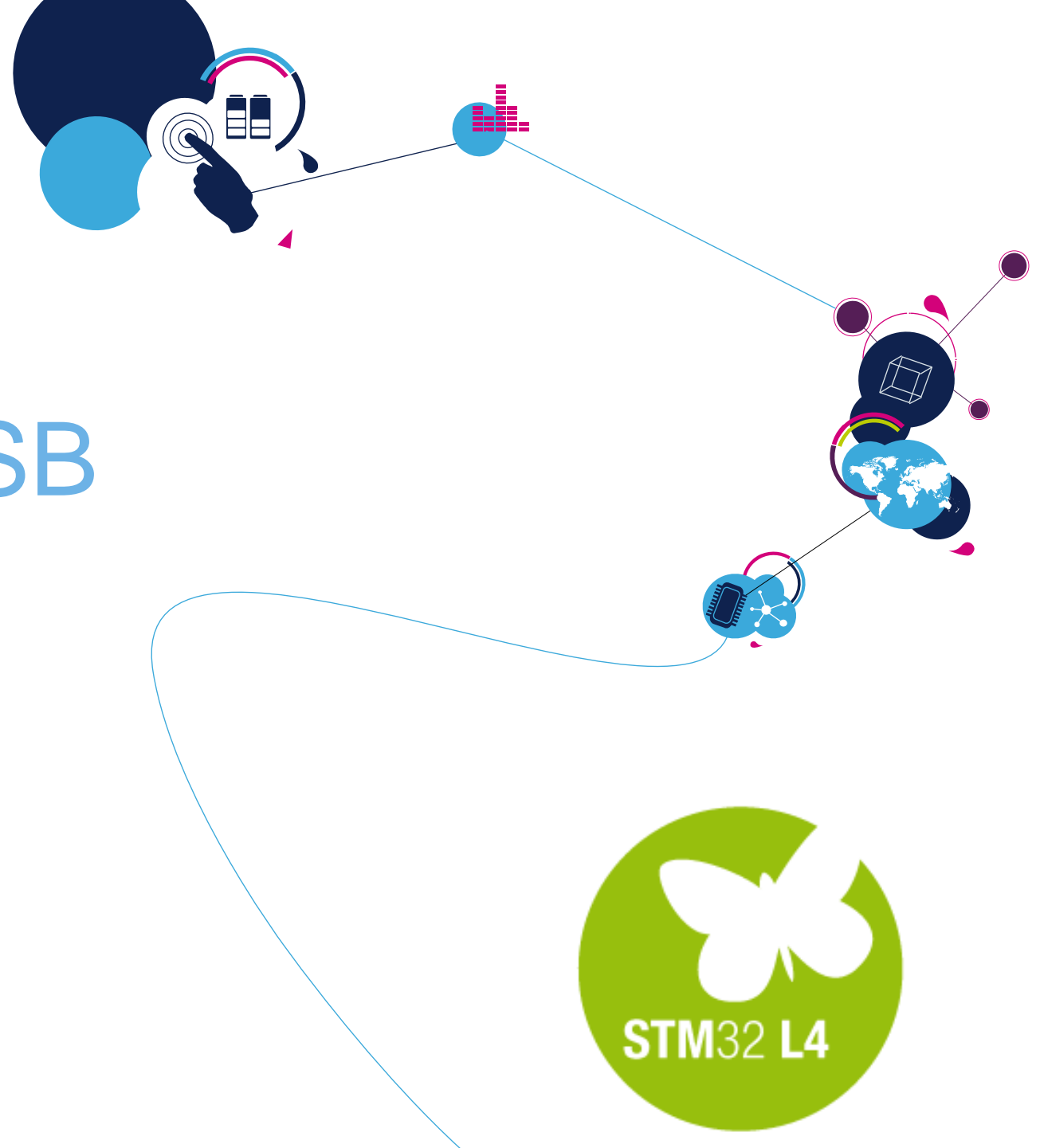
External Quad-SPI: Micron N25Q256A13EF840E / XiP Mode - Internal Flash: ART enable - Compiler: IAR v7.30.1.7746

The external Flash consumption depends on the Quad-SPI Flash device.

We measured ~4.7 mA @ 80 MHz/SDR and ~6.1 mA @48 MHz/DDR on data read benchmark for the selected part.

STM32L4 – USB

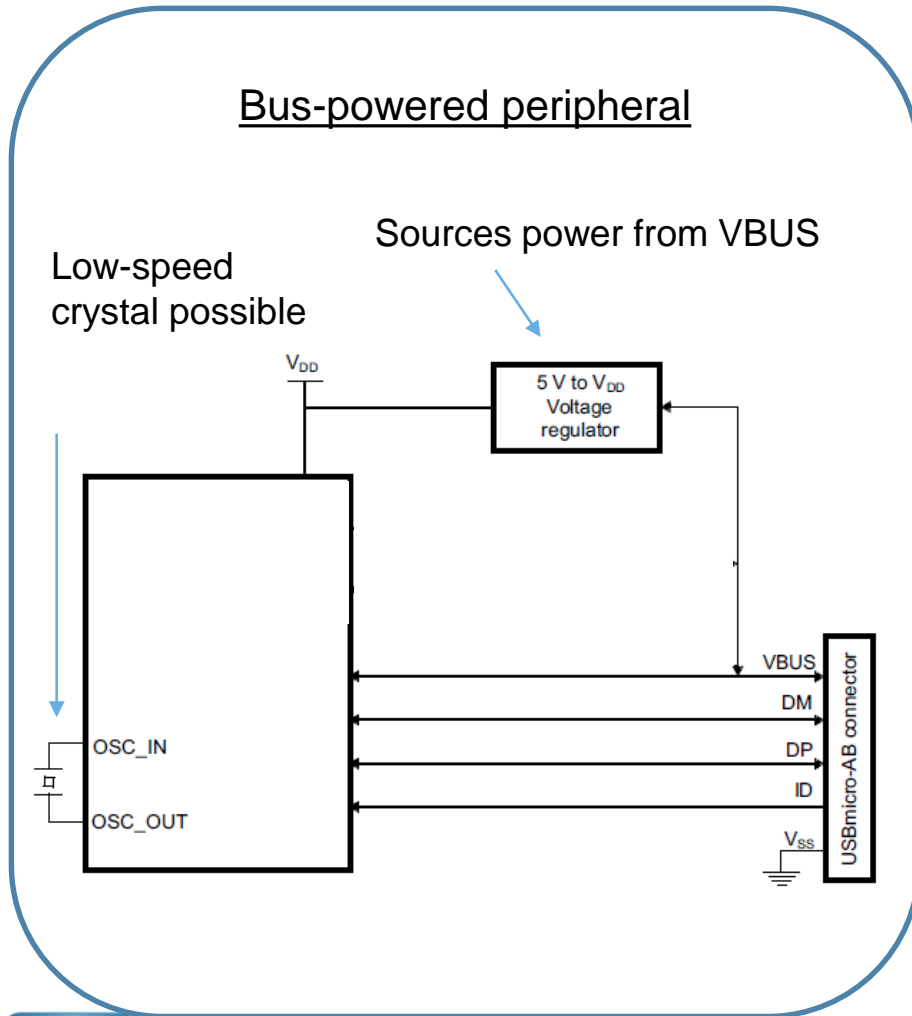
Extended functionality



- Provides USB 2.0 Full Speed interface
 - Supports OTG specification (OTG 2.0)
 - Includes battery charger detection (BC1.2)
 - ADP (Attach Detect Protocol)
 - Soft disconnection feature

Application benefits

- Separated power supply pin (V_{USB})
- VBAT charging feature w/ built-in serial resistor controllable by software
- Can work using internal 48MHz MSI oscillator
- On-The-Go (OTG) functionality
- Charging feature thanks to battery charger (BC) detection (up to 1.5A)



STM32L4 - DFSDM

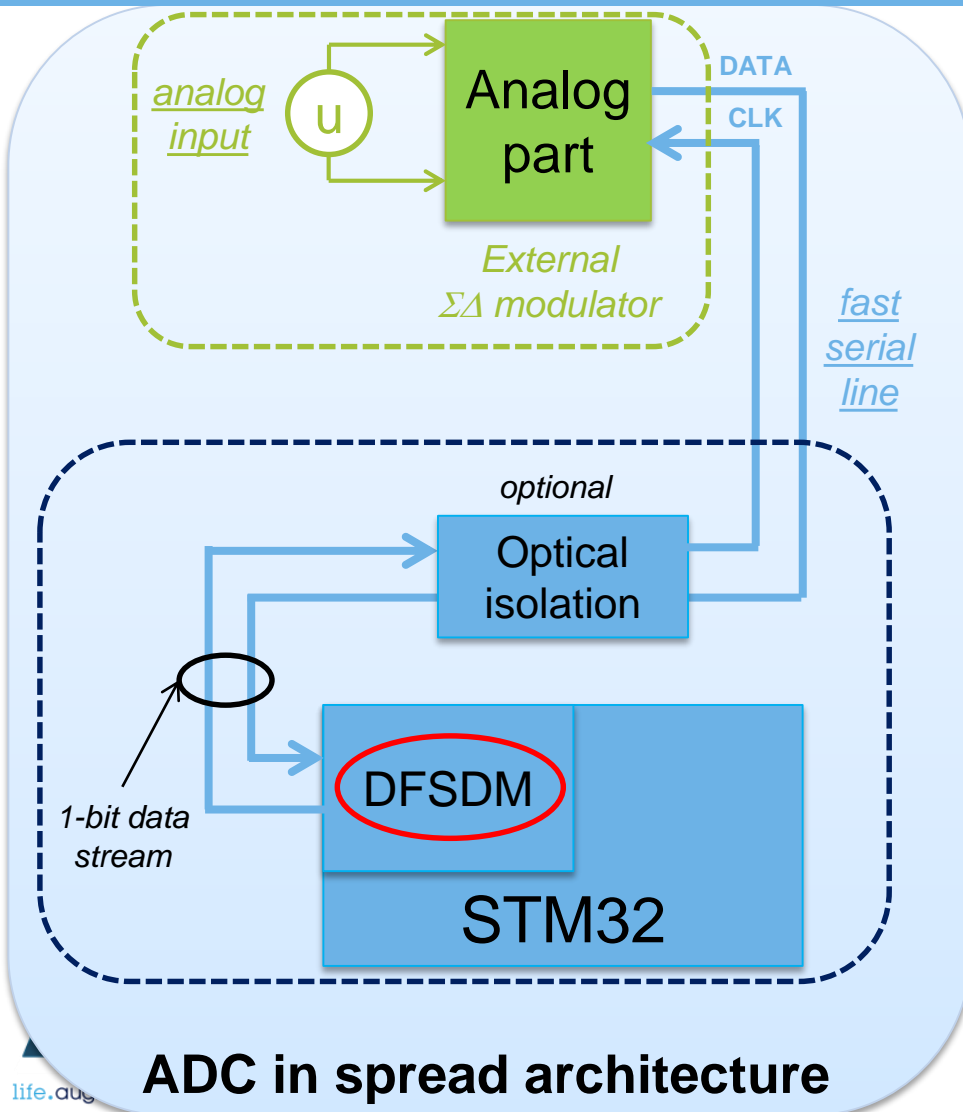
Digital filter for Sigma-Delta modulators
interface



DFSDM: introduction and typical usage

15

Behavior like ADC with scalable speed/resolution and external analog front end



- Split of analog and digital part:
 - Benefit from external analog selection
 - Benefit from internal digital features (DFSDM)

Application benefits

- External analog part: selection according needs: precision, less noise, extra fast, galvanic isolation, linearity, cheap, high voltage-side operation
- Digital part: serial line interface (1 or 2 wires), scalable speed vs. resolution (up to 24 bits), full features like ADC
- Examples: electricity meter, motor control, medical applications, MEMS microphone audio,

Decreased CPU burden and low-latency HW safety features

- Transceivers

- Fast serial input (20 MHz):
 - SPI or Manchester-coded mode (with clock absence detection)
 - Clock generation
- Internal parallel data input
 - 16-bit register data input (write by CPU/DMA)

- Filters

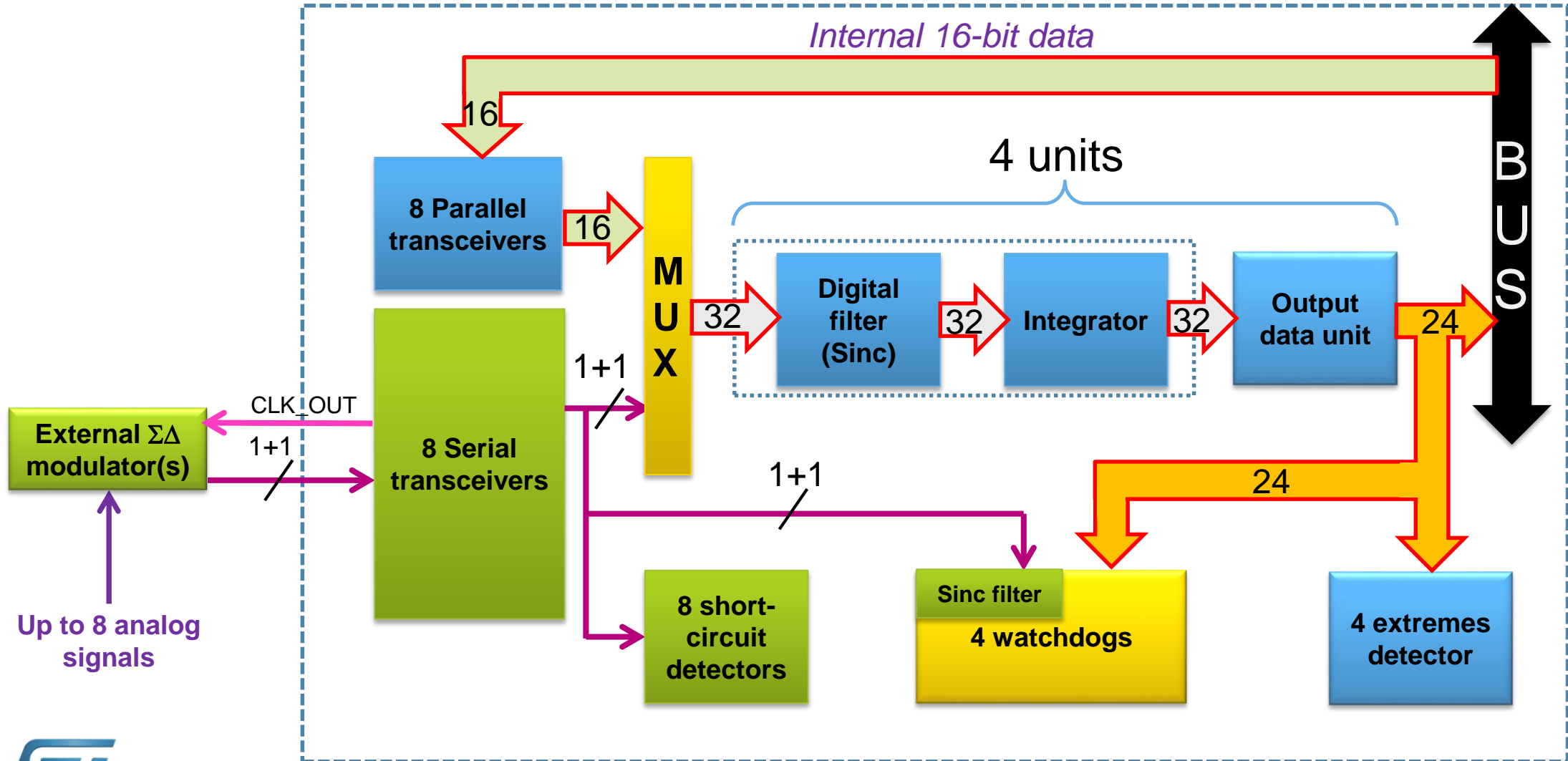
- Sinc1, Sinc2, Sinc3, Sinc4, Sinc5 and FastSinc filters with oversampling ratio up to 1024
- Integrator with oversampling ratio up to 1024

Application Benefits

- Support for various $\Sigma\Delta$ modulators suppliers (ST, TI, Analog Devices,...)
- Speed vs. resolution selection by filter configuration
- Internal data post-processing (SAR ADC results, ...)
- Additional functions: watchdog, short-circuit detector, extremes detector, offset correction

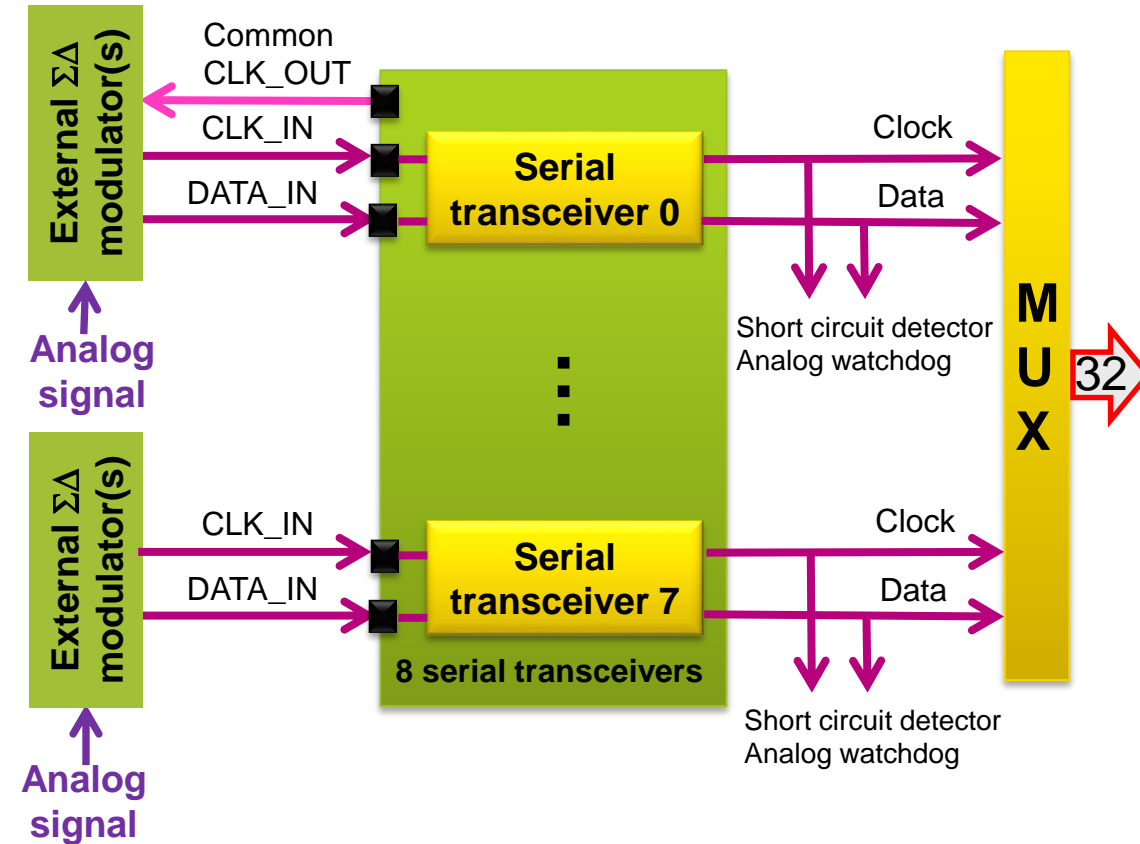
Block diagram

17



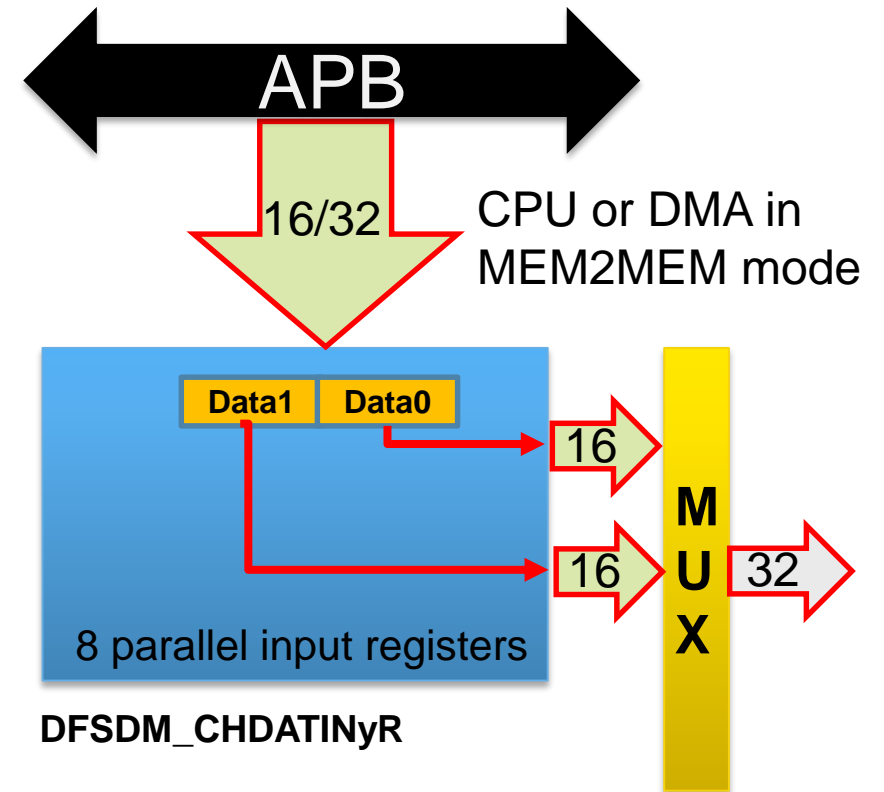
Compatible with any $\Sigma\Delta$ modulator output protocol

- To receive raw 1 bit serial stream from $\Sigma\Delta$ modulator and provide data & clock to the filter stage (up to 8 input serial channels)
- Any $\Sigma\Delta$ modulator output protocol support:
 - SPI mode (clock and data wire): falling/rising sampling edge, data rate measurement, clock presence detection
 - 1-wire Manchester-coded mode: lowest system cost (single isolator per input channel)
- Output clock generation on external pin:



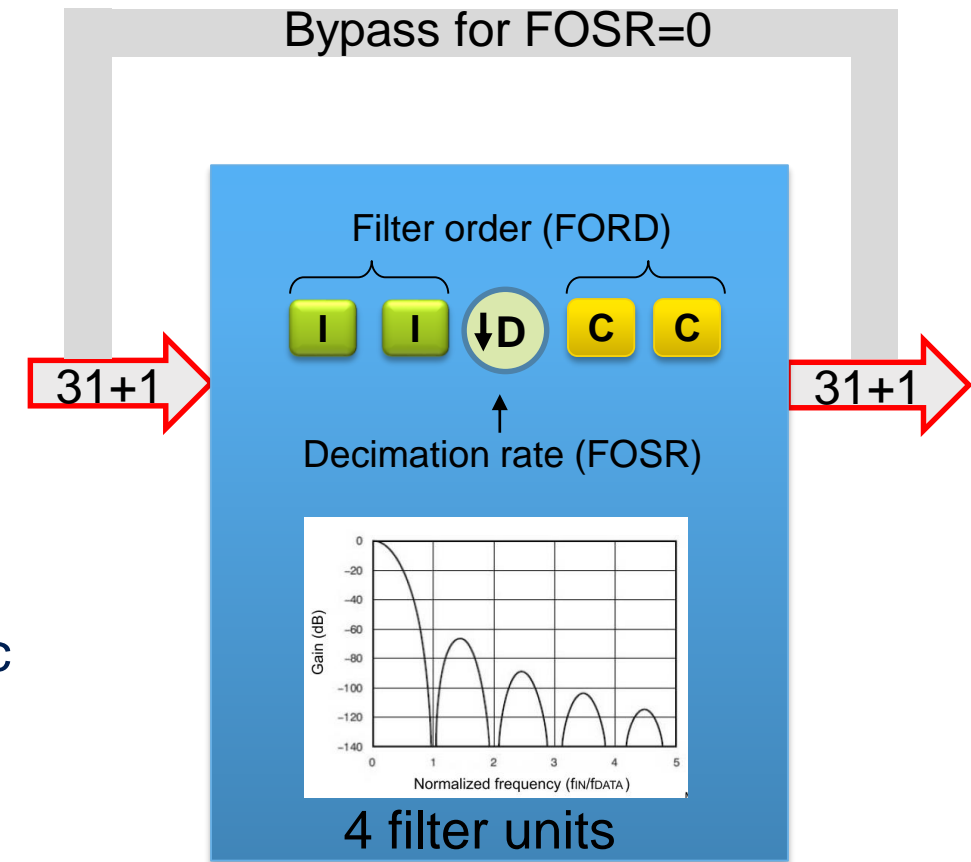
Fast hardware filtering of internal data

- To receive 16-bit parallel data stream from internal sources to the filter stage (up to 8 parallel channels/registers)
- RAM data post-processing
 - Data processing from internal ADCs
 - Data post-processing from collected data
- DMA or CPU can provide data to input registers



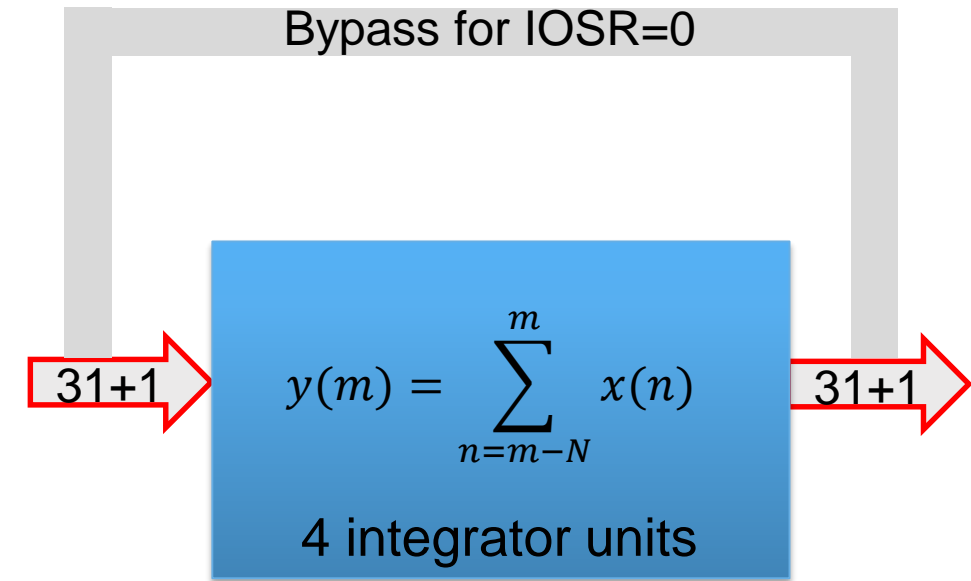
CPU free digital filtering

- Digital filter stage performs digital filtering of input data stream
 - Mean value of input data stream from $\Sigma\Delta$ modulator is the final ADC value (averaging)
 - Sinc filter performs moving average over given number of samples (oversampling ratio)
- Configuration options:
 - Filter type: Sinc1, Sinc2, Sinc3, Sinc4, Sinc5 and FastSinc
 - Oversampling ratio (FOSR): 1-1024 (can be bypassed)
 - Speed vs. resolution balance selection
 - Filter data resolution is 31-bit max



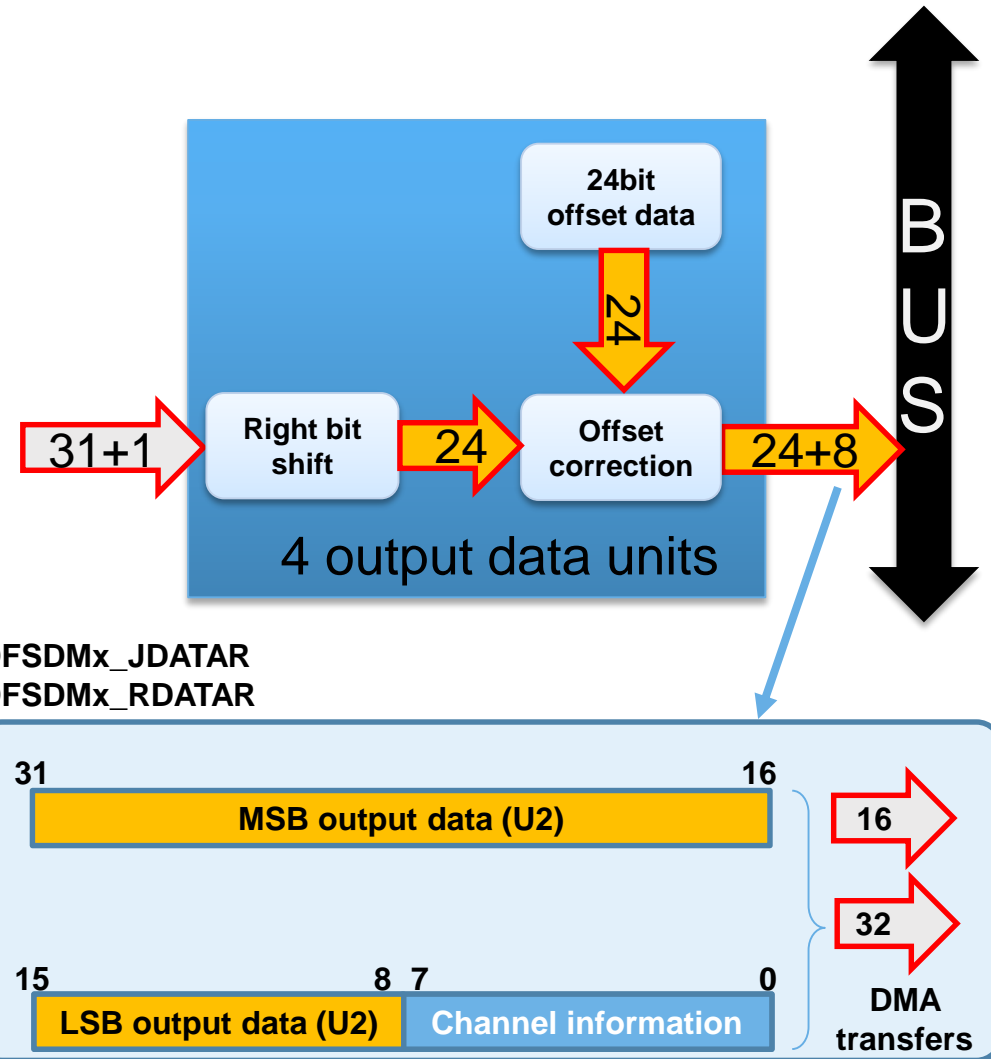
Additional increase of resolution

- Integrator stage performs additional signal processing – averaging of data from digital filter (summing N samples)
- Configuration:
 - 1 to 256 samples (N) to sum
 - Can be bypassed (if IOSR=0)
- Final result is sent to the output data unit



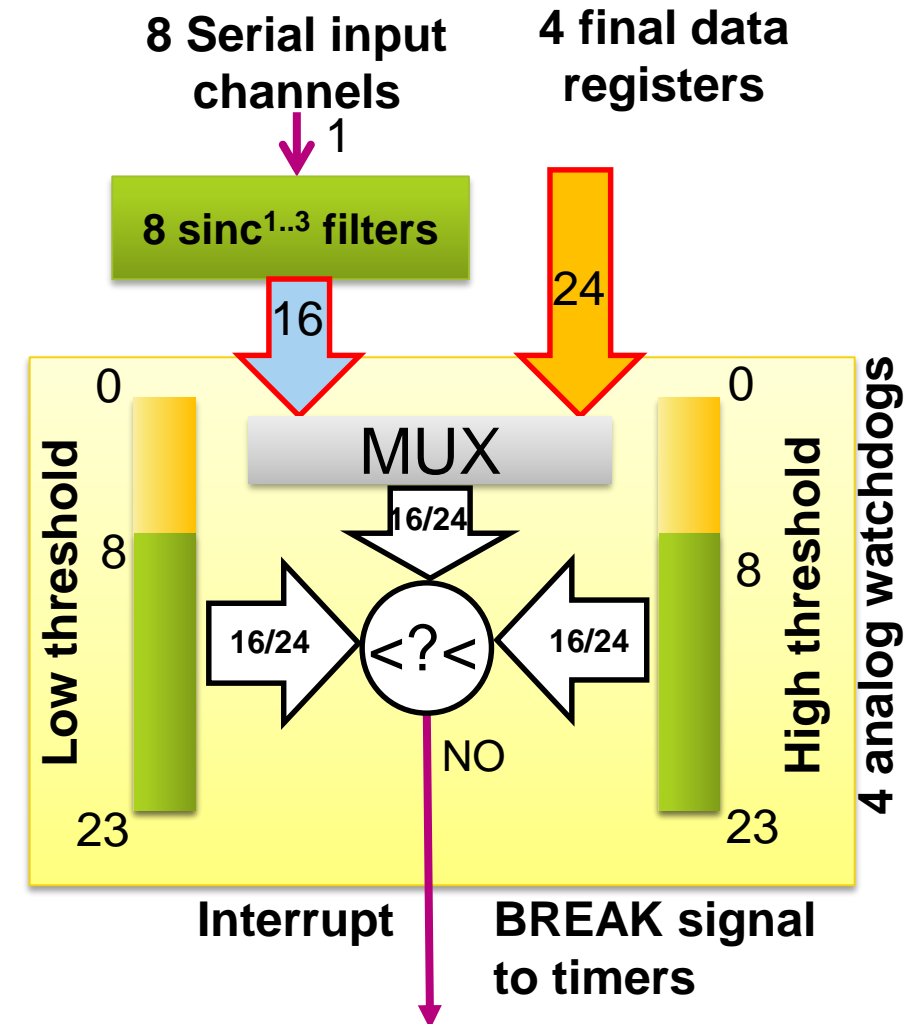
CPU-free external offset removal and data formatting

- Performs final post-processing functions on final data:
 - Offset compensation/subtraction
 - Programmable right-bit-shifting
- Offset correction feature:
 - Offset is stored in register by user (from user calibration procedure) - for each input channel
- 24-bit final data register width:
 - Configurable right bit shift to convert internal 31-bit resolution into final data register resolution



Safety and emergency functions such as monitoring of critical motor control values

- Monitoring if value is outside selected boundary
 - Final data result monitoring
 - Or independent input channels data monitoring
- Support for safety/emergency functions
 - Break or Interrupt signal generation
 - Separate flags for high and low boundaries
- Input channels monitoring has configurable filters:
 - Sinc1, Sinc2 and Sinc3 filter with an oversampling range 1 to 32
 - Watchdog data filters are available for user

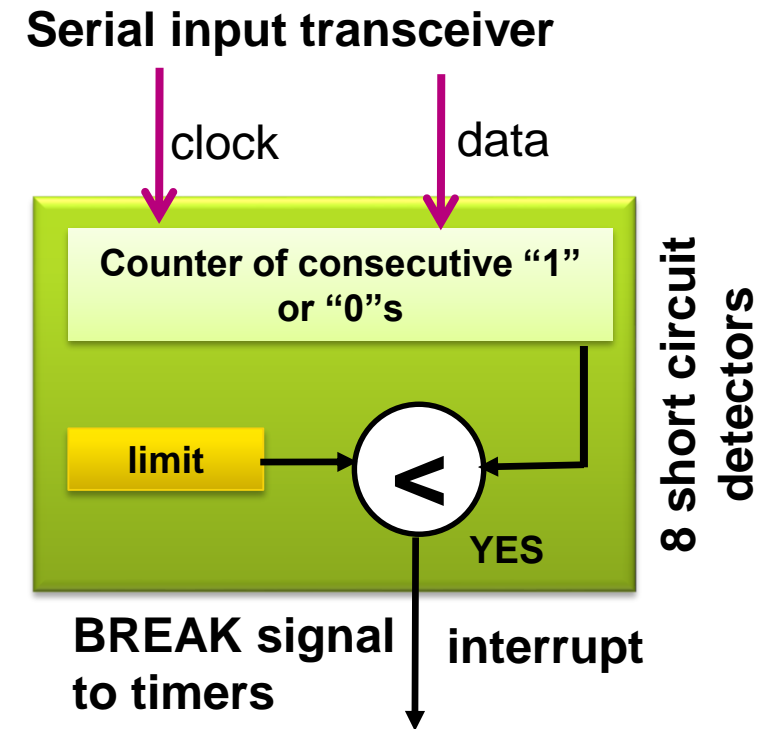


Short circuit detector

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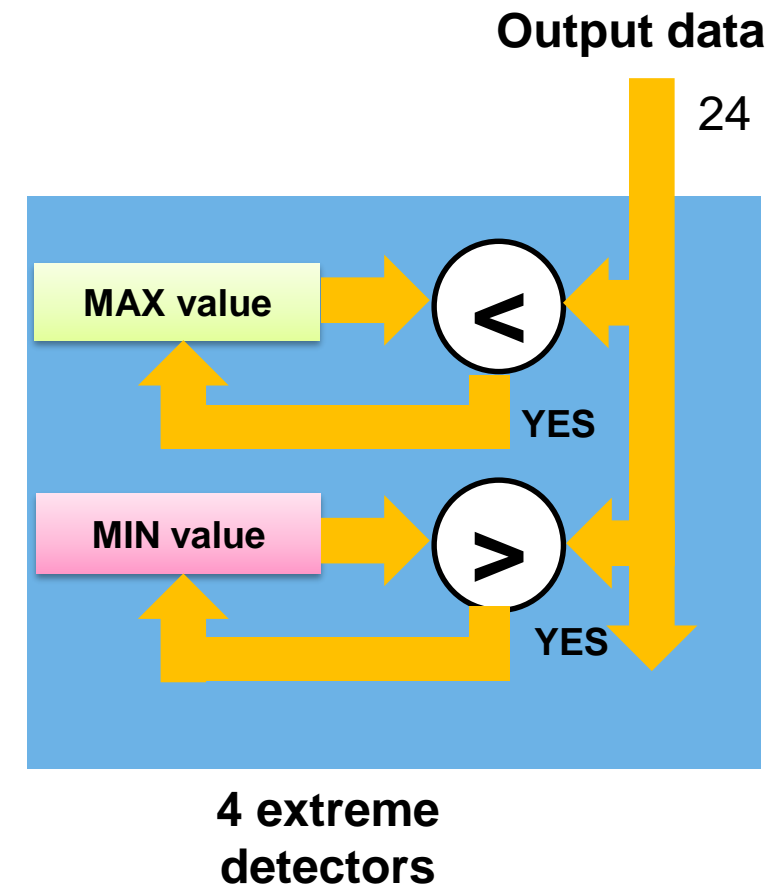
Very fast safety and emergency functions
such as motor control short-circuit monitoring

- Very fast detection of critical state:
 - Saturation of input signal for longer time means overcurrent (short circuit) or overvoltage
- Detection if signal is saturated for given time
 - Configurable time: 1 to 256 consecutive 1s or 0s in the $\Sigma\Delta$ stream (all 1s or 0s)
- Independent monitoring on all input channels
 - Also if main conversion is stopped
 - Interrupt generation (for software intervention) or break signal (for example: to shutdown PWM generation with no latency)



Hardware detection of peak values Example: audio data normalization

- Watching for minimum and maximum values in data output results
- Store the maximum and minimum values of the output data values into registers for selected channels
- Hardware monitoring of extreme values
- Extreme values are refreshed by software (by reading min/max registers)



- **Regular conversions**

- Only one channel selection (from 8 input channels)
- Launched by software only (no HW trigger)
- Continuous mode feature
- Can be immediately interrupted by injected conversion (with flag signaling this interruption)

- **Injected conversions**

- Can be set on more input channels (to add them into injected selection group)
- Scan mode (by trigger event): all selected channels (whole group) are converted
- Single mode (by trigger event): only one channel is converted and next is selected
- Launched by SW or HW trigger: timers outputs or external pins
- No continuous mode (can be emulated by timer triggered mode)

Very fast signal processing in hardware: consumption reduction.
All existing $\Sigma\Delta$ modulators speeds are supported.

- **Clock speeds**

- Maximum DFSDM clock: same as system clock (max. 80 MHz)
- Maximum input serial clock into channel (Input data rate)
 - SPI mode: DFSDM clock divided by 4 (max. 20 MHz)
 - Manchester mode: DFSDM clock divided by 6 (max. 10 MHz)
- Maximum output frequency on clock output: DFSDM clock divided by 4 (max. 20 MHz)

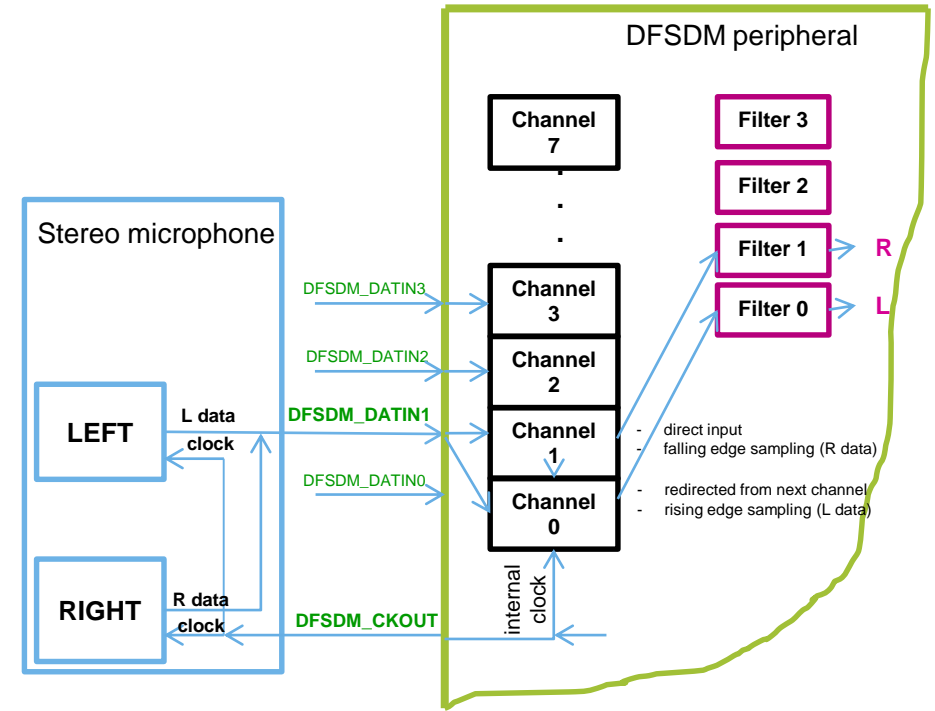
- **Output data rate**

- Depends on filter and integrator oversampling ratio (FOSR, IOSR):
 - Output data rate = Input data rate / (FOSR * IOSR) , where: FOSR = 1-1024, IOSR = 1-256

Application example 1

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- **Stereo MEMS microphone (with PDM output) playback**
 - Only 2 wires are used to connect 2 microphones (stereo) – common clock and data wire with different sampling edges for left and right channel (and using DFSDM feature: redirection of data from given input channel pin to another channel data input).
 - Regular conversions are used for two DFSDM channels in continuous mode.
 - Low CPU load: one DMA transfers output audio data to RAM and second DMA transfers those data to I2S interface (which sends them to external audio codec and headphones).

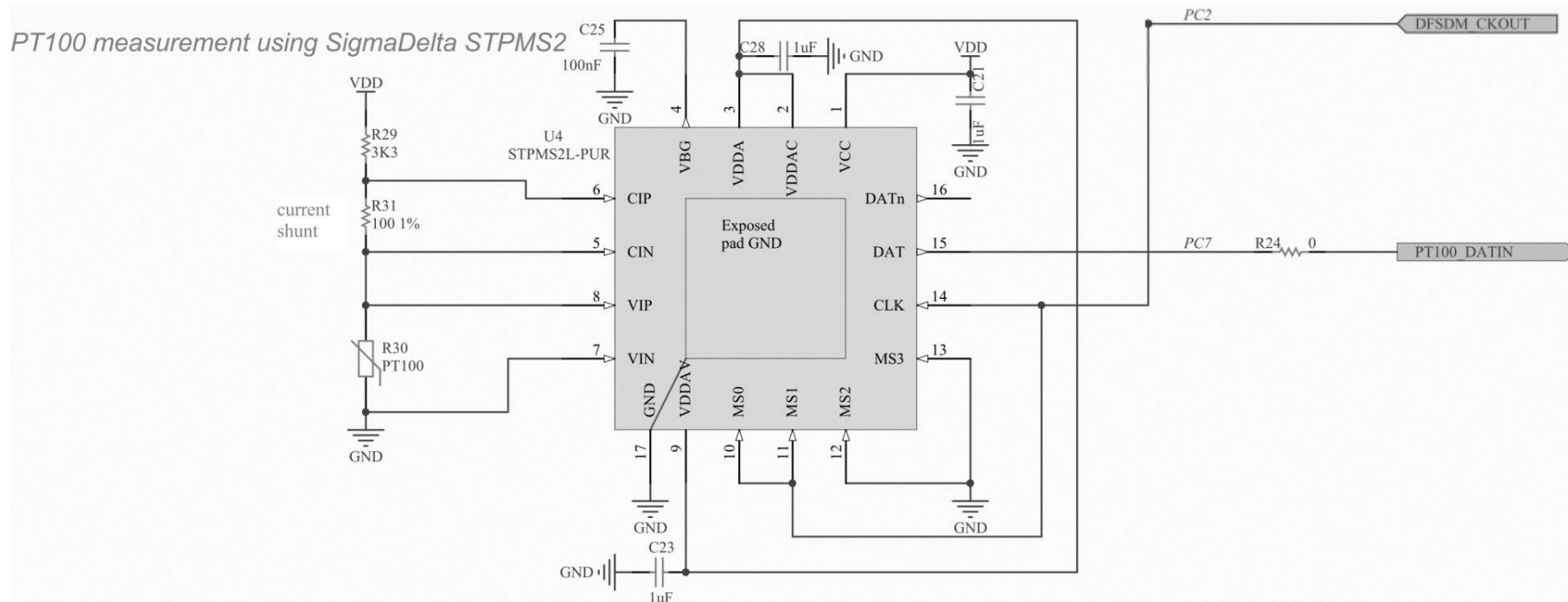


Application example 2

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- **PT100 thermometer**

- An external STPMS2 device (dual-channel, second-order sigma-delta modulator) is used to sense 2 input channels
- One channel senses voltage on PT100 sensor, second channel senses current over PT100 sensor (on shunt). Ratio of channels data results is the PT100 sensor resistance.
- Injected scan conversion is used for those 2 channels with 1-sec periodic timer trigger.

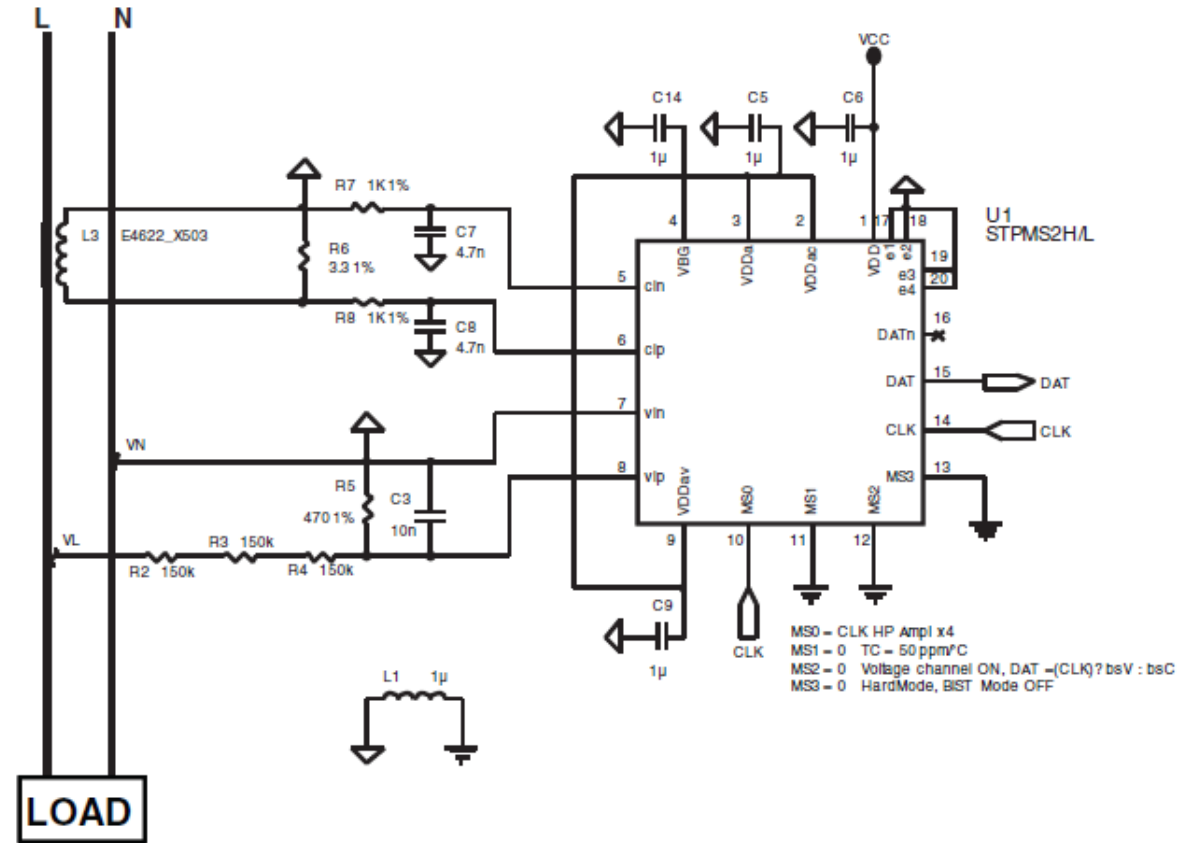


Application example 3

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• Electricity meter with STPMS2

- External STPMS2 device (dual $\Sigma\Delta$ modulator) is used to sense 2 input channels: voltage (voltage divider) and current (current transformer or shunt).
- Voltage and current samples are sent to DFSDM by serial interface (clock and data wire only).
- The DFSDM processes the voltage and current samples into wide resolution.
- STM32 firmware calculates electric power and energy.



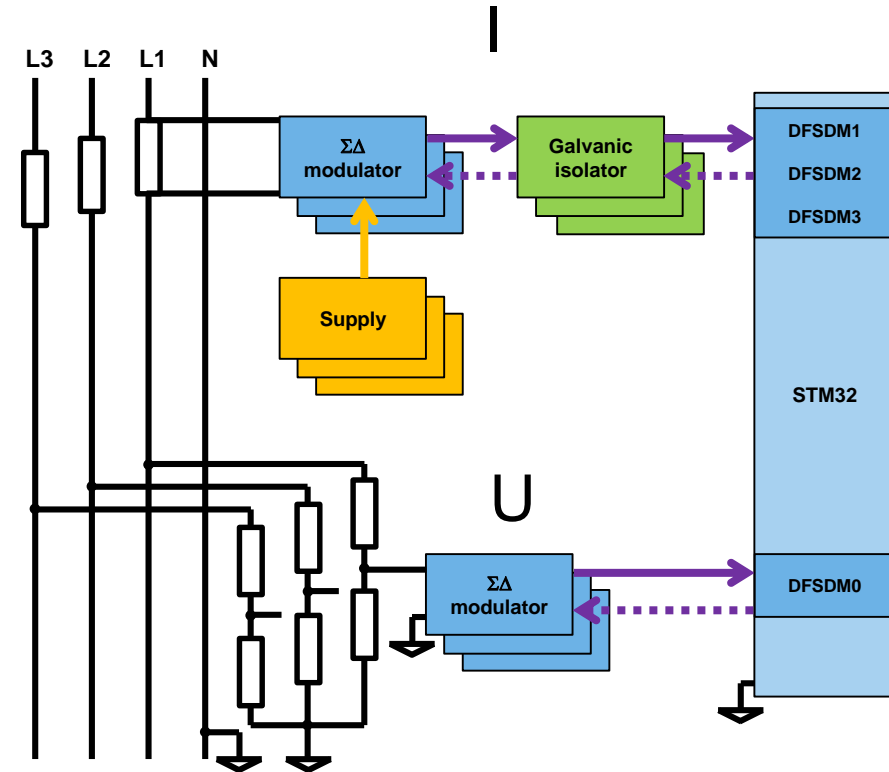
Application example 4

33

- **3-phase electricity meter**

(using shunts, no transformers)

- Voltages (U) are sensed by resistor dividers. One DFSDM filter with 3 multiplexed inputs is used to scan 3-phase voltages.
- Currents (I) are sensed by shunt resistors with galvanic isolated $\Sigma\Delta$ modulators. One or two isolation lines per phase are necessary only for current data transfers to DFSDM channels (Manchester-coded mode requires only 1 line).
- STM32 firmware calculates electric power and energy.



STM32L4 – other changes



What else ?

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ADC, DAC

Voltage reference buffer with output on the pin

FLASH

ECC feature with IRQ/NMI generation

GPIO

Default configuration of I/O lines is **analog input** for low power consumption



PWR

Programmable pull-up/pull-down resistors in Standby mode

Peripherals Voltage Monitoring (PVM)

RCC

Low speed clock output pin (LSCO) to put LSE/LSI clock outside (even in STOP1/2 and STANDBY modes)

WWDG

Early wakeup function within Window Watchdog



STM32L4 – BOM reduction

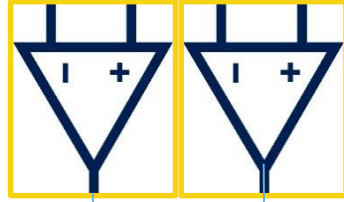
How we can reduce list of components by using STM32L4 device

Nice to have, but...

37

Low cost, low power 2-channel ADC (Single Integration):

2 external comparators
2 external capacitors



External ADC converter data processing:

High CPU load on data processing

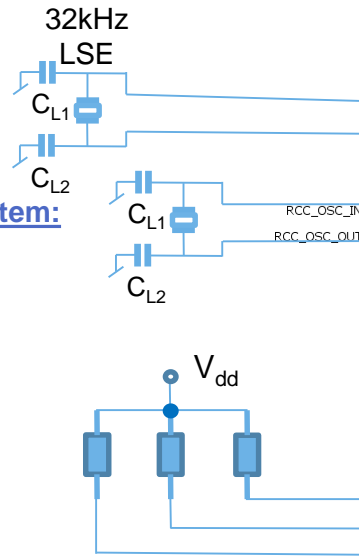
Data collection from stereo MEMS microphone:

High CPU load on PDM decoding



Precise clock for USB and system:

2 lines for the crystal
3 external components

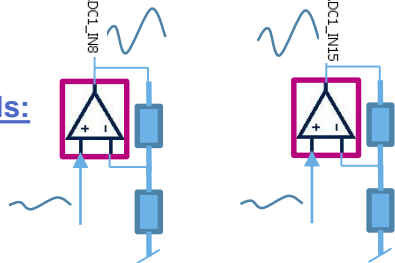


Configured state on N I/O lines in STANDBY mode:

N external pull-up/pull-down resistors

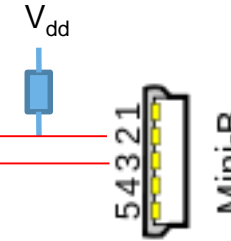
Measurement of low amplitude analog signals:

External OpAmps
2 external resistors per OpAmp



USB connector to the host:

Power supply >3.3V
External resistor
Additional hardware for USB reconnection



External Flash memory to store more data

NOR Flash over FSMC:
19 lines (16 data, 3 control)



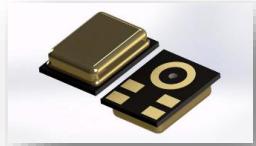
Low cost, low power 2-channel ADC (Single Integration):
Built-in comparators

STM32L4 offer

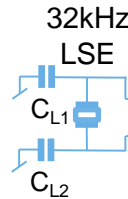
38

External $\Sigma\Delta$ ADC converter data processing:
Built-in Digital Filter for Sigma Delta Modulators

Data collection from stereo MEMS microphone:
Built-in Digital Filter for Sigma Delta Modulators
(HW processing of PDM signal)

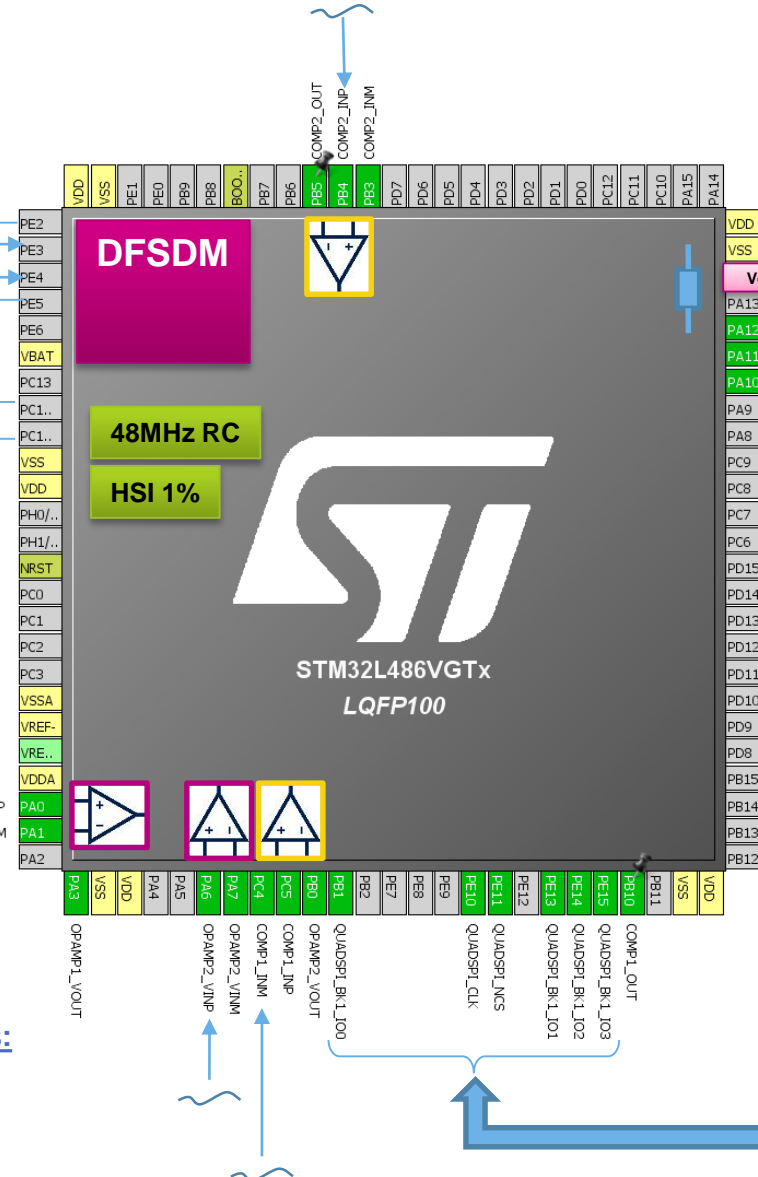


Precise clock for USB and system:
Built-in precise RC oscillators:
MSI 48MHz – self-trimmable to LSE



Configured state on N I/O lines in STANDBY mode:
Programmable pull-ups/pull-downs on I/O lines

Measurement of low amplitude analog signals:
Built-in PGA (programmable gain amplifiers)
Possible to add external components

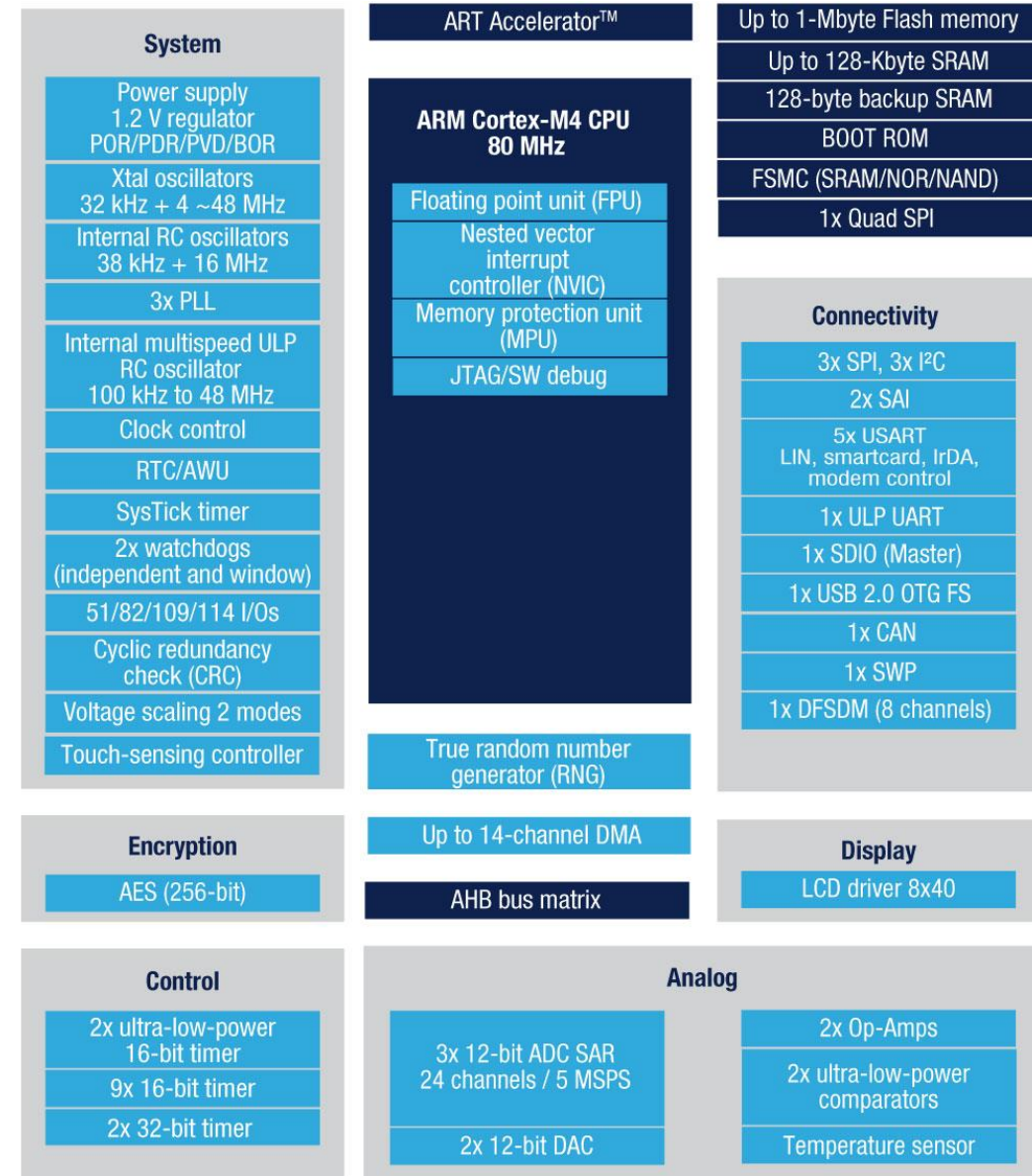


USB connector to the host:
Separate USB power supply
Built-in pull-up resistor on DP line
Software reconnection

External Flash memory to store more data
QSPI Flash memory:
6 lines (4 data, 2 control)



- Separate Vddio2 power supply for PG[2..15] I/O lines
 - connection of peripherals working with voltage down to 1.08V without level shifters
- Built-in voltage supervisors (working even in Standby mode)
 - No need for use of external ones
- Smaller current peaks due to more stable current consumption
 - Less complex PCB layout
- Lower power consumption in low power modes
 - Smaller battery needed
- Built-in interconnection matrix
 - No need for use of external connections between peripherals
- Built in reference voltage (also available on the pin)
 - No need for use of external reference voltage



Enjoy!



The image is a composite graphic. On the left, a dancer in a purple tank top and red pants is captured mid-air against a light blue background. On the right, a dark blue background features a large green circle with a white butterfly logo and the text "STM32 L4". To the right of this circle is a network diagram with a central node containing a dancer silhouette, connected to three peripheral nodes: a cube, a microchip, and a smartphone. At the bottom, a grey bar contains three social media links: a Facebook icon followed by "/STM32", a Twitter icon followed by "@ST_World", and an "e2e" logo followed by "st.com/e2e".

 /STM32

 @ST_World

 st.com/e2e

www.st.com/stm32l4