4.6 Serial Port Clocking

The CS43L22 serial audio interface port operates either as a slave or master, determined by the M/$\overline{S}$ bit. It accepts externally generated clocks in Slave Mode and will generate synchronous clocks derived from an input master clock (MCLK) in Master Mode. Refer to the tables below for the required setting in register 05h and 06h associated with a given MCLK and sample rate.

Referenced Control	Register Location
M/$\overline{S}$.....	"Master/Slave Mode" on page 40
Register 05h.....	"Clocking Control (Address 05h)" on page 38
Register 06h.....	"Interface Control 1 (Address 06h)" on page 40

MCLK (MHz)	Sample Rate, Fs (kHz)	SPEED[1:0] (AUTO='0'b)	32kGROUP	VIDEOCLK	RATIO[1:0]	MCLKDIV2
12.2880	8.0000	11	1	0	00	0
	12.0000	11	0	0	00	0
	16.0000	10	1	0	00	0
	24.0000	10	0	0	00	0
	32.0000	01	1	0	00	0
	48.0000	01	0	0	00	0
	96.0000	00	0	0	00	0
11.2896	11.0250	11	0	0	00	0
	22.0500	10	0	0	00	0
	44.1000	01	0	0	00	0
	88.2000	00	0	0	00	0
18.4320 (Slave Mode ONLY)	8.0000	11	1	0	00	0
	12.0000	11	0	0	00	0
	16.0000	10	1	0	00	0
	24.0000	10	0	0	00	0
	32.0000	01	1	0	00	0
	48.0000	01	0	0	00	0
	96.0000	00	0	0	00	0
16.9344 (Slave Mode ONLY)	*8.0182...	11	0	0	10	0
	11.0250	11	0	0	00	0
	22.0500	10	0	0	00	0
	44.1000	01	0	0	00	0
	88.2000	00	0	0	00	0
12.0000	8.0000	11	1	0	01	0
	*11.0294...	11	0	0	11	0
	12.0000	11	0	0	01	0
	16.0000	10	1	0	01	0
	*22.0588...	10	0	0	11	0
	24.0000	10	0	0	01	0
	32.0000	01	1	0	01	0
	*44.1176...	01	0	0	11	0
	48.0000	01	0	0	01	0
	*88.2353...	00	0	0	11	0
	96.0000	00	0	0	01	0
24.0000	8.0000	11	1	0	01	1
	*11.0294...	11	0	0	11	1
	12.0000	11	0	0	01	1
	16.0000	10	1	0	01	1
	*22.0588...	10	0	0	11	1
	24.0000	10	0	0	01	1
	32.0000	01	1	0	01	1
	*44.1176...	01	0	0	11	1
	48.0000	01	0	0	01	1
	*88.2353...	00	0	0	11	1
	96.0000	00	0	0	01	1
27.0000	8.0000	11	1	1	01	0
	12.0000	11	0	1	01	0
	24.0000	10	0	1	01	0
	32.0000	01	1	1	01	0
	*44.1176...	01	0	1	11	0
	48.0000	01	0	1	01	0
	*11.0294...	11	0	1	11	0
	*22.0588...	10	0	1	11	0
	16.0000	10	1	1	01	0

Note: *The marked sample rate values are not exact representations of the actual frame clock frequency They have been truncated to 4 decimal places. The exact value can be calculated by dividing the MCLK being used by the desired MCLK/LRCK ratio.

Table 1. Serial Port Clocking

4.8 Initialization

The CS43L22 enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in the "Register Description" on page 37.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

4.9 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable.
2. Bring $\overline{\text{RESET}}$ high.
3. The default state of the "Power Ctl. 1" register (0x02) is 0x01. Load the desired register settings while keeping the "Power Ctl 1" register set to 0x01.
4. Load the required initialization settings listed in Section 4.11.
5. Apply MCLK at the appropriate frequency, as discussed in Section 4.6. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the "Power Ctl 1" register (0x02) to 0x9E.
7. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.11 Required Initialization Settings

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0x80 to register 0x47.
3. Write '1'b to bit 7 in register 0x32.
4. Write '0'b to bit 7 in register 0x32.
5. Write 0x00 to register 0x00.

5. CONTROL PORT OPERATION

The control port is used to access the registers allowing the CS43L22 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates using an I²C interface with the CS43L22 acting as a slave device.

5.1 I²C Control

SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The AD0 pin sets the LSB of the chip address; '0' when connected to DGND, '1' when connected to VL. This pin may be driven by a host controller or directly connected to VL or DGND. The AD0 pin state is sensed and the LSB of the chip address is set upon the release of the RESET signal (a low-to-high transition).

The signal timings for a read and write cycle are shown in Figure 16 and Figure 17. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS43L22 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write).

The upper 6 bits of the address field are fixed at 100101. To communicate with the CS43L22, the chip address field, which is the first byte sent to the CS43L22, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS43L22 after each input byte is read and is input to the CS43L22 from the microcontroller after each transmitted byte.

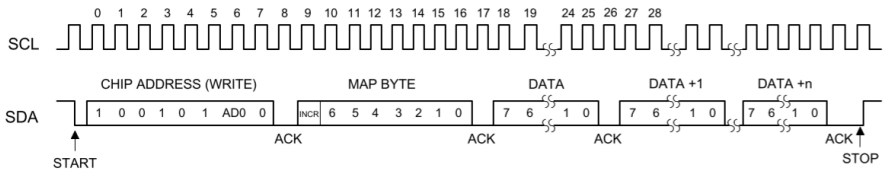

Figure 16. Control Port Timing, I²C Write

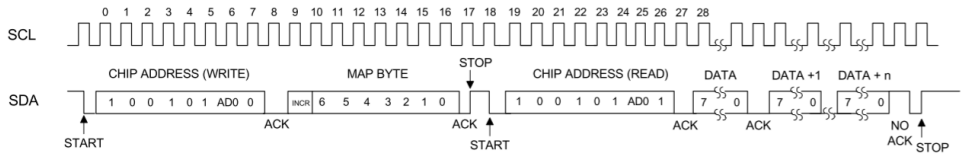

Figure 17. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 17, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Important register

7.15 Beep Frequency & On Time (Address 1Ch)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

7.15.1 Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	**Frequency** *(Fs = 12, 24, 48 or 96 kHz)*	**Pitch**
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	"Beep Generator" on page 22	

7.15.2 Beep On Time

Sets the on duration of the beep signal.

ONTIME[3:0]	**On Time** *(Fs = 12, 24, 48 or 96 kHz)*
0000	~86 ms
0001	~430 ms
0010	~780 ms
0011	~1.20 s
0100	~1.50 s
0101	~1.80 s
0110	~2.20 s
0111	~2.50 s
1000	~2.80 s
1001	~3.20 s
1010	~3.50 s
1011	~3.80 s
1100	~4.20 s
1101	~4.50 s
1110	~4.80 s
1111	~5.20 s
Application:	"Beep Generator" on page 22

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep on time will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode.

7.16 Beep Volume & Off Time (Address 1Dh)

7	6	5	4	3	2	1	0
OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0

7.16.1 Beep Off Time

Sets the off duration of the beep signal.

OFFTIME[2:0]	**Off Time** *(Fs = 48 or 96 kHz)*
000	~1.23 s
001	~2.58 s
010	~3.90 s
011	~5.20 s
100	~6.60 s
101	~8.05 s
110	~9.35 s
111	~10.80 s
Application:	"Beep Generator" on page 22

7.16.2 Beep Volume

Sets the volume of the beep signal.

BEEPVOL[4:0]	Gain
00110	+6.0 dB
…	…
00000	-6 dB
11111	-8 dB
11110	-10 dB
…	…
00111	-56 dB
Step Size:	2 dB
Application:	"Beep Generator" on page 22

Note: This setting must not change when BEEP is enabled.

7.17 Beep & Tone Configuration (Address 1Eh)

7	6	5	4	3	2	1	0
BEEP1	BEEP0	BEEPMIXDIS	TREBCF1	TREBCF0	BASSCF1	BASSCF0	TCEN

7.17.1 Beep Configuration

Configures a beep mixed with the HP/Line and SPK output.

BEEP[1:0]	Beep Occurrence
00	Off
01	Single
10	Multiple
11	Continuous
Application:	"Beep Generator" on page 22

Notes:

1. When used in analog pass through mode, the output alternates between the signal from the Passthrough Amplifier and the beep signal. The beep signal does not mix with the analog signal from the Passthrough Amplifier.
2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration.

7.17.2 Beep Mix Disable

Configures how the beep mixes with the serial data input.

BEEPMIXDIS	Beep Output to HP/Line and Speaker
0	Mix Enabled; The beep signal mixes with the digital signal from the serial data input.
1	Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input.
Application:	"Beep Generator" on page 22

Note: This setting must not change when BEEP is enabled.