FPGA to FPGA protocol

The FPGA communication protocol is as follows. First, the transmitter drives the “send” signal high for one clock cycle, and waits for receiver’s acknowledgement, which is also one clock cycle. Then, the transmitter prepares its data and drives the “send” high for one clock cycle again when it’s ready, and waits for receiver’s acknowledgement. Repeat this process until eight bits are sent. After that, the transmitter drives the data signal as the parity bit and the finish signal high. The receiver then checks if eight bits are actually received, and the parity bit is correct, then drives the “acknowledge” signal high for one clock cycle. If error occurs, the receiver drives the “error” signal high instead, in which case the transmitter must re-send the data from the start.

FPGA to FPGA receiver

(Block diagram here)

(ASM chart here)