UART Transmitter

(Block diagram here)

(ASM chart here)

SD card reader

(Block diagram here)

(ASM chart here)

FPGA to FPGA protocol

The data will be sent one byte for each start signal. After a byte is sent, the finish signal must be driven high before transmitting the next byte. The transmission uses four wires, which will be connected directly through FPGA’s I/O pins.

* Send: A signal from the transmitter to the receiver to tell that a data is being sent.
* Acknowledge: A signal from the receiver to the transmitter to tell that a data is received.
* Finish: A signal from the transmitter to the receiver to end the current byte.
* Data: The data line. Data will be sent serially, one bit at a time, with least significant bit first.

First, the transmitter drives the “send” signal high for one clock cycle, and waits for receiver’s acknowledgement, which is also one clock cycle. Then, the transmitter prepares its data and drives the “send” high for one clock cycle again when it’s ready, and waits for receiver’s acknowledgement. Repeat this process until eight bits are sent. After that, the transmitter drives the finish signal high. The receiver then drives the “acknowledge” signal high for one clock cycle.

FPGA to FPGA receiver

(Block diagram here)

(ASM chart here)