Datasheet

1. LIS302DL : Accelerometer

Description of what is LIS302DL and how to communicate with it :

Description

The LIS302DL is an ultra compact low-power three axes linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I^2C/SPI serial interface.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface is manufactured using a CMOS process that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

Serial interface and pin description :

Digital interfaces

The registers embedded inside the LIS302DL may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, CS line must be tied high (i.e connected to Vdd_IO).

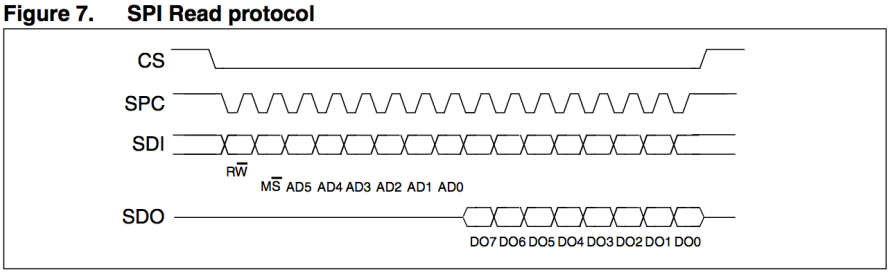
Table 8. Serial interface pin description

PIN name	PIN description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO	SPI Serial Data Output (SDO)

SPI read information :

SPI Read

Figure 7. SPI Read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

bit 16-... : data DO(...-8). Further data in multiple byte reading.

Useful Registers :

CTRL_REG1 (20h)

Table 18. CTRL_REG1 (20h) register

DR	PD	FS	STP	STM	Zen	Yen	Xen

Table 19. CTRL_REG1 (20h) register description

DR	Data rate selection. Default value: 0 (0: 100 Hz output data rate; 1: 400 Hz output data rate)
PD	Power Down Control. Default value: 0 (0: power down mode; 1: active mode)
FS	Full Scale selection. Default value: 0 (refer to *Table 3* for typical full scale value)
STP, STM	Self Test Enable. Default value: 0 (0: normal mode; 1: self test P, M enabled)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

Output registers's address and information of each axis :

OUT_X (29h)

Table 28. OUT_X (29h) register

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

X axis output data.

OUT_Y (2Bh)

Table 29. OUT_Y (2Bh) register description

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

Y axis output data.

OUT_Z (2Dh)

Table 30. OUT_Z (2Dh) register

ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

Z axis output data.

2. MP45DT02 : Microphone

Description of MP45DT02 :

The MP45DT02 is a compact, low-power, top-port, omnidirectional, digital MEMS microphone. The MP45DT02 is built with a sensing element and an IC interface with stereo capability.

The sensing element, capable of detecting acoustic waves, is manufactured using a

Pin description and functionality :

Figure 1. Pin connections

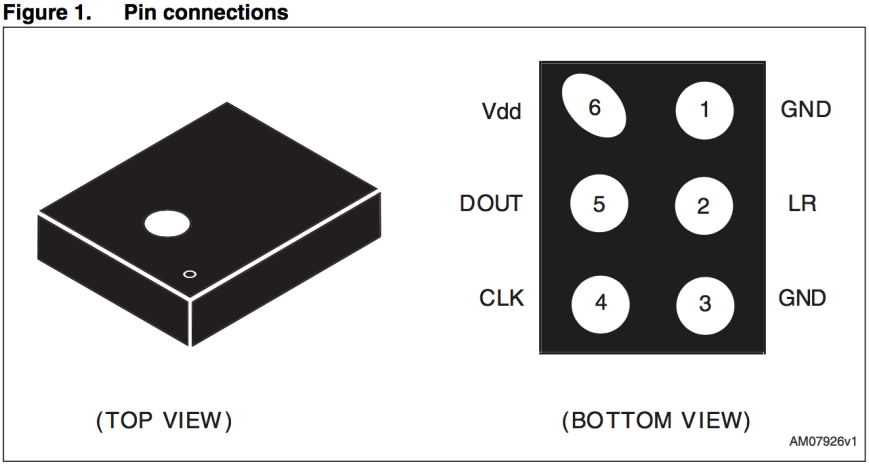


Table 2. Pin description

Pin #	Pin name	Function
1	GND	0 V supply
2	LR	Left/right channel selection; MIC1 LR is connected to GND or Vdd and MIC2 LR is connected to Vdd or GND (see *Figure 5*)
3	GND	0 V supply
4	CLK	Synchronization input clock
5	DOUT	Left/right PDM data output
6	Vdd	Power supply

L/R channel selection

The L/R digital pad lets the user select the DOUT signal pattern as explained in *Table 8*. The L/R pin must be connected to Vdd or GND.

Table 8. L/R channel selection

L/R	CLK low	CLK high
GND	Data valid	High impedence
Vdd	High impedence	Data valid

3. CS43L22 : Stereo DAC w/Headphone & Speaker Amps

Initialization :

Initialization

The CS43L22 enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in the "Register Description" on page 37.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable.
2. Bring $\overline{\text{RESET}}$ high.
3. The default state of the "Power Ctl. 1" register (0x02) is 0x01. Load the desired register settings while keeping the "Power Ctl 1" register set to 0x01.
4. Load the required initialization settings listed in Section 4.11.
5. Apply MCLK at the appropriate frequency, as discussed in Section 4.6. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the "Power Ctl 1" register (0x02) to 0x9E.
7. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

Required Initialization Settings

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0x80 to register 0x47.
3. Write '1'b to bit 7 in register 0x32.
4. Write '0'b to bit 7 in register 0x32.
5. Write 0x00 to register 0x00.

Useful registers :

Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	**Frequency** *(Fs = 12, 24, 48 or 96 kHz)*	**Pitch**
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	"Beep Generator" on page 22	

Beep On Time

Sets the on duration of the beep signal.

ONTIME[3:0]	**On Time** *(Fs = 12, 24, 48 or 96 kHz)*
0000	~86 ms
0001	~430 ms
0010	~780 ms
0011	~1.20 s
0100	~1.50 s
0101	~1.80 s
0110	~2.20 s
0111	~2.50 s
1000	~2.80 s
1001	~3.20 s
1010	~3.50 s
1011	~3.80 s
1100	~4.20 s
1101	~4.50 s
1110	~4.80 s
1111	~5.20 s
Application:	"Beep Generator" on page 22