**LIS302DL 3-axis accelerometer**

The LIS302DL is an ultra compact low-power three axes linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I2C/SPI serial interface.

**SPI bus interface**The LIS302DL SPI is a bus slave. The SPI allows to write and read the registers of the device.

**SPI Read**

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The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

**bit 0:** READ bit. The value is 1.

**bit 1:** MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

**SPI Write**

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The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

**bit 0:** WRITE bit. The value is 0.

**bit 1:** MS bit. When 0 do not increment address, when 1 increment address in multiple writing.

**bit 2 -7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

**Register address map** (**Only used register**)

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Type** | **Register address (HEX)** | **Default** |
| Ctrl\_Reg1 | rw | 20 | 00001111 |
| OutX | r | 29 | output |
| OutY | r | 2B | output |
| OutZ | r | 2D | output |

**Register description**   
 **CTRL\_REG1 (20h)**  
**register**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| DR | PD | FS | STP | STM | Zen | Yen | Xen |

**Register description**

|  |  |
| --- | --- |
| DR | Data rate selection. Default value: 0  (0: 100 Hz output data rate; 1: 400 Hz output data rate) |
| PD | Power Down Control. Default value: 0  (0: power down mode; 1: active mode) |
| FS | Full Scale selection. Default value: 0  (refer to *Table 3* for typical full scale value) |
| STP, STM | Self Test Enable. Default value: 0  (0: normal mode; 1: self test P, M enabled) |
| Zen | Z axis enable. Default value: 1  (0: Z axis disabled; 1: Z axis enabled) |
| Yen | Y axis enable. Default value: 1  (0: Y axis disabled; 1: Y axis enabled) |
| Xen | X axis enable. Default value: 1  (0: X axis disabled; 1: X axis enabled) |

**OUT\_X (29h) register :** x asis output data

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |

**OUT\_Y (2Bh) register :** y asis output data

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |

**OUT\_Z (2Dh) register :** z asis output data

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| ZD7 | ZD6 | ZD5 | ZD4 | ZD3 | ZD2 | ZD1 | ZD0 |

**MP45DT02: digital microphone**

The MP45DT02 is a compact, low-power, topport, omnidirectional, digital MEMS microphone. The MP45DT02 is built with a sensing element and an IC interface with stereo capability.



The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process to produce audio sensors.   
 The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit able to provide a digital signal externally in PDM format.

**Timing Waveform**

**CS43L22: audio DAC, speaker driver**

The CS43L22 is a highly integrated, low power stereo DAC with headphone and Class D speaker amplifiers. The CS43L22 offers many features suitable for low power, portable system applications

The DAC output path includes a digital signal processing engine with various fixed function controls. Tone Control provides bass and treble adjustment of four selectable corner frequencies. Digital Volume controls may be configured to change on soft ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC also includes de-emphasis, limiting functions and a BEEP generator delivering tones selectable across a range of two full octaves

**Initialization**

The CS43L22 enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down state until the **RESET** pin is brought high.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

**Recommended Power-Up Sequence**

1. Hold **RESET** low until the power supplies are stable.

2. Bring **RESET** high.

3. The default state of the “Power Ctl. 1” register (0x02) is 0x01. Load the desired register settings while keeping the “Power Ctl 1” register set to 0x01.

4. Load the required initialization settings.

5. Apply MCLK at the appropriate frequency. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.

6. Set the “Power Ctl 1” register (0x02) to 0x9E.

7. Bring **RESET** low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

**Recommended Power-Down Sequence**

To minimize audible pops when turning off or placing the DAC in standby,

1. Mute the DAC’s and PWM outputs.

2. Disable soft ramp and zero cross volume transitions.

3. Set the “Power Ctl 1” register (0x02) to 0x9F.

4. Wait at least 100 μs. The device will be fully powered down after this 100 μs delay. Prior to the removal of the master clock (MCLK), this delay of at least 100 μs must be implemented after step 3 to avoid premature disruption of the DAC’s power down sequence. A disruption in the device’s power down sequence (i.e. removing the MCLK signal before this 100 μs delay) has consequences on both the headphone and PWM speaker amplifiers: The charge pump may stop abruptly, causing the headphone amplifiers to drive the outputs up to the +VHP supply. Also, the last state of each ‘+’ and ‘-’ PWM output terminal before the premature removal of MCLK could randomly be held at either VP or AGND. When this event occurs, it is possible for each PWM terminal to output opposing potentials, creating a DC source into the speaker voice coil. The disruption of the device’s power down sequence may also cause clicks and pops on the output of the DAC’s as the modulator holds the last output level before the MCLK signal was removed.

5. MCLK may be removed at this time.

6. To achieve the lowest operating quiescent current, bring **RESET** low. All control port registers will bereset to their default state.

**Required Initialization Settings**

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.

2. Write 0x80 to register 0x47.

3. Write ‘1’b to bit 7 in register 0x32.

4. Write ‘0’b to bit 7 in register 0x32.

5. Write 0x00 to register 0x00.

**I²C Control**

****

**REGISTER DESCRIPTION**

**Power Control 1 (Address 02h)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| PDN7 | PDN6 | PDN5 | PDN4 | PDN3 | PDN2 | PDN1 | PDN0 |

|  |  |
| --- | --- |
| **PDN[7:0]** | **Status** |
| 0000 0001 | Powered Down - same as setting 1001 1111 |
| 1001 1110 | Powered Up |
| 1001 1111 | Powered Down - same as setting 0000 0001 |

**Note:** All states of PDN[7:0] not shown in the table are reserved.

**Interface Control 1 (Address 06h)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| M/S | INV\_SCLK | Reserved | DSP | DACDIF1 | DACDIF0 | AWL1 | AWL0 |

**Master/Slave Mode**

|  |  |
| --- | --- |
| **M/S** | **Serial Port Clocks** |
| 0 | Slave (input ONLY) |
| 1 | Master (output ONLY) |

**SCLK Polarity**

|  |  |
| --- | --- |
| **INV\_SCLK** | **SCLK Polarity** |
| 0 | Not Inverted |
| 1 | Inverted |

**DSP Mode**

|  |  |
| --- | --- |
| **DSP** | **DSP Mode** |
| 0 | Disabled |
| 1 | Enabled |

**Notes:**1. Select the audio word length using the AWL[1:0] bits 2. The interface format for the DAC must be set to “Left-Justified” when DSP Mode is enabled.

**DAC Interface Format**

|  |  |
| --- | --- |
| **DACDIF[1:0]** | **DAC Interface Format** |
| 00 | Left Justified, up to 24-bit data |
| 01 | I²S, up to 24-bit data |
| 10 | Right Justified |
| 11 | Reserved |

**Note:** Select the audio word length for Right Justified using the AWL[1:0] bits

**Audio Word Length**

|  |  |  |
| --- | --- | --- |
| **AWL[1:0]** | **Audio Word Length** | |
| **DSP Mode** | **Right Justified** |
| 00 | 32-bit data | 24-bit data |
| 01 | 24-bit data | 20-bit data |
| 10 | 20-bit data | 18-bit data |
| **AWL[1:0]** | **Audio Word Length** | |
| **DSP Mode** | **Right Justified** |
| 11 | 16-bit data | 16-bit data |

**Beep Frequency & On Time (Address 1Ch)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| FREQ3 | FREQ2 | FREQ1 | FREQ0 | ONTIME3 | ONTIME2 | ONTIME1 | ONTIME0 |

**Beep Frequency**

|  |  |
| --- | --- |
| **FREQ[3:0]** | **Pitch** |
| 0000 | C4 |
| 0001 | C5 |
| 0010 | D5 |
| 0011 | E5 |
| 0100 | F5 |
| 0101 | G5 |
| 0110 | A5 |
| 0111 | B5 |
| 1000 | C6 |
| 1001 | D6 |
| 1010 | E6 |
| 1011 | F6 |
| 1100 | G6 |
| 1101 | A6 |
| 1110 | B6 |
| 1111 | C7 |

**Notes:**

1. This setting must not change when BEEP is enabled.

2. Beep frequency will scale directly with sample rate, Fs, but is fixed at the nominal Fs within each speed mode.

**Beep On Time**

|  |  |
| --- | --- |
| **ONTIME[3:0]** | **On Time (Fs = 12, 24, 48 or 96 kHz)** |
| 0000 | ~86 ms |
| 0001 | ~430 ms |
| 0010 | ~780 ms |
| 0011 | ~1.20 s |
| 0100 | ~1.50 s |
| 0101 | ~1.80 s |
| 0110 | ~2.20 s |
| 0111 | ~2.50 s |
| 1000 | ~2.80 s |
| 1001 | ~3.20 s |
| 1010 | ~3.50 s |
| 1011 | ~3.80 s |
| 1100 | ~4.20 s |
| 1101 | ~4.50 s |
| 1110 | ~4.80 s |
| 1111 | ~5.20 s |

**Notes:**

1. This setting must not change when BEEP is enabled.

2. Beep on time will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode.

**Beep & Tone Configuration (Address 1Eh)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| BEEP1 | BEEP0 | BEEPMIXDIS | TREBCP1 | TREBCF0 | BASSCF1 | BASSCF0 | TCEN |

**Beep Configuration**

|  |  |
| --- | --- |
| **BEEP[1:0]** | **Beep Occurrence** |
| 00 | Off |
| 01 | Single |
| 10 | Multiple |
| 11 | Continuous |

**Notes:**

1. When used in analog pass through mode, the output alternates between the signal from the Passthrough Amplifier and the beep signal. The beep signal does not mix with the analog signal from

the Passthrough Amplifier.

2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration

**Beep Mix Disable**

|  |  |
| --- | --- |
| **BEEPMIXDIS** | **Beep Output to HP/Line and Speaker** |
| 0 | Mix Enabled; The beep signal mixes with the digital signal from the serial data input. |
| 1 | Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input. |

**Note:** This setting must not change when BEEP is enabled.

**Treble Corner Frequency**

|  |  |
| --- | --- |
| **TREBCF[1:0]** | **Treble Corner Frequency Setting** |
| 00 | 5 kHz |
| 01 | 7 kHz |
| 10 | 10 kHz |
| 11 | 15 kHz |

**Bass Corner Frequency**

|  |  |
| --- | --- |
| **BASSCF[1:0]** | **Bass Corner Frequency Setting** |
| 00 | 50 kHz |
| 01 | 100 kHz |
| 10 | 200 kHz |
| 11 | 250 kHz |

**Tone Control Enable**

|  |  |
| --- | --- |
| **TCEN** | **Bass and Treble Control** |
| 0 | Disabled |
| 1 | Enabled |