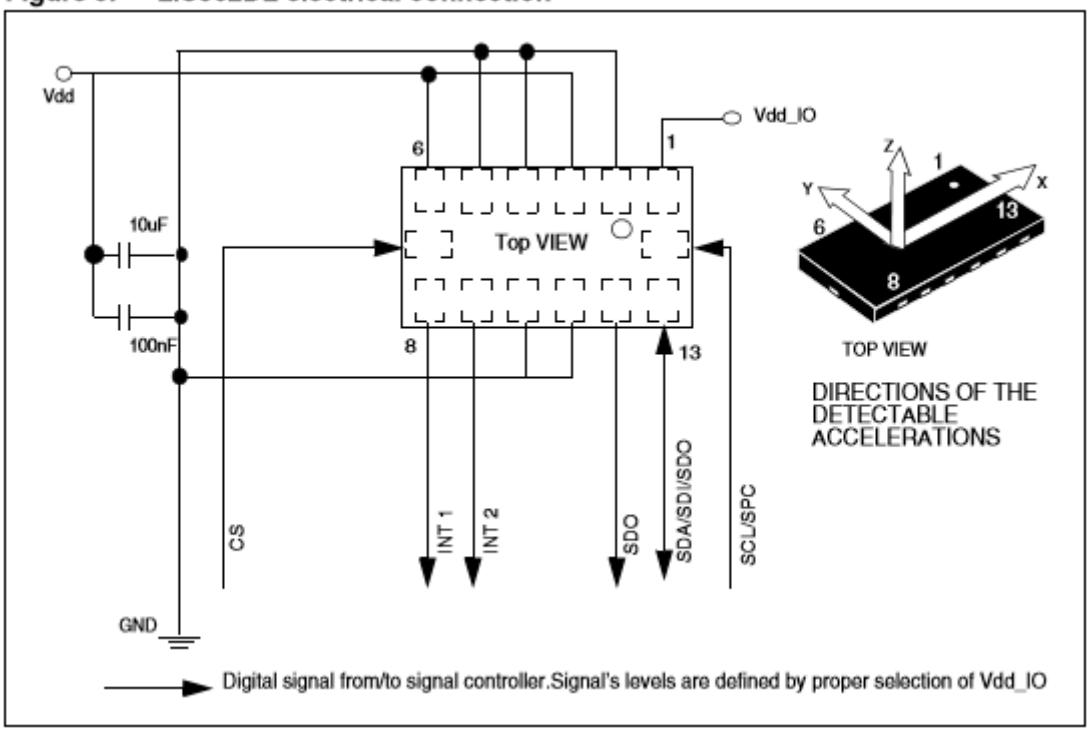
IC DATASHEET

LIS302DL : 3-axis accelerometer

- The LIS302D is an ultra-compact low-power 3-axis linear accelerometer.
- The registers inside the LIS302DL may be accessed through SPI serial interfaces.
- The LIS302DL can be configured in full scales of +-2g/+-8g and it is capable of measuring acceleration with an output rate of 100Hz to 400Hz.

Figure 5. LIS302DL electrical connection



2.1 Mechanical characteristics

Table 3. Mechanical characteristics(1)
(All the parameters are specified @ Vdd=2.5 V, T = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range(3)	FS bit set to 0	±2.0	±2.3		g
		FS bit set to 1	±8.0	±9.2		

SPI

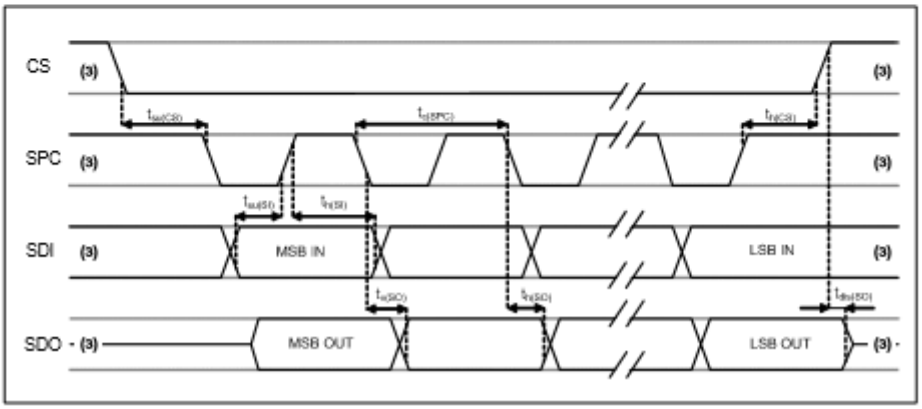
2.3.1 SPI - Serial Peripheral Interface

Subject to general operating conditions for Vdd and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

Figure 3. SPI slave timing diagram (2)



Write ------- RW := 0 MS := 1

Read ------- RW := 1 MS := 1

REGISTER USED

CTRL_REG1 (20h)

Table 18. CTRL_REG1 (20h) register

DR	PD	FS	STP	STM	Zen	Yen	Xen

Table 19. CTRL_REG1 (20h) register description

DR	Data rate selection. Default value: 0 (0: 100 Hz output data rate; 1: 400 Hz output data rate)
PD	Power Down Control. Default value: 0 (0: power down mode; 1: active mode)
FS	Full Scale selection. Default value: 0 (refer to *Table 3* for typical full scale value)
STP, STM	Self Test Enable. Default value: 0 (0: normal mode; 1: self test P, M enabled)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

OUT_X (29h)

Table 28. OUT_X (29h) register

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

X axis output data.

OUT_Y (2Bh)

Table 29. OUT_Y (2Bh) register description

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

Y axis output data.

OUT_Z (2Dh)

Table 30. OUT_Z (2Dh) register

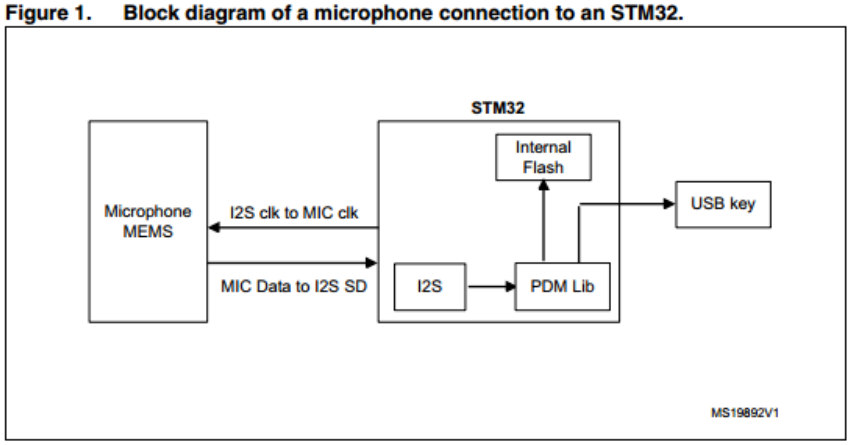
ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

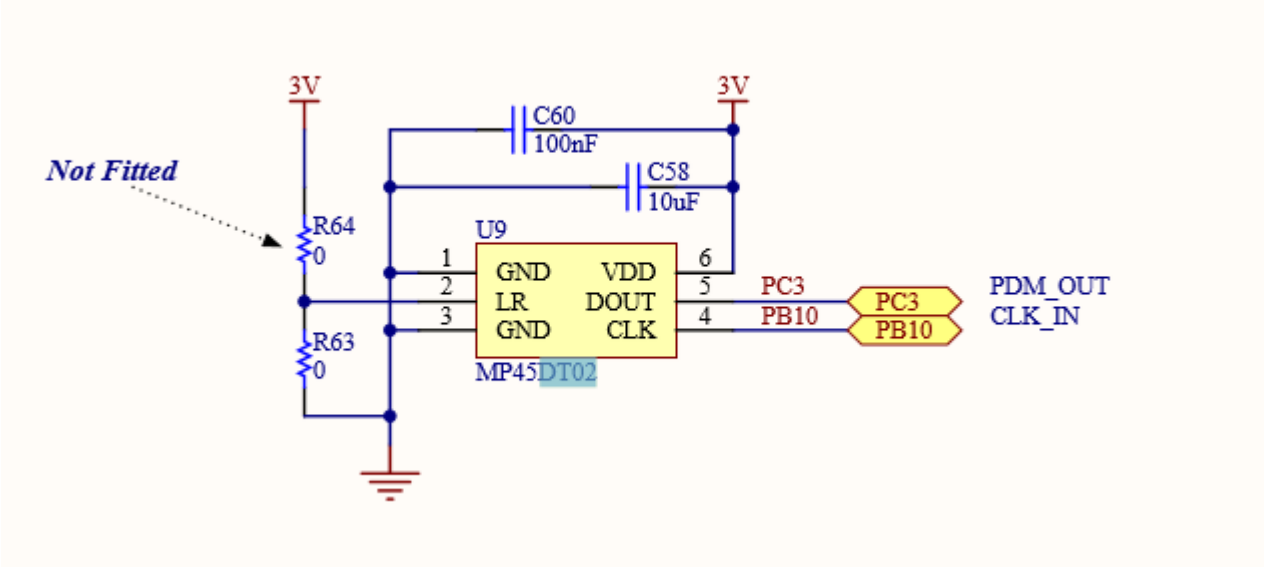
Z axis output data.

MP45DT02 : digital microphone

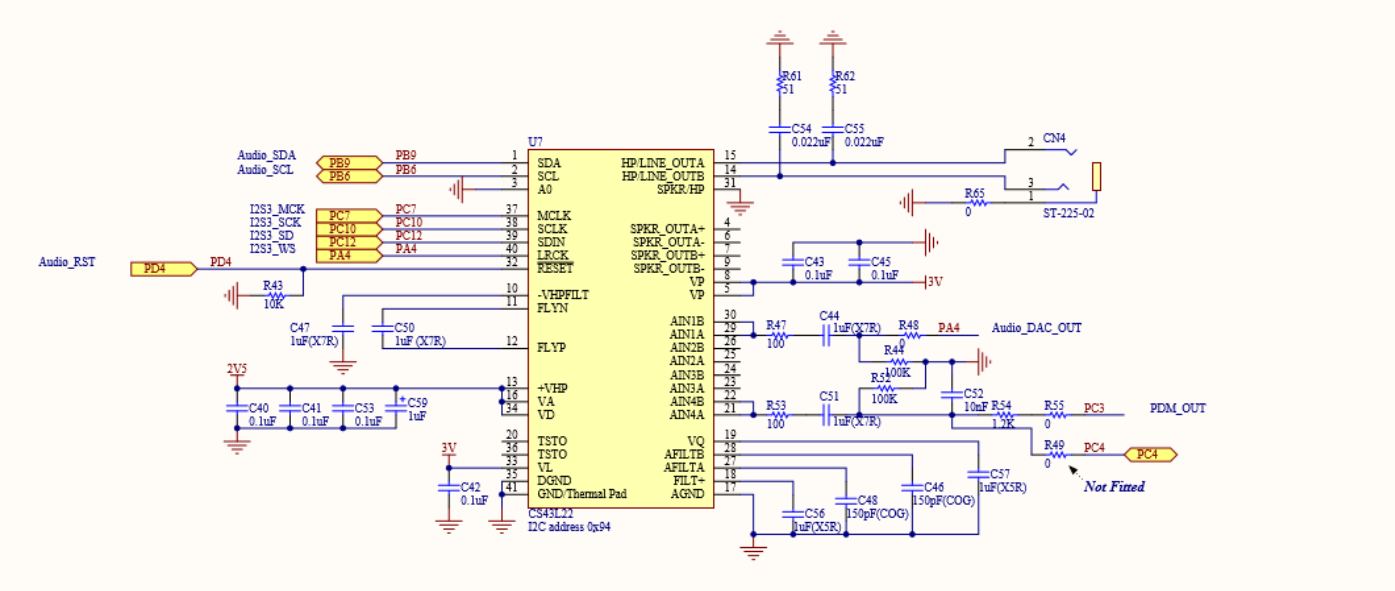
- Using PDM protocol [PDM : Pulse Density Modulation]
- Convert analog to digital

Figure 1. Block diagram of a microphone connection to an STM32.





CS43L22 : audio DAC, speaker driver



- The STM32F4 uses an audio DAC (CS43L22) to output sounds through the audio mini jack connector.
- Controlled audio by using I2C interface.

Initial setting

Required Initialization Settings

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0x80 to register 0x47.
3. Write '1'b to bit 7 in register 0x32.
4. Write '0'b to bit 7 in register 0x32.
5. Write 0x00 to register 0x00.

REGISTER USED

7.15 Beep Frequency & On Time (Address 1Ch)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

7.15.1 Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	**Frequency** *(Fs = 12, 24, 48 or 96 kHz)*	**Pitch**
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	"Beep Generator" on page 22	

7.15.2 Beep On Time

Sets the on duration of the beep signal.

ONTIME[3:0]	**On Time** *(Fs = 12, 24, 48 or 96 kHz)*
0000	~86 ms
0001	~430 ms
0010	~780 ms
0011	~1.20 s
0100	~1.50 s
0101	~1.80 s
0110	~2.20 s
0111	~2.50 s
1000	~2.80 s
1001	~3.20 s
1010	~3.50 s
1011	~3.80 s
1100	~4.20 s
1101	~4.50 s
1110	~4.80 s
1111	~5.20 s
Application:	"Beep Generator" on page 22

7.17 Beep & Tone Configuration (Address 1Eh)

7	6	5	4	3	2	1	0
BEEP1	BEEP0	BEEPMIXDIS	TREBCF1	TREBCF0	BASSCF1	BASSCF0	TCEN

7.17.1 Beep Configuration

Configures a beep mixed with the HP/Line and SPK output.

BEEP[1:0]	Beep Occurrence
00	Off
01	Single
10	Multiple
11	Continuous
Application:	"Beep Generator" on page 22

Notes:

1. When used in analog pass through mode, the output alternates between the signal from the Passthrough Amplifier and the beep signal. The beep signal does not mix with the analog signal from the Passthrough Amplifier.
2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration.

7.17.2 Beep Mix Disable

Configures how the beep mixes with the serial data input.

BEEPMIXDIS	Beep Output to HP/Line and Speaker
0	Mix Enabled; The beep signal mixes with the digital signal from the serial data input.
1	Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input.
Application:	"Beep Generator" on page 22

Note: This setting must not change when BEEP is enabled.

7.17.3 Treble Corner Frequency

Sets the corner frequency (-3 dB point) for the treble shelving filter.

TREBCF[1:0]	Treble Corner Frequency Setting
00	5 kHz
01	7 kHz
10	10 kHz
11	15 kHz

7.17.4 Bass Corner Frequency

Sets the corner frequency (-3 dB point) for the bass shelving filter.

BASSCF[1:0]	Bass Corner Frequency Setting
00	50 Hz
01	100 Hz
10	200 Hz
11	250 Hz

7.17.5 Tone Control Enable

Configures the treble and bass activation.

TCEN	Bass and Treble Control
0	Disabled
1	Enabled
Application:	"Beep Generator" on page 22