College of Charleston
Computer Science Department

CSCI 350 Digital Logic and Computer Organization
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Assignment 5 **Due Friday October 14, 2011**
Fall, 2011

Course Outcomes Being Addressed

7. Understand basic MSI components such as adders, decoders, multiplexers, etc. and use them in more complex circuits.
8. Use of LSI components (e.g. PLA or ROM) in combinational circuit design.

Assignment Problems

1. a. Use the model of the 12-input, 6-output programmable logic array (PLA) to design a 4-input, 3-output PLA. Here, however, rather than draw all of the little fuses we will just use straight lines and cross-out any lines we do not want to use.

   b. Use your PLA from part a, to implement a full adder. Use C_{out} and S as labels for the carry-out and sum output lines respectively.

2. In class I handed out a page with a diagram of a 4 × 4 ROM. Use this to implement a full added. Once again use C_{out} and S as labels for the carry-out and sum output lines respectively (if you don't have this page, it will be posted on OAKS along with this assignment).

The purpose of the rest part of the assignment is to familiarize you better with the notion of propagation delays for signals in a circuit and for you to see some of the tradeoffs that arise in circuit design because of attention to propagation delay. As I mentioned in class at various times,, the *propagation delay* for a gate is the time it takes for a gate to (possibly) change its output value following a change in its input values.

3. Consider the full adder circuit in your textbook on page 154 (which we also designed in class).
   a. Assuming each of the logic gates used in this circuit has a propagation delay of 4 ns (nanoseconds), what are the delays for generating the sum and carry-out for this full adder?
   b. Using the "ripple adder" approach that we discussed in class to implement a 4-bit adder from four 1-bit adder , calculate the propagation delays for the sum and carry-out for this 4-bit adder.

4. In this exercise we are going to show how we can speed up the propagation delays for ripple adders.
   a. Your textbook describes an alternate type of adder known as a ***carry-select adder*** on page 155. Show how you could implement a 2-bit adder from 1-bit adders using this approach and calculate the propagation times for the sum and final carry-out.
   b. Now use carry-select to design a 4-bit adder from 2 bit adders that were themselves designed by carry-select. Calculate the propagation times for the sum and final carry-out for this 4-bit adder.

5. The approach described in problem 13 on page 227 of your textbook implements what is known as a carry-look-ahead adder. Use carry-look-ahead to implement a 4-bit adder from four 1-bit adders and calculate the propagation times for the sum and final carry-out for this 4-bit adder.