College of Charleston
Computer Science Department

CSCI 350 Digital Logic and Computer Organization
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Digital Design Laboratory 1
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1. Use a minimized SOP expression to implement the function $f(x,y,z)=\Sigma(0,2,4,6,7)$. Use logic switches 2,1, and 0 to generate values for x, y, and z respectively and use LED0 to show the function's value. You may only use inverters, AND gates, and an OR gate for this circuit.

2. Redo problem 1, but this time use only NAND gates. Note that chip 7410 contains 3-input NAND gates, while 7420 contains 4-input NAND gates. You cannot use any of the inverters on the 7404 chips.

3. Redo problem 1, but this time use only inverters (if necessary) and the 8-1 multiplexer of chip 74151.

4. Redo problem 1, but this time use only one of the 4-1 multiplexers on the 74153 chip and any inverters you may need for the input signals.

5. Implement the full adder we designed in class using AND gates, OR gates, XOR gates (7486), and inverters as necessary.

6. Implement the full adder we designed in class using the two 4-1 multiplexers on the 74153 chip. Note, these multiplexers are not completely independent as they share select lines.