Dependence of V_{TH} Stability on Gate-Bias Under Reverse-Bias Stress in E-mode GaN MIS-FET

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***Abstract*— In this letter, we investigated the threshold voltage V_{TH} stability under reverse-bias step-stress in the E-mode LPCVD-SiN_x/PECVD-SiN_x/GaN MIS-FET. Under the OFF-state reverse-bias stress with the same net gate-to-drain voltage (V_{GD}), the V_{TH} shift shows an obvious dependence on the negative gate bias. With a V_{GS} of 0 V, the V_{TH} shift is small and recoverable, while the V_{TH} shifts are substantially larger with more negative gate bias (V_{GS} = −20 V). This larger V_{TH} shifts caused by the negative V_{GS} can be explained with a hole-induced degradation model. An important indication revealed by this model is that negative gate bias should be well confined in high-power switching applications of GaN E-mode MIS-FET for a stable V_{TH}.**

***Index Terms*— GaN, enhancement-mode, MIS-FET, reverse- bias step-stress.**

I. Introduction

GaN FIELD-EFFECT transistor (FET) with fully recessed gate structure and metal–insulator–semiconductor (MIS) gate is especially attractive for high power switching applications [1], [2]. However, the development of MIS-FET has been hindered by major concerns of gate dielectric reliability and V_{TH} stability.

The most critical reliability issue of the gate dielectric is time-dependent dielectric breakdown (TDDB). It is difficult to achieve long gate operation lifetime with Al_2O_3 or SiO_2 prepared by atomic layer deposition (ALD) or plasma-enhanced chemical vapor deposition (PECVD) as the gate dielectric, due to the low deposition temperature (∼300 °C) which tends to result in low film quality with high defects density. To overcome this problem, silicon nitride (SiN_x) deposited at temperature around 800 °C by low-pressure chemical vapor deposition (LPCVD) has been under intense investigation as gate dielectric in MIS-FET, and has shown promising performance in terms of low gate leakage, large gate swing and long TDDB lifetime [3], [4].

To take full advantage of the low-loss benefit of GaN power switches, large positive gate bias V_{GS} is usually deployed for a large gate overdrive ($V_{GS} - V_{TH}$) to fully turn-on the E-mode MIS-FETs. Meanwhile, under negative gate-bias stress, electron de-trapping may result in a negative V_{TH} shift [5] and aggravate false turn-on of GaN MIS-FETs. Thus, both positive/negative bias temperature instability (PBTI/NBTI) are important stability/reliability issues for GaN MIS-FETs [6]–[8], and these issues usually originate from the interface/border trap states. Small BTI was obtained in the LPCVD-SiN_x MIS-FET, benefiting from the reliable gate dielectric with reduced interface/border trap density [4].

Although the BTI and TDDB issues have been intensively investigated, the V_{TH} stability under OFF-state high drain-bias stress with a large negative gate-to-drain voltage V_{GD} (defined as the reverse-bias in this work) is still rarely studied in GaN MIS-FET. Under reverse-bias stress, the potential distribution near the gate edge is similar to that under NBTI stress because of a relatively long gate length [9], but the depletion region is much further extended toward the drain terminal as a result of the large drain bias. Even at the OFF-state, the non-zero leakage current suggests that hot electrons can be generated (although in small quantity) in the gate-to-drain region and induce impact ionization that results in electron-hole generation. The holes could then move toward the gate and source under the influence of electric field. As there are no electrons in the OFF-state channel, holes could survive and accumulate over a long period of time in the channel [10]. The impact of these holes under the gate of GaN MIS-FETs is of great importance to the device stability and reliability.

In this work, we investigated the V_{TH} stability of fully-recessed E-mode GaN MIS-FET under reverse-bias step-stress with different gate bias. Larger positive V_{TH} shifts were observed with a more negative gate bias under stress even when the same V_{GD} is applied. Stretch-out of the turn-on behavior in the transfer curves also occurs during stress with a more negative gate bias. A hole-induced degradation model is proposed to explain the degradation accelerated by the negative gate bias under reverse-bias stress.

II. Reverse-Bias Step-Stress Measurements

The E-mode MIS-FETs with dimensions of $L_{GS}/L_G/L_{GD}$ = 2/1.5/15 μm studied in this work are fabricated with the same process as described in [4]. Fig. 1 (a) shows the schematic device structure. A thin PECVD-SiN_x (∼2 nm) interlayer is used to protect the exposed GaN surface after gate recess etching from degradation (e.g. decomposition or chemical reaction) during the high-temperature LPCVD process [4]. This

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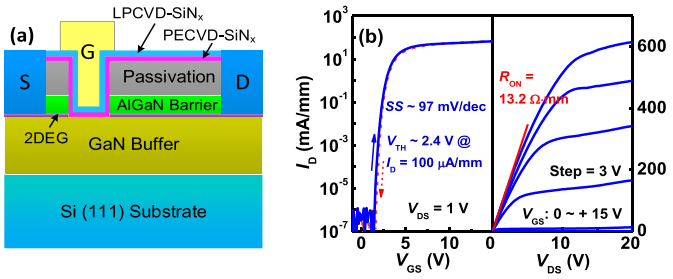

Fig. 1. (a) Schematic cross-sectional view of the LPCVD-SiN_x MIS-FET with PECVD-SiN_x interface protection layer and fully recessed gate structure. (b) Transfer and output characteristics of the LPCVD-SiN_x MIS-FET.

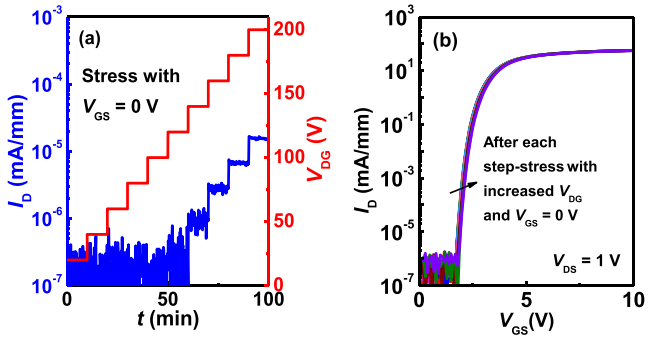

Fig. 2. (a) Waveform of drain bias V_{DS} and drain leakage I_D during the reverse-bias step-stress with V_{GS} of 0 V. (b) Monitored transfer characteristics during the step-stress.

interface protection layer is proven to be necessary to reduce the interface/border trap density and improve the V_{TH} stability. The E-mode MIS-FET has a positive V_{TH} of 2.4 V and on-resistance R_{ON} of 13.2 Ω· mm (Fig. 1 (b)). These devices are without field-plates and subjected to harsh electrical stress in terms of the electric field strength near the gate edge.

The reverse-bias step-stress was conducted with the gate biased at 0 V and the drain-to-gate voltage V_{DG} sweeping from 20 V to 200 V with a step of 20 V. Each step-stress lasts 10 minutes (Fig. 2 (a)). During the step-stress, threshold voltage V_{TH} was monitored by repeatedly interrupting the stress experiment for the execution of I_D-V_{GS} measurement. The transfer curves were measured with V_{DS} = 1 V and a sweeping rate of 0.7 V/s (Fig. 2 (b)). The threshold voltage V_{TH} shows a small positive shift (ΔV_{TH} < 0.14 V) and the subthreshold swing (*SS*∼97 mV/dec) is well maintained. Both gate injection from the gate electrode to the gate dielectric [11] and Zener trapping [7] could result in positive V_{TH} shifts. The small ΔV_{TH} indicates: 1) weak electron injection from the gate electrode benefiting from the low bulk trap density in LPCVD-SiN_x and 2) weak Zener trapping as a result of low defect density in AlGaN/GaN heterojunction. After the reverse-bias step-stress, the V_{TH} shifts can be fully eliminated with UV illumination (with a wavelength of 360 nm) for 5 minutes, indicating that negligible new trap states are generated during the step-stress.

Inherently, an E-mode GaN device does not require a negative gate bias to turn off. However, negative gate bias is still used in some high-power switching applications to prevent false turn-on and ensure safe operation against the voltage spike on the gate. Therefore, we also conducted the

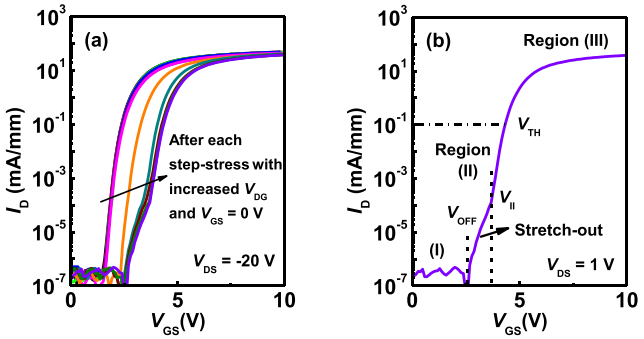

Fig. 3. (a) Transfer characteristics during the step-stress with V_{GS} = −20 V and VDG sweeping from 20 V to 200 V. (b) Stretch-out of the transfer curves.

reverse-bias step-stress with a negative gate bias V_{GS} of −20 V and the same V_{DG} from 20 V to 200 V. The V_{TH} shows aggravated positive shifts. Stretch-out of the transfer curves was also observed during the stress (Fig. 3). The positive V_{TH} shifts were much larger than that during the step-stress with V_{GS} of 0 V (Fig. 4 (a)), especially for the V_{DG} higher than 100 V. In addition, the V_{TH} shifts under step-stress with V_{GS} = −20 V cannot be recovered with UV illumination for 10 minutes. Since electron trapping due to gate injection or Zener trapping can be completely released by UV illumination, the unrecoverable V_{TH} shifts indicate that a different destructive degradation process is triggered or obviously enhanced by the negative gate bias under reverse-bias stress with high drain voltage. The source-to-gate voltage V_{SG} is also increased with more negative gate bias under the same V_{GD}, but it makes insignificant difference in the V_{TH} shifts, which can be confirmed from the negative gate-bias stress test in [4]. The V_{TH} shift after stress with V_{GS} = −30 V for 10^4 s is much smaller (ΔV_{TH} < 0.1 V) than the ΔV_{TH} under reverse-bias stress with V_{GS} = −20 V and V_{DG} > 100 V. Thus, the accelerated V_{TH} shifts by the negative gate bias is not due to the enlarged electrical stress in the gate-to-source side, but can stem from a different mechanism.

In contrast, the static and dynamic R_{ON} only increase slightly during stress, but are independent of V_{GS} used in stress (Fig. 4 (b)). Static R_{ON} and dynamic R_{ON} were measured with a constant gate over-drive (V_{GS}-V_{TH} = 8 V) to exclude the effects of V_{TH} shifts on the R_{ON}. In particular, dynamic R_{ON} was measured with V_{DS_OFF} = 200 V and the setup is the same as descripted in [12]. It indicates the negative V_{GS} induced degradation is concentrated in the gate dielectric instead of the GaN channel or the access region near the gate edge.

III. Mechanism and Discussion

The strong dependence of V_{TH} shifts on the negative gate bias can be explained with a hole-induced degradation model as shown in Fig. 4 (b). Holes can be generated by impact ionization [13] or inter-band tunneling (or Zener trapping in the presence of gap states) [7] in reverse-bias stress tests as a high electric field is formed in the gate-to-drain edge. The generated holes will flow to the source and gate following the electric potential distributions [10]. With a more negative

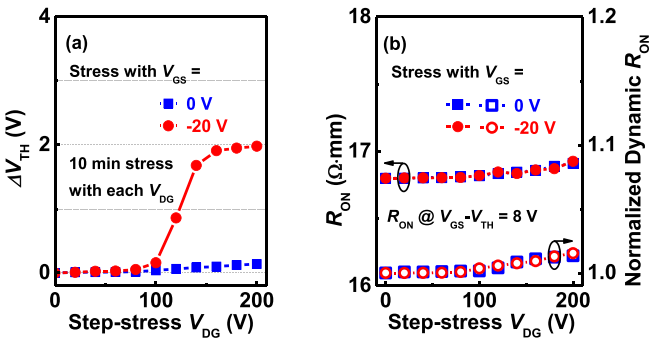

Fig. 4. (a) V_{TH} shifts and (b) R_{ON} and normalized dynamic R_{ON} degradation during the reverse-bias step-stress with $V_{GS} = 0$ V and -20 V.

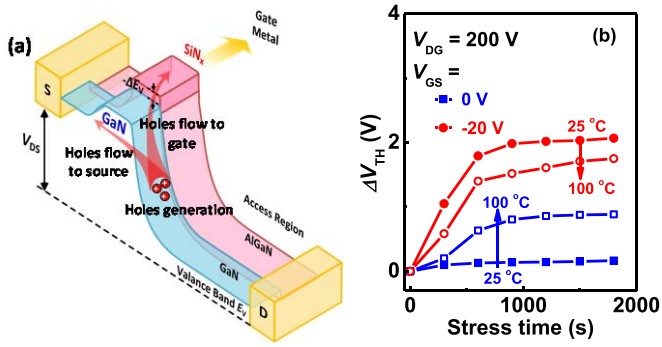

Fig. 5. (a) Schematic band-diagram laterally along channel to illustrate the model of hole-accelerated degradation. (b) V_{TH} shifts during reverse-bias stress at 25 °C and 100 °C with $V_{GS} = 0$ V and -20 V, respectively.

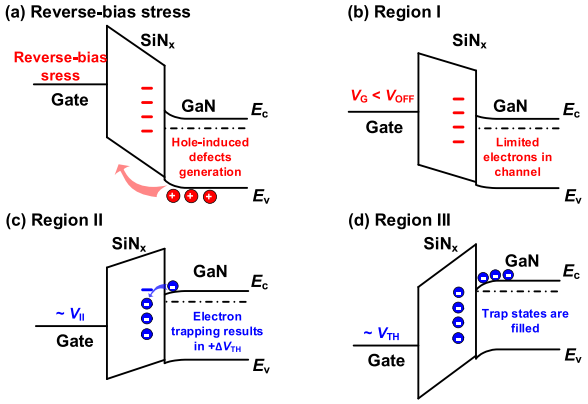

Fig. 6. Schematic band-diagram vertically along MIS-gate to illustrate hole-induced defects during stress and V_{TH} shifts during I_D-V_G measurement.

gate bias, the flow of holes to the gate side is enhanced. The holes passing through the gate dielectric could lead to the generation of new defects in the gate dielectric (Fig. 5 (a)), in a mechanism similar to what dominates the time-dependent dielectric breakdown (TDDB) of SiN_x. The new trap states generated in the reverse-bias stress would trap electrons during the transfer curve measurement, resulting in the positive shifts of V_{TH}. As the hole generation and V_{GS}-dependent hole transport could happen not only in the LPCVD-SiN_x MIS-FET, similar V_{GS}-dependence of V_{TH} shift could also be observed during the reverse-bias stress in the MIS-FET with other gate dielectrics although the hole transport mechanisms shall vary with different dielectric materials.

To reveal the temperature dependence, the reverse-bias stress (with $V_{DG} = 200$ V, $V_{GS} = 0$ V and -20 V) were conducted at 25 °C and 100 °C, respectively. As shown in Fig. 5 (b), the V_{TH} shift with $V_{GS} = 0$ V increased at higher temperature, which could be due to enlarged source-to-drain leakage that initiates the impact ionization process. On the other hand, the V_{TH} shifts with $V_{GS} = -20$ V decreased at higher temperature, indicating a weakened impact ionization.

In the step-stress tests, there is an absence of negative V_{TH} shift under a wide range of negative drain bias, suggesting weak hole-trapping in the gate dielectric [14] and low-density interface/border traps that tend to slowly emit trapped electrons to cause negative V_{TH} shifts. With the same V_{GD}, the electric fields are identical on the drain side because of the relatively long channel, indicating a similar hole-generation process on the drain side. Thus, the enhanced flow of holes to the gate under more negative V_{GS} is the main reason for the greatly increased V_{TH} shifts.

The stretch-out of transfer curve can be explained with a detailed trapping process as shown in Fig. 6. Under a reverse-bias stress with high drain bias, trap states are generated in the gate dielectric (Fig. 6 (a)). Then the device is switched from off-state stress to on-state transfer characteristic measurement. In region I ($V_G < V_{OFF}$) (Fig. 6 (b)), there are limited electrons in the channel to be captured by the trap states in the gate region. With the gate bias increasing, the trap states are pulled down to the Fermi level, electrons start to accumulate at the gate dielectric/GaN interface and fill the trap states (Fig. 6 (c)). In this gate-bias region, the V_{TH} keeps shifting positively with V_{GS} increasing, resulting the stretch-out of the transfer curves as shown in Fig. 3 (b). The trap states have both large capture and emission time constant, indicating that the newly generated traps are located inside the gate dielectric instead of at the SiN_x/GaN interface. Then after all the trap states are filled (Fig. 6 (d)), the slope of transfer curve becomes the same as that before stress. During the stress period with $V_{DG} > 160$ V, the positive shift of V_{TH} slows down. It indicates a saturating trap generation process, or the newly generated trap states are further away from the SiN_x/GaN interface and cannot be detected with transfer curves measurement. Further investigation is still needed to identify the exact cause for the slow-down of V_{TH} shift. For good gate reliability, it is suggested to limit the off-state gate bias to a narrower range in application. A less negative gate bias would result in less energetic holes in the dielectric and suppressed defect generation, which results in a better V_{TH} stability.

IV. Conclusion

Threshold voltage stability was characterized under reverse-bias step-stress with different gate bias in the E-mode LPCVD-SiN_x/PECVD-SiN_x/GaN MIS-FETs. Under the reverse-bias stress with the same V_{GD}, more negative V_{GS} will result in much larger V_{TH} shifts. It is due to enhanced holes transport through the gate dielectric under the larger negative V_{GS}, which could result in new defects generation in the gate dielectric and more electron traps under positive V_{GS}. Therefore, the negative gate bias is preferrably confined within a suitable range to obtain a stable V_{TH} in high-power switching applications if E-mode GaN MIS-FETs are employed.

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