中国科学技术大学
University of Science and Technology of China

数字集成电路设计

第九章　组合电路设计

白雪飞

中国科学技术大学微电子学院

提纲

- 引言
- 电路系列
- 电路隐患
- 绝缘体上硅电路设计

引　言

引言

电路系列

- 静态CMOS逻辑：鲁棒性好、速度快、能量效率高、易于设计
- 其他CMOS逻辑：可用于对速度、功耗、电路密度等有特别严格限制的情况
  - 有比电路、动态电路、传输管电路等

快速电路设计

$$I = C\frac{\mathrm{d}V}{\mathrm{d}t} \quad \Rightarrow \quad t_{pd} \propto \frac{C}{I}\Delta V$$

- 降低电容、增加电流、减小电压摆幅
- 逻辑努力正比于C/I
  - 逻辑门的输入电容与能够提供相同输出电流的反相器的输入电容之比
- 在同等尺寸和电容的情况下，NMOS管能够比PMOS管提供更大的电流
  - 很多快速电路系列力图使输入端只驱动NMOS管

电路系列

静态CMOS逻辑

- **优点**
  - 鲁棒性好、速度快、能量效率高、易于设计
  - 只要逻辑设计和制造过程未出错，对于给定的正确输入，总能产生正确输出
  - 绝大多数电路采用静态CMOS逻辑

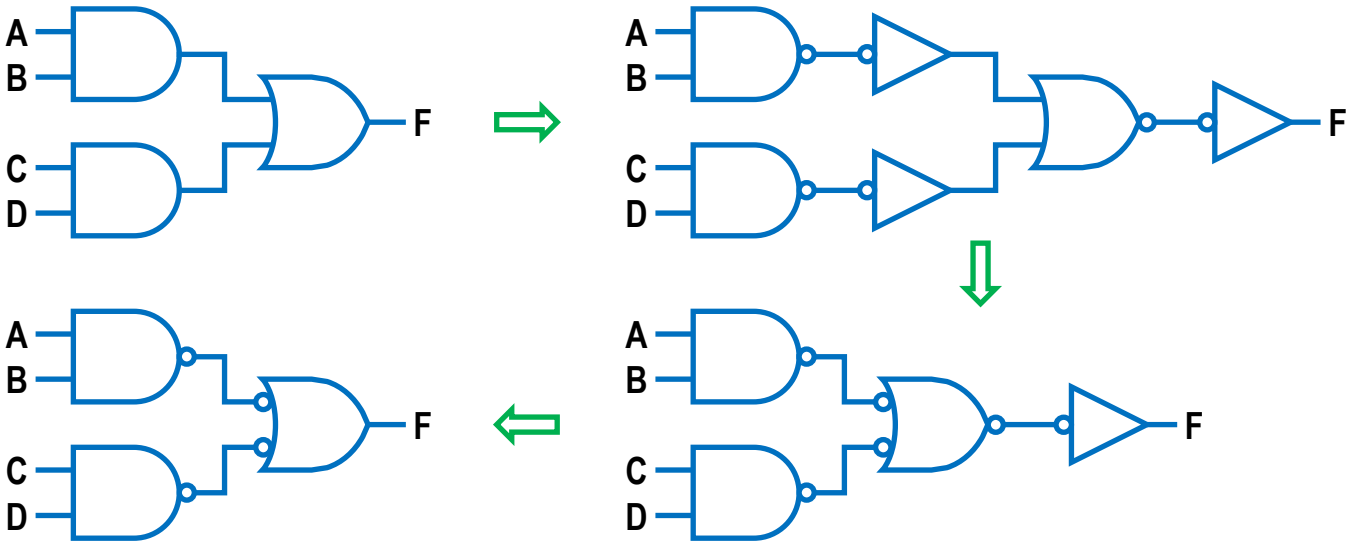
- **缺点**
  - 每个输入端上同时有NMOS管和PMOS管，逻辑努力较大
  - 所有节点电压必须在0和V_{DD}之间翻转

推气泡 (Bubble Pushing)

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

根据DeMorgan定理推气泡



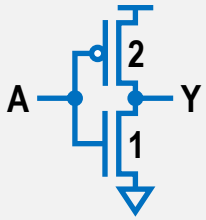
$$F = AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$$

利用推气泡方法把AND和OR转换成NAND和NOR

复合门

Unit Inverter

$Y = \overline{A}$

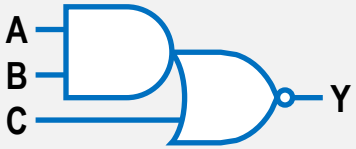


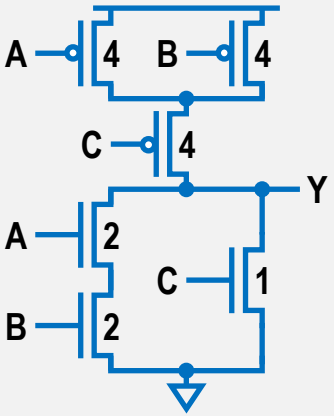
$g_A = 3/3$

$p = 3/3$

AOI21

$Y = \overline{A \cdot B + C}$





$g_A = 6/3$

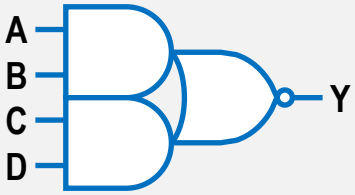
$g_B = 6/3$

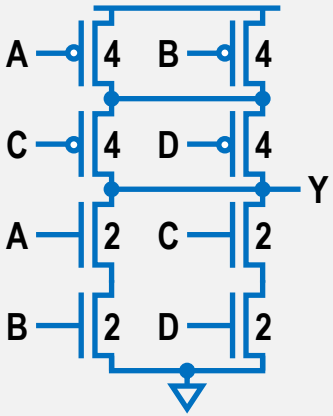
$g_C = 5/3$

$p = 7/3$

AOI22

$Y = \overline{A \cdot B + C \cdot D}$





$g_A = 6/3$

$g_B = 6/3$

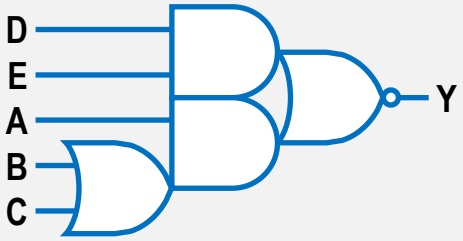
$g_C = 6/3$

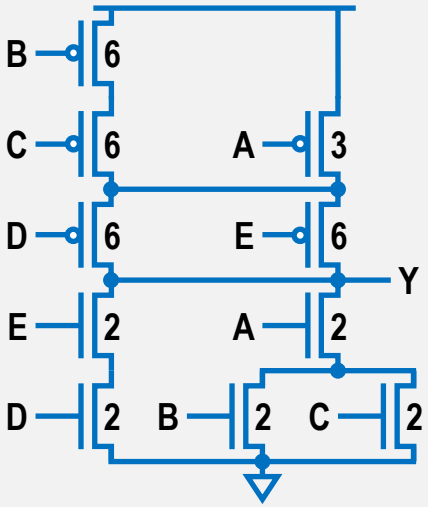
$g_D = 6/3$

$p = 12/3$

Complex AOI

$Y = \overline{A \cdot (B + C) + D \cdot E}$





$g_A = 5/3$ $g_D = 8/3$

$g_B = 8/3$ $g_E = 8/3$

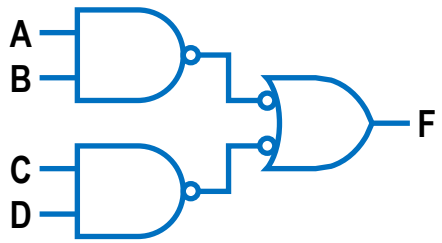
$g_C = 8/3$ $p = 16/3$

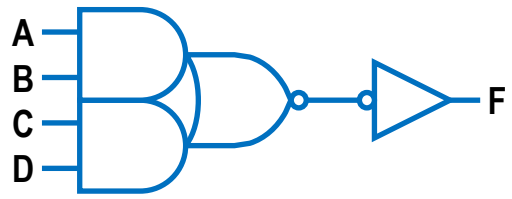
与或非门的逻辑努力和寄生延时

复合门举例

- **例：** 如下两种结构的与或门电路，每个输入端驱动的晶体管总宽度最多为20λ，输出端驱动相当于晶体管宽度为100λ的负载。

  求： 这两个电路的最小延时，以及达到最小延时的晶体管尺寸。





$$H = 100/20 = 5; \quad B = 1; \quad N = 2$$

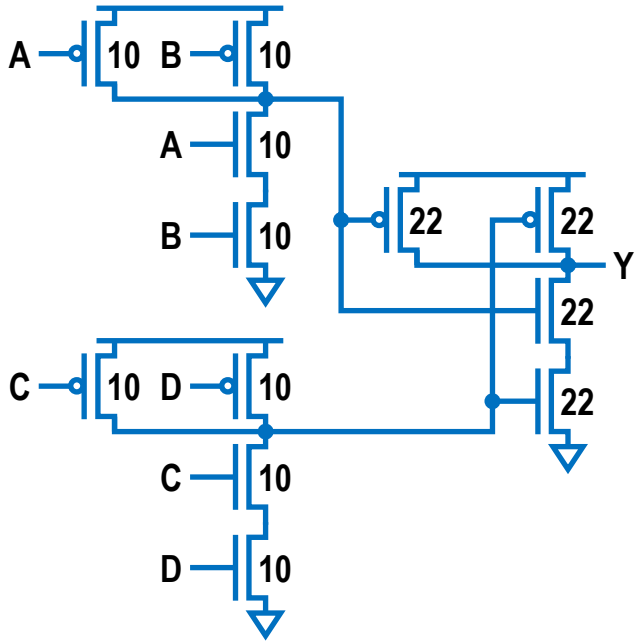
$$G = (4/3) \times (4/3) = 16/9$$
$$P = 2 + 2 = 4$$
$$F = GBH = 80/9$$
$$\hat{f} = F^{1/N} = 3.0$$
$$D = NF^{1/N} + P = 10.0\tau$$

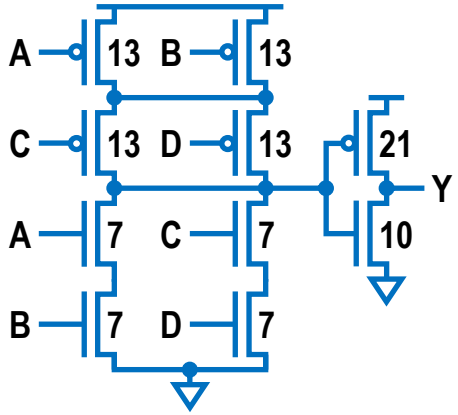
$$G = (6/3) \times 1 = 2$$
$$P = 12/3 + 1 = 5$$
$$F = GBH = 10$$
$$\hat{f} = F^{1/N} = 3.2$$
$$D = NF^{1/N} + P = 11.3\tau$$

复合门举例

- **例：** 如下两种结构的与或门电路，每个输入端驱动的晶体管总宽度最多为20λ，输出端驱动相当于晶体管宽度为100λ的负载。

  求： 这两个电路的最小延时，以及达到最小延时的晶体管尺寸。





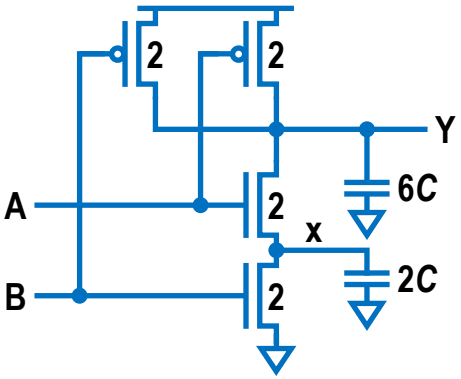
$$C_{in_2} = \frac{C_{out} \times g}{\hat{f}} = \frac{100\lambda \times (4/3)}{3.0} = 44\lambda$$

$$C_{in_2} = \frac{C_{out} \times g}{\hat{f}} = \frac{100\lambda \times 1}{3.2} = 31\lambda$$

输入顺序对延时的影响

与非门延时估计

- 若输入A保持为“1”，输入B从“0”上升为“1”
  - 初始状态时　$V_x = V_{DD} - V_t \approx V_{DD}$
  - Elmore延时为　$(R/2)(2C) + R(6C) = 7RC = 2.33\tau$
- 若输入B保持为“1”，输入A从“0”上升为“1”
  - 初始状态时　$V_x = 0$
  - Elmore延时为　$R(6C) = 6RC = 2\tau$

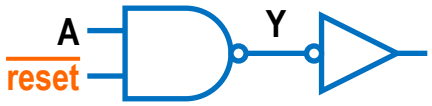


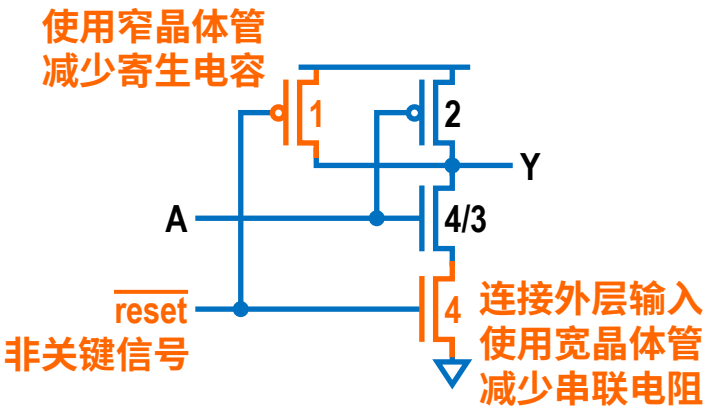
与非门延时估计

外层输入和内层输入

- 外层输入(Outer Input)：靠近电源轨线的输入，例如B
- 内层输入(Inner Input)：靠近输出端的输入，例如A
- 内层输入最后翻转时寄生延时最小
- 若已知某输入最后到达，则此输入连接到内层输入时逻辑门速度最快

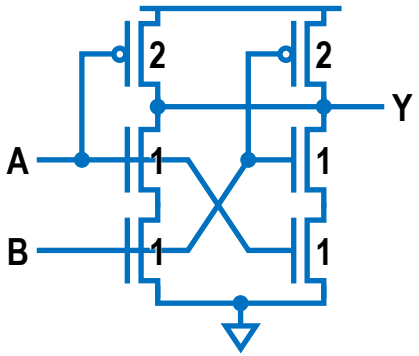
不对称门和完全对称门





$$g_{\mathrm{A}} = 10/9$$

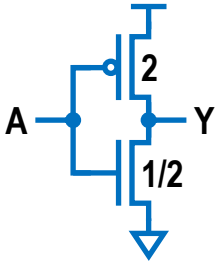
优化数据输入的缓冲器



完全对称的二输入与非门

偏斜门 (Skewed Gate)

高偏斜反相器

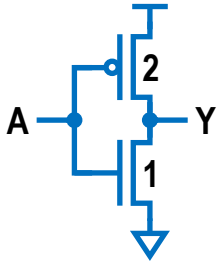


$$C_{\text{in}} = (5/2)C$$

$$g_u = C_{\text{in}}/C_{\text{in}-u} = 5/6$$

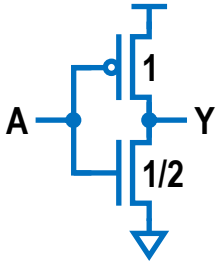
$$g_d = C_{\text{in}}/C_{\text{in}-d} = 5/3$$

不偏斜反相器
（相等的上升电阻）



$$C_{\text{in}-u} = 3C$$

不偏斜反相器
（相等的下降电阻）

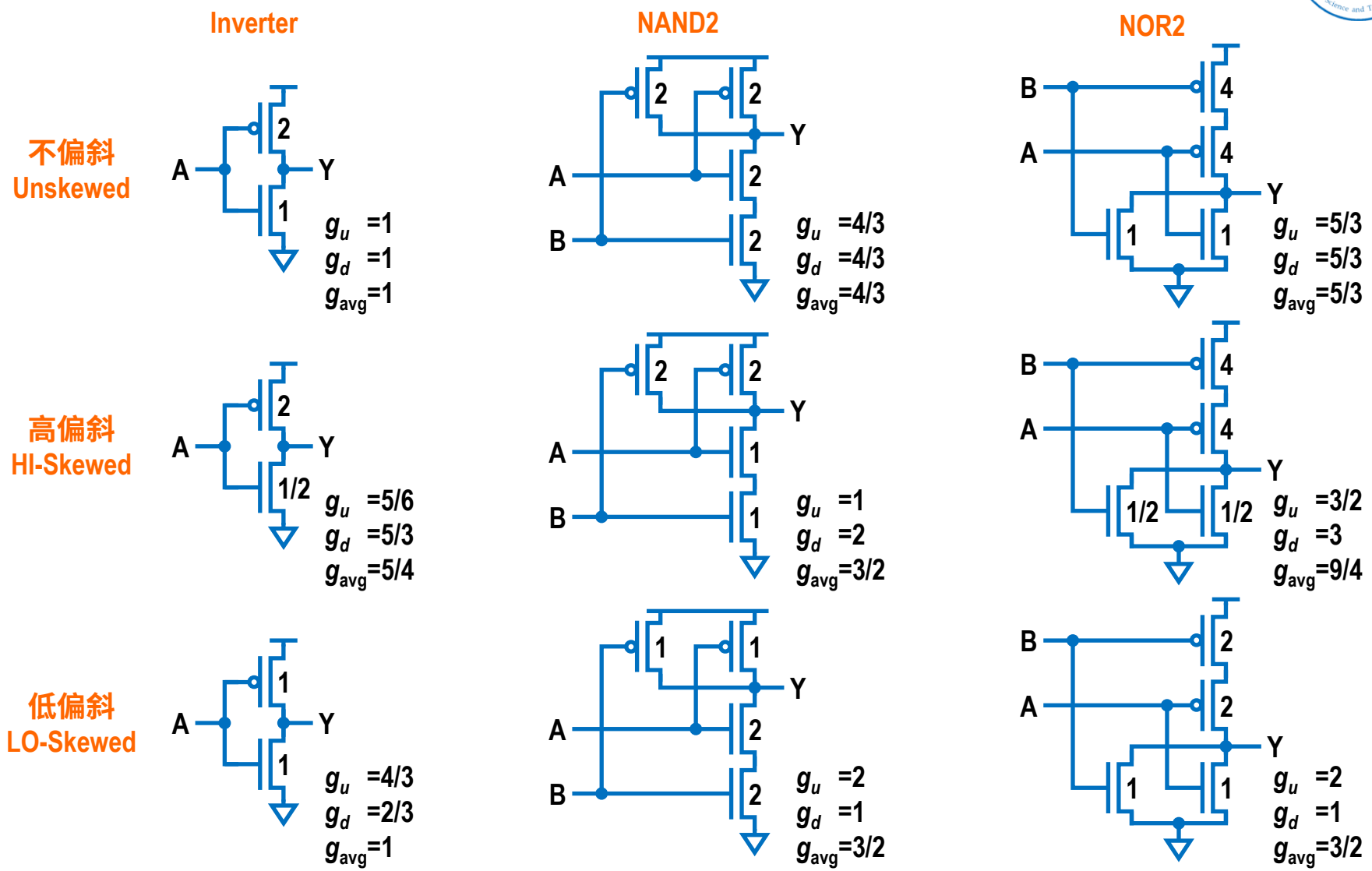


$$C_{\text{in}-d} = (3/2)C$$

高偏斜反相器的逻辑努力

偏斜门的逻辑努力：输入电容与“对应跳变具有相同驱动能力的不偏斜反相器输入电容”之比

偏斜门的分类

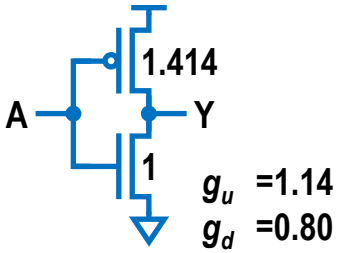


偏斜门的分类

P/N比

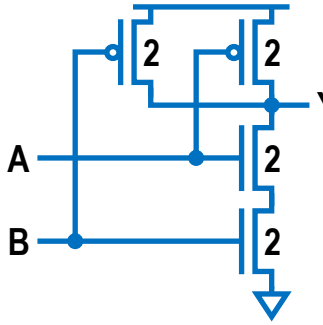
Fastest P/N Ratio

Inverter



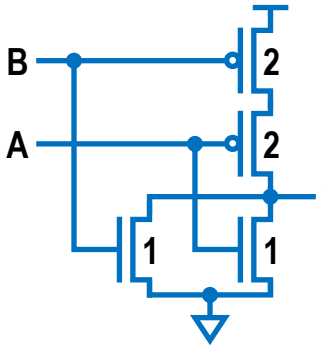
g_u =1.14
g_d =0.80
g_{avg}=0.97

NAND2



g_u =4/3
g_d =4/3
g_{avg}=4/3

NOR2



g_u =2
g_d =1
g_{avg}=3/2

最小延时逻辑门的P/N比

平均延时最小的P/N比等于上升和下降延时相等时P/N比的平方根

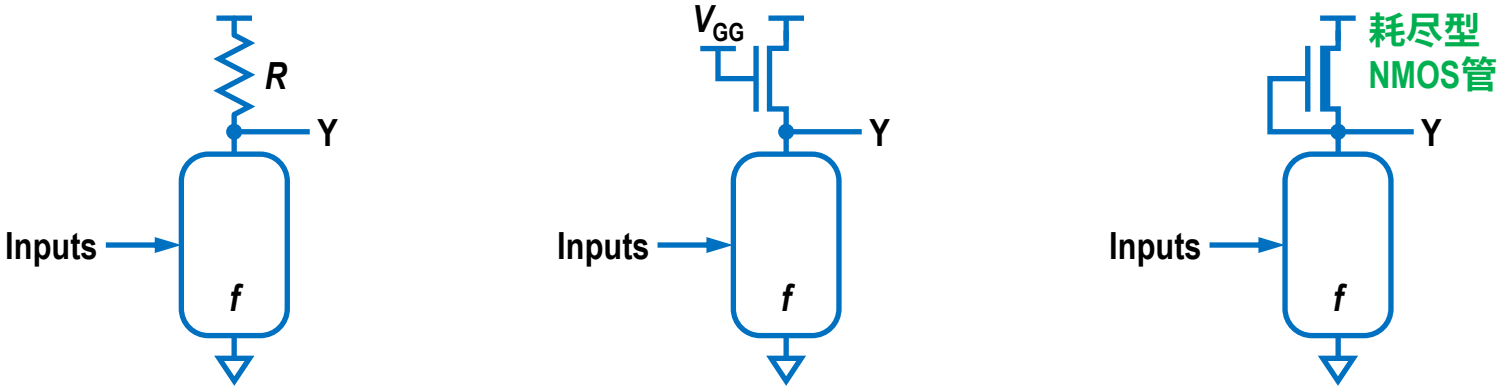
有比电路

有比电路

- 能否正确工作取决于器件是否选择了合适的尺寸或电阻

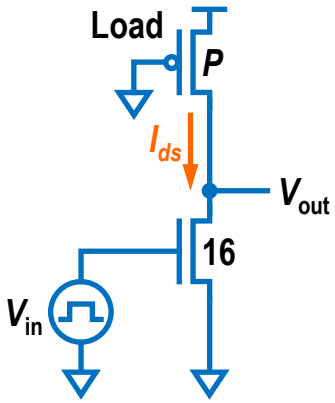
NMOS有比逻辑门

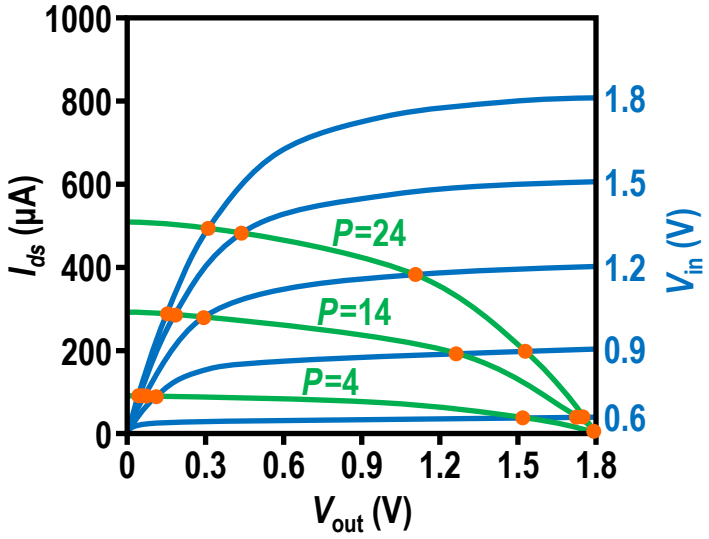
- 由NMOS下拉网络和静态负载构成
- 下拉网络截止时，静态负载将输出上拉至“1”
- 下拉网络导通时，将与静态负载竞争，并使输出下拉至可接受的“0”电平
- 静态负载应足够弱，二者之间存在一个比值约束

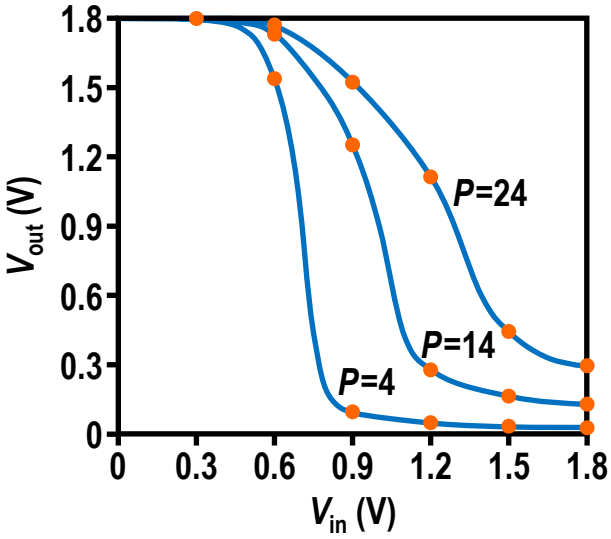


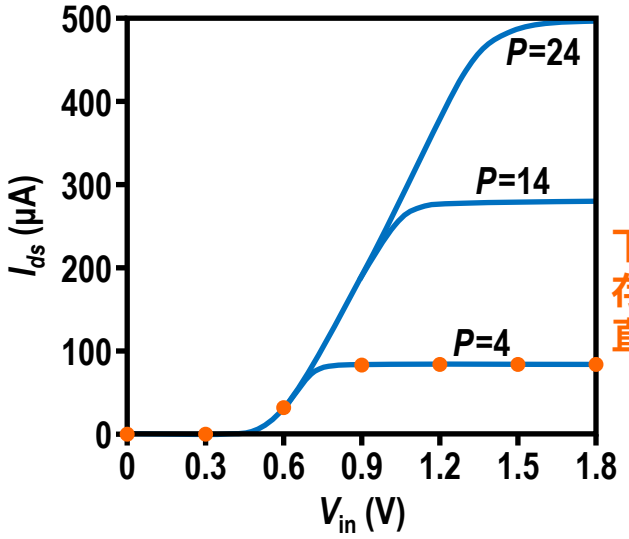
NMOS有比逻辑门

伪NMOS反相器





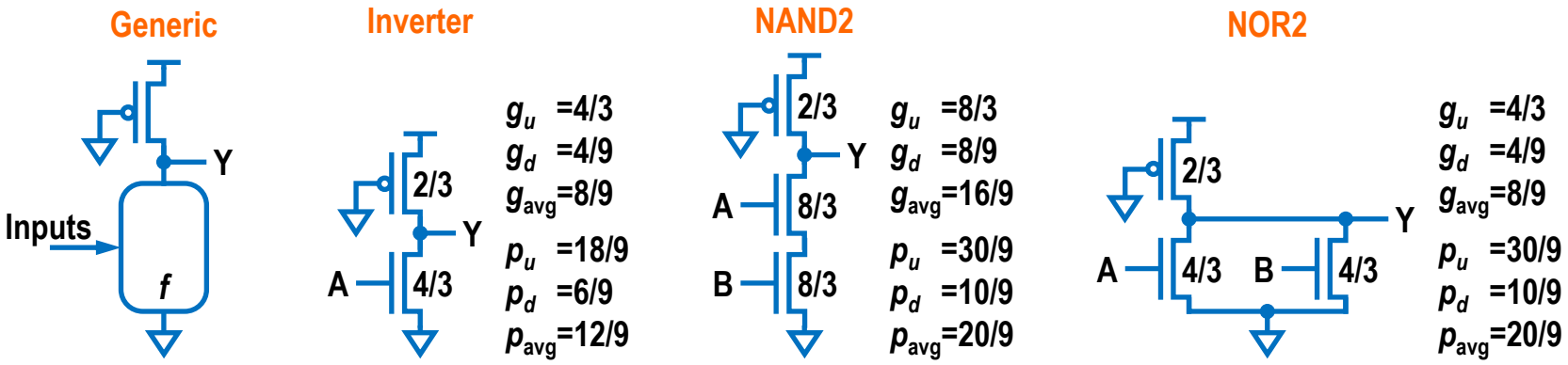




下拉导通
存在静态
直流电流

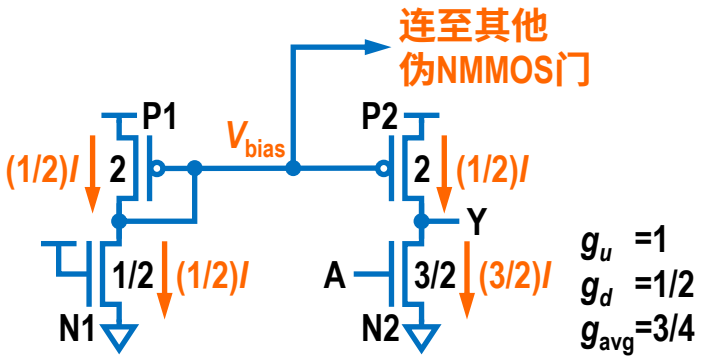
180-nm工艺伪NMOS反相器及其直流传输特性

伪NMOS逻辑门



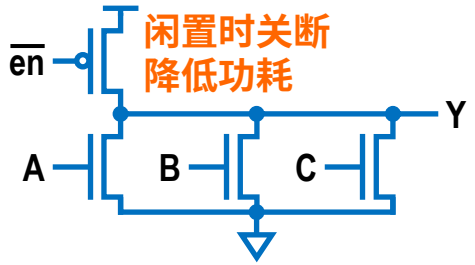
伪NMOS逻辑门

PMOS管宽度的选择使其驱动强度为NMOS下拉网络的1/4左右(1/6~1/3)



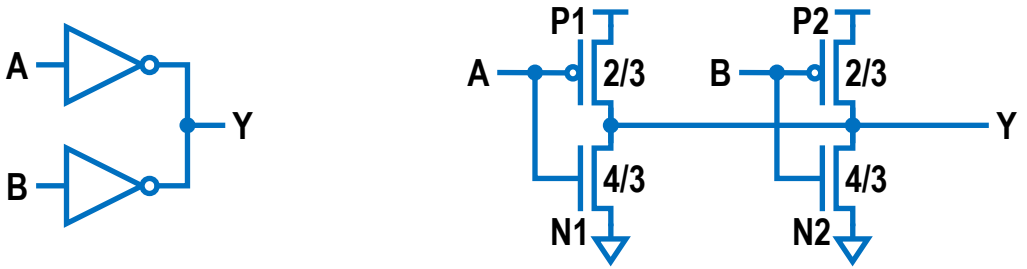
伪NMOS逻辑门的复制偏置

P2和N2电流比与迁移率相对大小无关



具有上拉使能的伪NMOS逻辑门

共输出CMOS电路



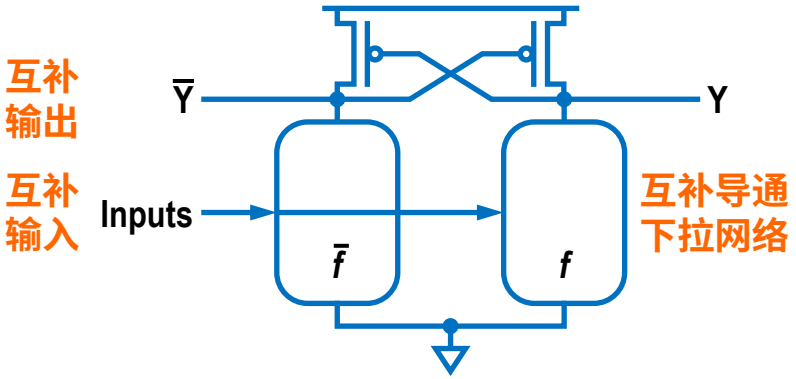
g_u =1
g_d =2/3
g_{avg}=5/6

对称二输入或非门

对称二输入或非门工作状态

A	B	N1	P1	N2	P2	Y
0	0	OFF	ON	OFF	ON	1
0	1	OFF	ON	ON	OFF	~0
1	0	ON	OFF	OFF	ON	~0
1	1	ON	OFF	ON	OFF	0

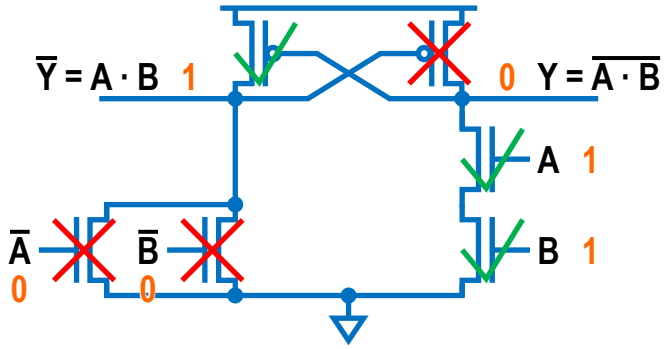
级联电压开关逻辑 (CVSL)



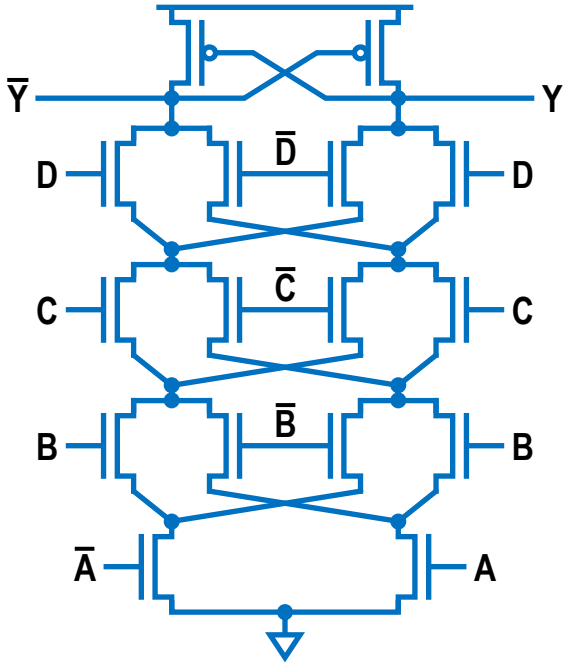
CVSL门一般形式

以A=1, B=1为例

没有静态电流

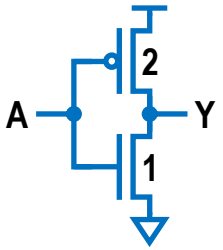


CVSL与门/与非门

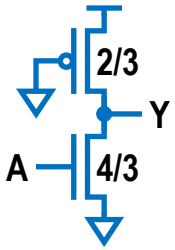


CVSL四输入异或门

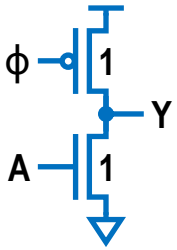
动态电路



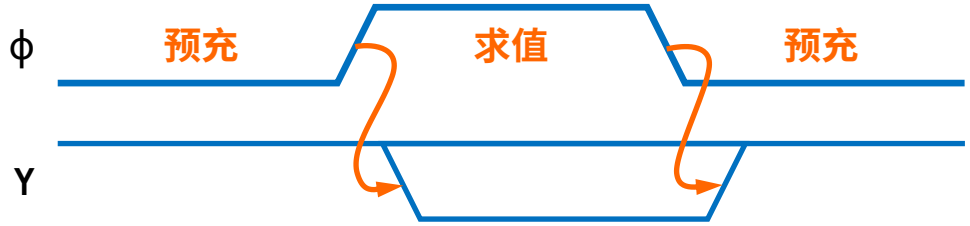
静态CMOS反相器



伪NMOS反相器



动态反相器



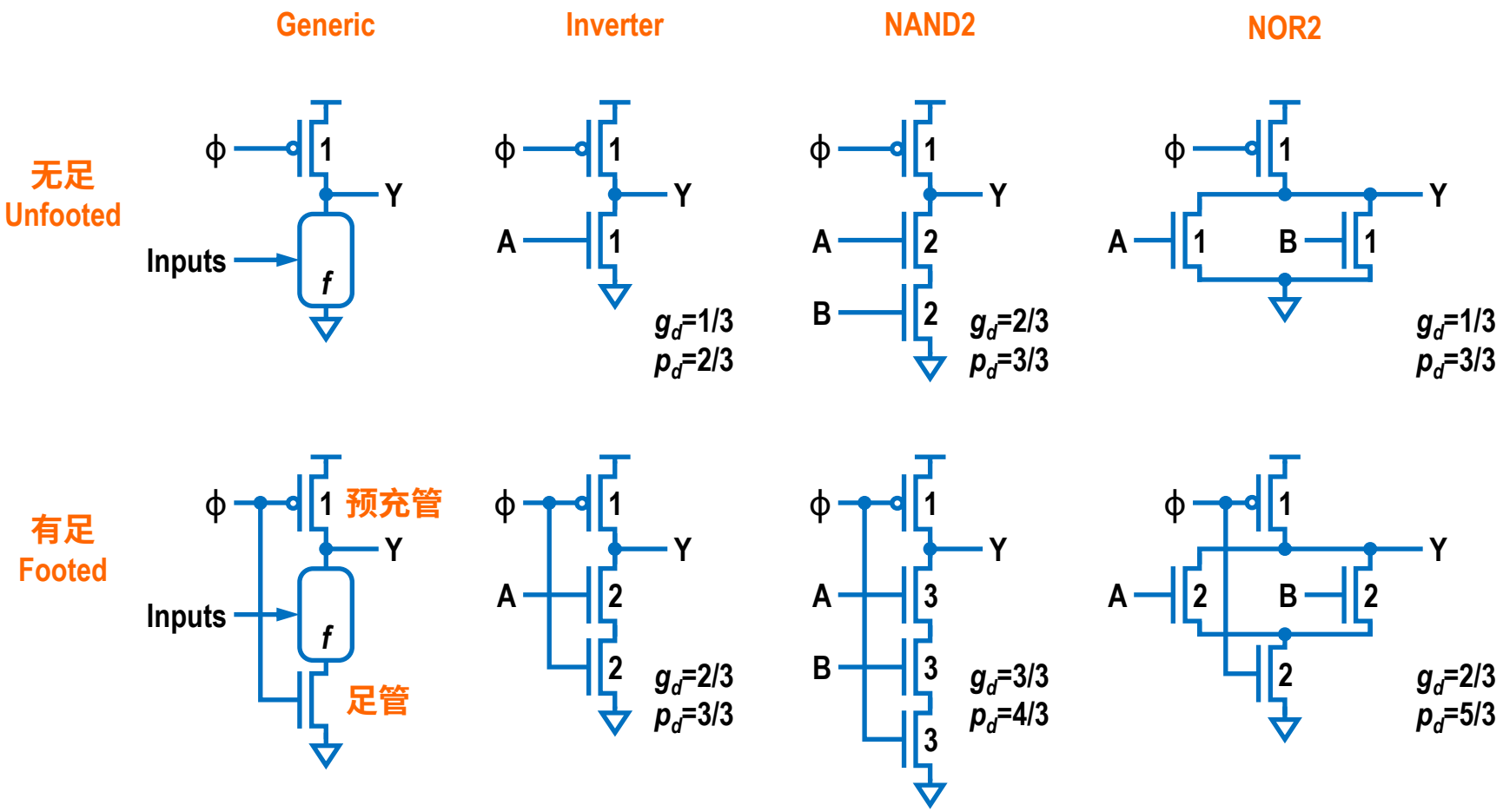
动态门的预充(Precharge)和求值(Evaluation)

预充：PMOS管导通，下拉网络应截止，输出端充电至高电平

求值：PMOS管截止，下拉网络若截止，输出端仍保持高电平

下拉网络若导通，输出端放电至低电平

有足和无足动态门

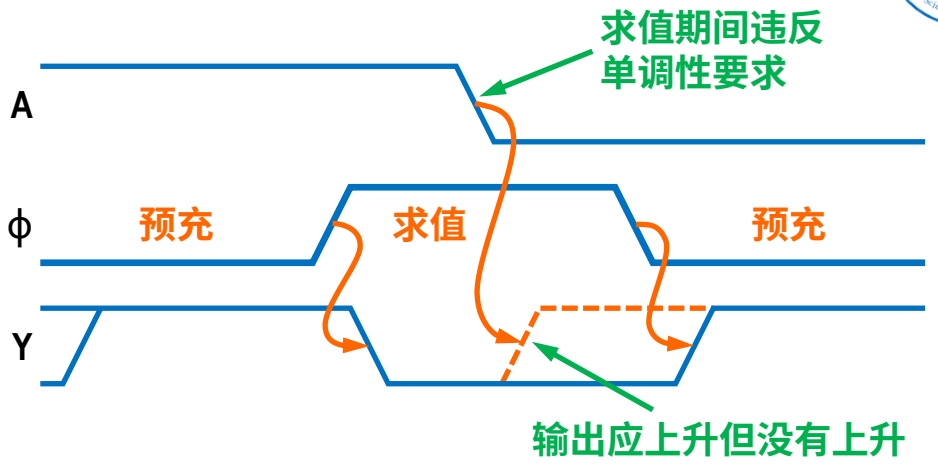


动态门的分类

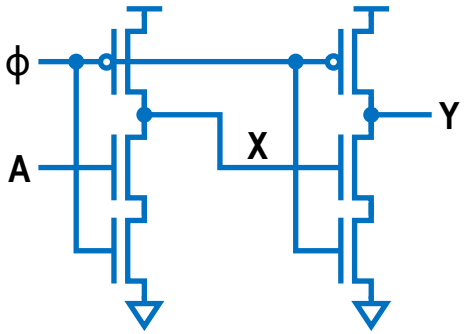
若输入不能保证在预充期使下拉网络截止，则增加足管避免发生竞争

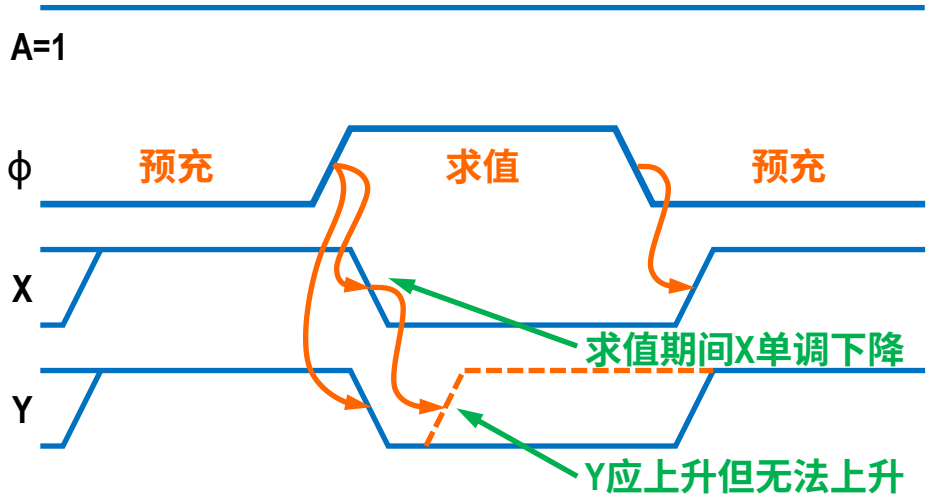
动态门输入的单调性问题

- 动态门输入在求值期间要求必须单调上升
- 动态门输出在求值期间单调下降，不适合作为下一级动态门的输入



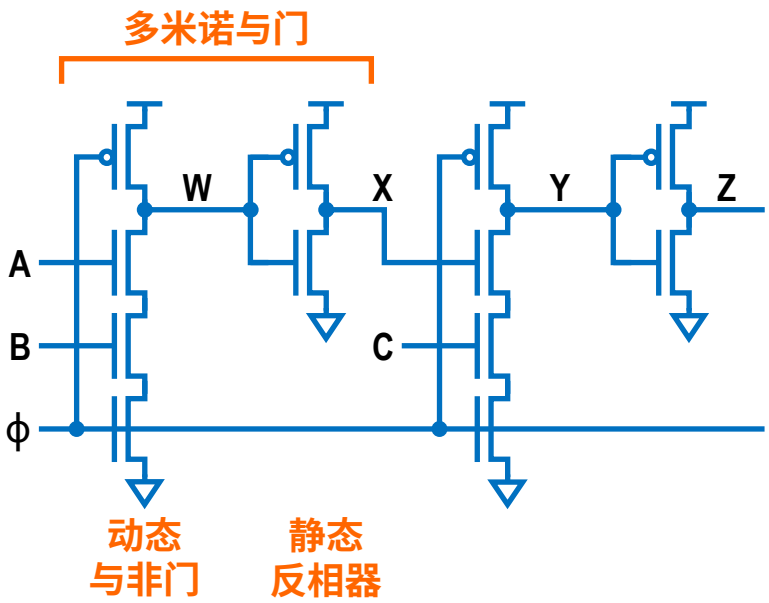
动态门输入的单调性问题



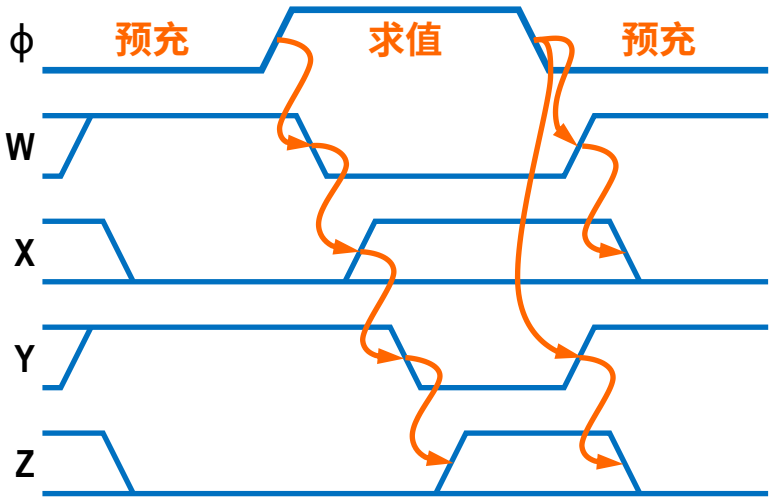


动态门的错误连接方式

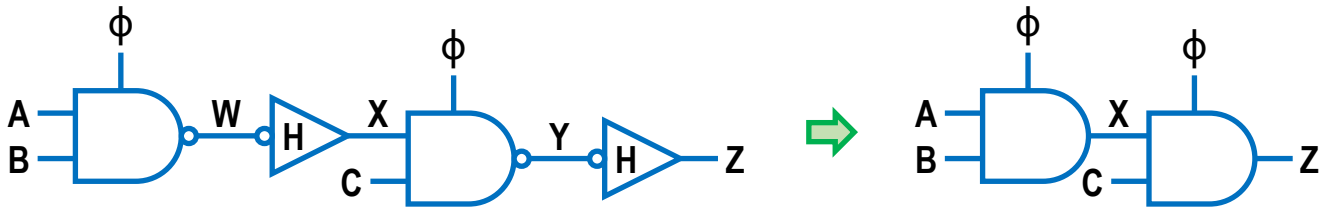
多米诺逻辑



多米诺(Domino)逻辑门

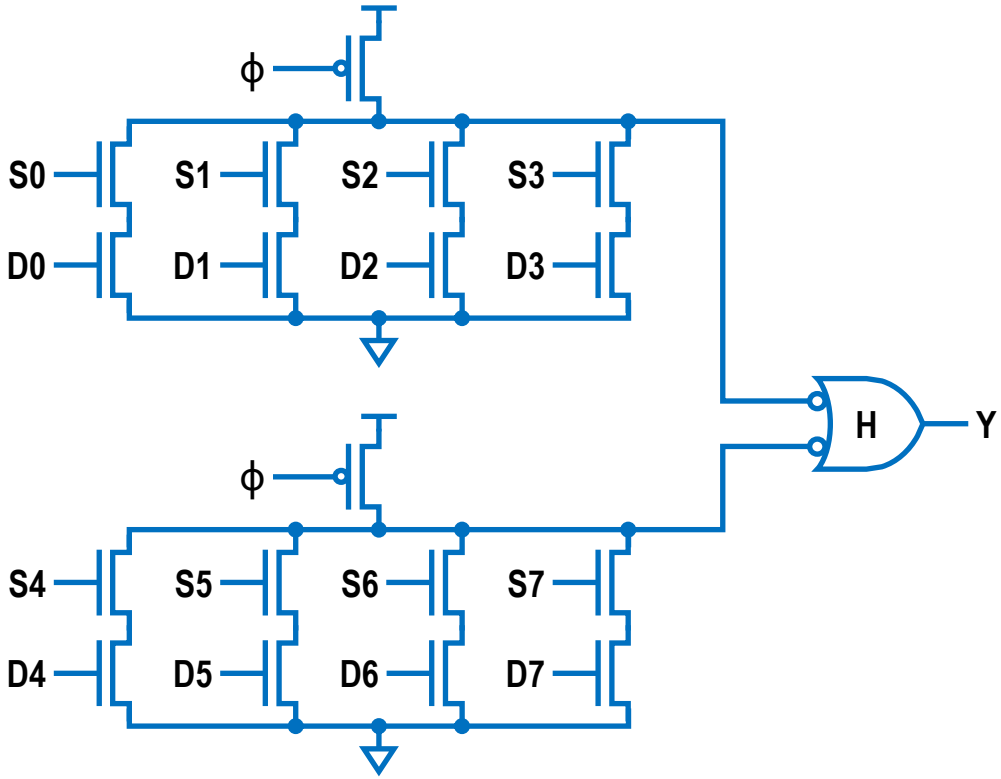


多米诺逻辑电路波形



多米诺逻辑门的符号

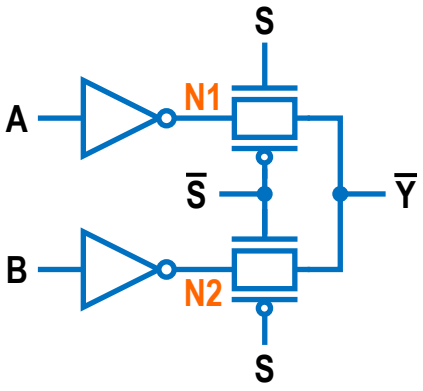
复合多米诺逻辑

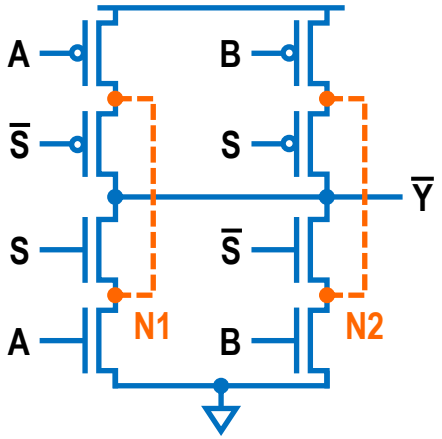


复合多米诺逻辑 (Compound Domino Logic)

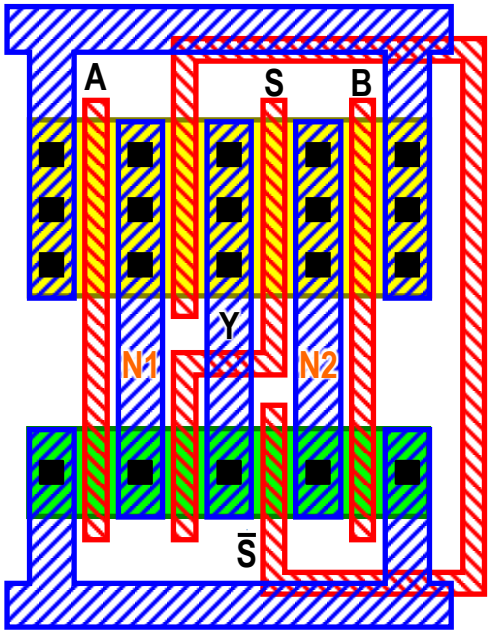
使用较为复杂的反相静态CMOS逻辑门代替多米诺逻辑门中的反相器

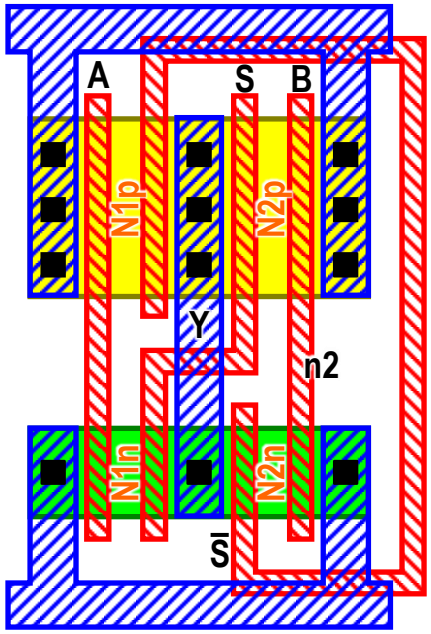
含传输门的CMOS电路





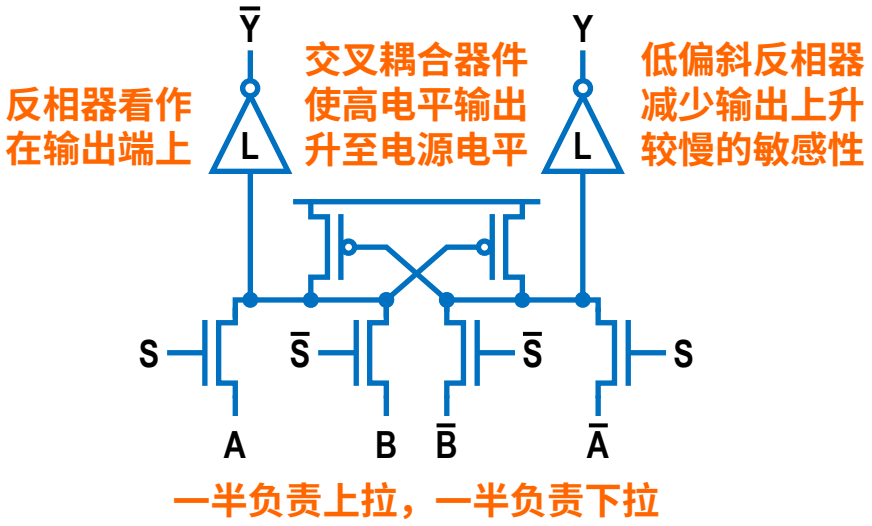
短接中间结点
等效电阻减少
等效电容增加

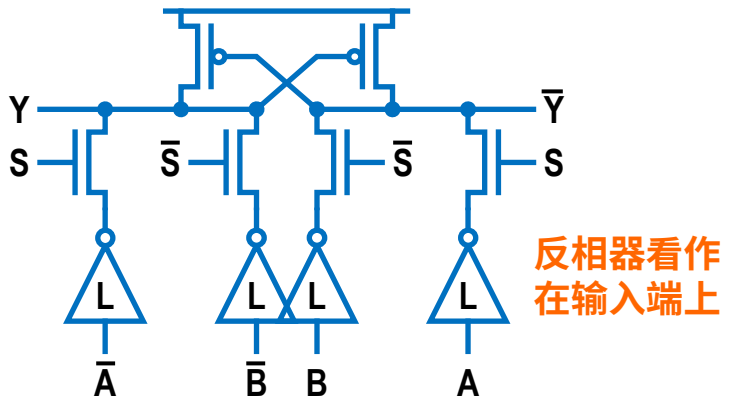


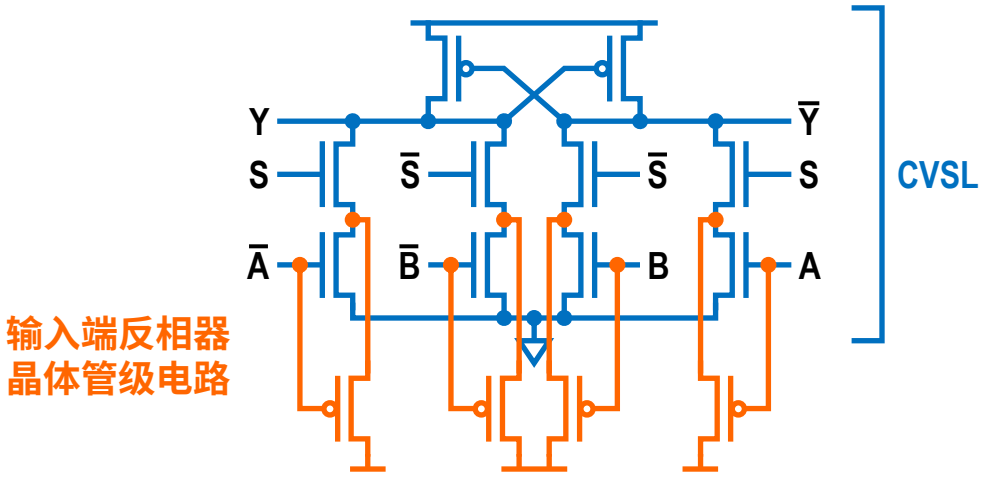


二输入多路反相开关中CMOS传输门的不同电路形式及其版图比较

互补传输管逻辑 (CPL)



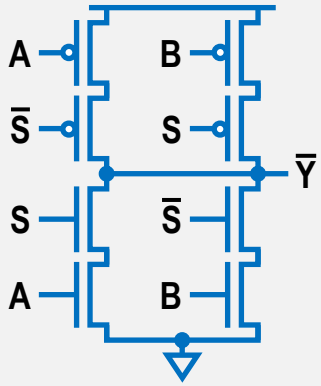




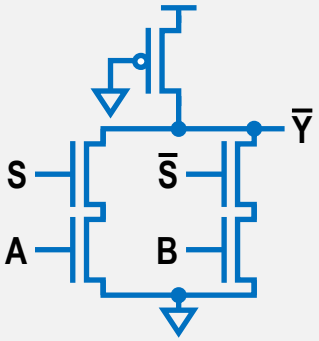
互补传输管逻辑多路开关电路图

电路系列比较

Static CMOS

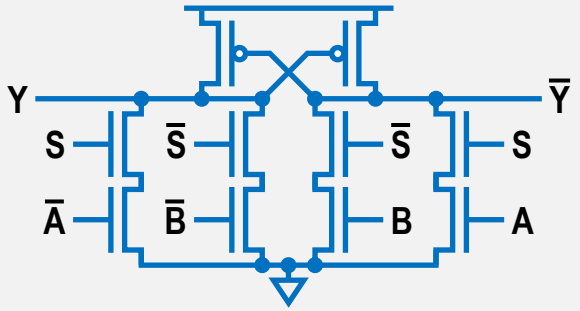


Pseudo-NMOS

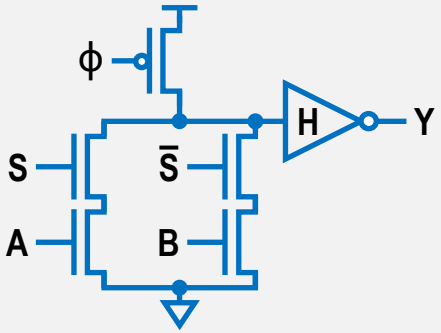


CVSL

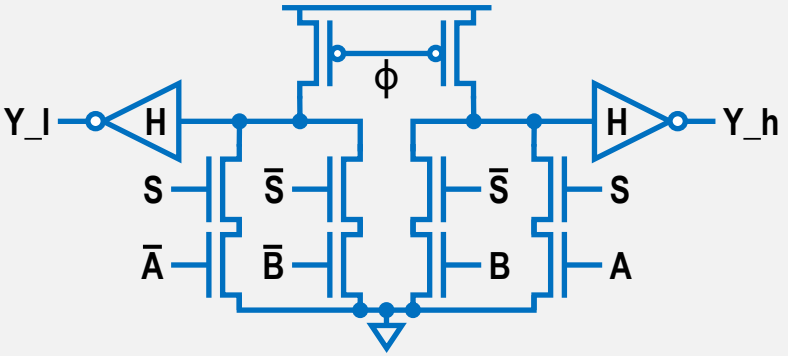
Cascode Voltage Switch Logic



Domino

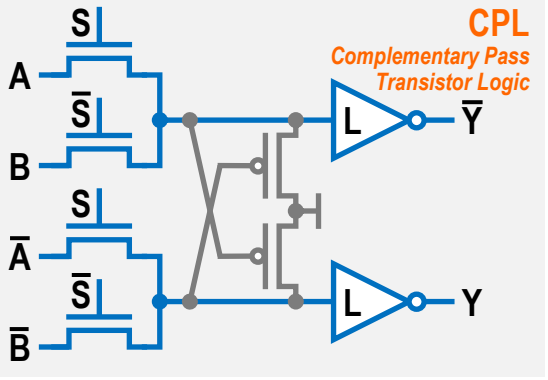


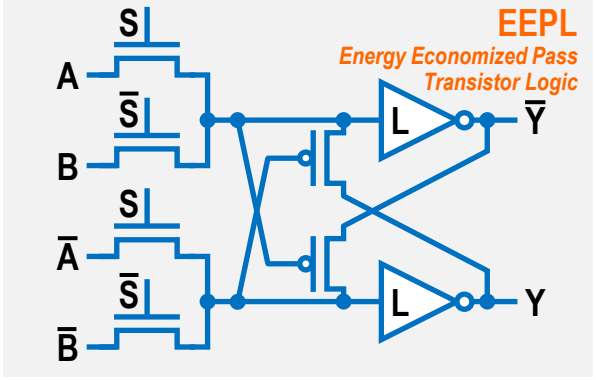
Dual-Rail Domino

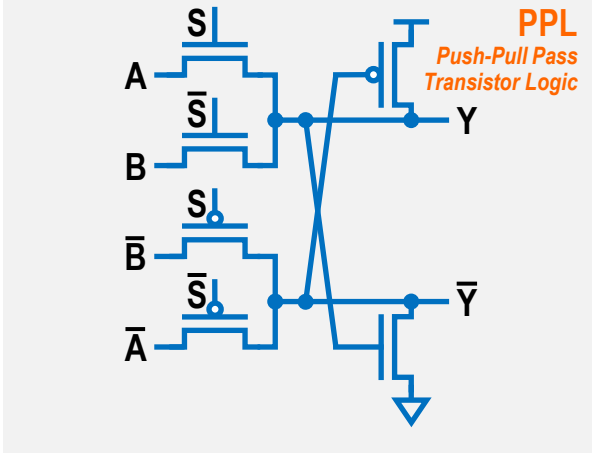


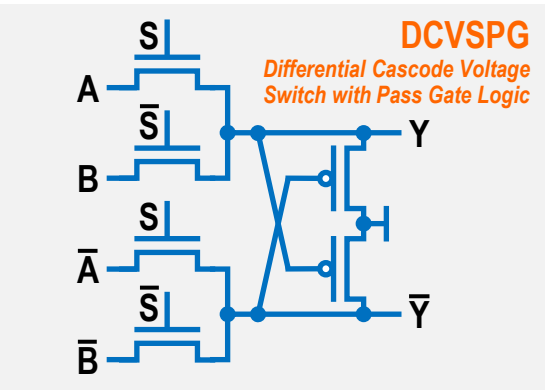
二输入多路开关的各种电路系列

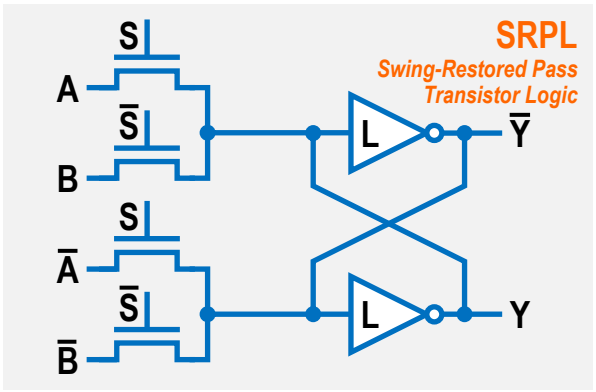
传输管电路系列比较

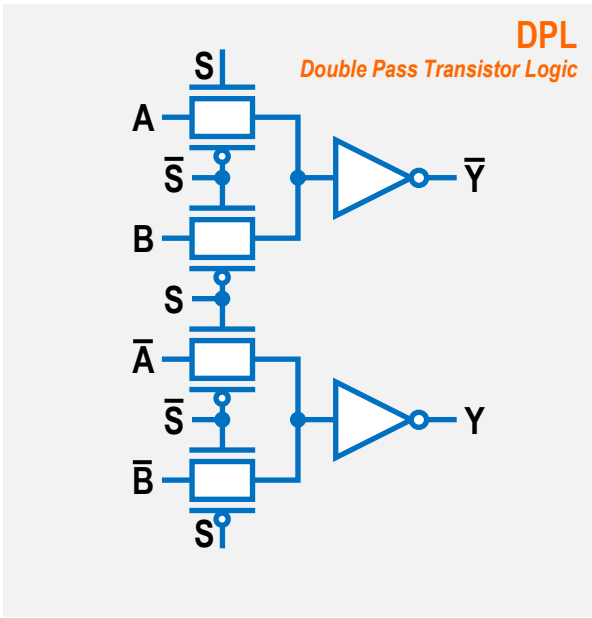


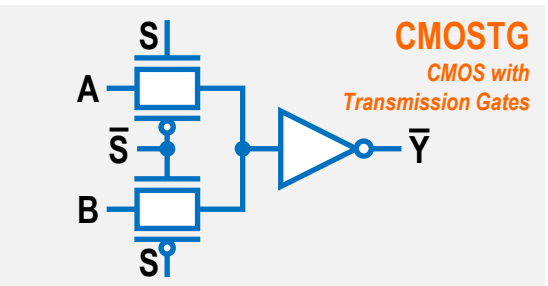


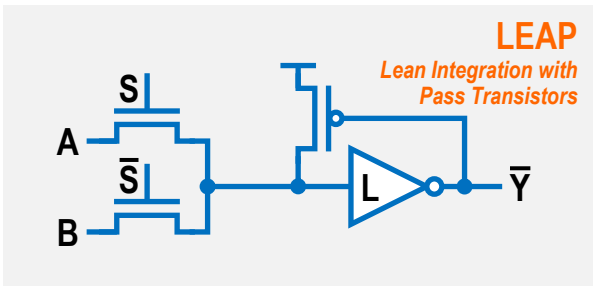








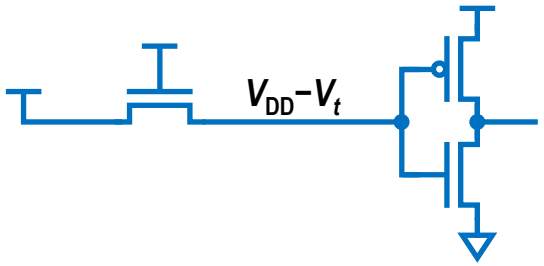




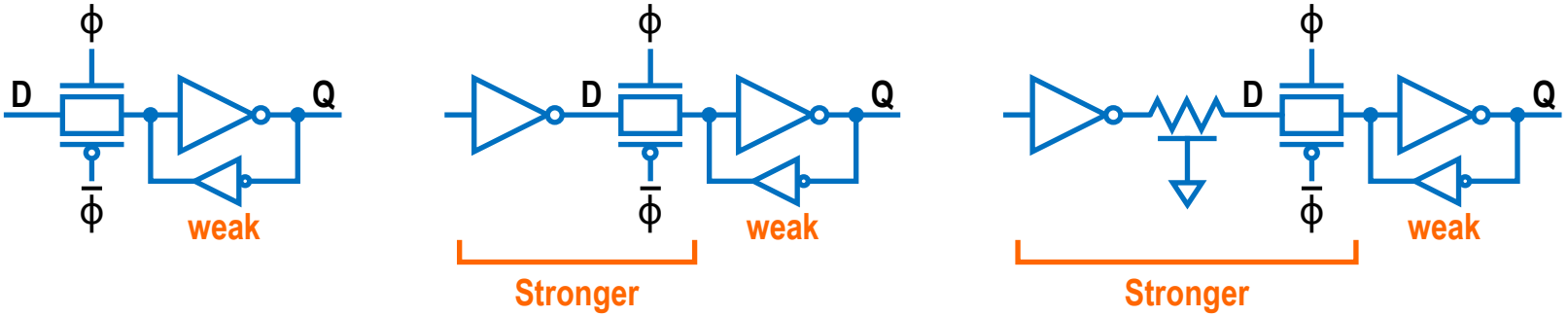
二输入多路开关的传输管电路系列

电路隐患

阈值损失和比值失效



传输管的阈值损失(Threshold Drop)



具有扩散区输入的静态锁存器的比值约束问题

必须整体检查锁存器和驱动器，验证弱反馈反相器比值约束

泄漏电流和工艺敏感性

泄漏电流

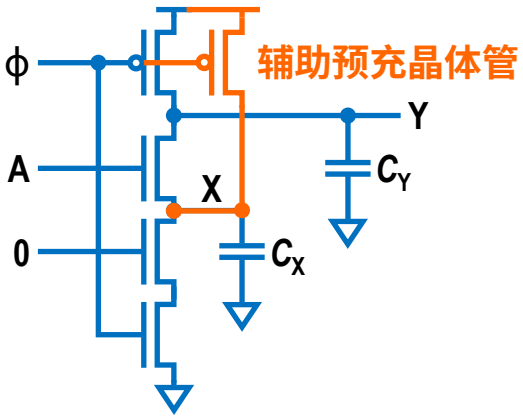
- 引起静态功耗
- 导致动态节点或弱驱动节点上出现不正确的电压值
- 泄漏电流使一个动态节点的电压扰动ΔV所需时间

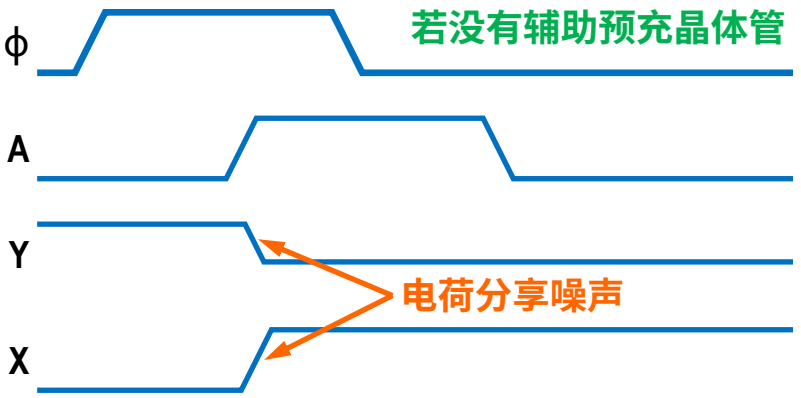
$$t = \frac{C_{\text{node}} \Delta V}{I_{\text{leak}}}$$

工艺敏感性

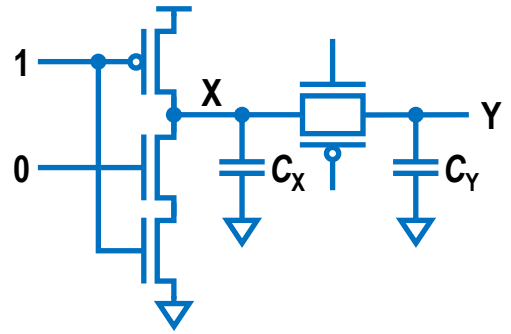
- 余量设计不充分的电路，可能会在某些工艺角或移植到另一种工艺时失效
- 应在所有工艺角进行仿真，验证是否能在各种PVT条件下正常工作

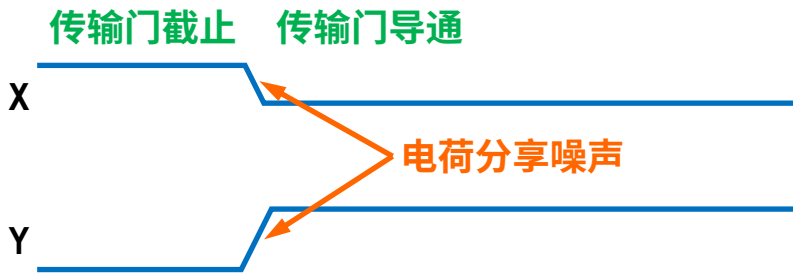
电荷分享





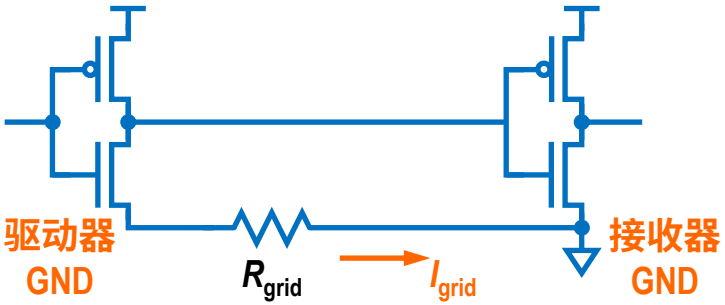
二输入动态与非门的电荷分享



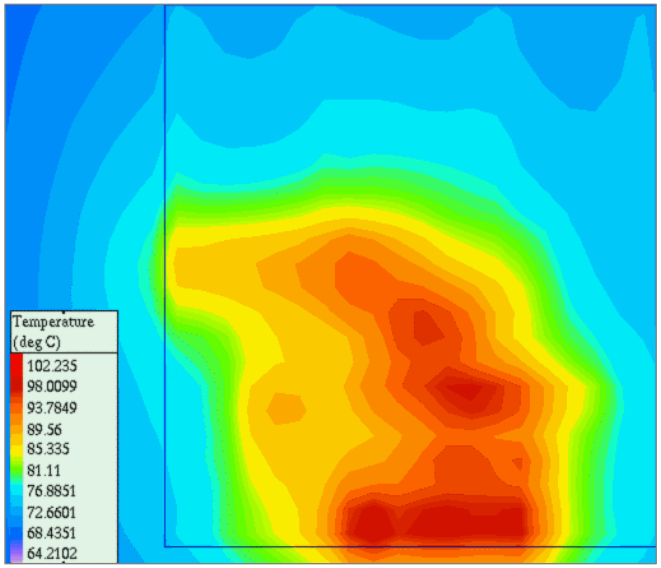


动态门驱动传输门时发生电荷分享

电源噪声和热斑

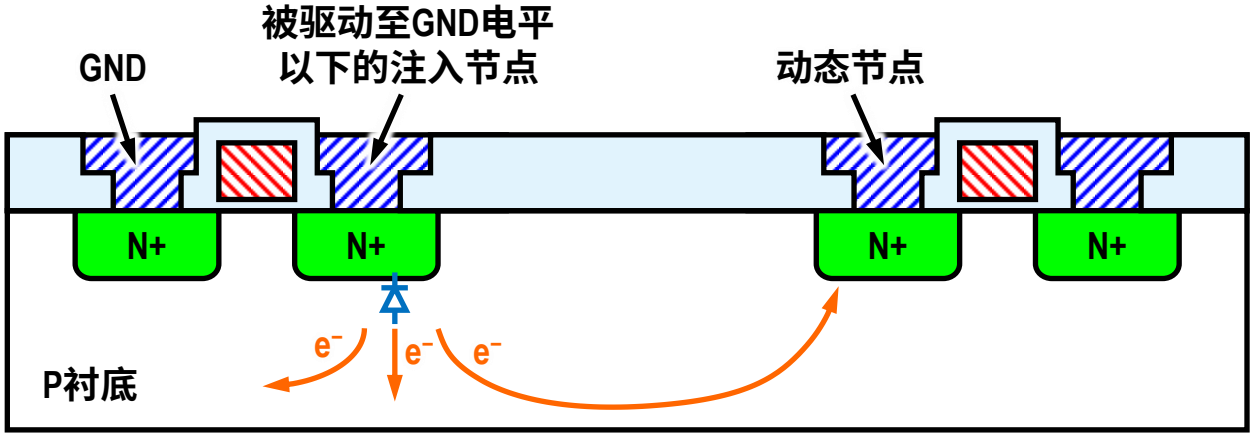


电源线上的IR压降

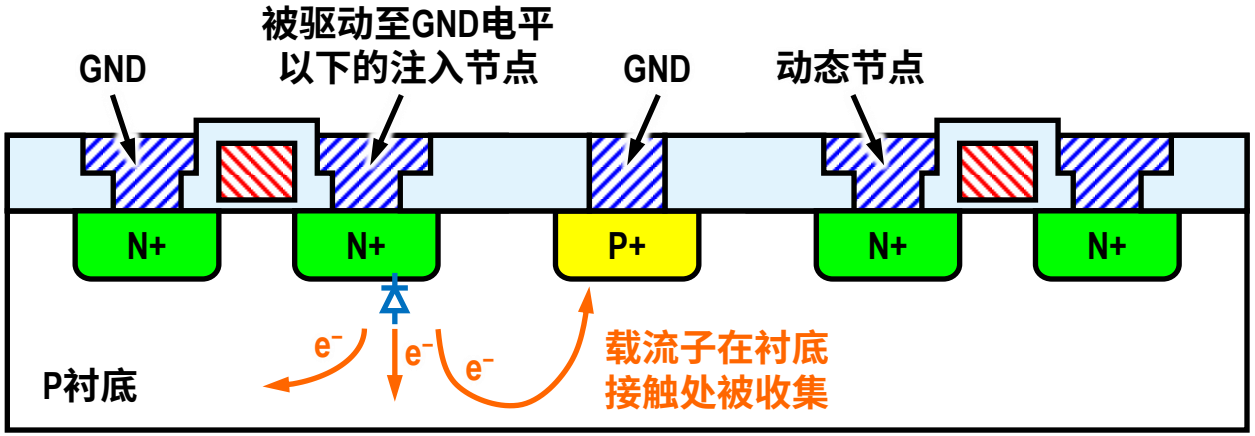


Itanium 2微处理器的热图

少数载流子注入

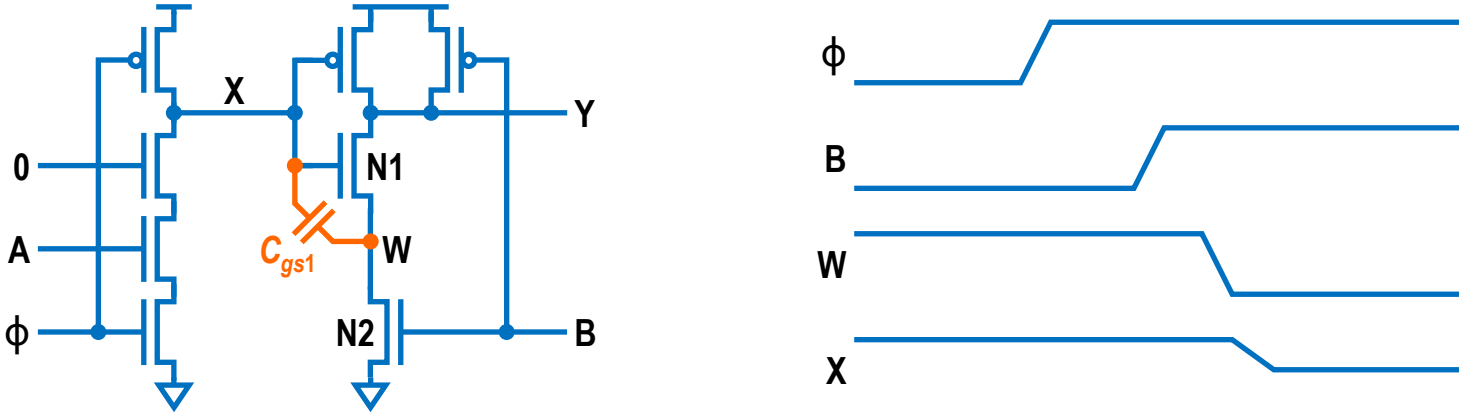


少数载流子的注入



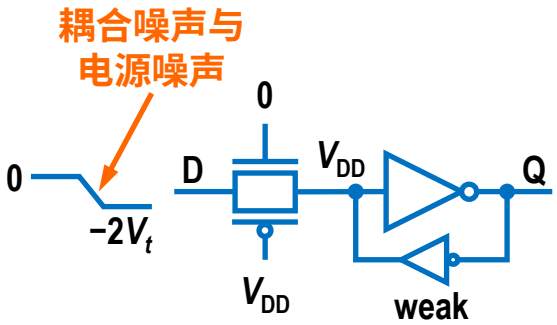
少数载流子的收集

背栅耦合和噪声敏感性



背栅耦合

使动态门驱动静态门中靠近电源轨线的输入可以消除背栅耦合效应

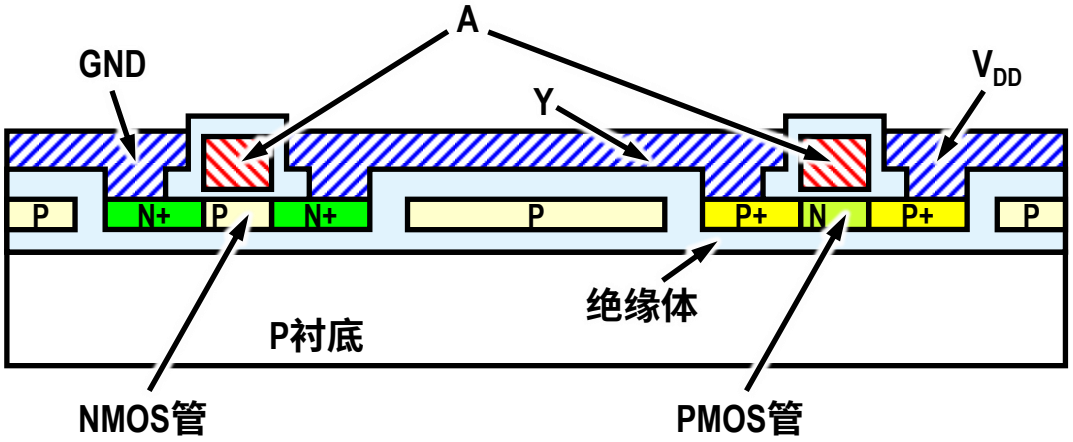


锁存器扩散区输入端上的噪声

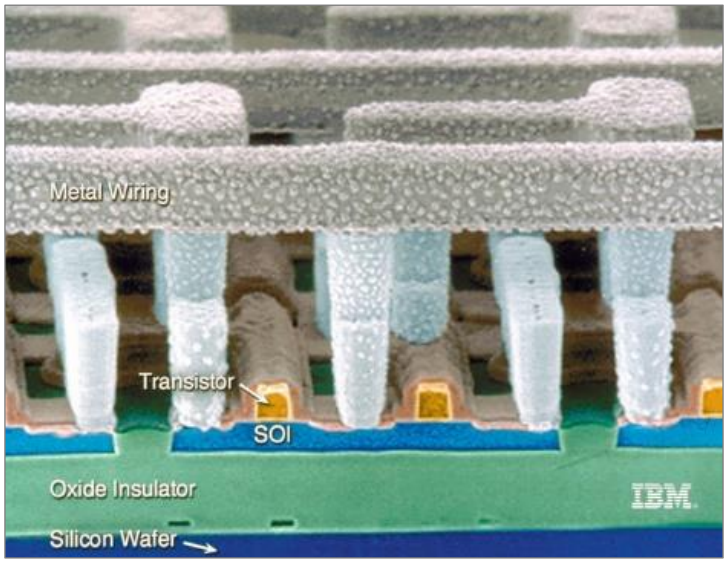
若噪声将输入电压驱动至低于$-V_t$或高于V_t，则传输门将会导通

绝缘体上硅电路设计

绝缘体上硅电路



绝缘体上硅反相器横截面图



IBM 0.22-μm绝缘体上硅工艺电子显微照片

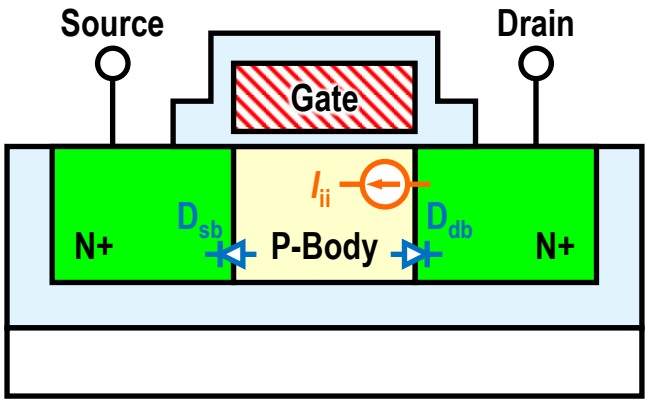
浮体电压

电荷流入浮体的机理

- 反向偏置的漏至体之间的结D_{db}以及源至体之间的结D_{sb}的二极管泄漏电流
- 高能量载流子引起碰撞电离，从而产生电子–空穴对，部分电子注入栅极或栅氧，相应的空穴在体中积累

电荷流出浮体的机理

- 体电压升高时，D_{sb}稍微正向偏置，从D_{sb}流出的电荷将等于D_{db}泄漏流入的电荷
- 栅极或漏极电压升高时，通过电容耦合使体电压也升高，D_{sb}正向强偏置，电荷从体中迅速泄放



流入/流出浮体的电荷通路

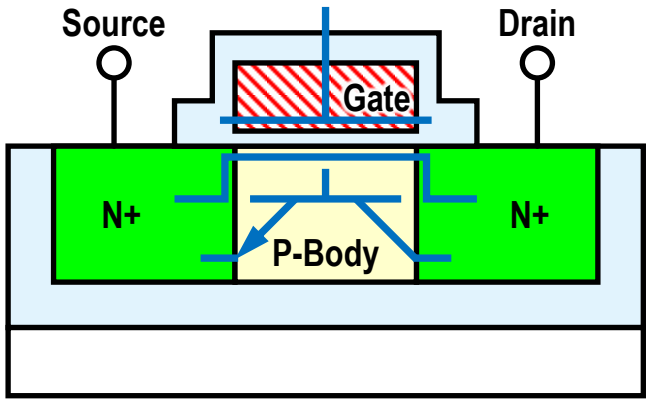
绝缘体上硅的优缺点

SOI的优点

- 扩散电容较小，从而寄生延时较小，动态功耗较低
- 有降低阈值电压的潜力
  - 阈值电压工艺偏差很小，额定V_t可以接近最坏情况下的阈值电压，使晶体管较快
- 氧化物消除了可能触发闩锁的寄生双极型器件，不会发生闩锁

SOI的缺点

- 历史效应：体电压的变化调制阈值电压，从而改变门延时，使匹配晶体管出现失配
- 每个晶体管内部存在一个寄生双极型晶体管，特定条件下导致从漏极流向源极的脉冲电流
- 由于氧化物是热的良绝缘体，因此热量容易积累，造成严重的自热



SOI中的寄生双极型晶体管

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