电子系统设计第二次作业

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1.

```
module unit (
    input   wire            cs_n,
    input   wire            en,
    input   wire    [3:0]   D,
    output  reg     [3:0]   Q
);

always @(*) begin
    if ({en,cs_n}==2'b10) begin
        Q <= D;
    end
    else begin
        Q <= Q;
    end
end
endmodule
```

2.

```
module decoder3_8 (
    input   wire    [2:0]   sel,
    input   wire    [3:0]   data_in,
    input   wire            en,

    output  wire    [3:0]   data_out_0,
    output  wire    [3:0]   data_out_1,
    output  wire    [3:0]   data_out_2,
    output  wire    [3:0]   data_out_3,
    output  wire    [3:0]   data_out_4,
    output  wire    [3:0]   data_out_5,
    output  wire    [3:0]   data_out_6,
    output  wire    [3:0]   data_out_7
);

    reg [7:0]   decoder_out;
    wire cs_0 = decoder_out[0];
```

```
    wire cs_1 = decoder_out[1];
    wire cs_2 = decoder_out[2];
    wire cs_3 = decoder_out[3];
    wire cs_4 = decoder_out[4];
    wire cs_5 = decoder_out[5];
    wire cs_6 = decoder_out[6];
    wire cs_7 = decoder_out[7];

    always @(*) begin
        case (sel)
            3'b000:decoder_out = ~8'b00000001;
            3'b001:decoder_out = ~8'b00000010;
            3'b010:decoder_out = ~8'b00000100;
            3'b011:decoder_out = ~8'b00001000;
            3'b100:decoder_out = ~8'b00010000;
            3'b101:decoder_out = ~8'b00100000;
            3'b110:decoder_out = ~8'b01000000;
            3'b111:decoder_out = ~8'b10000000;
        endcase
    end

unit U0( cs_0,en,data_in,data_out_0);
unit U1( cs_1,en,data_in,data_out_1);
unit U2( cs_2,en,data_in,data_out_2);
unit U3( cs_3,en,data_in,data_out_3);
unit U4( cs_4,en,data_in,data_out_4);
unit U5( cs_5,en,data_in,data_out_5);
unit U6( cs_6,en,data_in,data_out_6);
unit U7( cs_7,en,data_in,data_out_7);

endmodule
```

3.

```
`timescale 10ms/1ms
module decoder3_8_tb();
reg [2:0]       sel;
reg [3:0]    data_in;
reg             en;
wire     [3:0]    data_out_0;
wire     [3:0]    data_out_1;
wire     [3:0]    data_out_2;
wire     [3:0]    data_out_3;
wire     [3:0]    data_out_4;
```

```
wire    [3:0]   data_out_5;
wire    [3:0]   data_out_6;
wire    [3:0]   data_out_7;

decoder3_8 U0(
sel,
data_in,
en,

data_out_0,
data_out_1,
data_out_2,
data_out_3,
data_out_4,
data_out_5,
data_out_6,
data_out_7
);

initial begin

//以下证明 en 对 data_in 和 sel 起控制作用

#0 en=1; #0 data_in=0; #0 sel=0;//设置初始状态
#1 en=0;
#2 data_in=1;
#3 en=1;
#4 en=0;
#5 sel=1;
#6 en=1;

//以下证明 data_in 的作用

#7 data_in=2;
#8 data_in=3;

//以下证明 sel 的作用

#9 sel=2;
#10 sel=3;
end
endmodule
```