电子系统设计第三次作业

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1.

```
module FSM(clk,reset_n,out_moore);
input clk;
input reset_n;
output [2:0] out_moore;
parameter S0=0,S1=1,S2=2,S3=3,S4=4,S5=5,S6=6,S7=7;
reg [2:0] st;

always @(posedge clk,negedge reset_n)
begin
	if(!reset_n) st<=S7;
	else begin
	case(st)
		S0: st<=S1;
		S1: st<=S2;
		S2: st<=S3;
		S3: st<=S4;
		S4: st<=S5;
		S5: st<=S6;
		S6: st<=S7;
		S7: st<=S0;
		default:st<=S7;
		endcase
		end
end

assign out_moore=st;

endmodule
```

2.

```
module seq_detector(clk,reset_n,data_in,detector_out);
input clk;
input reset_n;
input data_in;
output reg detector_out;
```

```
reg [3:0] st;
parameter S0=0,S1=1,S2=2,S3=3,S4=4,S5=5,S6=6,S7=7,S8=8,S9=9;
reg Moore;

always @(posedge clk,negedge reset_n)
begin
    if(!reset_n) st<=S0;
    else begin
    case(st)
        S0:st<=(data_in?S1:S0);
        S1:st<=(data_in?S2:S0);
        S2:st<=(data_in?S3:S0);
        S3:st<=(data_in?S3:S4);
        S4:st<=(data_in?S5:S0);
        S5:st<=(data_in?S2:S6);
        S6:st<=(data_in?S1:S7);
        S7:st<=(data_in?S8:S0);
        S8:st<=(data_in?S9:S0);
        S9:st<=(data_in?S1:S0);
        default:st<=S0;
        endcase
    end
end

always @(st)
begin
    case(st)
    S9:detector_out<=1;
    default:detector_out<=0;
    endcase
end

endmodule
```