# 电子系统设计第三次作业

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1.

module FSM(clk,reset\_n,out\_moore);

input clk;

input reset\_n;

output [2:0] out\_moore;

parameter S0=0,S1=1,S2=2,S3=3,S4=4,S5=5,S6=6,S7=7;

reg [2:0] st;

always @(posedge clk,negedge reset\_n)

begin

if(!reset\_n) st<=S7;

else begin

case(st)

S0: st<=S1;

S1: st<=S2;

S2: st<=S3;

S3: st<=S4;

S4: st<=S5;

S5: st<=S6;

S6: st<=S7;

S7: st<=S0;

default:st<=S7;

endcase

end

end

assign out\_moore=st;

endmodule

2.

module seq\_detector(clk,reset\_n,data\_in,detector\_out);

input clk;

input reset\_n;

input data\_in;

output reg detector\_out;

reg [3:0] st;

parameter S0=0,S1=1,S2=2,S3=3,S4=4,S5=5,S6=6,S7=7,S8=8,S9=9;

reg Moore;

always @(posedge clk,negedge reset\_n)

begin

if(!reset\_n) st<=S0;

else begin

case(st)

S0:st<=(data\_in?S1:S0);

S1:st<=(data\_in?S2:S0);

S2:st<=(data\_in?S3:S0);

S3:st<=(data\_in?S3:S4);

S4:st<=(data\_in?S5:S0);

S5:st<=(data\_in?S2:S6);

S6:st<=(data\_in?S1:S7);

S7:st<=(data\_in?S8:S0);

S8:st<=(data\_in?S9:S0);

S9:st<=(data\_in?S1:S0);

default:st<=S0;

endcase

end

end

always @(st)

begin

case(st)

S9:detector\_out<=1;

default:detector\_out<=0;

endcase

end

endmodule